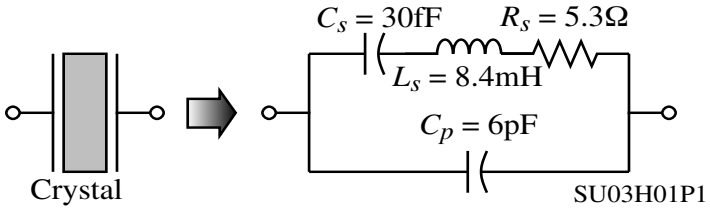
PLL PROBLEMS AND SOLUTIONS

Problem 1

Solve for and evaluate the series and parallel resonance frequencies of the crystal whose model is shown. It is suggested to make appropriate assumptions as the exact frequencies are difficult to achieve.



Solution

Solving the exact frequencies for this problem is very challenging. It is better to assume that series resonance (minimum impedance) will occur approximately when the impedance of C_s cancels the impedance of L_s. This gives series resonance as

$$\omega_s^2 = \frac{1}{L_s C_s} \quad \rightarrow \quad f_s = \frac{1}{2\pi\sqrt{L_s C_s}} \approx \underline{\underline{10.026\text{MHz}}}$$

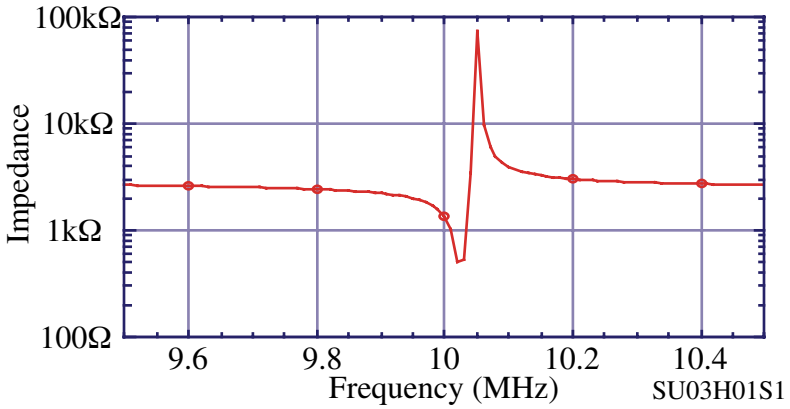
The parallel resonance can be approximated by assuming that it will occur close to the frequency when the impedance of the series branch equals the negative impedance of the parallel branch. This condition is given as,

$$\frac{1}{\omega C_p} = \omega L_s + \frac{1}{\omega C_s} \rightarrow \omega_p^2 = \frac{1}{L_s}\left(\frac{1}{C_s} + \frac{1}{C_p}\right) \rightarrow f_p = \frac{1}{2\pi}\sqrt{\frac{1}{L_s}\left(\frac{1}{C_s} + \frac{1}{C_p}\right)}$$

$$f_p \approx \underline{\underline{10.051\text{MHz}}}$$

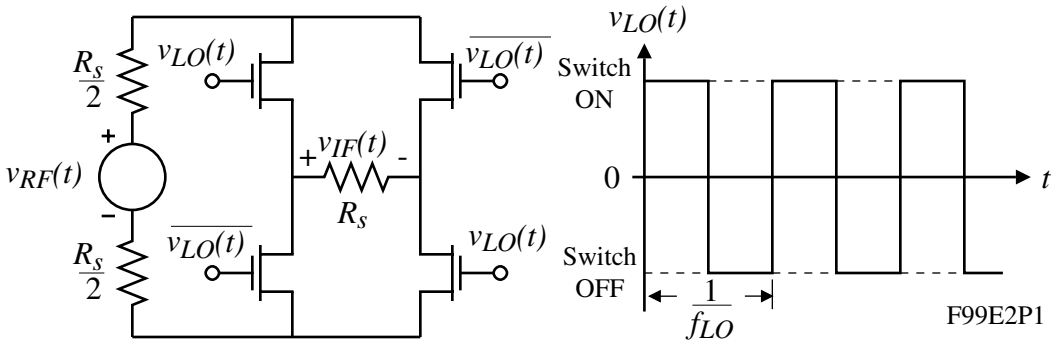
SPICE Simulation:

```
Homework H01P1 - Crystal Impedance
IIN 0 1 AC 1.0
CP 1 0 6PF
CS 1 2 30FF
LS 2 3 8.4MH
RS 3 0 5.3OHM
RBIG 1 0 1GOHM
.AC LIN 101 9.5MEG 10.5MEG
.PRINT AC V(1)
.PROBE
.END
```



Problem 2

A simple, doubly balanced passive CMOS mixer is shown along with the local oscillator waveform, $v_{OL}(t)$. Assume that $v_{RF}(t) = A_{RF}cos(\omega_{RF}t)$ and $v_{LO}(t)$ is the waveform shown below. (a.) Find the mixer gain, G_c, in dB if the switches are ideal. (b.) Find the mixer gain in dB if the switches have an ON resistance of $R_s/2$.



Solution

Assume the switches have an ON resistance of R_{ON} and work both parts (a) and (b) simultaneously. Also, The equation for $v_{IF}(t)$ can be written as,

$$v_{IF}(t) = \left(\frac{R_s}{2R_s+2R_{ON}}\right) v_{RF}(t) \cdot \text{sgn}[v_{LO}(t)]$$

$$V_{IF}(j\omega) = \left(\frac{R_s}{2R_s+2R_{ON}}\right) A_{RF}cos(\omega_{RF}t) \cdot \left[\frac{4}{\pi}cos(\omega_{LO}t) + \frac{4}{3\pi}cos\,(3\omega_{LO}t) + \cdots\right]$$

$$\therefore \quad V_{IF}(j\omega) \approx \left(\frac{R_s}{2R_s+2R_{ON}}\right) \frac{4A_{RF}}{\pi} cos(\omega_{RF}t) \cdot cos(\omega_{LO}t)$$

$$= \left(\frac{R_s}{2R_s+2R_{ON}}\right) \frac{2A_{RF}}{\pi} cos[\omega_{RF} - \omega_{LO})t]$$

The conversion gain in general is written as

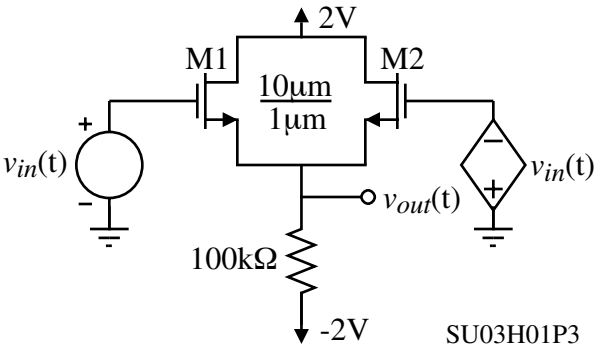
$$G_c = \frac{|V_{IF}|}{|V_{RF}|} = \left(\frac{R_s}{2R_s+2R_{ON}}\right) \frac{2}{\pi}$$

(a.) For $R_{ON} = 0$, $G_c = \frac{1}{\pi}$ → $\boxed{G_c = \frac{1}{\pi} = -9.943\text{dB}}$

(b.) For $R_{ON} = 0.5R_s$, $G_c = \frac{2}{3\pi}$ → $\boxed{G_c = \frac{2}{3\pi} = -13.465\text{dB}}$

Problem 3

Use SPICE to demonstrate that the following circuit is a frequency doubler. If $v_{in}(t)$ is a sinusoid of 10kHz and 1.5V peak, show $v_{in}(t)$ and $v_{out}(t)$ as a function of time. The model parameters of the MOSFETS are $K_N' = 110\mu A/V^2$, $V_{TN} = 0.7V$, and $\lambda_N = 0.04V\text{-}1$.



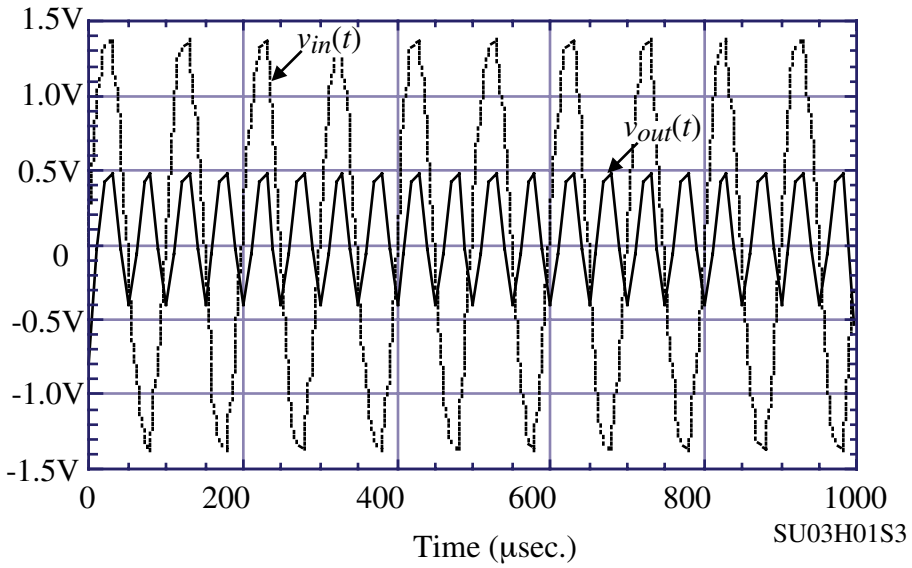
Solution

The results of this problem are below.

SPICE Input File:

```
Homework H01P3 - Frequency Doubler
VIN 1 0 DC 0.0 SIN(0 1.5 10KHz)
EVIN 0 2 1 0 1.0
VDD 4 0 DC 2.0
VSS 5 0 DC -2.0
M1 4 1 3 3 NMOS1 W=10U L=1U
M2 4 2 3 3 NMOS1 W=10U L=1U
RTAIL 3 5 100K
.MODEL NMOS1 NMOS VTO=0.7 KP=110U LAMBDA=0.04
.OP
.TRAN (10U 1000U)
.PRINT TRAN V(1) V(2) V(3)
.PROBE
.END
```

Output Plots:



Problem 4

An 10nH inductor has a Q of 5 and is used to create a tank circuit with a 10pF capacitor. Assume the capacitor is ideal. (a.) What is the resonant frequency of this circuit? (b.) What value of parallel negative resistance should be used to create an oscillator? (c.) If C is changed to 20 pF, what is the new value of the parallel negative resistance?

Solution

C = 10pF:

$$L_p = \left(1+\frac{1}{Q^2}\right) = \frac{26}{25}\cdot 10\text{nH} = 10.4\text{nH}$$

$$\omega_o = \frac{1}{\sqrt{L_p C}} = \frac{1}{\sqrt{10.4\text{nH}\cdot 10\text{pF}}} = 3.1623\text{x}10^9 \text{ radians/sec.}$$

$$Q = \frac{\omega_o L_s}{R_s} \quad \rightarrow \quad R_s = \frac{\omega_o L_s}{Q} = 6.201\Omega$$

$$\therefore \quad R_p = (1+Q^2)R_s = 26\cdot 6.201\Omega = \underline{\underline{161.245\Omega}}$$

C = 20pF:

$$\omega_o = \frac{1}{\sqrt{L_p C}} = \frac{1}{\sqrt{10.4\text{nH}\cdot 20\text{pF}}} = 2.1926\text{x}10^9 \text{ radians/sec.}$$

$$Q = \frac{\omega_o L_s}{R_s} \quad \rightarrow \quad R_s = \frac{\omega_o L_s}{Q} = 4.3853\Omega$$

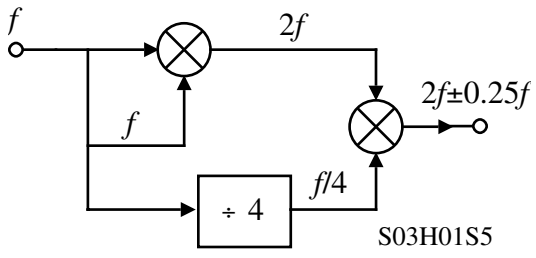
$$\therefore \quad R_p = (1+Q^2)R_s = 26\cdot 4.3853\Omega = \underline{\underline{114.017\Omega}}$$

Problem 5

Give a block diagram of simple brute-force coherent direct synthesizer that will generate 1.75f from f. The input frequency f is to vary from 12 MHz to 15MHz. Since f is variable, you cannot use frequency multipliers (integer frequency dividers and mixers are allowed) in your design. A simple design will receive more credit. What other frequencies will be present at the output?

Solution

Approach: $f_{out} = f\text{x}f - f/4 = 1.75f$



The frequency 2.25f will also be present at the output.

Problem 6

A phase-locked loop has a center frequency of 10^5 rads/s, a K_o of 10^3 rad/V-s, and a K_d of 1 V/rad. Assume there is no other gain in the loop. Determine the loop bandwidth in the first-order loop configuration. Determine the single-pole, loop-filter pole location to give the closed-loop poles located on 45° radials from the origin of the complex frequency plane.

Solution

The loop bandwidth = $K_v = K_o K_p = \dfrac{10^3}{\text{s}}$

In order to produce poles at 45° to the axis, we add a loop filter pole at ω_1 where

$$\omega_1 = 2K_v = 2000 \text{ rads/sec.}$$

The filter transfer function becomes,

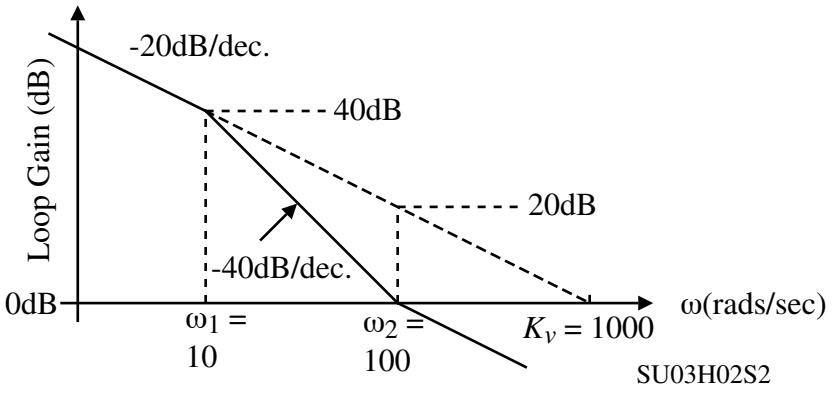
$$F(s) = \frac{\omega_1}{s+\omega_1} = \frac{2000}{s+2000}$$

Problem 7

For the same PLL of the previous problem, design a loop filter with a zero that gives a crossover frequency for the loop gain of 100 rads/sec. The loop phase shift at the loop crossover frequency should be –135°.

Solution

A plot of the desired loop gain is shown below.



If ω_2 (the zero frequency) is at the unity gain point, then the loop phase shift will be –135° at this point. Therefore, we require that $\omega_2 = 100$ radians/sec.. If $\omega_1 = 10$ radians/sec., the requirement will be satisfied as shown in the above plot.

The design of the filter becomes,

$$\omega_2 = \frac{1}{R_2 C} \quad \text{and} \quad \omega_1 = \frac{1}{(R_1+R_2)C}$$

$$\therefore \quad \frac{\omega_2}{\omega_1} = 1 + \frac{R_1}{R_2} = 10 \quad \rightarrow \quad R_1 = 9R_2$$

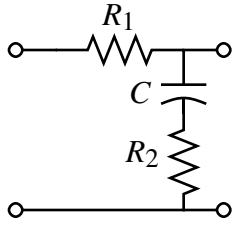


Fig. SU03H02S2A

Now appropriate values of R_1 , R_2, and C can be chosen.

Problem 8

Estimate the capture range of the PLL of the previous problem assuming that it is not artificially limited by the VCO frequency range.

Solution

For capture we need

$$|(\omega_i - \omega_o)| < \frac{\pi}{2} Kv|F(j(\omega_i - \omega_o)|$$

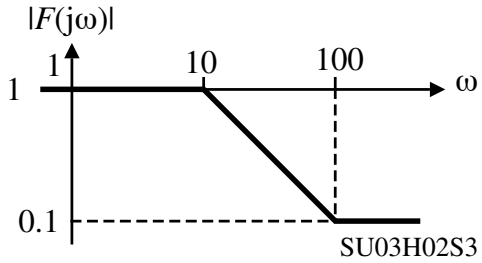
If we assume that

$$|(\omega_i - \omega_o)| = \frac{\pi}{2} Kv|F(j(\omega_i - \omega_o)|$$

then with $\omega_o = 10^5$ rads/sec and $K_v = 1000$ rads/sec. we get,

$$|(\omega_i - \omega_o)| = 1570|F(j(\omega_i - \omega_o)|$$

Now from the previous problem, we know that $|F(j\omega)|$ is given as



From this figure we can solve the above equation to find that

$(\omega_i - \omega_o) =$ 157 rads/sec.

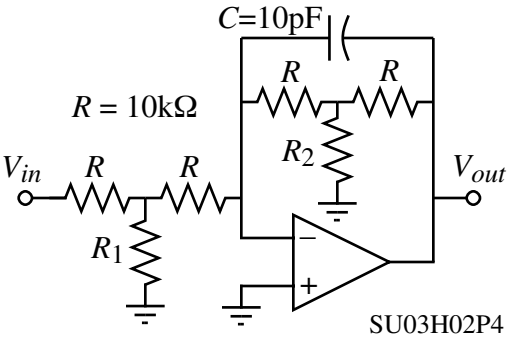
which is the capture range.

Problem 9

A filter for a phase locked loop is specified as

$$|F(s)| = \frac{10\omega_1}{s+\omega_1} = \frac{1{,}000{,}000}{s+100{,}000}$$

and must be implemented on a CMOS chip using resistors no larger than 10kΩ and capacitors no larger than 10pF. Using the circuit shown, find the values of R_1 and R_2 that will satisfy the component value constraints.



Solution

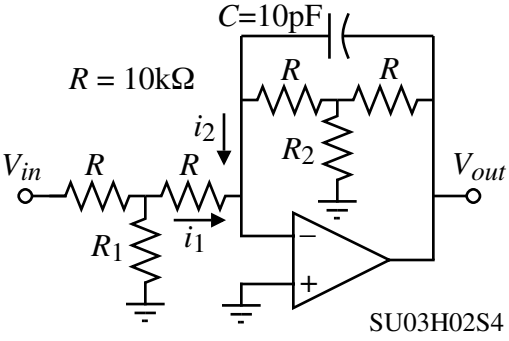
Find the currents i_1 and i_2,

$$i_1 = \frac{v_{in}}{R + \frac{RR_1}{R+R_1}} \frac{R}{R+R_1} = \frac{R_1\, v_{in}}{2RR_1 + R^2} = \frac{v_{in}}{R_{T1}}$$

and

$$i_2 = \frac{v_{out}}{R + \frac{RR_1}{R+R_1}} \frac{R}{R+R_1} + sCv_{out}$$

$$= \frac{R_2\, v_{out}}{2RR_2 + R^2} + sCv_{out} = \frac{v_{out}}{R_{T2}} + sCv_{out}$$



Solving for the sum of the currents flow toward the minus op amp input terminal gives,

$$\frac{v_{in}}{R_{T1}} + \frac{v_{out}}{R_{T2}} + sCv_{out} = 0 \qquad \rightarrow \qquad \frac{v_{out}}{v_{in}} = -\frac{R_{T2}}{R_{T1}} \frac{1}{sCR_{T2}+1} = -10\, \frac{1}{\frac{s}{10^5}+1}$$

$$\therefore \qquad CR_{T2} = 10^{-5} \quad \rightarrow R_{T2} = \frac{10^{-5}}{10^{-11}} = 10^6$$

$$R_{T2} = \frac{2RR_2 + R^2}{R_2} = 2R + \frac{R^2}{R_2} = 20\text{x}10^3 + \frac{100\text{x}10^6}{R_2} = 10^6$$

$$\therefore \qquad R_2 = \frac{100\text{x}10^6}{10^6\text{-}20\text{x}10^3} = \underline{\underline{100\Omega}}$$

$$R_{T1} = \frac{R_{T2}}{10} = 10^5 \qquad \rightarrow \qquad 2R + \frac{R^2}{R_1} = 20\text{x}10^3 + \frac{100\text{x}10^6}{R_1} = 10^5$$

$$\therefore \qquad R_1 = \frac{100\text{x}10^6}{10^5\text{-}20\text{x}10^3} = \underline{\underline{1000\Omega}}$$

This problem shows how a clever circuit technique can make a filter suitable for integrated circuit implementation.

Problem 10

This homework is designed to provide practical inductor design experience for students. Use ASITIC for the design and analysis. However, other tools are acceptable if they give all the results including layout.

A 5GHz LC tank will be designed as a part of LC oscillator. C value is given as 1pF.

(a) Find L value. (b) Design and simulate a spiral inductor with this L value (± 5% range). Optimize design parameters, W, S, D and N to get a high Q (Q_{min} = 5). Show L, Q, f_{SR} value obtained from simulation. (c) Show the layout. (d) Give a lumped circuit model with component values.

Solution

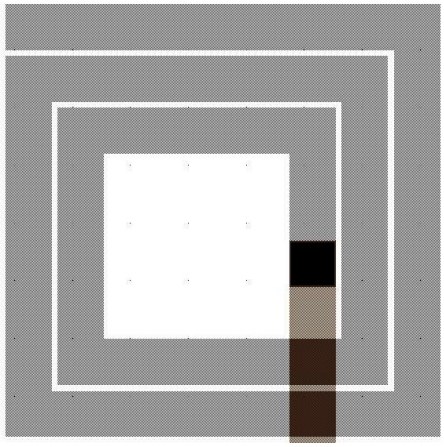
(a) LC tank oscillation frequency is given as 5GHz.

$$L = \frac{1}{\omega_{osc}^2 \cdot C} = \frac{1}{(2\pi \cdot 5\text{x}10^9)(1\text{x}10^{-12})} = 1.01\text{x}10^{-9}$$

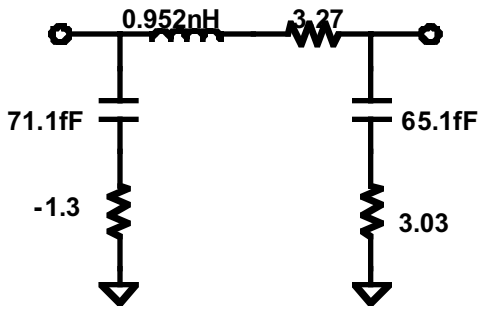
(b) One possible solution is

- Parameters: W = 16um, S = 2um, D = 150um, N =2.5
- Resulting inductor: L = 0.952nH, Q = 8.54, f_{SR} = 19.35GHz @ 5GHz

(c) Layout



(d) Pi model from ASITIC is shown below. This is the analysis result from 'pix' command.

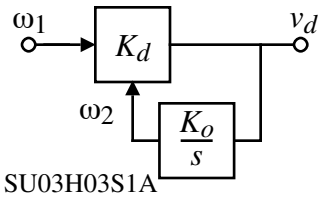


Problem 11

Assume an LPLL has $F(s)$ =1 and the PLL parameters are K_d = 0.8V/radians, K_o = 100 MHz/V, and the oscillation frequency, f_{osc} = 500MHz. Sketch the average control voltage at the output of the phase detector if the input frequency jumps from 500MHz to 550MHz.

Solution

Find the transfer function from the input frequency, f_{in}, to the output of the phase detector, v_d.



SU03H03S1A

$$V_d = K_d(\theta_1-\theta_2) = K_d\theta_1 - \frac{K_dK_o}{s}V_d$$

$$V_d\left(1+\frac{K_dK_o}{s}\right) = K_d\theta_1 = K_d\left(\frac{\omega_1}{s}\right)$$

$$\therefore \quad \frac{V_d}{\omega_1} = \frac{K_d}{s+K_dK_o} \rightarrow \qquad V_d(s) = \frac{K_d}{s+K_dK_o}\omega_1(s) = \frac{K_d}{s+K_dK_o}\frac{\Delta\omega_1}{s} = \frac{k_1}{s}+\frac{k_2}{s+K_dK_o}$$

By partial fraction expansion we can show that $k_1 = -k_2 = \frac{K_d\Delta\omega_1}{K_dK_o} = \frac{K_d\Delta\omega_1}{K_v} = 0.4\text{V}$

Note the units of $\frac{K_d\Delta\omega_1}{K_v}$ are $\frac{(\text{V/rad})(\text{rad/sec})}{1/\text{sec}} = \text{V}$

and $K_v = (2\pi\cdot 100\text{MHz/V})(0.8\text{V/rad.}) = 502.65\text{x}10^6$ (1/sec.)

$$\therefore \quad v_d(t) = \frac{K_d\Delta\omega_1}{K_v}(1-e^{-K_vt}) = 0.4(1-e^{-502.65\text{x}10^6t})$$

A plot of $v_d(t)$ is shown below.

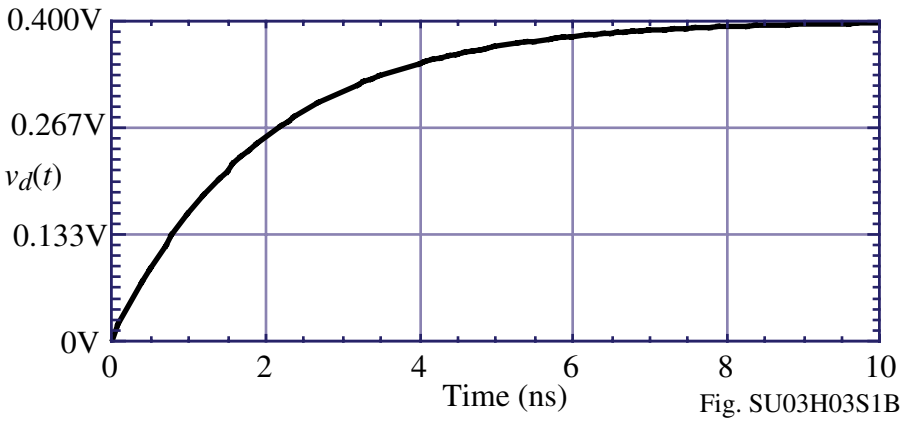
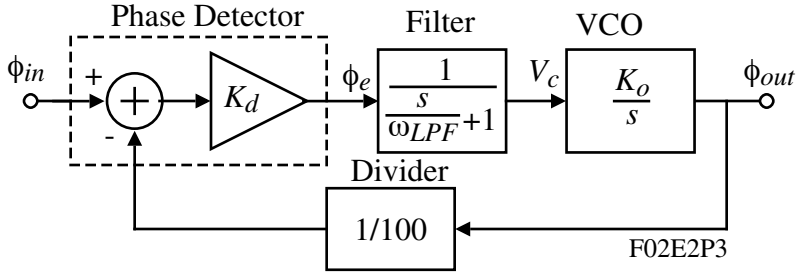


Fig. SU03H03S1B

Problem 12

A Type I PLL incorporates a VCO with K_o = 100MHz/V, a phase detector with K_d = 1V/rad, and a first-order, lowpass filter with $\omega_{LPF} = 2\pi \text{ x} 10^6$ radians/s shown below. A divider of 100 has been placed in the feedback path to implement a frequency synthesizer. (a.) Find the value of the natural damping frequency, ω_n, and the damping factor, ζ, for the transfer function $\phi_{out}(s)/\phi_{in}(s)$, for this PLL. (b.) If a step input of $\Delta\phi_{in}$ is applied at $t = 0$, what is the steady-state phase error at the output of the phase detector, ϕ_e? The steady-state error is evaluated by multiplying the desired phase by s and letting $s \rightarrow 0$.



Solution

(a.) $$\phi_{out} = \frac{K_o}{s}\left(\frac{1}{\frac{s}{\omega_{LPF}}+1}\right)K_d\left(\phi_{in} - \frac{\phi_{out}}{N}\right) \rightarrow \phi_{out}\left[1 + \frac{K_o}{sN}\left(\frac{K_d}{1 + \frac{s}{\omega_{LPF}}}\right)\right] = \frac{K_o}{s}\left(\frac{K_d}{\frac{s}{\omega_{LPF}}+1}\right)\phi_{in}$$

$$\therefore \frac{\phi_{out}(s)}{\phi_{in}(s)} = \frac{K_o K_d}{s\left(1 + \frac{s}{\omega_{LPF}}\right) + \frac{K_o K_d}{N}} = \frac{K_o K_d \omega_{LPF}}{s^2 + \omega_{LPF}\, s + \frac{K_o K_d \omega_{LPF}}{N}} = \frac{{\omega_n}^2}{s^2 + 2\zeta\omega_n s + {\omega_n}^2}$$

Thus, $${\omega_n}^2 = \frac{K_o K_d \omega_{LPF}}{N} = \frac{2\pi\text{x}10^6 \cdot 2\pi\text{x}10^8}{100} = 4\pi^2\text{x}10^{12} \rightarrow \omega_n = 2\pi\text{x}10^6$$

$$\zeta = \frac{\omega_{LPF}}{2\omega_n} = \frac{\omega_{LPF}}{2\sqrt{\frac{K_o K_d \omega_{LPF}}{N}}} = \frac{1}{2}\sqrt{\frac{N\omega_{LPF}}{K_o K_d}} = \frac{1}{2}\sqrt{\frac{100 \cdot 2\pi\text{x}10^6}{1 \cdot 2\pi\text{x}10^8}} = 0.5$$

$\therefore$ $\boxed{\omega_n = 2\pi\text{x}10^6 \text{ and } \zeta = 0.5}$

(b.) First we must solve for $\phi_e(s)$ which is found as

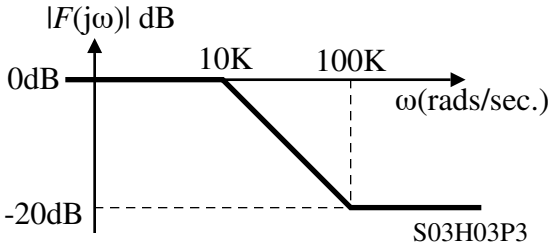
$$\phi_e(s) = \frac{s\left(1 + \frac{s}{\omega_{LPF}}\right)}{K_o}\phi_{out}(s) = \frac{s\left(1 + \frac{s}{\omega_{LPF}}\right)}{K_o}\frac{K_o K_d \omega_{LPF}}{s^2 + \omega_{LPF}\, s + \frac{K_o K_d \omega_{LPF}}{N}}\phi_{in}(s)$$

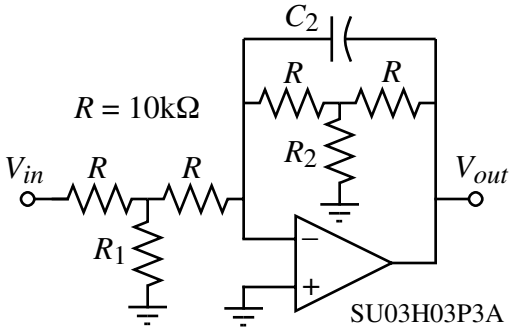
If $\phi_{in}(s) = \frac{\Delta\phi_{in}}{s}$, then we can write $s\phi_e(s) = \frac{K_d(s^2 + \omega_{LPF}\, s)\Delta\phi_{in}}{s^2 + \omega_{LPF}\, s + \frac{K_o K_d \omega_{LPF}}{N}}$

Therefore, we see that the steady-state error is $\boxed{\phi(t=\infty) = 0.}$

Problem 13

Modify the active filter shown of Problem 9 to design the lag-lead loop filter shown below. The capacitors can be no larger than 10pF. Give the values of R_1, R_2, C_1 and C_2.





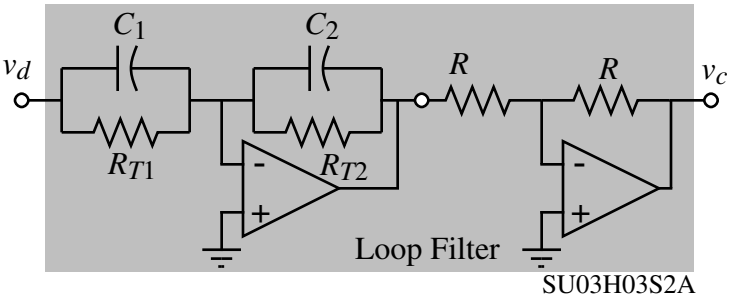
Solution

The transfer function corresponding to the above Bode plot is,

$$F(s) = \frac{\frac{s}{10^5} + 1}{\frac{1}{10^4} + 1}$$

The modification of the filter is shown where from Prob. 9,

$$R_{Ti} = \frac{2RR_i + R^2}{R_i}$$



The transfer function of this filter is found as,

$$F(s) = \frac{V_c(s)}{V_d(s)} = \left(\frac{R_{T2}}{R_{T1}}\right)\frac{sR_{T1}C_1+1}{sR_{T2}C_2+1} \Rightarrow \quad R_{T2} = R_{T1} = R_T\,,\; R_TC_1 = 10^{-5} \text{ and } R_TC_2 = 10^{-4}$$

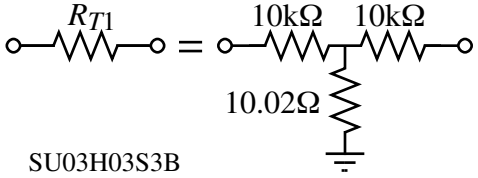
We see if $R_{T2} = R_{T1}$, then $C_2 = 10C_1$. Choosing $C_2 = 10$pF gives $C_1 = 1$pF. This gives

$$R_T = \frac{10^{-4}}{C_2} = \frac{10^{-4}}{10^{-11}} = 10^7$$

$$R_T = \frac{2RR_i + R^2}{R_i} = 2R + \frac{R^2}{R_1} = 20\text{x}10^3 + \frac{100\text{x}10^6}{R_1} = 10^7 \Rightarrow R_1 = \frac{100\text{x}10^6}{10^7\text{-}20\text{x}10^3} = 10.02\Omega$$

Therefore, $R_1 = R_2 = \underline{10.02\Omega}$, $C_1 = \underline{1\text{pF}}$ and $C_2 = \underline{10\text{pF}}$

The realization is completed by replacing each of the R_T resistors with the following equivalent:



Problem 14

Using the filter of Problem 13, find the value of ω_n and ζ of the PLL if K_d = 1V/radians, K_o = 2Mradians/V·sec. What is the steady state phase error in degrees if a frequency ramp of 10^9 radians/sec.^{2} is applied to the PLL?

Solution

Using the definition give in the notes for the time constants of the passive lag-lead filter we get,

$$F(s) = \frac{\frac{s}{10^5} + 1}{\frac{1}{10^4} + 1} = \frac{s\tau_2 + 1}{s(\tau_1+\tau_2) + 1} \qquad \Rightarrow \qquad \tau_2 = 10^{-5} \text{ sec. and } \tau_1 = 9\text{x}10^{-5} \text{ sec.}$$

$$\therefore \qquad \omega_n = \sqrt{\frac{K_o K_d}{\tau_1+\tau_2}} = \sqrt{\frac{2\text{x}10^6}{10^{-4}}} = \sqrt{2}\ \text{x}10^5 = \underline{\underline{141.4\text{x}10^3 \text{ radians/sec.}}}$$

$$\zeta = \frac{\omega_n}{2}\left(\tau_2 + \frac{1}{K_o K_d}\right) = \frac{\sqrt{2}\text{x}10^5}{2}\left(10^{-5} + \frac{1}{2\text{x}10^6}\right) = \frac{1}{\sqrt{2}}\left(1 + \frac{1}{20}\right) = \underline{\underline{0.742}}$$

Assuming the PLL has a high loop gain, then the steady-state phase error can be found as

$$\theta_e(\infty) = \frac{\Delta\dot{\omega}}{\omega_n^2} = \frac{10^9}{2\text{x}10^{10}} = \frac{1}{20} \text{ radians} = \underline{\underline{2.86^\circ}}$$

Problem 15

Solve for the crossover frequency of the PLL of Problems 13 and 14 and find the phase margin. Use SPICE to find the open-loop frequency response of the PLL and from your plot determine the crossover frequency and phase margin and compare with your calculated values.

Solution

The crossover frequency can be found as,

$$\omega_c = \omega_n\sqrt{2\zeta^2 + \sqrt{4\zeta^4+1}} = \sqrt{2}\,x10^5\sqrt{2\cdot 0.742^2 + \sqrt{4\cdot 0.742^4+1}}$$

$$= \sqrt{2}\,x10^5(1.6089) = 2.275x10^5 \text{ radians/sec.} = 36.208\text{kHz}$$

The open loop transfer function is given as

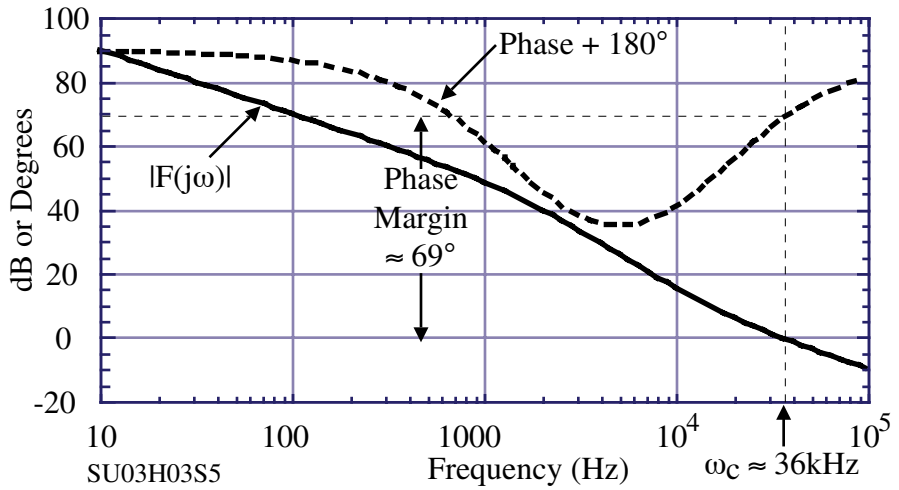
$$LG(s) = \frac{K_v}{s}\left(\frac{1+s\tau_1}{1+s\tau_2}\right) = \frac{\sqrt{2}x10^5}{s}\left(\frac{1+s10^{-5}}{1+s10^{-4}}\right)$$

The phase margin can be written as,

$$PM = 180° - 90° + \tan^{-1}\left(\frac{\omega_c}{10^5}\right) - \tan^{-1}\left(\frac{\omega_c}{10^4}\right) = 90° + 66.27° - 87.48° = \underline{\underline{68.79°}}$$

SPICE Results:

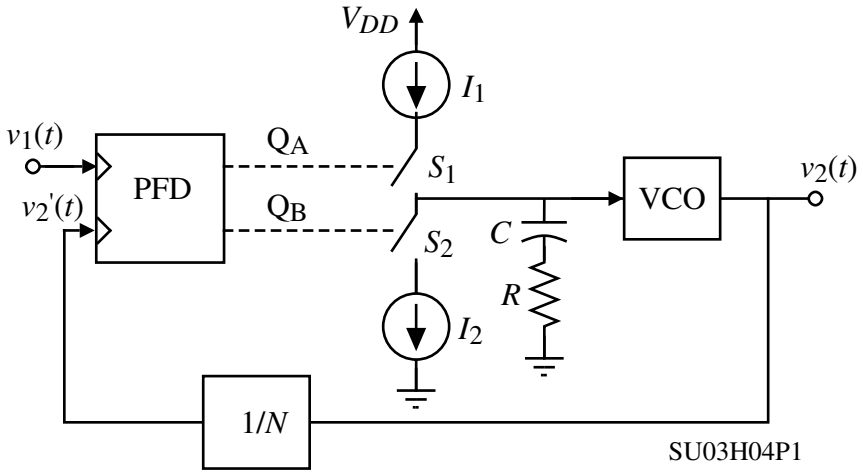
```
Problem H3P5-Open Loop Response of an LPLL with Lead-Lag Filter
VS 1 0 AC 1.0
R1 1 0 10K
* Loop bandwidth = Kv =2xE+6    Tau1=1E-4   Tau2=1E-5
ELPLL 2 0 LAPLACE {V(1)}=
+{(2E+6/(S+0.001))*((1+1E-5*S)/(1+1E-4*S))}
* Note: The 0.001 added to "S" in the denominator is to prevent
* blowup of the problem at low frequencies.
R2 2 0 10K
*Steady state AC analysis
.AC DEC 20 10 100K
.PRINT AC VDB(2) VP(2)
.PROBE
.END
```



The simulation results agree well with the calculated results.

Problem 16

For the DPLL shown assume that $N = 1000$ and the –3dB bandwidth is 1000 Hz. (a.) Assume that $\zeta = 0.2$ and solve for the natural pole frequency, ω_n, the filter time constant, $\tau = RC$, and the phase margin. (b.) Repeat part (a.) if $\zeta = 0.7$. (c.) Repeat part (a.) if $\zeta = 1$. Verify your answers with PSPICE.



Solution

The filter output can be written as,

$$V_f(s) = \frac{K_d}{s}(s\tau+1)(\theta_1-\theta_2') = \frac{K_d}{s}(s\tau+1)\left(\theta_1 + \frac{\theta_2}{N}\right) \qquad \text{where } \tau = RC$$

$$\theta_2(s) = \frac{K_o}{s}V_f(s) = \frac{K_oK_d}{s^2}(s\tau+1)\left(\theta_1 + \frac{\theta_2}{N}\right) = \frac{K_v(s\tau+1)}{s^2}\theta_1(s) + \frac{K_v(s\tau+1)}{Ns^2}\theta_2(s)$$

The closed-loop response is given as,

$$\frac{\theta_2(s)}{\theta_1(s)} = \frac{K_v(s\tau+1)}{s^2 + \frac{K_v\tau}{N}s + \frac{K_v}{N}} = \frac{K_v(s\tau+1)}{s^2 + 2\omega_n\zeta s + \omega_n{}^2}$$

$$\therefore \qquad \omega_n = \sqrt{\frac{K_v}{N}} \quad \text{and} \quad \tau = \frac{2\zeta}{\omega_n}$$

We know that the loop bandwidth, $\omega_{\text{-3dB}}$, can be expressed as

$$\omega_{\text{-3dB}} = \omega_n\sqrt{2\zeta^2+1+\sqrt{(2\zeta^2+1)^2+1}} \quad \rightarrow \quad \omega_n = \frac{\omega_{\text{-3dB}}}{\sqrt{2\zeta^2+1+\sqrt{(2\zeta^2+1)^2+1}}}$$

$\zeta = 0.2$:

$\omega_n = 3933$ rads/sec., $\tau = 102\mu s$ and $PM = 0° + \tan^{-1}(2000\pi \cdot 102\mu s) = 32.6°$

$\zeta = 0.7$:

$\omega_n = 3066$ rads/sec., $\tau = 457\mu s$ and $PM = 0° + \tan^{-1}(2000\pi \cdot 457\mu s) = 70.8°$

$\zeta = 1$:

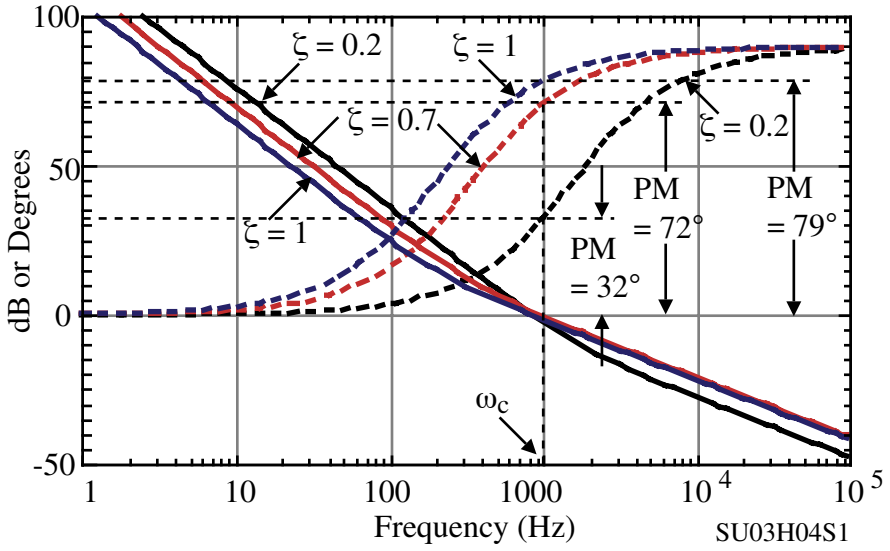
$\omega_n = 2531$ rads/sec., $\tau = 790\mu s$ and $PM = 0° + \tan^{-1}(2000\pi \cdot 790\mu s) = 78.6°$

Problem 16 – Continued

PSPICE Input File:

```
Homework4, Problem 1
VS 1 0 AC 1.0
R1 1 0 10K
ELPLL1 2 0 LAPLACE {V(1)}= {5044*5044*(1+102E-6*S)/(S+0.01)/(S+0.01)}
R2 2 0 10K
ELPLL2 3 0 LAPLACE {V(1)}= {3513*3513*(1+457E-6*S)/(S+0.01)/(S+0.01)}
R3 3 0 10K
ELPLL3 4 0 LAPLACE {V(1)}= {2531*2531*(1+790E-6*S)/(S+0.01)/(S+0.01)}
R4 4 0 10K
*Steady state AC analysis
.AC DEC 20 1 100K
.PRINT AC VDB(2) VP(2) VDB(3) VP(3) VDB(4) VP(4)
.PROBE
.END
```

Plot of Results:



Problem 17

A type-I, second-order DPLL synthesizer is to be made with components having the following values:

$K_o = 4\text{x}10^8$ rads/sec./V $\quad f_{ref} = 12.5$ kHz $\quad K_d = 0.15$ V/rad $\quad \beta = 2\pi$

Design a type-I, second-order synthesizer having the following specifications:

1.) Output frequency range = 50MHz

2.) Lock range = 10MHz at the output

3.) Damping factor = 0.75.

Determine the components for the loop filter. Let $C = 0.5\mu$F. Make a sketch of your filter with all components carefully labeled. Once your design is complete, determine the pull-in range in Hz (at the output) and the lock time of your loop.

Solution

$$N = \frac{f_{out}}{f_r} = \frac{50\text{MHz}}{12.5\text{kHz}} = 4000 \quad \text{and} \quad K_v = \frac{K_o K_d}{N} = \frac{4\text{x}10^8 \cdot 0.15}{4000} = 15{,}000 \text{ sec.}^{-1}$$

$$\Delta\omega_H = \beta K_v N = 2\pi \cdot 15\text{x}10^3 \cdot 4000 = 377\text{x}10^6 \text{ rads/sec.}$$

$$\Delta\omega_L = \frac{\tau_2}{\tau_1}\Delta\omega_H = \frac{\tau_2}{\tau_1}\ 377 \text{ Mrads/sec.} \rightarrow \quad \frac{\tau_2}{\tau_1} = \frac{\Delta\omega_L}{\Delta\omega_H} = \frac{62.8\text{Mrads/sec}}{377\text{Mrads/sec}} = \frac{1}{6}$$

$\therefore \quad \tau_1 = 6\tau_2$

$$\zeta = 0.5\sqrt{\frac{1}{K_v\tau_1}}(1+\tau_2 K_v) \rightarrow 1.5 = \sqrt{\frac{1}{K_v\tau_1}}(1+\tau_2 K_v) \rightarrow 2.25 = \frac{1}{K_v\tau_1}(1+\tau_2 K_v)^2$$

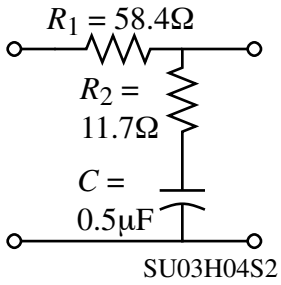
$$2.25 \cdot K_v(6\tau_2) = 13.5\ K_v\tau_2 = 1 + 2\ K_v\tau_2 + (K_v\tau_2)^2 \rightarrow 0 = 1 - 11.5x + x^2$$

where $x = K_v\tau_2$. Solving for x gives $x = K_v\tau_2 = \frac{11.5}{2} \pm \frac{1}{2}\sqrt{11.5^2 - 4} = 0.0876$

$$\therefore \quad \tau_2 = \frac{0.0876}{15{,}000} = 5.84\mu\text{s} = R_2 C = R_2(0.5\mu\text{F}) \quad \rightarrow R_2 = \frac{5.84}{0.5\mu\text{F}} = \underline{\underline{11.7\Omega}}$$

$$\tau_1 = 6\tau_2 = 35\mu\text{s} = (R_1+R_2)C \rightarrow R_1+R_2 = \frac{35}{0.5\mu\text{F}} = 70.08\Omega \rightarrow \quad R_1 = \underline{\underline{58.4\Omega}}$$

Filter schematic:



SU03H04S2

$$\Delta\omega_P = N\beta\sqrt{2}\sqrt{2\zeta\omega_n K_v F(0) - \omega_n^2} \quad \text{and} \quad \omega_n = \sqrt{\frac{K_v}{\tau_1}} = 20{,}702 \text{ rads/sec}$$

$$\therefore \quad \Delta\omega_P = 4000 \cdot 2\pi\sqrt{2}\sqrt{2 \cdot 0.75 \cdot 20{,}702 \cdot 15{,}000 - (20{,}702)^2} = 216.85 \text{ Mrads/sec.}$$

$$\Delta f_P = \underline{\underline{34.51 \text{ MHz}}}$$

$$T_L = \frac{2\pi}{\omega_n} = \frac{6.283}{20{,}702} = \underline{\underline{303.5\mu\text{s}}}$$

Problem 18

Given the DPLL described by

$$K_d = 2.2 \text{ V/rad} \qquad F(s) = \frac{1+\tau_2 s}{1+\tau_1 s} = \frac{1+5\text{x}10^{-6}s}{1+2\text{x}10^{-5}s}$$

$$f_{ref} = 12 \text{ kHz} \quad K_o = 25 \text{ MHz/V} \qquad \beta = 2\pi \qquad N = 15{,}000$$

Determine the type number and order of the system and then find:

(a.) The output frequency in Hz.

(b.) The crossover frequency in Hz.

(c.) The noise bandwidth (Hz).

(d.) The closed-loop phase –3dB bandwidth in Hz

(e.) The steady-state phase error in response to a phase step of 0.1 radian.

(f.) The hold range (±Hz at the output).

(g.) The lock range (±Hz at the output).

(h.) The lock time.

(i.) The pull-in range (±Hz at the output)

(j.) The steady-state phase error in radians in response to a frequency step equal to the lock range.

Solution

This is a type-I, second-order system. The closed loop transfer function is,

$$\theta_2 = \frac{K_v F(s)}{s}\left(\theta_1 - \frac{\theta_2}{N}\right) \rightarrow \frac{\theta_2}{\theta_1} = \frac{K_v F(s)}{s + \dfrac{K_v F(s)}{N}} = \frac{K_v\left(\dfrac{1+\tau_2 s}{1+\tau_1 s}\right)}{s + \dfrac{K_v\left(\dfrac{1+\tau_2 s}{1+\tau_1 s}\right)}{N}} = \frac{K_v(1+\tau_2 s)}{s(1+\tau_1 s) + \dfrac{K_v(1+\tau_2 s)}{N}}$$

$$\frac{\theta_2}{\theta_1} = \frac{\dfrac{K_v}{\tau_1}(1+\tau_2 s)}{s^2 + \dfrac{s}{\tau_1}\left(1 + \dfrac{K_v}{N}\tau_2\right) + \dfrac{K_v}{\tau_1 N}} = \frac{K_v(1+\tau_2 s)}{s^2 + 2\zeta\omega_n s + \omega_n{}^2}$$

$$\therefore \qquad \omega_n = \sqrt{\frac{K_v}{N\tau_1}} = \sqrt{\frac{2\pi\cdot 25\text{x}10^6\cdot 2.2}{2\text{x}10^{-5}\cdot 15{,}000}} = 33.94 \text{ Krads/sec}$$

$$\zeta = 0.5\sqrt{\frac{N}{K_v\tau_1}}\left(1+\frac{\tau_2 K_v}{N}\right) = 0.5\sqrt{\frac{15{,}000}{2\pi\cdot 25\text{x}10^6\cdot 2.2\cdot 2\text{x}10^{-5}}}\left(1 + \frac{2\pi\cdot 25\text{x}10^6\cdot 2.2\cdot 5\text{x}10^{-6}}{15{,}000}\right)$$

$$= (0.5)(1.4732)(1.115) = 0.821$$

(a.) $f_o = Nf_r = 15{,}000\cdot 12\text{kHz} =$ <u>180MHz</u>

(b.) $f_c = \dfrac{\omega_n}{2\pi}\sqrt{2\zeta^2 + \sqrt{4\zeta^4+1}} = \dfrac{33{,}940}{2\pi}\sqrt{2(0.821)^2+\sqrt{4(0.821)^4+1}} =$ <u>9,397 Hz</u>

Problem 18 - Continued

(c.) $B_n = \frac{\omega_n}{2}\left(\zeta + \frac{1}{4\zeta}\right) = \frac{33{,}940}{2}\left(0.821 + \frac{1}{4\cdot 0.821}\right) = \underline{\underline{19.1\text{kHz}}}$

(d.) $\omega_{-3\text{dB}} = \omega_n\sqrt{b + \sqrt{b^2+1}}$ where $b = 2\zeta^2 + 1 - \frac{N\omega_n}{K_v}\left(4\zeta - \frac{N\omega_n}{K_v}\right)$

$$b = 2(0.821)^2 + 1 - \frac{33{,}940\cdot 15{,}000}{2\pi\cdot 25\text{x}10^6\cdot 2.2}\left(4\cdot 0.821 - \frac{33{,}940\cdot 15{,}000}{2\pi\cdot 25\text{x}10^6\cdot 2.2}\right) = -0.320$$

$$\omega_{-3\text{dB}} = 33{,}940\sqrt{-0.320 + \sqrt{(-0.320)^2+1}} = 29{,}003 \text{ rads/sec.} \rightarrow f_{-3\text{dB}} = \underline{\underline{4615\text{Hz}}}$$

(e.) Because this is a Type-I, second-order system, the phase error in response to a phase step is zero provided that $\Delta\theta < \beta$.

(f.) $\Delta\omega_H = \beta NK = \beta K_v \quad \rightarrow \quad \Delta f_H = \frac{\beta K_v}{2\pi} = (2\pi\cdot 25\text{x}10^6\cdot 2.2) = \underline{\underline{\pm 345.6\text{MHz}}}$

(g.) $\Delta\omega_L = \frac{\tau_2}{\tau_1}\Delta\omega_H \quad \rightarrow \quad \Delta f_L = \pm 345.6\text{MHz}\left(\frac{5\text{x}10^{-6}}{2\text{x}10^{-5}}\right) = \underline{\underline{\pm 86.39\text{MHz}}}$

(h.) Lock time $= T_L = \frac{2\pi}{\omega_n} = \frac{2\pi}{33{,}940} = \underline{\underline{185\mu\text{s}}}$

(i.) Pull-in range.

$$\Delta\omega_P = N\beta\sqrt{2}\sqrt{\frac{2\zeta\omega_n K_v F(0)}{N} - \omega_n{}^2} \text{ where } F(0) = 1 \text{ for the filter selected.}$$

$$\therefore \quad \Delta f_P = \frac{15{,}000\cdot 2\pi\sqrt{2}}{2\pi}\sqrt{\frac{2\cdot 0.821\cdot 33{,}940\cdot 2\pi\cdot 25\text{x}10^6\cdot 2.2}{15{,}000} - (33{,}940^2)} = \underline{\underline{243.7\text{MHz}}}$$

Note that,

$$\Delta f_L < \Delta f_P < \Delta f_H$$

(j.) $\varepsilon_{ss} = \frac{\Delta\omega_{osc}}{K_v} = \frac{2\pi\cdot 86.39\text{x}10^6}{2\pi\cdot 25\text{x}10^6\cdot 2.2} = \underline{\underline{1.57 \text{ rads}}} < \beta$ as required

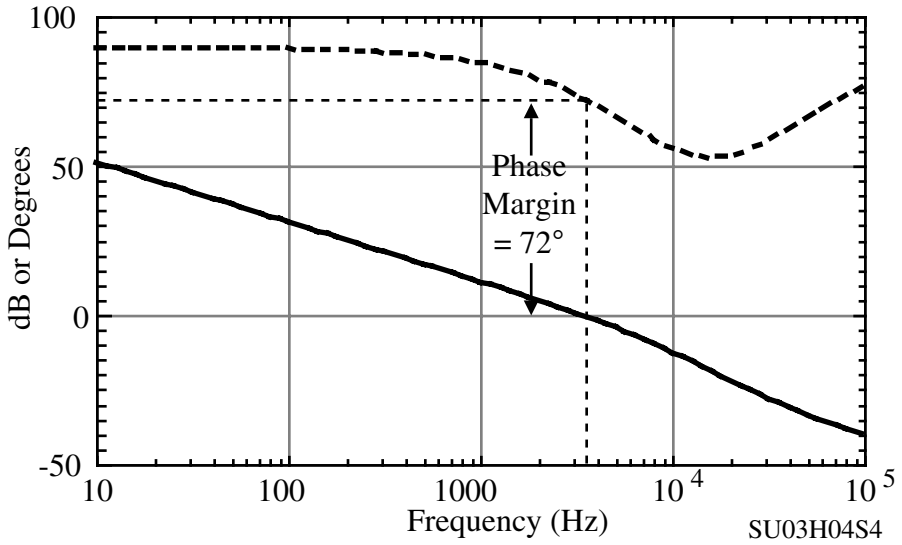
Problem 19

Construct an accurate Bode plot of the synthesizer in Problem 18. Use this Bode plot to determine the phase margin.

Solution

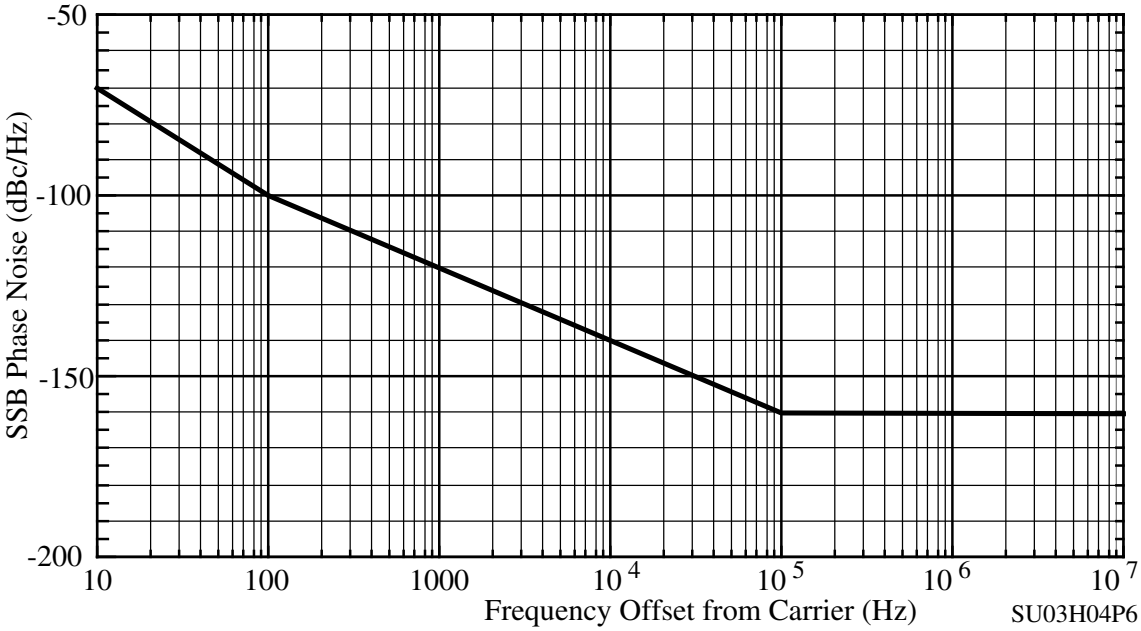
PSPICE was used to solve this problem. The input file and the results are shown below.

```
Problem H4P4-Open Loop Response of an DPLL with Lead-Lag Filter
VS 1 0 AC 1.0
R1 1 0 10K
ELPLL 2 0 LAPLACE {V(1)}= {23.04E+3*(1+5E-6*S)/(1+2E-
5*S)/(S+0.001)}
R2 2 0 10K
*Steady state AC analysis
.AC DEC 20 10 100K
.PRINT AC VDB(2) VP(2)
.PROBE
.END
```



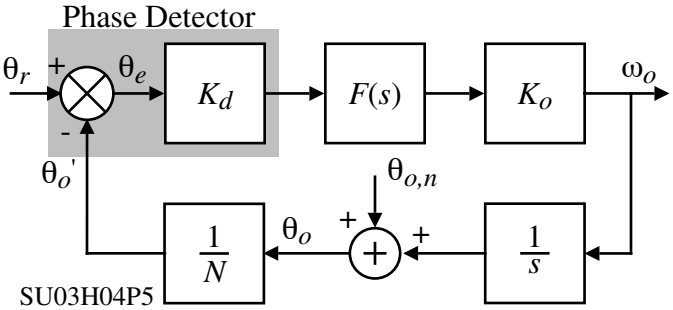
Problem 20

Write the transfer functions giving: (1) The VCO phase noise in the output, (2) the reference oscillator phase noise in the output. Use the literal form of the equations. The phase noise of the VCO used in the synthesizer of Problem 3 is shown below. Make an accurate plot of the VCO phase noise in the output of the synthesizer.



Solution

The following block diagram will be used to find the phase noise in the output due to the VCO phase noise.



$$\theta_o = \left[\theta_{o,n} - \frac{K_v F(s)\theta_o}{sN}\right]$$

$$\frac{\theta_o}{\theta_{o,n}} = \frac{s}{s + \frac{K_v F(s)}{N}}$$

$$\boxed{\frac{\theta_o}{\theta_{o,n}} = \frac{s}{s + \frac{K_v}{N}\left(\frac{1+\tau_2 s}{1+\tau_1 s}\right)} = \frac{s(1+\tau_1 s)}{s^2\tau_1 + s\left(1 + \frac{K_v\tau_2}{N}\right) + \frac{K_v}{N}}}$$

From Problem 3 of this assignment we get,

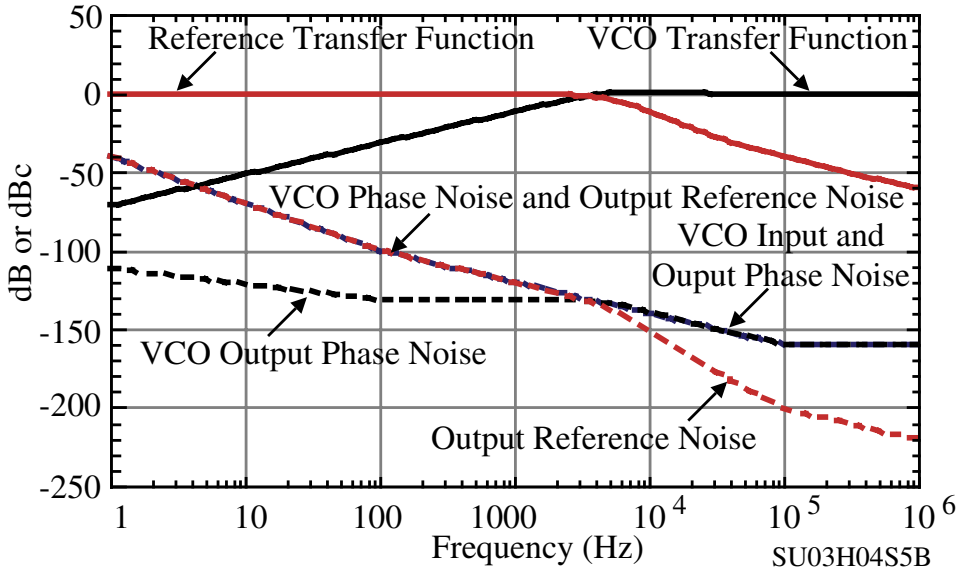
$$\boxed{\frac{\theta_o}{\theta_{r,n}} = \frac{1}{N}\,\frac{\frac{K_v}{\tau_1}(1+\tau_2 s)}{s^2 + \frac{s}{\tau_1}\left(1 + \frac{K_v}{N}\tau_2\right) + \frac{K_v}{\tau_1 N}}}$$

Problem 20 – Continued

The following PSPICE input file gives the results plotted below.

```
Homework 4, Problem 5 -In/Out VCO Phase Noise, Transfer Function
.PARAM N=15000, KVCO=157.1E6, T1=2E-5, T2=5E-6, KD=2.2, E=0.001
*Input Phase Noise
vphasenoise 1 0 ac 1.0
R1 1 0 10k
EPN 2 0 freq {v(1)} = (1,-40,0) (10,-70,0) (100,-100,0)
+(1E5,-160,0) (1E6,-160,0)
RPN 2 0 10k
*VCO Noise Transfer Function
EDPLL1 3 0 LAPLACE {V(1)}=
+{S*(T1*S+1)/(S*S*T1+KD*KVCO*T2/N*S+S+KD*KVCO/N)}
RDPLL1 3 0 10K
*VCO Noise at the Output
EDPLL2 4 0 LAPLACE {V(2)}=
+{S*(T1*S+1)/(S*S*T1+KD*KVCO*T2/N*S+S+KD*KVCO/N)}
RDPLL2 4 0 10K
*Reference Noise Transfer Function
EDPLL3 5 0 LAPLACE {V(1)}=
+{KD*KVCO*(1+T2*S)/(S*S*T1+S+KD*KVCO/N*S+KD*KVCO/N)/N}
RDPLL3 5 0 10K
*Reference Noise at the Output
EDPLL4 6 0 LAPLACE {V(2)}=
+{KD*KVCO*(1+T2*S)/(S*S*T1+S+KD*KVCO/N*S+KD*KVCO/N)/N}
RDPLL4 6 0 10K
*Steady state AC analysis
.AC DEC 20 1 1000K
.PRINT AC VDB(2) VDB(3) VDB(4) VDB(5) VDB(6)
.PROBE
.END
```

VCO Output Noise (and Reference Output Noise):



Problem 21

Sketch the time variation and frequency spectrum of an RF signal with 75 percent amplitude modulation. Show several cycles of the modulated wave. Make the modulation frequency 1/10 of the carrier frequency. The unmodulated carrier has a peak amplitude of 1.0V.

Solution

The expression for the general form of amplitude modulation is,

$$v(t) = 1.0\left[1 + m_a \cos\left(\frac{\omega_c t}{10}\right)\right]\cos(\omega_c t) = [1 + 0.75\cos(0.1\omega_c t)]\cos\omega_c t$$

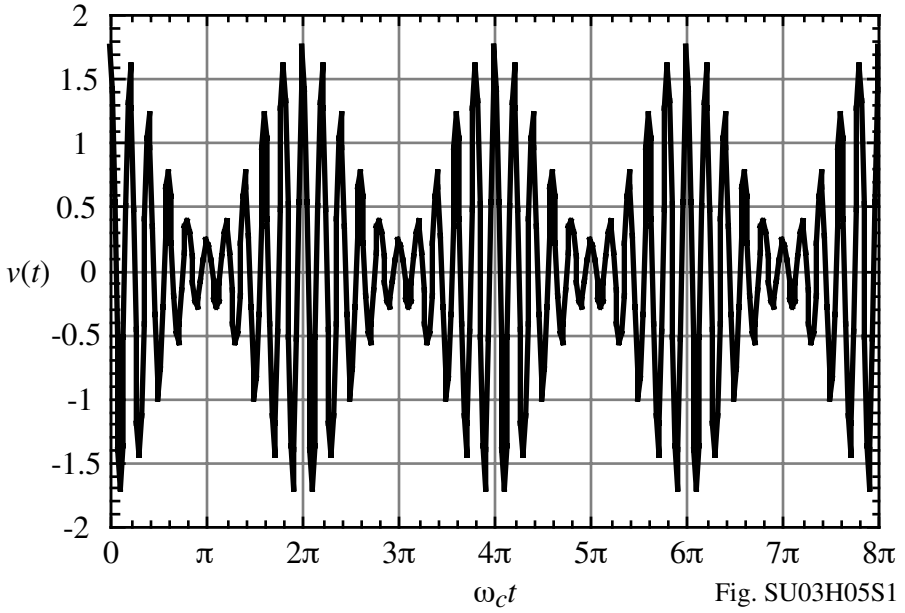


Fig. SU03H05S1

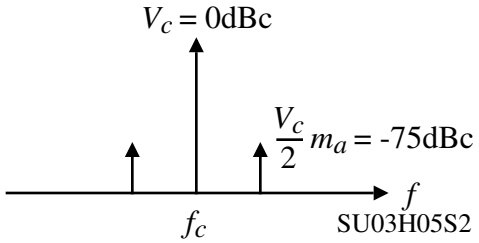
$v_{max.} = 1.75V$ and $v_{min.} = 0.25V$

Problem 22

The level of an SSB AM spur is observed to be –75 dBc. If the carrier has a peak amplitude of 1V, what is the variation of the carrier in ±V needed to produce the observed spur?

Solution

The observed spectrum is



SU03H05S2

$$SSB = 20\log_{10}\left(\frac{m_a}{2}\right) \quad \rightarrow \quad m_a = 2\cdot 10^{SSB/20}$$

$$\therefore \quad m_a = 2\cdot 10^{-75/20} = 335.6\text{x}10^{-6}$$

If $V_{peak} = 1V$, then $m_a = \frac{\Delta v}{V_p}$ $\rightarrow$ $\Delta v = \underline{\underline{3.35.6\mu V}}$

Problem 23

A pair of 5 kHz PM/FM spurs appear on a 10 MHz carrier. The level of each spur is –50dBc. (a.) What phase deviation in ±degrees is need to produce the spurs? (b.) What frequency deviation in ±Hz is needed to produce the spurs?

Solution

(a.) The single sideband spurs can be expressed as,

$$SSB = 20\ log_{10}\left(\frac{\theta_d}{2}\right) = 20\ log_{10}\left(\frac{\beta}{2}\right)$$

Solving for θ_d gives,

$$\theta_d = 2 \cdot 10^{SSB/20} = 2 \cdot 10^{-50/20} = 2 \cdot 0.003162 = 6.325 \text{ milliradians} = \underline{\underline{\pm 0.3624^\circ}}$$

(b.) We know that $\theta_d = \beta = \frac{\Delta f_c}{f_m}$ which gives

$$\Delta f_c = \beta f_m = \theta_d f_m = 6.325 \text{x} 10^{-3} \cdot 5 \text{x} 10^{+3} = \underline{\underline{\pm 31.6 \text{ Hz}}}$$

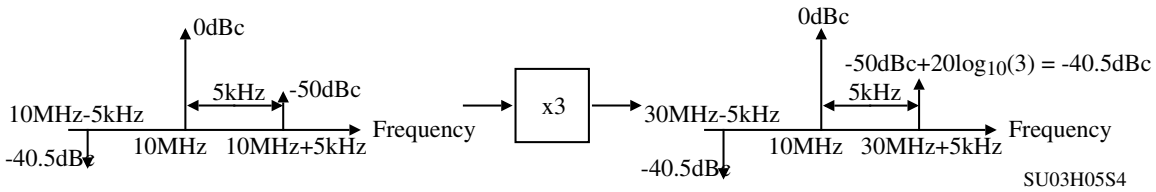
Problem 24

The carrier and spurs of Problem 3 above are passed through a frequency tripler. Make a sketch of the output spectrum of the tripler. Label and show all important features of the spectrum.

Solution

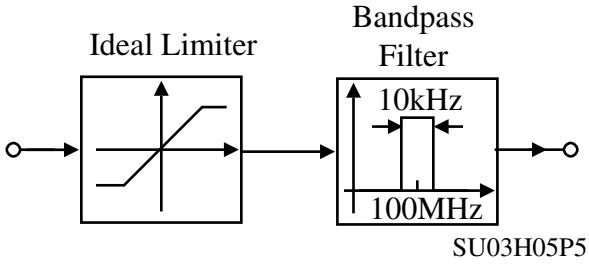
After passing through a tripler, the SSB spur is increased by $20log_{10}(3)$ or +9.54dB.

The resulting spectrum is shown as,



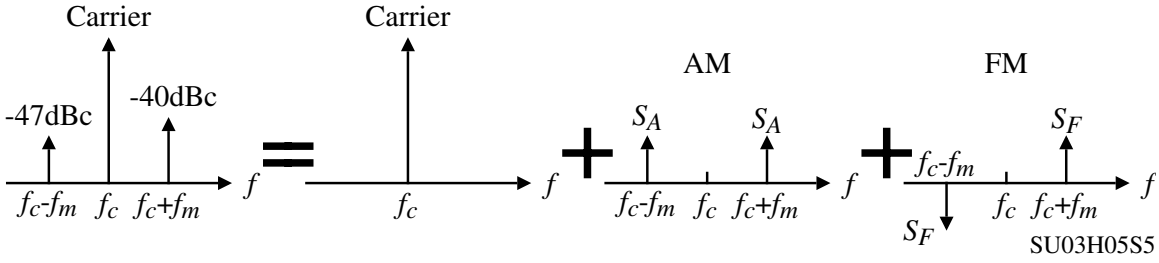
Problem 25

A 100 MHz carrier having a –40 dBc upper sideband at 100.002 MHz and a –47 dBc lower sideband at 99.998 MHz is passed through an ideal limiter followed by a bandpass filter centered at 100 MHz with a 10 kHz total bandwidth. Make a sketch of the spectrum at the output of the filter. Label all frequencies and amplitudes.



Solution

Asymmetrical sidebands imply the presence of both AM and FM as show below.



$-40\text{dBc} = 10^{-40/20} = 0.01$ and $-47\text{dBc} = 10^{-47/20} = 4.467\text{x}10^{-3}$

Solve for S_A and S_F as follows,

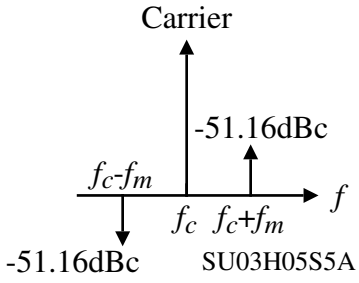
$$S_A + S_F = \text{Upper sideband} = 0.01$$

$$S_A - S_F = \text{Lower sideband} = 4.467\text{x}10^{-3}$$

$$S_A = \frac{\text{Upper sideband + Lower sideband}}{2} = 7.234\text{x}10^{-3}$$

$$S_F = \frac{\text{Upper sideband - Lower sideband}}{2} = 2.767\text{x}10^{-3}$$

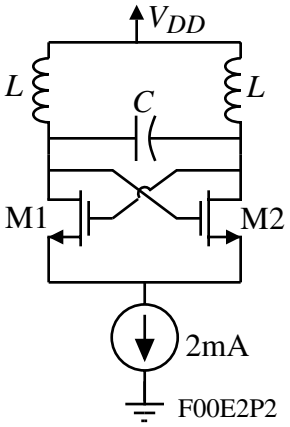
The limiter will remove all AM sidebands and the filter removes all products other than the sidebands at ±2kHz. Therefore the output spectrum will appear as,



where f_c = 100MHz and f_m = 2kHz.

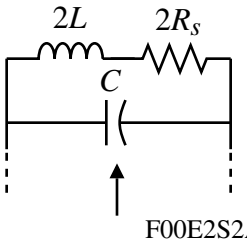
Problem 26

An LC oscillator is shown. The value of the inductors, L, are 5nH and the capacitor, C, is 5pF. If the Q of each inductor is 5, find (a.) the frequency of oscillation, (b.) the value of negative resistance that should be available from the cross-coupled, source-coupled pair (M1 and M2) for oscillation and (c.) design the W/L ratios of M1 and M2 to realize this negative resistance.



Solution

(a.) The equivalent circuit seen by the negative resistance circuit is:



The frequency of oscillation is given as $1/\sqrt{2LC}$ or $\omega_o = 2\pi x10^9$ radians/sec.

Therefore the series resistance, R_s, is found as

$$R_s = \frac{\omega L}{Q} = \frac{2\pi x10^9 \cdot 5x10^{-9}}{5} = 2\pi\ \Omega$$

Converting the series impedance of $2L$ and $2R_s$ into a parallel impedance gives,

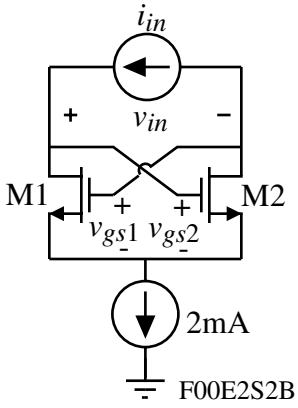
$$Y = \frac{1}{2R_s + j\omega 2L} = \frac{0.5}{R_s + j\omega L} \cdot \frac{R_s - j\omega L}{R_s - j\omega L} = \frac{0.5R_s}{R_s^2 + \omega^2 L^2} - j\frac{0.5\omega L_s}{R_s^2 - \omega^2 L^2}$$

The reciprocal of the conductance is the parallel resistance, R_p, given as

$$R_p = \frac{R_s^2 + \omega^2 L^2}{0.5R_s} = \frac{4\pi^2 + 4\pi^2 \cdot 25}{\pi} = 4\pi(26) = 326.7\Omega$$

$\therefore$ $\underline{\underline{R_{neg} = -104\pi\ \Omega = -326.7\Omega}}$

(b.) The negative resistance seen by the RLC circuit is found as follows.



$$i_{in} = g_{m1}v_{gs1} - g_{m2}v_{gs2} = g_m(v_{gs1} - v_{gs2}) = -g_m v_{in} \qquad \therefore \quad R_{in} = \frac{-1}{g_m}$$

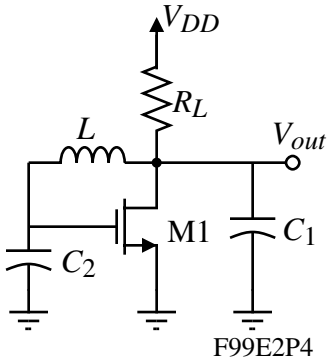
Assuming the 2mA splits evenly between M1 and M2 for the negative resistance calculation gives,

$$\text{Thus, } g_m = g_{m1} = g_{m2} = \frac{1}{104\pi} = \sqrt{2\text{mA} \cdot 110x10^{-6}\,(W/L)} = \frac{\sqrt{W/L}}{2132}$$

$$\therefore\ W/L = \left(\frac{2132}{104\pi}\right)^2 = 42.6 \quad \Rightarrow \quad \underline{\underline{W/L = 42.6}}$$

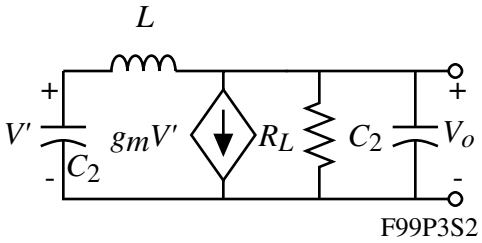
Problem 27

An LC oscillator is shown. Find an expression for the frequency of oscillation and the value of $g_m R_L$ necessary for oscillation. Assume that the output resistance of the FET, r_{ds}, can be neglected.



Solution

An open-loop, small-signal model of this oscillator is shown below.



Writing a nodal equation at the output and input gives,

$$g_m V' + G_L V_o + sC_2 V_o + \frac{V_o - V'}{sL} = 0 \quad \text{and} \quad \frac{V_o - V'}{sL} = sC_2 V' \quad \rightarrow \quad V_o = V'(1+s^2 LC_2)$$

$$\therefore \quad g_m V' + \left(G_L + sC_1 + \frac{1}{sL}\right)(1+s^2 LC_2)V' - \frac{V'}{sL} = 0$$

Assuming a non-zero value of V' gives,

$$g_m + \left(G_L + sC_1 + \frac{1}{sL}\right)(1+s^2 LC_2) - \frac{1}{L} = g_m + G_L + sC_1 + \frac{1}{sL} + s^2 LC_2 G_L + s^3 LC_1 C_2 + sC_2 - \frac{1}{sL} = 0$$

or $\quad (g_m + G_L - \omega^2 LG_L C_2) + j\omega[C_1 - \omega^2 LC_1 + C_2] = 0$

Therefore, the frequency of oscillation is,

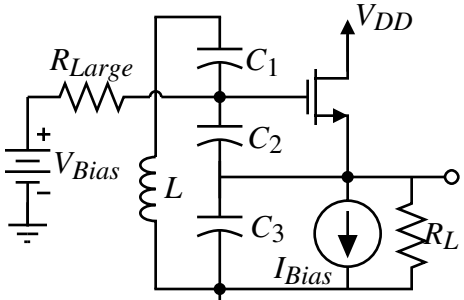
$$\boxed{\omega_{osc} = \sqrt{\frac{C_1 + C_2}{LC_1 C_2}} = \frac{1}{\sqrt{\frac{LC_1 C_2}{C_1 + C_2}}}}$$

The value of $g_m R_L$ necessary for oscillation is

$$g_m + G_L = LG_L C_2 \omega_{osc}^2 = G_L\left(1 + \frac{C_2}{C_1}\right) \qquad \rightarrow \qquad \boxed{g_m R_L = \frac{C_2}{C_1}}$$

Problem 28

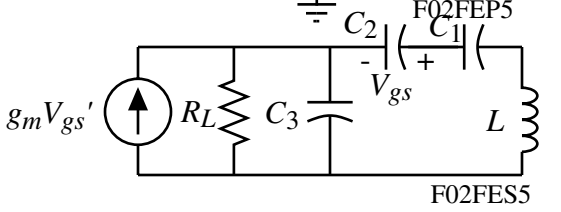
A Clapp oscillator which is a version of the Colpitt's oscillator is shown. Find an expression for the frequency of oscillation and the value of $g_m R_L$ necessary for oscillation. Assume that the output resistance of the FET, r_{ds}, and R_{Large} can be neglected (approach infinity).



F02FEP5

Solution

The small-signal model for this problem is shown below.



F02FES5

The loop gain will be defined as V_{gs}/V_{gs}'. Therefore,

$$V_{gs} = \frac{-g_m V_{gs}' \, R_L \| (1/sC_3)}{R_L \| (1/sC_3) + \frac{1}{sC_1} + \frac{1}{sC_2} + sL} \left(\frac{1}{sC_2}\right)$$

$$= \frac{-g_m V_{gs}' \, \frac{R_L(1/sC_3)}{R_L + (1/sC_3)} \, \frac{1}{sC_2}}{\frac{R_L(1/sC_3)}{R_L + (1/sC_3)} + \frac{1}{sC_1} + \frac{1}{sC_2} + sL}$$

$$T(s) = \frac{V_{gs}}{V_{gs}'} = \frac{\frac{-g_m R_L}{sR_LC_3+1} \, \frac{1}{sC_2}}{\frac{R_L}{sR_LC_3+1} + \frac{1}{sC_1} + \frac{1}{sC_2} + sL} = \frac{\frac{-g_m R_L}{sC_2}}{R_L + (sR_LC_3+1)\left(\frac{1}{sC_1} + \frac{1}{sC_2} + sL\right)}$$

$$T(s) = \frac{-g_m R_L}{sC_2R_L + (sR_LC_3+1)(s^2LC_2 + \frac{C_2}{C_1} + 1)}$$

$$T(s) = \frac{-g_m R_L}{sC_2R_L + s^3R_LC_3LC_2 + sR_L\frac{C_2C_3}{C_1} + sC_3R_L + s^2LC_2 + \frac{C_2}{C_1} + 1}$$

$$T(j\omega) = \frac{-g_m R_L}{[1 + \frac{C_2}{C_1} - \omega^2 LC_2] + j\omega[R_L(C_2+C_3) + R_L\frac{C_2C_3}{C_1} - \omega^2 R_LC_3LC_2]} = 1 + j0$$

$$\therefore \quad C_2 + C_3 + \frac{C_2C_3}{C_1} = \omega_{osc}^2 C_3LC_2 \quad \rightarrow \quad \boxed{\omega_{osc} = \sqrt{\frac{1}{L}\left(\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}\right)}}$$

Also, $g_m R_L = \omega_{osc}^2 LC_2 - 1 - \frac{C_2}{C_1} = C_2\left(\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}\right) - \frac{C_2}{C_1} - 1 = \frac{C_2}{C_3} \rightarrow \boxed{g_m R_L = \frac{C_2}{C_3}}$

Problem 29

The objective of this problem is to use passive LC tank and negative feedback circuit to design an LC oscillator that meets the GSM specification. At first, show the condition that the ideal circuit oscillates at $\omega_{osc} = \frac{1}{\sqrt{LC}}$ and find quality factor, Q. The transistors should be modeled with the standard small-signal model using g_m and r_{ds} or r_{out} in this part of the problem. Second, use SPICE to obtain a transient simulation. Third, simulate the oscillator that replaces the ideal inductor with the lumped inductor model shown, and use the program referenced below [1] to layout the inductor. Use the model parameters given in [2] for this problem.

Fig.1. Ideal LC VCO

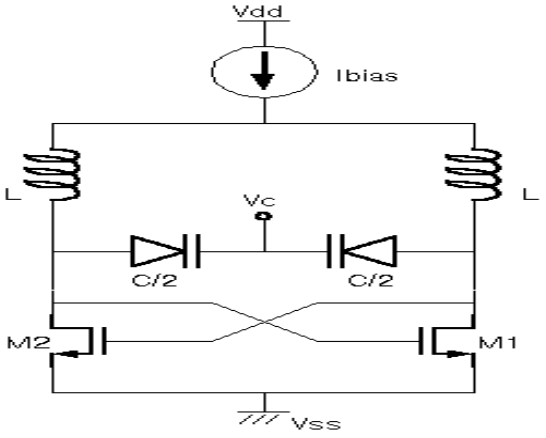
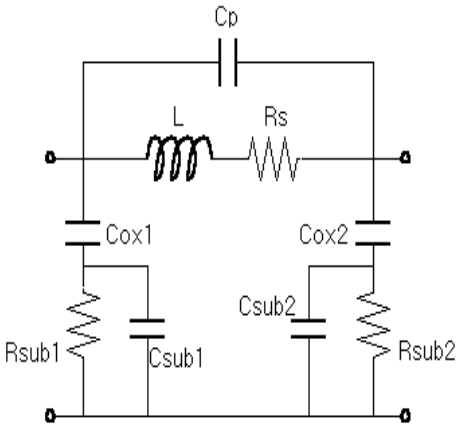


Fig.2. Lumped Inductor Model



GSM specifications:

Frequency range = 935 ~ 960MHz v_c = 0.75 ~ 1.75V

Switching time = 800μsec V_{DD} = 2.5V

Technology parameter:

Metal sheet resistance = 35 mΩ/sq.

Substrate layer resistivity = 0.015 Ω-cm

Metal to substrate capacitance = 5.91 aF/μm^2

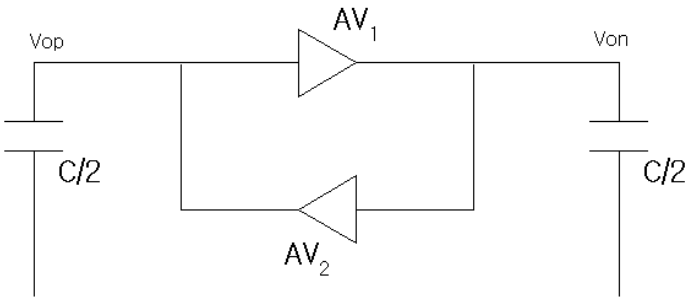
Metal to metal capacitance = 98.0 aF/μm

C_{sub}, R_{sub}, C_p can be ignored

Problem 29 - Continued

Solution

LC VCO equivalent



$A_{v1} = A_{v2} = G_m * (r_{out} \parallel L \parallel C/2)$

$A_{v1}(s) = A_{v2}(s) = G_m \dfrac{1}{\dfrac{1}{r_{out}} + \dfrac{1}{Ls} + \dfrac{C}{2}\,s} = Gm\ s\ L \dfrac{1}{1 + s\dfrac{L}{r_{out}} + s^2\ L\ \dfrac{C}{2}}$ where G_m and r_{out} are the transconductance and the output resistance of M1 and M2 transistors respectively, C/2 is the total output capacitance at the outputs V_{on} and V_{op}. For this circuit to oscillate, the gain around the loop must be equal to negative one; therefore, each cross coupled gain stage can be presented as shown below. Hence, the total gain equation around the loop is equal to $H(s) = \dfrac{A_{v1}(s)}{1 - A_{v1}(s)}$.

Substituting for $A_{v1}(s)$,

$$H(s) = \frac{\dfrac{Gm\ s\ L}{1 + s\dfrac{L}{r_{out}} + s^2\ L\ \dfrac{C}{2}}}{1 - \dfrac{Gm\ s\ L}{1 + s\dfrac{L}{r_{out}} + s^2\ L\ \dfrac{C}{2}}} = \frac{G_m\ s\ L}{1 - s\ L\ (G_m - G_{out}) + s^2\ L\ \dfrac{C}{2}}$$

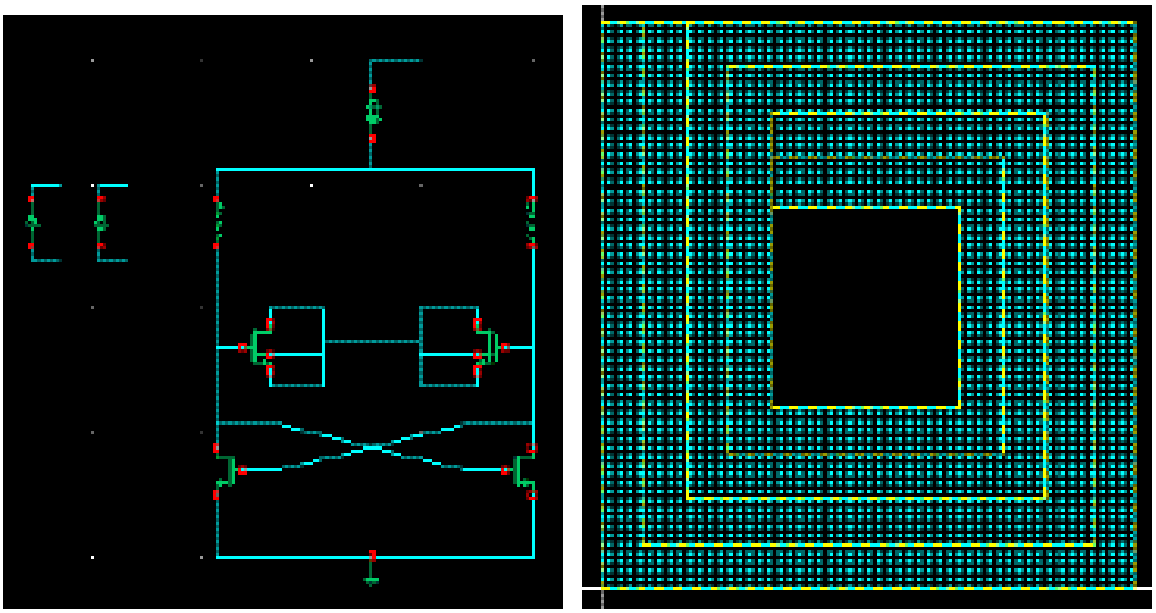
For this circuit to oscillate at $\omega_{osc} = \dfrac{1}{\sqrt{L\dfrac{C}{2}}}$, it is necessary for the s term in the denominator to be equal to zero; hence, $G_m = \dfrac{1}{r_{out}} = G_{out}$

By forcing G_m greater than Gout a pair of complex poles are forced in the right side plane. This is the condition to start oscillation. Once the oscillation starts, the G_{eff} parameter ($G_{eff} = G_m - G_{out}$) approaches zero and the oscillation becomes sustaining, giving a $Q = \dfrac{\sqrt{L\ \dfrac{C}{2}}}{L\ G_{eff}} = \sqrt{\dfrac{C}{2L}}\,R_{eff}$

Problem 29 – Continued

Inductor Layout:

LC VCO schematic and inductor layout



Each element size

Negative resistance transistor(M1 and M2): L=.25um, W=25um, M=20

Accumulation Capcitor(C1 and C2): L=.5um, W=345um, M=50

Ideal inductor size: .865nH

Inductor's layout figure: turns=2, spacing=.5um, width=40um, diameter=250um

Inductor's parasitic resistor, R_s=1.186 Ohms (from layout and its technology parameter)

Inductor's parasitic cap, C_{ox1} and C_{ox2}=160.22fF (from layout and its technology parameter)

Current source: 1mA, Tunning voltage: 0.75~1.75

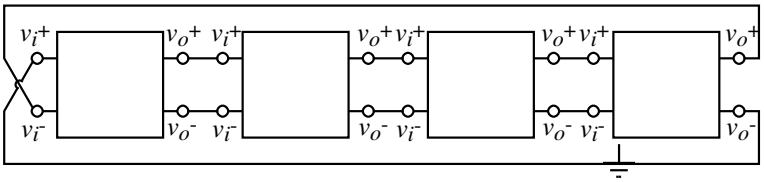
Problem 30

A four-stage ring oscillator used as the VCO in a PLL is shown. Assume that M1 and M2 are matched and M3 and M4 are matched. Also assume that

$$g_m = \sqrt{2K'\frac{W}{L}I_D} \qquad \text{where } K'_N = 100\mu A/V^2 \text{ and } K'_P = 50\mu A/V^2$$

and that $r_{ds} = \infty$. The parasitic capacitors to ground at the outputs are 0.1pF each.

(a.) If I =2mA, find the frequency of oscillation in Hertz. (b.) Find the W/L ratio of M1 (M2) necessary for oscillation when I =2mA. (c.) If the current I is used to vary the frequency, express the relationship between ω_{osc} and I. In otherwords, find $\omega_{osc} = f(I)$.



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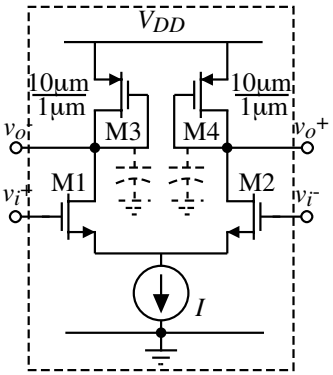


Solution

(a.) The small-signal transfer function of the stages can be written as,

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{g_{m1}/g_{m3}}{s\dfrac{C}{g_{m3}}+1} \quad \rightarrow \quad \text{Arg}\left[\frac{V_{out}(j\omega)}{V_{in}(j\omega)}\right] = -\tan^{-1}\left(\frac{\omega C}{g_{m3}}\right)$$

From the above, we see that each stage must contribute –45° of phase to oscillate. Therefore,

$$\omega_{osc} = \frac{g_{m3}}{C} = \frac{\sqrt{2K'\,10\cdot 0.5I}}{C} = \frac{\sqrt{2\cdot 50\text{x}10^{-6}10\cdot 10^{-3}}}{10^{-13}} = 10^{10} \text{ rads/s} \rightarrow \boxed{f_{osc} = 1.59\text{GHz}}$$

(b.) The gain of the 4-stage ring oscillator at ω_{osc} should be equal to 1 so we can write,

$$1 = \left(\frac{g_{m1}/g_{m3}}{\sqrt{1+1}}\right)^4 = \frac{(g_{m1}/g_{m3})^4}{4} \rightarrow \qquad g_{m1} = 4^{0.25}\, g_{m3} = \sqrt{2}\, g_{m3} = \sqrt{2}\text{ mS}$$

$$\sqrt{2}\text{ mS} = \sqrt{2K'_N\,(W/L)\cdot 1\text{mA}} = \sqrt{2\cdot 100\text{x}10^{-6}\,(W/L)\cdot 1\text{mA}}$$

$$\therefore\ (W/L)_1 = \frac{2\text{mS}}{0.2\text{mS}} = 10 \quad \rightarrow \quad \boxed{(W/L)_1 = 10}$$

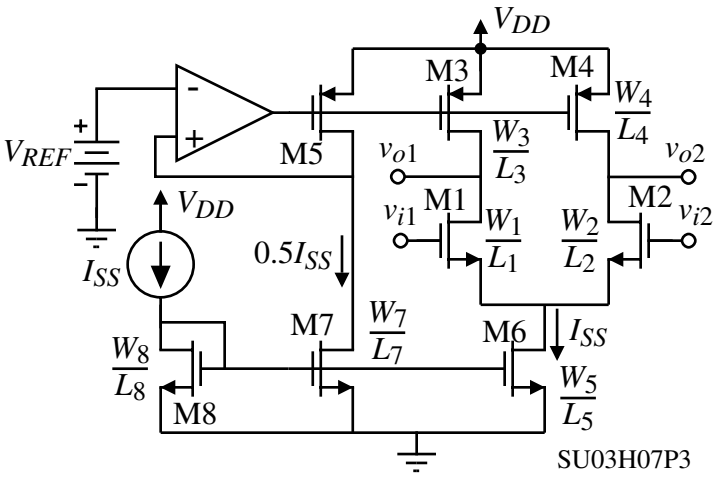
(c.) From part (a.) we get,

$$\omega_{osc} = \frac{g_{m3}}{C} = \frac{\sqrt{2K'\,10\cdot 0.5I}}{C} = \frac{\sqrt{2\cdot 50\text{x}10^{-6}10\cdot 0.5I}}{10^{-13}} = 2.36\text{x}10^{11}\sqrt{I}$$

$$\boxed{\omega_{osc} = 2.36\text{x}10^{11}\sqrt{I}}$$

Problem 31

How does the oscillation frequency depend on I_{SS} for a ring oscillator using the stage shown? Express your answer in terms of V_{DD}, V_{REF}, I_{SS}, the simple large signal model parameters of the MOSFETs (K', V_T, λ) and the W/L values of the MOSFETs.



Solution

This topology uses a replica biasing circuit to define the on-resistance of M3 and M4 based on the on-resistance of M5. The on-resistance of M5 is

$$R_{on5} = \frac{V_{DD} - V_{REF}}{0.5I_{SS}}$$

We can either assume that the W/Ls of M3, M4 and M5 are equal or since we know that R_{on} is inversely proportional to the W/L ratio, we can write that,

$$R_{on3} = R_{on4} = \frac{W_5/L_5}{W_3/L_3} R_{on5}$$

where $W_3/L_3 = W_4/L_4$.

Assuming a capacitance at each output of C_L, allows us to write the transfer function of the ring oscillator stage as,

$$\frac{V_{o2} - V_{o1}}{V_{i1} - V_{i2}} = \frac{g_{m1}R_{on3}}{sR_{on3}C_L + 1}$$

The phase shift due to a stage can be written as,

$$\theta i(j\omega) = -\tan^{-1}(\omega R_{on3}C_L)$$

To oscillate, this phase shift needs to be equal to some value, say k (in degrees). Therefore we can write that,

$$\omega_{osc} = \frac{k}{R_{on3}C_L} = \frac{0.5I_{SS}\ k}{\frac{W_5/L_5}{W_3/L_3}(V_{DD} - V_{REF})C_L}$$

Therefore, the oscillation frequency varies linearly with I_{SS}.

Problem 32

In every practical oscillator, the LC tank is not the only source of phase shift. Hence, the actual oscillation frequency may differ somewhat from the resonant frequency of the tank. Using the time-varying model, explain why the oscillators's phase noise can degrade if such off-frequency oscillations occur.

Solution

If there is any off-frequency oscillations that are close to the actual oscillation frequency or harmonics of it, we know from the LTV theory that these frequencies and their associated noise will "fold" into the noise spectrum around the actual frequency and degrade the oscillator's phase noise. The following diagram illustrates the process.

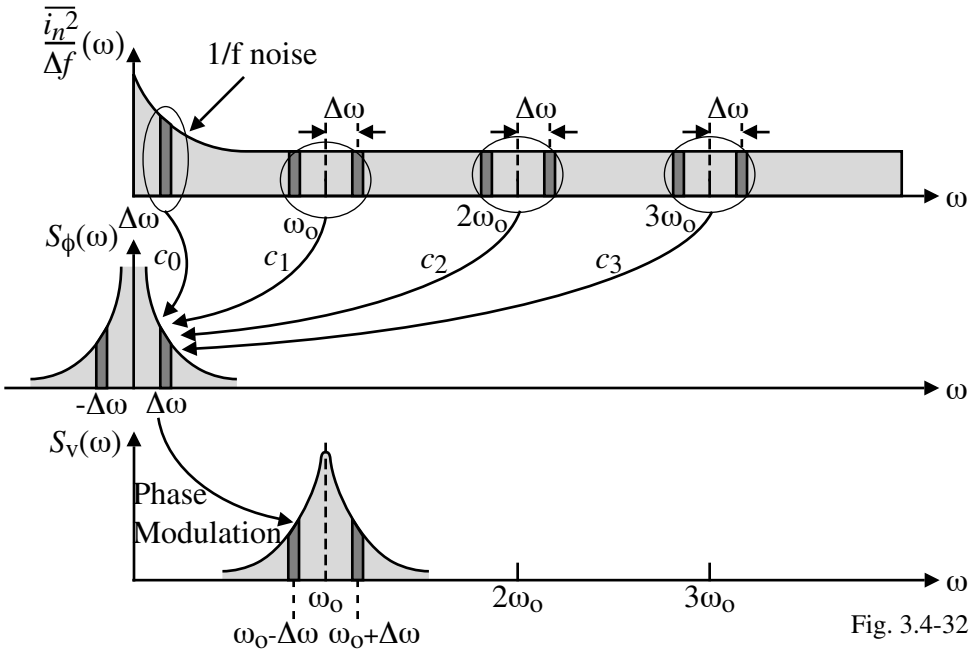
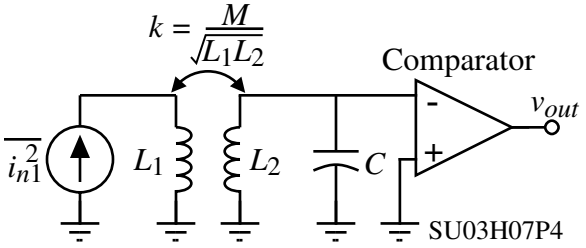


Fig. 3.4-32

Problem 33

Assume that the steady-state output amplitude of the following oscillator is 1V. Calculate the phase noise in dBc/Hz at an offset of 100kHz from the carrier from the signal coming out of the ideal comparator. Assume that L_1 = 25nH, L_2 = 100nH, M = 10nH, and C = 100pF. Further assume that the noise current is



$$\overline{i_{n1}^2} = 4kTG_{eff}\Delta f$$

where $1/G_{eff} = 50\Omega$. The temperature of the circuit is 300°K.

Solution

First of all, several assumptions must be made to work this problem. They are:

1.) The load on the secondary of the transformer approximates a short.

2.) The output of the comparator is a square wave of amplitude 0.5V.

Our objective is to find the value of

$$\mathcal{L}\{f_m\} = 10\log_{10}\left[\frac{\overline{i_{n2}^2}/\Delta f\, \Gamma_{rms}^2}{2q_{max}^2 (f_m)^2}\right]$$

First, the influence of the transformer. The equations of a general transformer are,

$$V_1 = sL_1I_1 + sMI_2 \qquad \text{and} \qquad V_2 = sMI_1 + sL_2I_2$$

If we assume that $V_2 \approx 0$, then $I_2 \approx \frac{M}{L_2} I_1 = 0.1I_1$. Since we are looking at the square of the current, we can write that the noise injected into the tank is

$$\frac{\overline{i_{n2}^2}}{\Delta f} = 0.01\frac{\overline{i_{n2}^2}}{\Delta f} = 0.04kTG_{eff} = \frac{0.04(1.381\text{x}10^{-23})300}{50} = 3.314\text{x}10^{-24}\ \text{A}^2/\text{Hz}$$

Next, we will evaluate Γ_{rms}^2. From the notes (page 160-21), we see that

$\Gamma_{rms}^2 = \frac{1}{2}\sum_{n=0}^{\infty} c_n^2$ where c_n are the coefficients of the ISF represented by a Fourier series.

What are the c_n? We shall assume that the ISF of the LC tank is a sinusoid of the same period. Therefore, only the c_1 coefficient is important. If the peak value of the ISF is 1V (a questionable assumption) then the *rms* value is 0.707. Thus $\Gamma_{rms}^2 \approx 0.25$.

$$q_{max} = Cv_{max} = 100\text{pF}(1\text{V}) = 10^{-10}\ \text{coulombs.}$$

$$\therefore \quad \mathcal{L}\{f_m\} = 10\log_{10}\left[\frac{3.314\text{x}10^{-24}(0.25)}{2\cdot 10^{-20}(10^5)^2}\right] = 10\log_{10}(4.14\text{x}10^{-13}) = -123.82\ \text{dBc/Hz}$$

$$\mathcal{L}\{f_m\} = \underline{\underline{-123.82\ \text{dBc/Hz}}}$$

Problem 34

A crystal reference oscillator and its associated transistor have the following specifications at 290°K.

Output frequency:	6.4MHz
Power output:	+10 dBm
Noise figure:	2.0 dB
Flicker corner:	15 kHz
Loaded Q:	$12\text{x}10^3$

(a.) Determine and plot the SSB phase noise in dBc as a function of the frequency offset from the carrier. Include the frequency range from 10Hz to 10MHz.

(b.) Suppose that this reference oscillator is used with a frequency synthesizer whose transfer function from the reference to the output is

$$\frac{\theta_{n,o}(s)}{\theta_{n,ref}(s)} = \frac{N}{Nref}\frac{2\zeta\omega_n s + \omega_n{}^2}{s^2 + 2\zeta\omega_n s + \omega_n{}^2}$$

where N = 19,000, N_{ref} = 256, ζ = 0.7, and ω_n = 908 sec.$^{-1}$. Make a plot of the SSB reference noise in the output of the synthesizer.

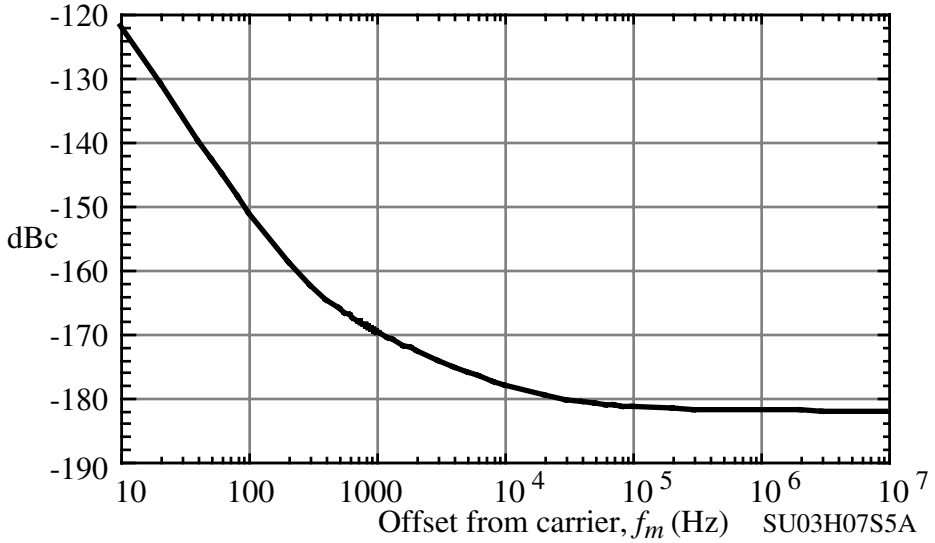
Solution

(a.) NF = 2.0dB, $F = 10^{2.0/10}$ = 1.585, and P_o = 10 dBm = 0.01W

$$\mathcal{L}\{f_m\} = 10\log\left[\frac{FkT}{P_s}\left(1 + \frac{1}{4Q^2}\left(\frac{f_o}{f_m}\right)^2\right)\left(1 + \frac{f_c}{f_m}\right)\right]$$

$$= 10\log\left[\frac{1.585\cdot 1.38\text{x}10^{-23}\cdot 290}{0.01}\left(1 + \frac{1}{4(12\text{x}10^3)^2}\left(\frac{6.4\text{x}10^6}{f_m}\right)^2\right)\left(1 + \frac{15\text{kHz}}{f_m}\right)\right]$$

$$\mathcal{L}\{f_m\} = 10\log\left[6.348\text{x}10^{-19}\left(1 + \frac{71.11\text{x}10^3}{f_m{}^2}\right)\left(1 + \frac{1.5\text{x}10^4}{f_m}\right)\right]$$



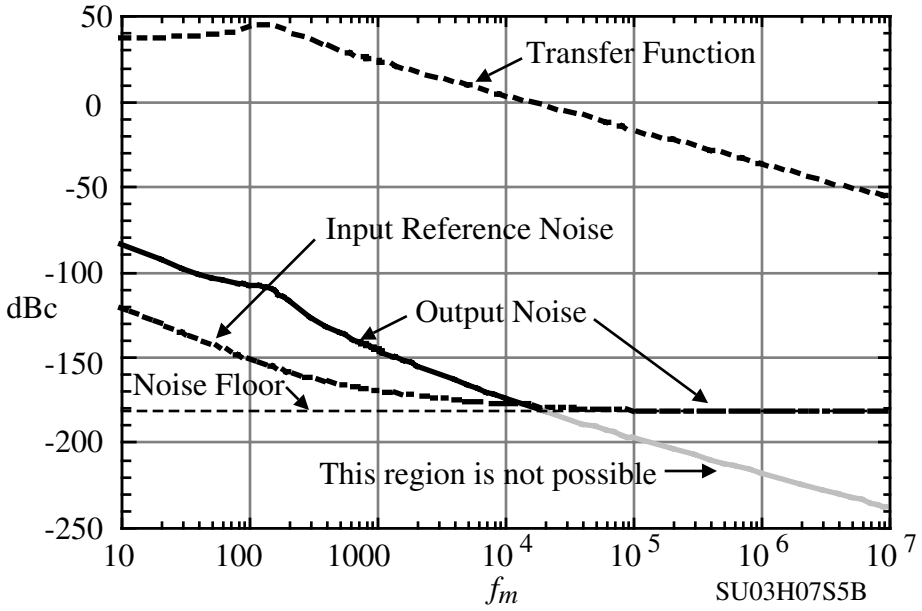
Problem 34

(b.) The VCO phase noise transfer function is

$$\frac{\theta_{n,o}(s)}{\theta_{n,ref}(s)} = \frac{N}{Nref}\frac{2\zeta\omega_n s + {\omega_n}^2}{s^2 + 2\zeta\omega_n s + {\omega_n}^2} = 74.219\,\frac{1271.2s^2 + 8.245\text{x}10^5}{s^2 + 635.6s + 8.245\text{x}10^5}$$

$$\theta_{n,ref}(\text{dBc}) = 10\log\left[\left|\frac{\theta_{n,o}(j\omega)}{\theta_{n,ref}(j\omega)}\right|^2 \mathcal{L}\{f_m\}\right]$$

Below is a plot of the above equation as well as the transfer function, $\theta_{n,o}(s)/\theta_{n,ref}(s)$, and the input reference noise.



Problem 35

Use the National Semiconductor website (www.national.com) to design a DPLL frequency synthesizer for the GSM (935-960MHz) application. The channel spacing is 200kHz. Choose an appropriate VCO from a manufacturer. Assume a 0.25μm CMOS process with a 3.3V power supply.

Your homework should show a block diagram for the resulting frequency synthesizer with the blocks identified. Give the following parameters that you selected for your design:

1.) N, the divider ratio.

2.) ζ, the damping ratio

3.) The type of PD/PFD and the value of K_d.

4.) The type of VCO, K_o, and V_{min} and V_{max}.

5.) τ_L, the lock-in time or settling time and ω_n, the natural frequency of the PLL

6.) Design of the loop filter including the time constants and component values.

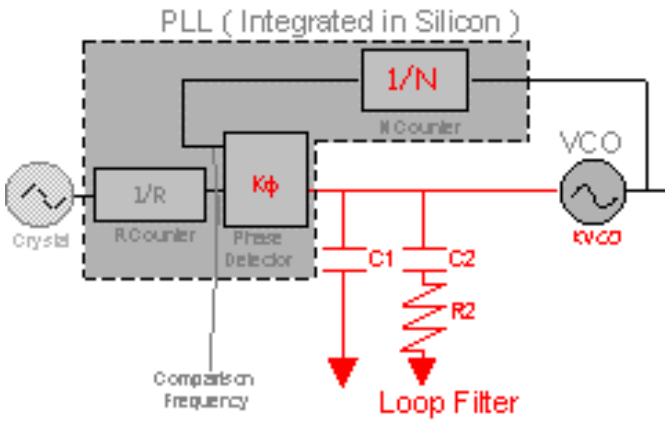
Solution

The problem specifications call for the following:

- Standard : GSM
- Frequency band : 935 MHz ~ 960 MHz
- Channel spacing : 200 kHz
- Power supply : 3.3 V
- Technology : 0.25 μm CMOS
- Switching time : < 800 μs (by GSM standard)

Design

The block diagram for this design is as follows:



The central frequency to use is the geometric mean of the extreme frequencies (947 MHz).

The devices chosen for this design are:

1. A low phase noise PLL (PFD), (chip code LMX2346) from National Semiconductors. This has a range of operation from 200 MHz to 2 GHz, so it is suitable here.
2. A VCO (chip code VCO191-947U) from Vari-L. Its frequency of operation is well-suited for this GSM application: 934 MHz to 960 MHz.
3. A second-order loop filter. This will reduce the number of capacitors in contrast with a higher order filter. And this can be done because the filter components are going to be off-chip, so the needed capacitance values –relatively high– are realizable. This filter is passive so as to avoid the non-idealities associated with an OPAMP (mainly, noise).

Problem 35 - Continued

The comparison frequency at the input of the phase/frequency detector was chosen to be equal to the channel spacing, i.e., 200 kHz. Therefore, the reference divider —ifusing a 10 MHz crystal source at the input— and the feedback divider ratio can be found as:

$$R = \frac{f_{CRYSTAL}}{f_{COMPARISON}} = \frac{10\,MHz}{200\,kHz} = 50$$

$$N = \frac{f_{OUTPUT}}{f_{COMPARISON}} = \frac{947\,MHz}{200\,kHz} = 4735$$

Other parameters for this design are:

VCO

- K_0 = 18 MHz/V
- V_{min} = typ. 0.8 V @ 934 MHz (min. 0.4 V)
- V_{max} = typ. 2.2 V @ 960 MHz (min. 2.6 V)

PFD

- K_ϕ (= K_d) = 4 mA (or $4/2\pi$ [mA/rad])

General

- Lock-in time = τ_L = 200 μs

The filter components were found to be (standard values given, ideal values in parenthesis):

C_1 = 910 pF (943.6 pF)
C_2 = 6.8 nF (6.6 nF)
R_2 = 5.6 kΩ (5.7 kΩ)

Simulation Results

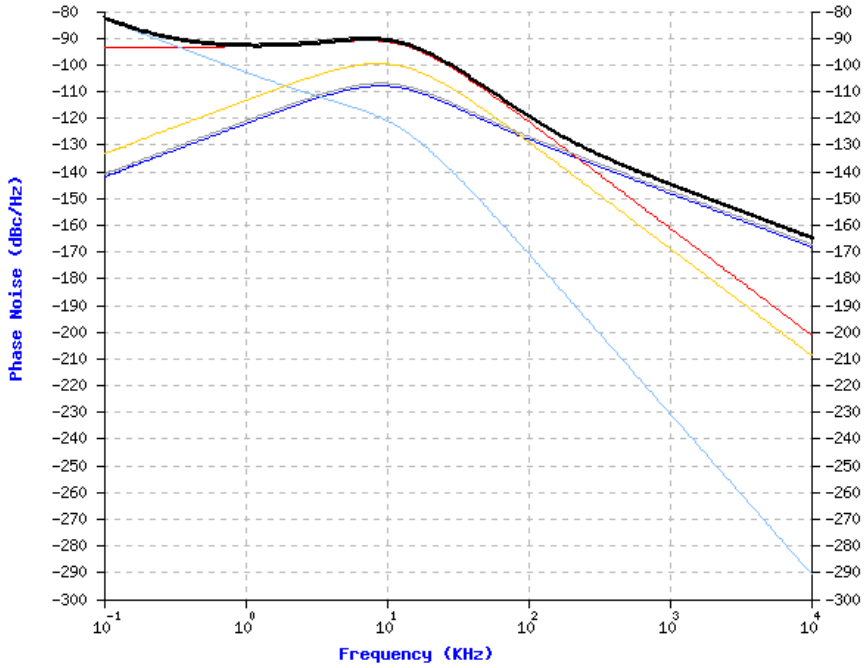
Simulation was performed using the computed *standard* values for the filter components and are as follows:

Phase Noise performance:

- 0 dB bandwidth = 14.80 kHz
- Peak frequency = 7.40 kHz
- Phase noise peaking = 2.47 dB
- Phase noise @ 10 kHz offset = -90.56 dB_c/Hz
- Phase noise @ 100 kHz offset = -118.86 dB_c/Hz
- RMS phase error = 0.33°

Problem 35 — Continued

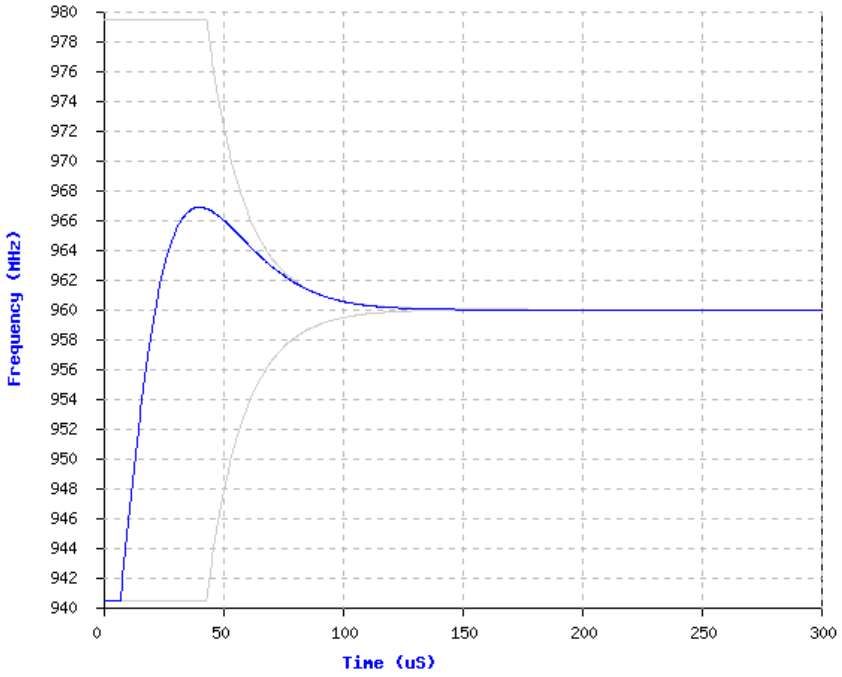
Phase Noise



Total noise
PLL noise
VCO noise
TCXO noise
R_2 noise

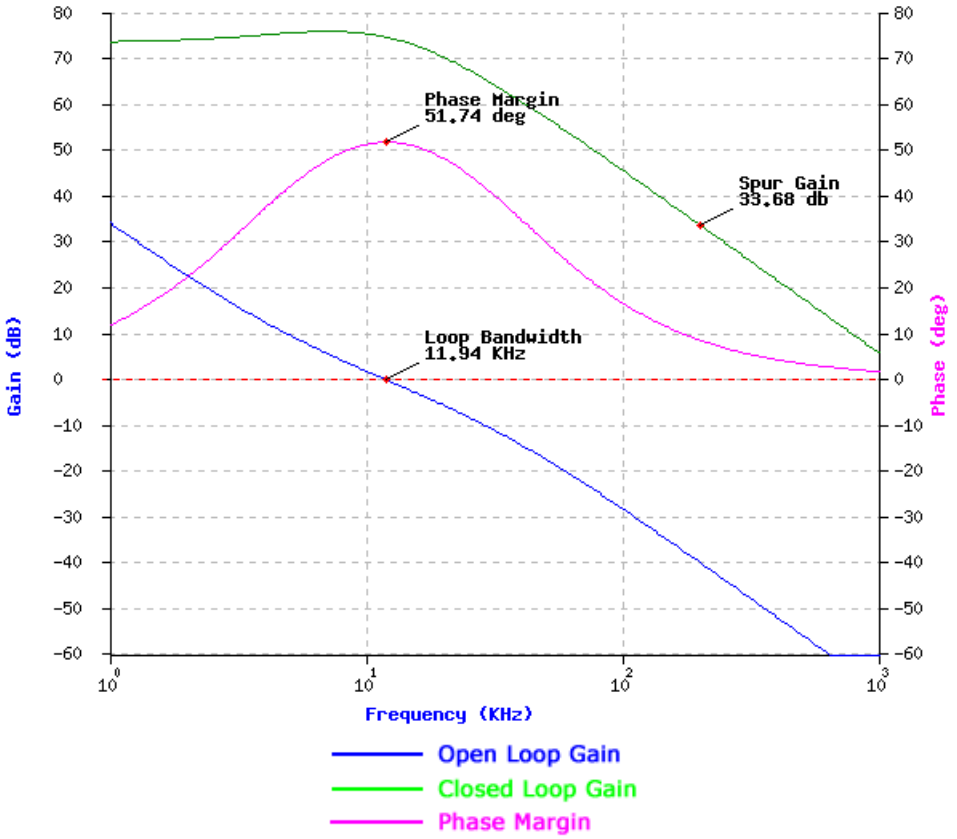
Lock-in time performance for a frequency jump from 934 MHz to 960 MHz (worst case) with a tolerance of 500 Hz:

- Lock-in time = τ_L = 215.31 μs



Problem 35 - Continued

Frequency analysis (Bode plots):



- Natural frequency = ω_n = 7.06 kHz
- Phase margin = 51.74°
- Spur gain at comparison frequency = 33.68 dB
- Loop bandwidth = 11.94 kHz
- Damping factor = ζ = 0.84

Spur level estimation

Spur Offset (kHz)	Description	Spur Gain (dB)	Leakage Component (dB_c)	Pulse Component (dB_c)	Spur Level (dB_c)
200	1st Spur	33.7	-90.5	-76.3	-76.1
400	2nd Spur	21.7	-102.4	-81.2	-81.1
600	3rd Spur	14.7	-109.4	-84.2	-84.2

Therefore, this design is suitable for use in the proposed GSM application.

Problem 36 – (10 points)

The phase noise of an oscillator is –40 dBc at 10 Hz offset and has a straight-line variation (on a dBc vs. log$f$ scale) variation to –85 dBc at 15 kHz offset. Determine the residual phase modulation in the range of 300 Hz to 3 kHz.

Solution

We will solve this problem modeling the phase noise as a simple line on the dBc vs. log f scale as $y = mx + b$ where

y = dBc and x = log$f$

The slope of the curve on the dBc vs. log f scale is found as,

$$m = \frac{-85 - (-40)}{\log(15\text{x}10^3) - \log(10)} = -14.186 \text{ dB/dec.}$$

The intercept, b, can be found as

$-40 = (-14.186 \text{ dB/dec.})\log(10) + b$

$b = -40 + (14.186 \text{ dB/dec})\log(10) = -40 + 14.186 = -25.832$ dBc

$\therefore$ y(dBc) = -14.186 dBc/dec (log$f$) – 25.832 dBc

Let $y = \mathcal{L}\{f\}$ dBc

We can write for both sidebands $\mathcal{L}\{f\} = 2(10^{-(25.832/10)})\, f^{-1.4186}$

Integrating from 300Hz to 3kHz, gives the residual PM,

$$\theta_{rms} = \sqrt{\int_{300}^{3000} 2[10^{-(25.832/10)}]\, f^{-1.4186}\, df} = 0.027 \text{ radians}$$

Problem 37

On page 160-33 of the class lecture notes, the approximate *rms* value of the impulse sensitivity function for single-ended ring oscillators is given as

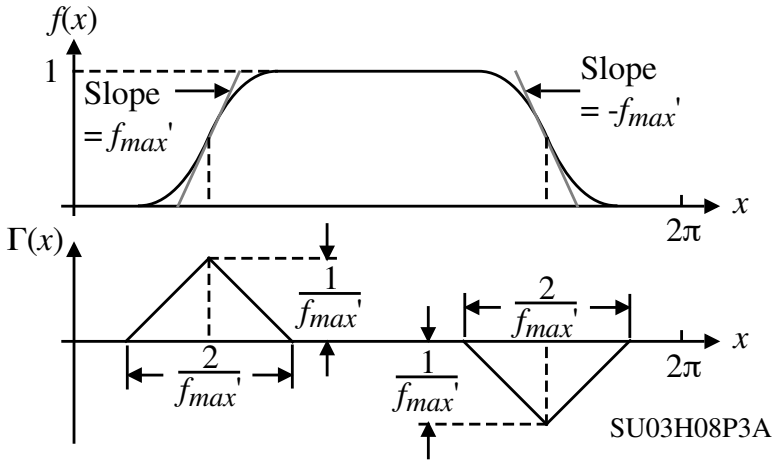
$$\Gamma_{rms} \approx \sqrt{\frac{2\pi^2}{3\eta^3}}\,\frac{1}{N^{1.5}}$$

Derive this approximate impulse sensitivity function.

Solution

This derivation follows that given in A. Hajimiri, et. al., "Jitter and Phase Noise in Ring Oscillators," *IEEE J. of Solid-State Circuits*, vol. 34, no. 6, June 1999, pp. 790-804.

The approximate waveform and the ISF for a single-ended ring oscillator is shown below and is based on the assumptions that the sensitivity during the transition is inversely proportional to the slope and the rise and fall times are symmetrical.



Problem 37 - Continued

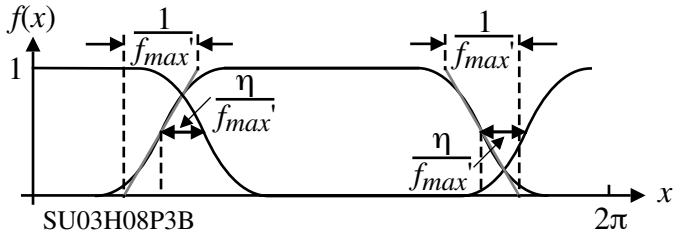
The Γ_{rms} can be estimated as,

$$\Gamma_{rms}^2 \approx \frac{1}{2\pi}\int_0^{2\pi}\Gamma^2(x)dx = \frac{1}{4\pi}\int_0^{1/f_{max}'}x^2dx = \frac{2}{3\pi}\left(\frac{1}{f_{max}'}\right)^3$$

The normalized delay per stage is given as

$$\hat{t}_D = \frac{\eta}{f_{max}'}$$

which is found from the following waveforms of the single-ended ring oscillator.



The period of the ring oscillator is $2N$ times larger than the normalized delay per stage and is

$$2\pi = 2N\hat{t}_D = \frac{2N\eta}{f_{max}'} \qquad \rightarrow \qquad \frac{1}{f_{max}'} = \frac{\pi}{N\eta}$$

$$\therefore \quad \Gamma_{rms}^2 \approx \frac{2}{3\pi}\left(\frac{\pi}{N\eta}\right)^3 = \frac{2\pi^2}{3\eta^3}\frac{1}{N^3}$$

The result is obtained as,

$$\boxed{\Gamma_{rms} \approx \sqrt{\frac{2\pi^2}{3\eta^3}\frac{1}{N^{1.5}}}}$$

Problem 38

A frequency synthesizer has a reference frequency of 5kHz and uses a 64/65 dual-modulus prescaler. Determine the values of the A and M counters to give an output frequency of 555.015 MHz.

Solution

$$f_o = Nf_r$$

$$N = \frac{f_o}{f_r} = 111003$$

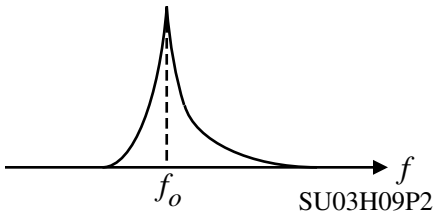
$$N = MP + A$$

$$M = \text{Interger}\left[\frac{N}{P}\right] = \text{Interger}\left[\frac{111003}{64}\right] = 1734, \qquad A = N - MP = 27$$

$$\therefore \quad \boxed{A = 27 \text{ and } M = 1734}$$

Problem 39 – (10 points)

When testing a frequency synthesizer, you observe the frequency display shown above on a spectrum analyzer. What important fact is obvious from the display?



Solution

Asymmetrical sidebands indicate the presence of both PM/FM and AM spurs.

Problem 40 – (10 points)

What is the main advantage of a fractional-*N* PLL synthesizer over an ordinary PLL synthesizer? Explain.

Solution

A fractional-*N* PLL synthesizer gives much high frequency resolution than possible with an ordinary PLL synthesizer having the same reference frequency.

Problem 41 – (10 points)

A 1600 MHz carrier together with a set of 20 kHz PM spurs are applied to a divide by 8 frequency divider. The power of the 200 MHz carrier frequency output of the divider is 0.2 mW and the 20 kHz spurs have an amplitude of 20 μV. What is the phase deviation of the signal at the input of the divider? All impedances are 50 ohms.

Solution

At the output,

$$V_s = 20\text{x}10^{-6}\text{ V} \quad \text{and} \quad P_o = 0.2\text{x}10^{-3}\text{ W}$$

$$\therefore \quad P_s = \frac{|V_s|^2}{50} = 8\text{x}10^{-12}\text{ W}$$

$$SSB = 10\log_{10}\left(\frac{P_s}{P_o}\right) = 10\log_{10}\left(\frac{8\text{x}10^{-12}}{0.2\text{x}10^{-3}}\right) = -73.979\text{ dB}$$

At the input,

$$SSB_{input} = SSB_{output} + 20\log_{10}(N) = -73.979\text{ dB} + 18.062\text{ dB} = -55.92\text{ dB}$$

$$SSB_{input} = 20\log_{10}\left(\frac{\theta_d}{2}\right) \qquad \rightarrow \qquad \theta_d = 2\cdot 10^{SSB_{input}/20} = \underline{\underline{0.0032\text{ radians}}}$$

Problem 42 – (10 points)

In the lecture notes, how a rotational frequency detector works is explained. Use explanation and accompanying diagram to clearly explain how the rotational frequency detector works.

Solution

Rotational Frequency Detector

When referenceless frequency acquisition is desired for CDR applications, a frequency detector as shown below can be used in a frequency locked loop for pulling the VCO frequency to the correct data rate. Once, the VCO frequency is centered to corresponding data rate, the phase locking loop takes over in order to sample the data at optimum sampling point.

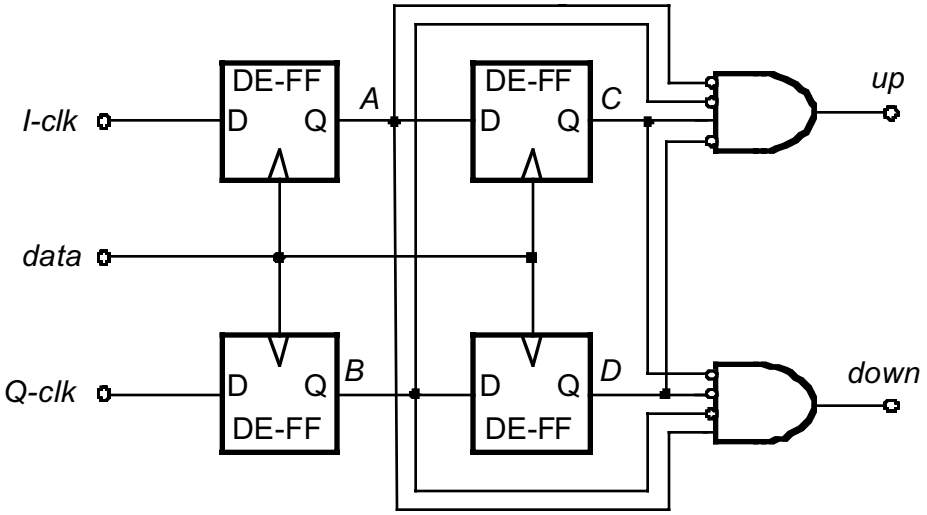


Figure 1: Rotational frequency detector. I and Q clocks come from the VCO. Data is the non-return to zero (NRZ) data to be resampled by the clock and data recovery circuit (CDR). The flip flops are double edge sampling FFs. States A and B hold the present sampled I and Q clocks whereas the C and D hold the previously sampled inputs (A and B are resampled) UP is 1 when AB CD = 00 10. DOWN is 1 when AB CD = 10 00.

A typical frequency detector waveform for data slower than VCO clock is shown below. Note that, anytime when AB changes from 00 to 10 a DOWN pulse is generated. In this example, there is no UP pulse since no 10 to 00 transition occurs.

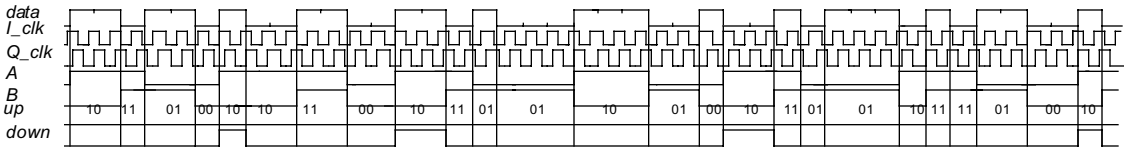


Figure 2: Typical FD waveform example.

In figure below, the I and Q VCO clocks are 12.5% faster than the incoming sampling clock. As a result, the beat frequency (frequency offset between VCO and sampling clocks) vector shown, takes 8 samples in counterclockwise direction to come to its initial position. Initially, the sampling clock is sampling I and Q clocks when I is low and Q is high (01). Next time, it samples IQ=01 one more time. Next two times, it samples 00. The next sampling result is 10. The decision point is 00 to 10 transition or 10 to 00 transition. In the former one, a DOWN signal is produced and in the later case an UP pulse is produced. During the entire beat period (i.e., 8 samples) only one down pulse is produced).

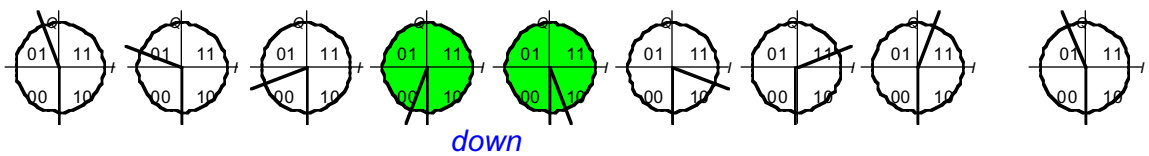


Figure 3: IQ clocks are 12.5% faster than sampling clock.

Problem 42 - Continued

In the example below, VCO clock is 25% faster. Therefore, the beat frequency completes its full rotation in 4 cycles. In 8 cycles there are two 00 to 10 transitions or equivalently two DOWN pulses are produced by the frequency detector.

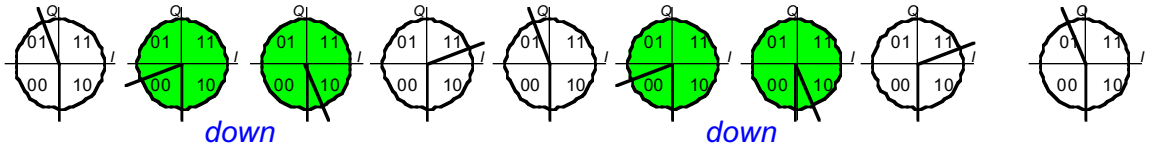


Figure 4: IQ clocks are 25.0% faster than sampling clock.

Now, let s look at what happens if the VCO clock is 37.5% faster than the sampling clock. The beat frequency rotation vector comes to its starting position in 8 cycles, and during which only one 00 to 10 transition is made. Note that from the 4th position to 5th position, the beat frequency vector, skip the quadrant 00. Therefore, the past state of the sampling state CD and present sampling state AB which goes to the four input AND signals are 01 and 10. As a result, both outputs remain at 0. No UP and DOWN generated when one of the decision quadrants are skipped.

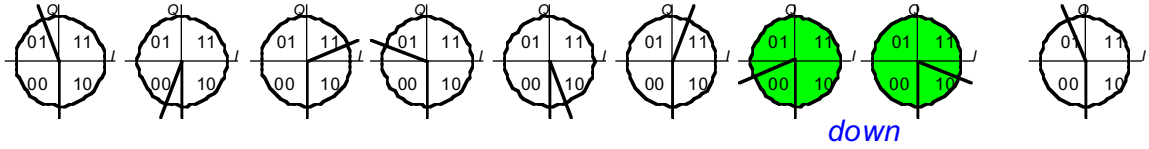


Figure 5: IQ clocks are 37.5% faster than sampling clock.

When the speed difference is 50%, there is no 00 to 10 transition. As a result no UP/DOWN pulses generated.

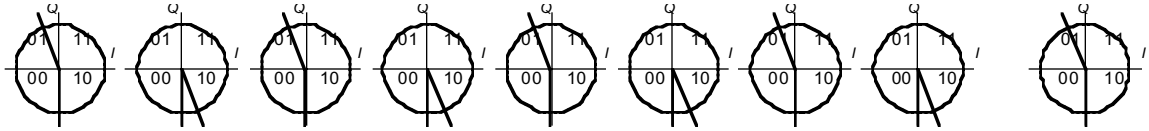


Figure 6: IQ clocks are 50% faster (or slower) than sampling clock.

The case where VCO is 62.5% percent faster than the sampling clock: During the 8 sampling period in which the beat frequency vector comes to its initial starting point, there is only one transition between quadrants 3 and 4. This transition, however is on the reverse direction. That is CD=10 to AB=00. The AND gates in this case generate an UP pulse. To the frequency detector, VCO appears to be 37.5% slower instead of 62.5% faster. A wrong pulse is generated.

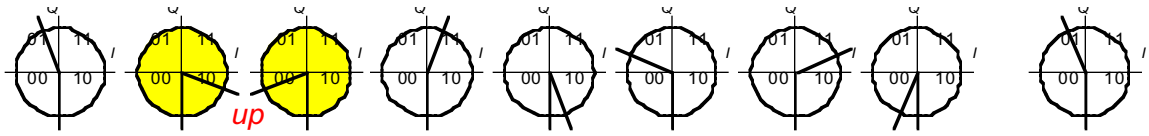


Figure 7: IQ clocks are 50% faster (frequency detector interprets this as VCO is 37.5% slower) than sampling clock.

The above examples is for the case when VCO is faster. The case in which the VCO is slower can be plotted similarly. When VCO is slow, the beat frequency vector traverses the IQ quadrant planes in clockwise direction. In the light of above vector diagrams, the following frequency detector output vs. frequency input waveform can be plotted.

Problem 42 - Continued

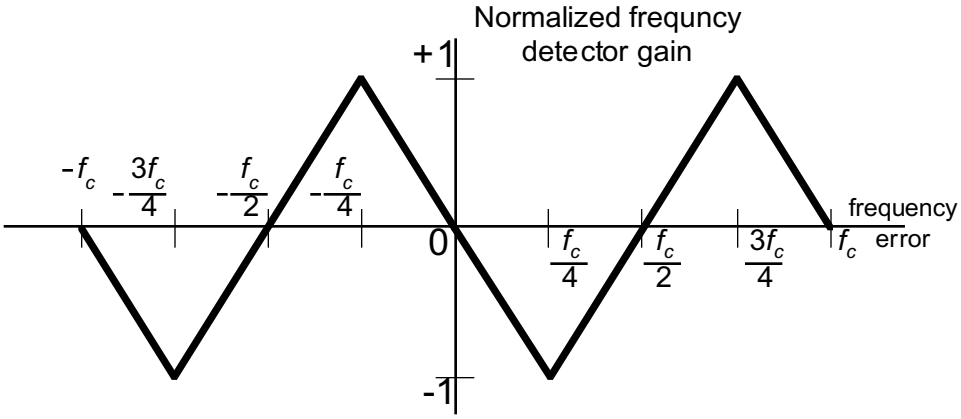


Figure 8: Frequency detector characteristics when the sampling input is clock instead of NRZ data.

Note that, the pulling range of this frequency detector is +/-50% when a full rate clock signal is rising (or falling) edge samples the I and Q VCO clocks, instead of data sampling the I and Q clocks at both rising and falling edges. This case is explained below.

From Figure 8, the detector gain is maximum for +/-25% frequency offset. (Two DOWN pulses in Figure 4 above). Above +/-50% frequency offset, the output changes polarity and VCO frequency is pulled to the wrong direction. The useful range is, therefore only +/-50%.

The above phase diagram example is for the case if the frequency detector input is a full-rate clock instead of NRZ data. We further assumed that, I and Q clocks are sampled only at one edge of the clock (either rising or falling). A pseudo random NRZ data resembles to a clock with 1/4th of the full speed clock as far as the transition density is concerned. If this fact is combined with the double edge sampling nature of the actual frequency detector, the data sampling the I and Q clocks can be assumed as half the full speed clock. That is, in above phasor diagrams, the IQ clocks are effectively sampled every other time. In this case, the frequency detector characteristics, changes polarity when VCO range exceeds +/-25% of the data rate. For actual data inputs, therefore the frequency characteristics resembles to the following figure. The rounded edges of the gain characteristics is due to the pseudo random nature of the input bit sequence (PRBS).

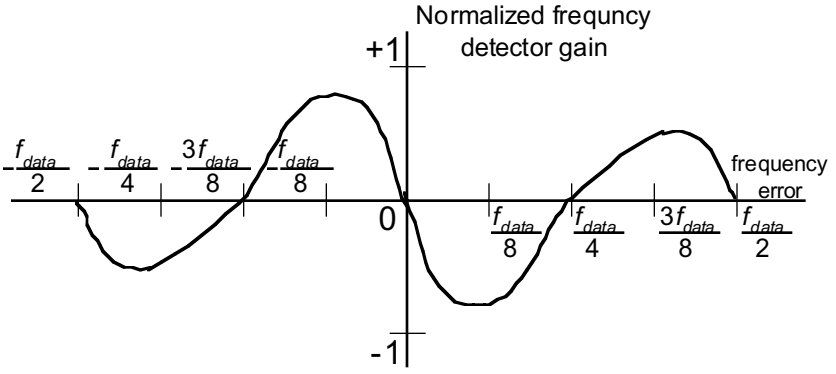


Figure 10: Rotational frequency detector characteristics for PRBS NRZ data.