LAB02 – BANDGAP DESIGN

Overview:

The objective of this laboratory is to design a bandgap voltage reference that will be insensitive to temperature, power supply, and process.

This voltage reference can be used in future laboratories

The steps in the laboratory are:

- Specifications
- Approach
- Simulation/Test Benches

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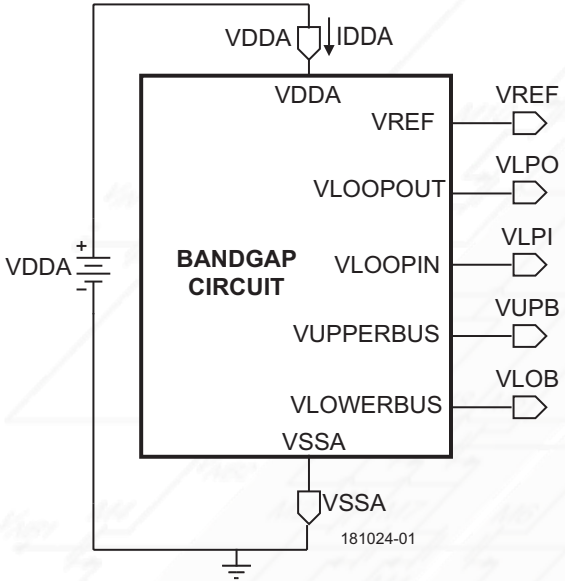
Version 190802

Lab02 - Specifications

Specifications

Technology - xFab XH035B

Block diagram:



Parameter	Symbol	Min	Typ	Max	Units
Power Supply Voltage	VDDA	3	3.3	3.6	V
Ground	VSSA	0	0	0	V
Bulk Bias Voltage	VBBA	0	0	0	V
Junction Temperature	TJ	-40	27	175	°C

Note: You are only responsible for the circuits within the box labelled **BANDGAP CIRCUIT**

Lab02 - Specifications

Specifications – Continued

(VDDA = 3.3V, TJ = 27°C, C_L = 5pF unless otherwise specified below)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Bias Current for Bandgap	IDDA	VDDA=3.3, TJ= 27°C			10	µA
Output Voltage Process Dependence	VREF(P)	Over Strong-Weak Corners	1.34	1.35	1.36	V
Output Voltage Temperature Dependence	VREF(T)	Over -40°C≤T≤125°C	1.34	1.35	1.36	V
Output Voltage VDDA Dependence	VREF(VDDA)	1.65 ≤ VDDA ≤ 3.3	1.34	1.35	1.36	V
VREF dependence on VDDA	PSR	vref/vdda at 1kHz			-60	dB
Phase Margin	PM	PM of combined ±feedback loops	50			Deg
VREF from Start Up Test Bench	VREF(SU)|	|1.35-VREF(SU)| at 100µs			10	mV

Test Bench 1

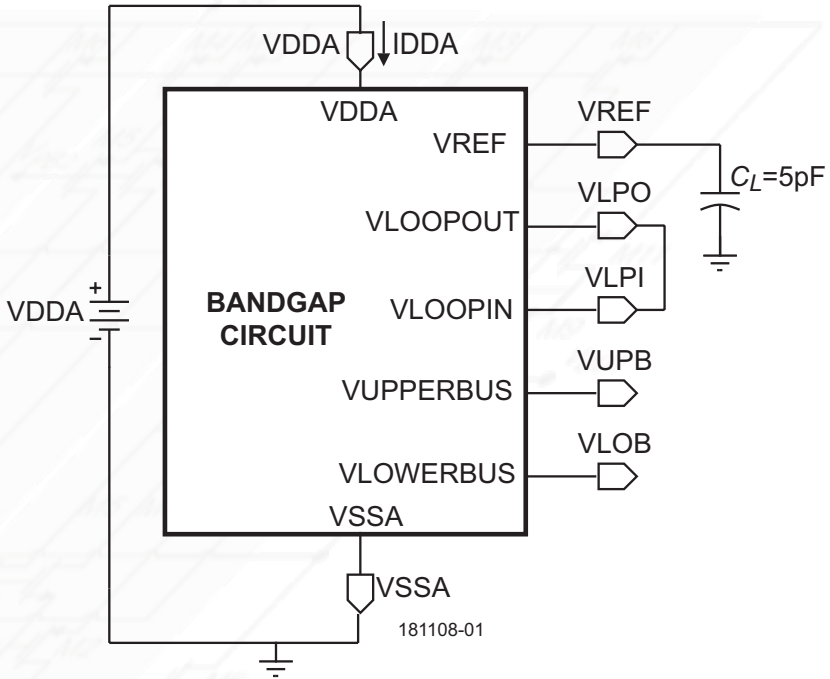
IDDA and VREF(P)- DC OP

This Test Bench does the following:

1.) Uses the following worst case models to determine the variation in VREF when VDDA = 3.3V.

- wp = worst case power = fast NMOS and fast PMOS
- ws = worst case speed = slow NMOS and slow PMOS

2.) Determines IDDA for nominal model, tm

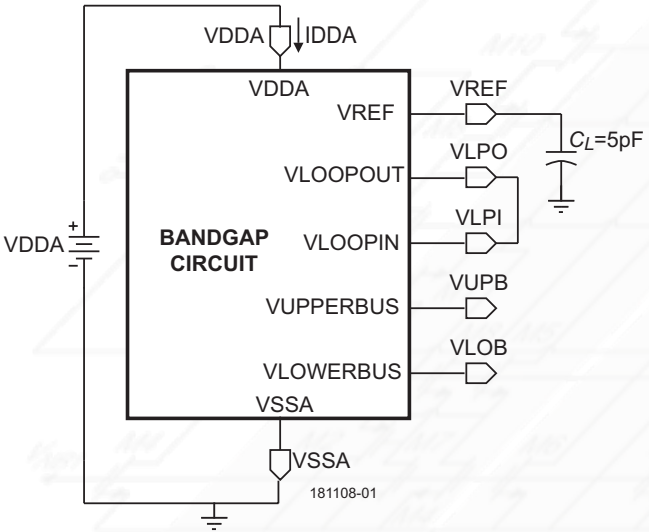


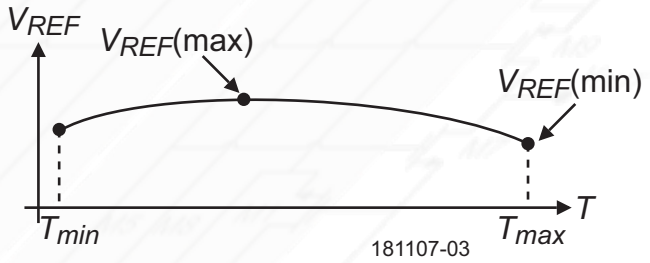
Test Bench 2

VREF(T) – TEMPERATURE SWEEP

This Test Bench does the following:

1.) Sweeps the temperature from -40°C to 125°C to find the minimum and the maximum value of VREF at VDDA = 3.3V and for nominal parameters.





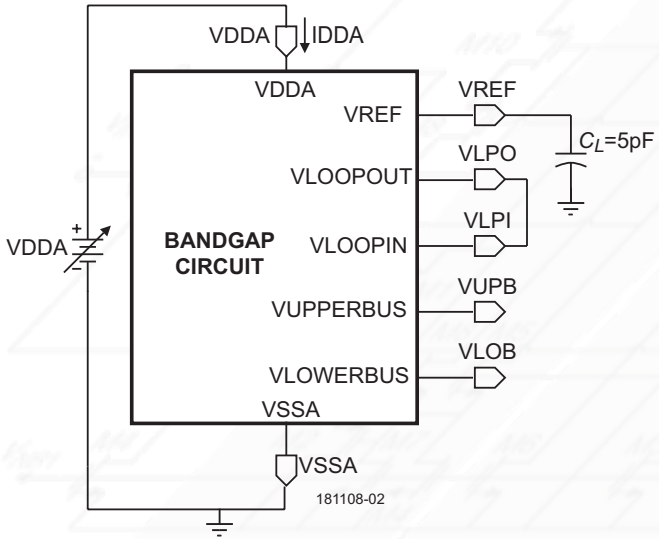
$$TC = \frac{[V_{REF}(max) - V_{REF}(min)] \times 10^6}{V_{REF}(Nom) \times (T_{max} - T_{min})}$$

Test Bench 3

VREF(VDDA) – DC SWEEP

This Test Bench does the following:

1.) Measures the maximum and minimum value of VREF as VDDA is swept from 1.65V to 3.3V at T = 27°C.

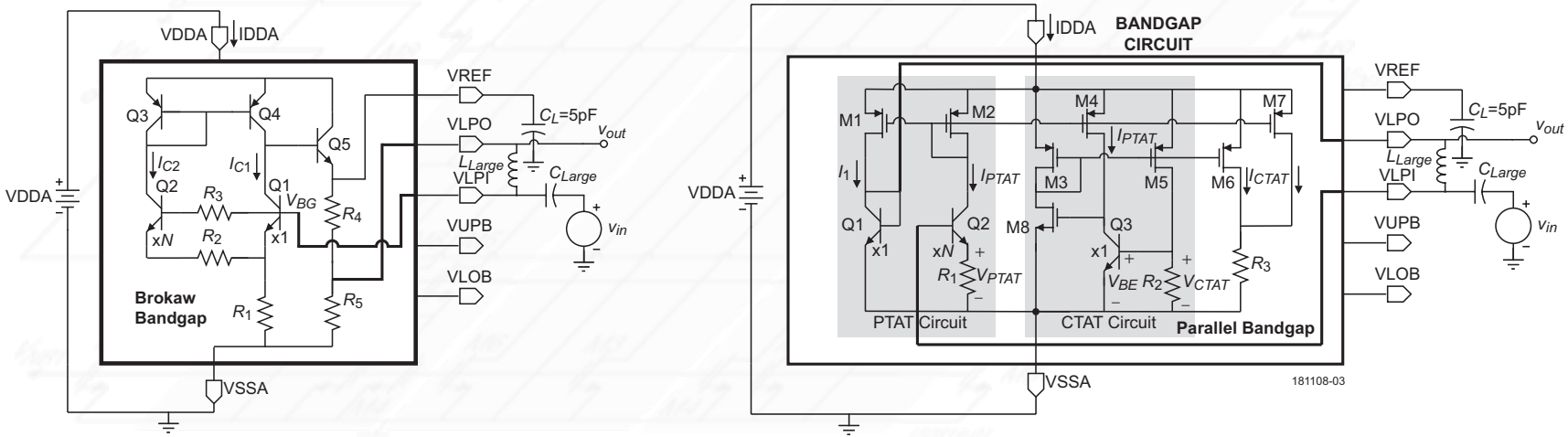


Test Bench 4

PHASE MARGIN - OPEN LOOP SWEEP

This Test Bench does the following:

1.) Measures the magnitude and phase of the combined ±feedback loops. You are responsible for designing your circuit so the connection from VLPO to VLPI is in series with the ±feedback loops of your design. If you design the parallel bandgap, test only the PTAT circuit for stability and ignore the CTAT circuit.

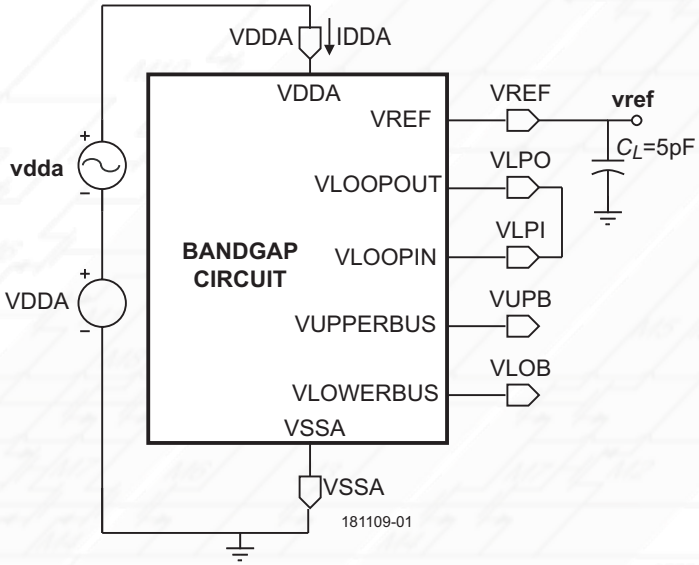


Test Bench 5

Power Supply Rejection – AC SWEEP

This Test Bench does the following:

1.) Applies a 1VAC in series with VDDA and measures the AC value of VREF at VDDA = 3.3V and T = 27°C.



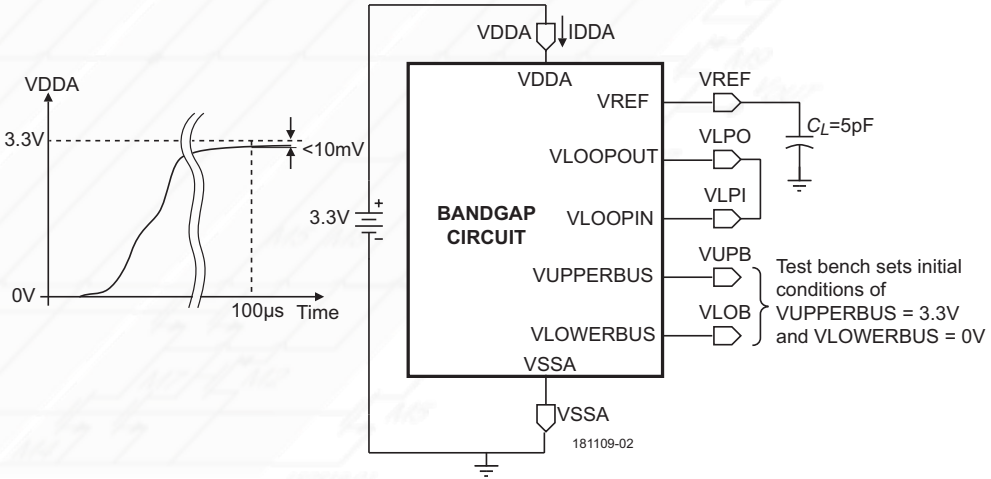
Test Bench 6

Start Up Test – TRAN with INITIAL CONDITIONS

This Test Bench does the following:

1.) Sets the initial conditions for the upper and lower busses of the bandgap design to 3.3V and 0V respectively and does a transient analysis. The output should be with ±10 mV of VREF for VDDA = 3.3V, typical model parameters, and T = 27°C at 100µs.

The upper bus is the common gates/bases of the current mirror PMOS/BJT transistors and lower bus is the common gates/bases of the current mirror NMOS/BJT transistors.



Electrical Design

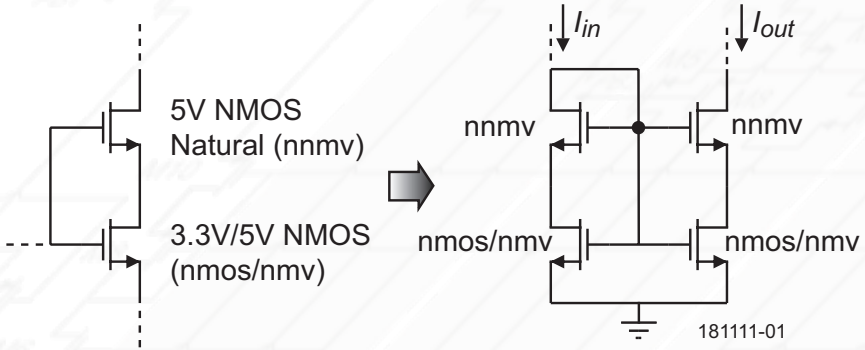
Steps

1. Choose one of the appropriate design procedures
2. Hand design using an appropriate design procedure
3. Use the test benches to determine the performance of your design keeping your design constant from test bench to test bench
4. After you have used the test benches provided to simulate your circuit, a specification sheet will be generated to indicate how well your circuit meets the specifications.
5. If you did not meet specifications, you are encouraged to modify your circuit in an attempt to meet specifications

Tips and Tricks

Helpful Ideas for Lab02

1. Use 5V natural to avoid V_{DS} problems in matching



2. Use resistors with low temperature coefficients for temperature sensitive circuits
3. Make sure all current mirrors match well over temperature
4. Adjust bandgap by increasing or decreasing the PTAT (or CTAT) contribution to the output reference voltage

Performing Lab02

Instructions

1. Go to efabless.com
2. Register using your LinkedIn account (get one if you don't already have one)
3. Agree to the terms
4. Receive approval to access the efabless platform by email
5. Click on the following link
   https://efabless.com/design_catalog/lab/AWgvI4enfpIjxkLb_BSd/
6. Click on the "Clone hard IP" button to have a copy of the Lab02 template placed in your Open galaxy project space which can be renamed
7. Create your design using Electric and connect it to the correct pins
8. Simulate your design using NGSpice to make sure it will meet the specifications
9. When the design is complete, click the "Characterize" button in the Open galaxy project manager followed by the "Simulate All" button and the "Save" button when finished
10. Modify your design as necessary and re-characterize it to meet the specifications
11. When complete, go to the Dashboard, click on My Projects and share the project with Dr. Allen by typing "Phillip Allen" in the "Share With" box

Help with Electric and NGSpice

Videos

The following two lessons provide examples of how to use Electric for schematic capture and NGSpice and SymProbe for simulation and viewing.

Lesson 6 – How to Use Electric

Lesson 7 – How to Use NGSpice

Summary – Lab02

Bandgap Design

- Understand the lab specifications
- Selection of an appropriate design procedure and topology
- Develop the design using the design procedure
- Use test benches to simulate and determine performance
- Modify as necessary

You will have opportunity to use this circuit to provide a stable voltage reference in future laboratories