LECTURE 1 - HOW TO DESIGN BIAS CIRCUITS INDEPENDENT OF V_{DD} AND TEMPERATURE

Topics:

- How temperature influences circuit performance
- Bias voltages independent of V_{DD} (V) and temperature (T)
- Series and parallel bias circuits
- Design procedures
- Examples

What will I learn?

- The principles of V_{DD} (V) and temperature (T) influence
- How to design voltage and current bias circuit that minimize the influence of temperature

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Temperature Influence (T) on Bias Circuits

How does temperature influence circuits?

1. MOSFETs: $i_D = \frac{K'_N W}{2L}(V_{GS} - V_T)^2$

$$K'_N(T) = K'_N(T_0)\left(\frac{T}{T_0}\right)^{-1.5} \text{ and } V_T(T) = V_T(T_0) + \alpha(T - T_0)$$

$\alpha \approx$ -2mV/°C to -3mV/°C for NMOS (PMOS has a positive sign)

2. BJTs: $i_C = \beta I_s exp\left(\frac{V_{BE}}{V_t}\right)$

$$\beta(T) \cong \beta(T_0)\left(\frac{T}{T_0}\right)^2, I_s(T) = AT^{\gamma} exp\left(\frac{-V_{BG}}{V_t}\right), \text{ and } V_t = \frac{kT}{q}$$

A is a temperature independent constant

3. Resistors:

$$R(T) = R(T_0) + TC_1 \times (T - T_o) + TC_2 \times (T - T_o)^2 + \cdots$$

4. Capacitors:

$$C(T) = C(T_0) + TC_1 \times (T - T_o) + TC_2 \times (T - T_o)^2 + \cdots$$

Temperature Independent Bias Circuits

Principle

Cancel a positive going TC with a negative going TC

$$V_{REF} = V_{PTAT}(T) + K \cdot V_{CTAT}(T)$$

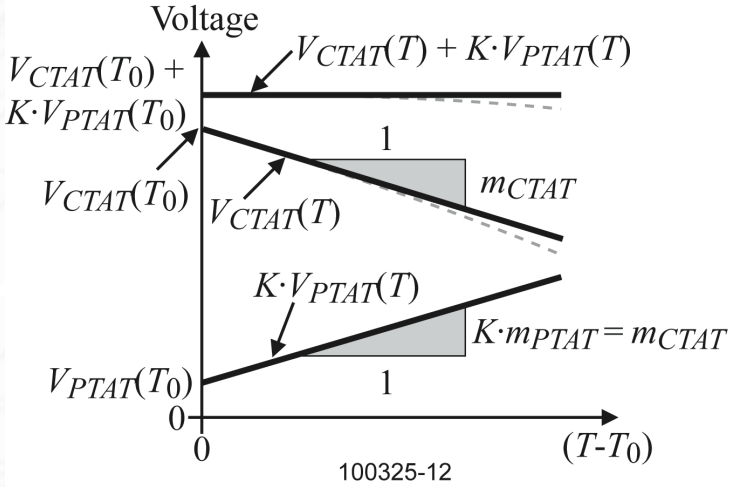
where

$V_{PTAT}(T)$ is a voltage that is *proportional to absolute temperature* (PTAT)

$V_{CTAT}(T)$ is a voltage that is *complimentary to absolute temperature* (CTAT)

and

K is a temperature independent constant that makes $V_{REF}(T)$ independent of temperature

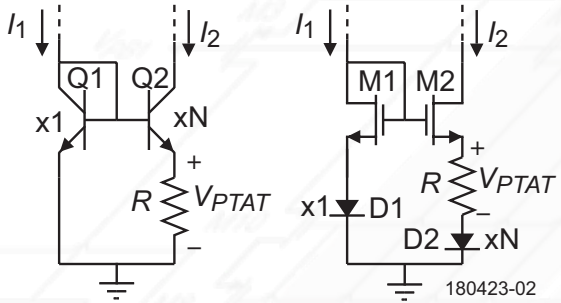


Problem – finding true PTAT and CTAT voltages!

PTAT and CTAT Voltages

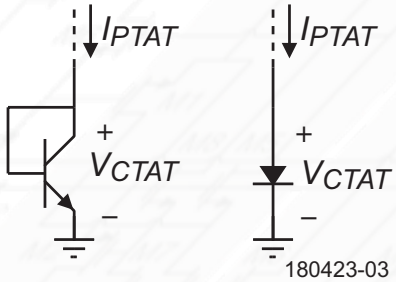
PTAT and CTAT Circuits

PTAT:



$$V_{PTAT} = V_t ln(N) \text{ if } I_1 = I_2$$

CTAT:



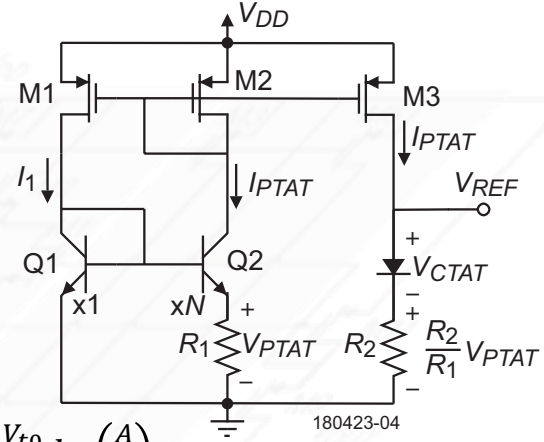
Nonlinear term

$$V_{CTAT} = V_{BG} - V_t(\gamma - \alpha) ln(T) - V_t ln\left(\frac{A}{B}\right)$$

where $I_s = AT^{\gamma} exp\left(\frac{-V_{BG}}{V_t}\right)$ and $i_{PTAT} = BT^{\alpha}$

Temperature and V_{DD} Independent Sources

Simple Series Bias Circuit



Circuit:

$$V_{REF} = I_{PTAT}R_2 + V_{CTAT} = (R_2/R_1)V_{PTAT} + V_{CTAT}$$
$$= KV_{PTAT} + V_{CTAT}$$

Substituting for V_{PTAT} and V_{CTAT} gives,

$$V_{REF} = KV_t \ln(N) + V_{BG} - V_t(\gamma - \alpha)ln(T) - V_t ln\left(\frac{A}{B}\right)$$

Differentiating with respect to T and setting $T=T_0$ gives,

$$\frac{dV_{REF}}{dT}(T = T_0) = K\frac{V_{t0}}{T_0}\ln(N) - \frac{V_{t0}}{T_0}(\gamma - \alpha)ln(T_0) - \frac{V_{t0}}{T_0}(\gamma - \alpha) - \frac{V_{t0}}{T_0} ln\left(\frac{A}{B}\right)$$

Setting the derivative equal to zero, gives,

$$K \ln(N) - ln\left(\frac{A}{B}\right) = (\gamma - \alpha)[1 + ln(T_0)]$$

Substituting back gives,

$$V_{REF} = (\gamma - \alpha)V_t[1 + ln(T_0)] + V_{BG} - V_t(\gamma - \alpha)ln(T) = V_{BG} + (\gamma - \alpha)V_t\left[1 + ln\left(\frac{T_0}{T}\right)\right]$$

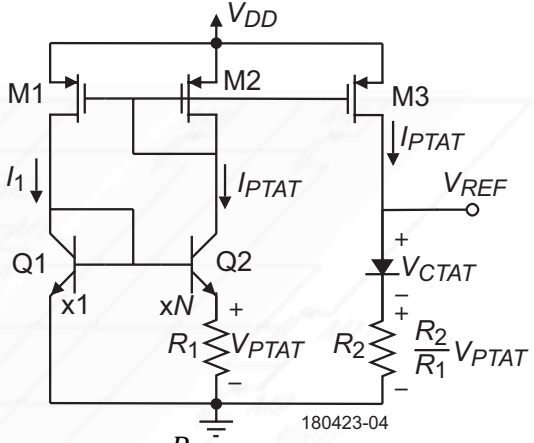
At $T = T_0$, the reference voltage is

$$V_{REF} = V_{BG} - V_t(\gamma - \alpha) = 1.205\text{V} + 0.057\text{V} = 1.262\text{V}\ (T = T_0 = 27°\text{C})$$

Temperature and V_{DD} Independent Sources

Design Procedure BT1

Step	Design Equations	Comments
1	Select I_1 and I_{PTAT}	$P_{diss} = V_{DD}(I_1 + 2I_{PTAT})$
2	Use Design Procedure BV1† to design Q1, Q2, M1 and M2. Let M3 = M2	
3	$R_1 = V_{PTAT}/I_{PTAT}$	
4	$R_2/R_1 = -\left(\frac{dV_{CTAT}/dT}{dV_{PTAT}/dT}\right) = -\left(\frac{dV_{CTAT}/dT}{200\mu V/°C}\right)$	$\frac{dV_{CTAT}}{dT} \approx$ -2mV/°C
5	$V_{REF} \approx$ 1.262V regardless and will require a startup circuit††	



$$V_{REF} = \frac{R_2}{R_1}V_{PTAT} + V_{CTAT}$$

Example 1

Use Example 1 of Bias Design Independent of V_{DD} and Process to design a series reference voltage.

1.) From BV1, I_{PTAT}=2μA, all PMOS are 50μm/10μm, area of Q1 is 10μm² and Q2 = 100μm² (actually replicate Q1 10 times), and R_1=29.93kΩ

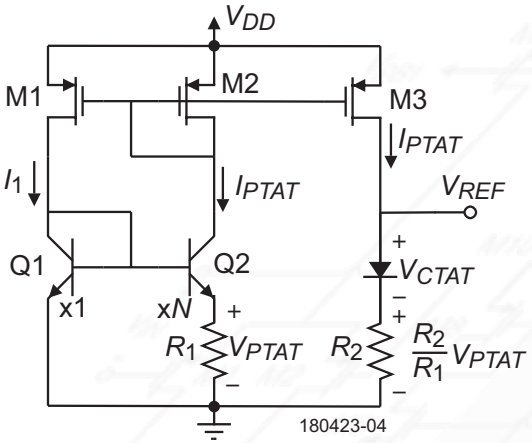
2.) R_2/R_1 = -[(-2000μV/°C)/(200μV/°C)] = 10 → R_2 = 10x29.93kΩ =299.3kΩ

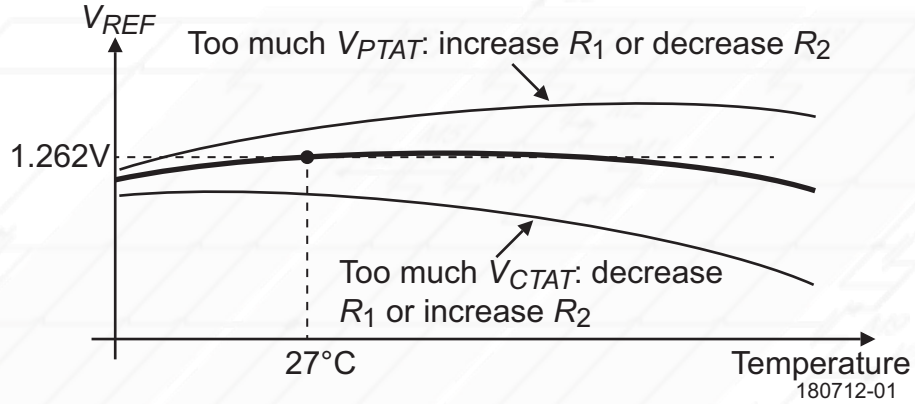
† See how to design common source bias circuits independent of V_{DD}

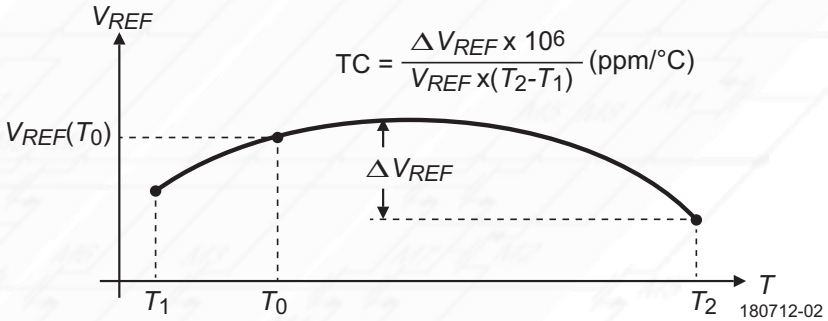
†† See how to design startup circuits

Temperature and V_{DD} Independent Sources

Tuning the Simple Temperature Independent Bias Circuit



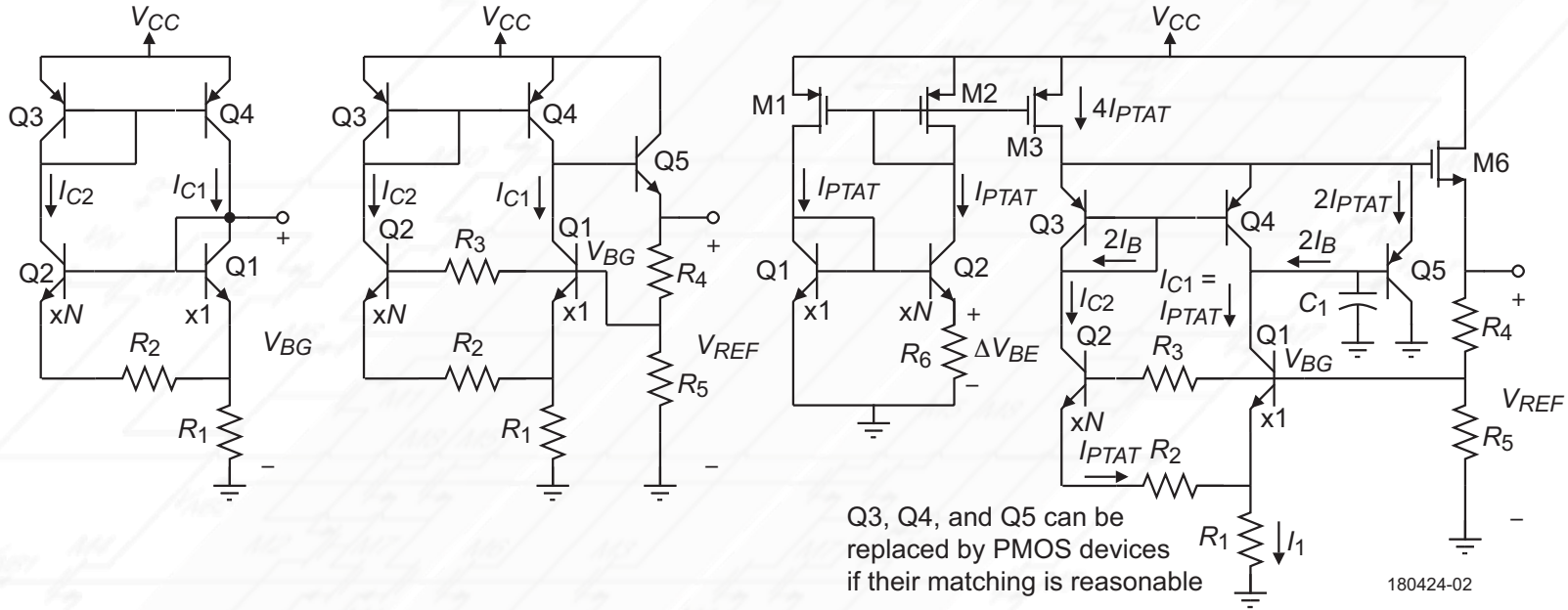




Temperature and V_{DD} Independent Sources

Brokaw Bandgap

Simple Bandgap Bandgap (V_{REF}>V_{BG}) Improved PSR Bandgap



Temperature and V_{DD} Independent Sources

Brokaw Design Procedure BT2

Step	Design Equations	Comments
Simple Brokaw Bandgap, $V_{REF} = V_{BG}$		
1	$R_2 = V_t \ln(N)/I_{PTAT}$	Choose I_{PTAT}, N = Area of Q2/Area of Q1
2	$R_1 = \frac{R_2 T(dV_{BE1}/dT)}{2V_t \ln(N)} = \frac{R_2 \cdot 300(\approx 2mV/°C)}{2 \cdot 0.0258 \ln(N)}$	Makes $dV_{BG}/dT \approx 0$, need a good value for $\lvert dV_{BE1}/dT \rvert$ or use 2mV/°C
Brokaw Bandgap with $V_{REF} > V_{BG}$		
3	$R_4 + R_5 = \frac{V_{REF}}{I_{4,5}}$	Choose the current through R_4 and R_5, $I_{4,5}$. V_{REF} is the output greater than V_{BG}.
4	$R_5 = \frac{V_{BG}}{V_{REF}}(R_4 + R_5)$ and $R_4 = (R_4 + R_5) - R_5$	Designs the increase of V_{BG} to V_{REF}
5	$R_3 = \frac{R_2 R_4 R_5}{R_1(R_4 + R_5)}$	Eliminates the base currents of Q1 and Q2
Brokaw Bandgap with improved PSR (PTAT circuit)		
6	$R_6 = V_t \ln(N)/I_{PTAT}$	Choose I_{PTAT}, N = Area of Q2/Area of Q1
7	Choose W/L of M1 and M2, M3 = 4xM2	Cancels base current of Q3, Q4, and Q5
8	Q3 = Q4 = Q5, M6 arbitrary	

Temperature and V_{DD} Independent Sources

Example 2 – Brokaw BG Design

Let V_{DD} = 5V and I_{Supply} ≤ 10μA. Design V_{REF} = 1.5V

1.) Let N=8 & choose I_{PTAT}= 2μA, therefore

$$R_2 = \frac{V_t \ln(8)}{I_{PTAT}} = 26.83k\Omega$$

2.) Design R_1, $R_1 = \frac{R_2 T(dV_{BE}/dT)}{2V_t \ln(N)} = \frac{26.83k\Omega \times 300°K(2mV/°C)}{2\times 0.0258\times 2.079}$

= 150kΩ

3.) Let $I_{4,5}$ = 2μA, then R_4+R_5 = 1.5V/2μA = 750kΩ

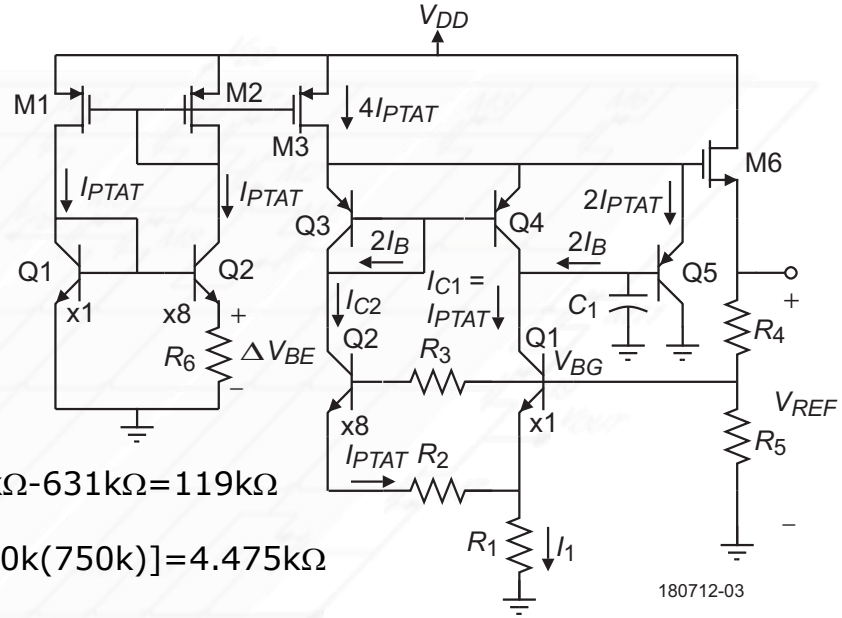
4.) $R_5 = \frac{V_{BG}}{V_{REF}}(R_4+R_5) = \left(\frac{1.262}{1.5}\right)(750k\Omega) = 631k\Omega$. R_4=750kΩ-631kΩ=119kΩ

5.) $R_3 = (R_2R_4R_5)/[R_1(R_4+R_5)] = (26.83k\cdot 119k\cdot 631k)/[150k(750k)] = 4.475k\Omega$

6.) $R_6 = V_t \ln(N)/I_{PTAT}$ = 0.0258·2.079/2μA = 26.82kΩ

7.) Choose $W_1/L_1 = W_2/L_2$ = 20μm/10μm and W_3/L_3 = 80μm/10μm

8.) Let the emitter area of Q1, Q3, and Q4 be 10μm², Q2 is x10Q1, Q5 is 2xQ1, and W_6/L_6 = 40μm/1μm.

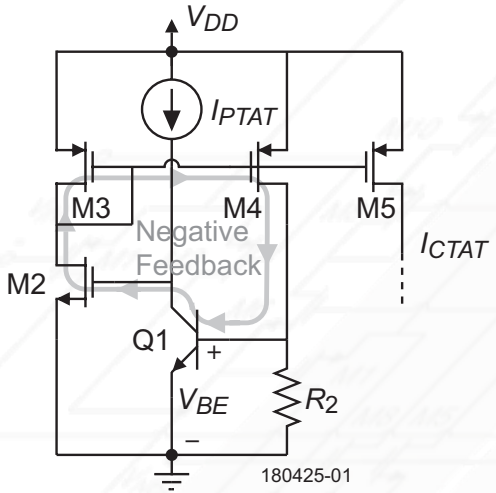


Temperature and V_{DD} Independent Sources

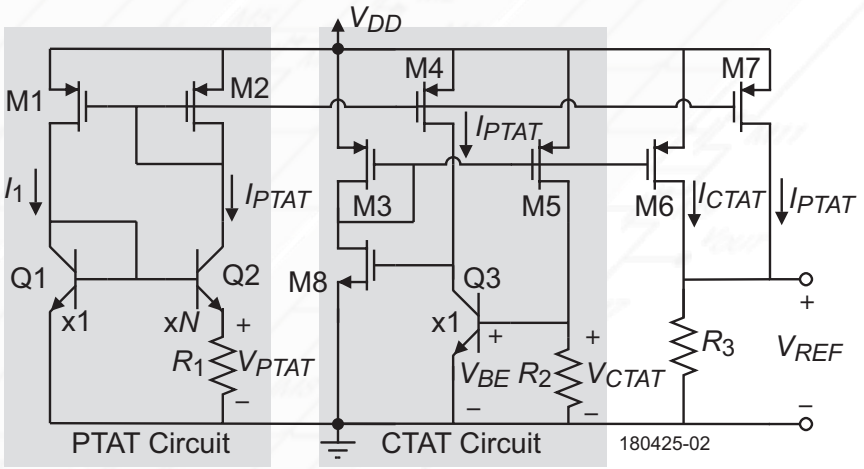
Parallel Bandgap

Combine I_{PTAT} with I_{CTAT} to yield a reference voltage.

I_{CTAT} circuit:



Parallel Bandgap Circuit:

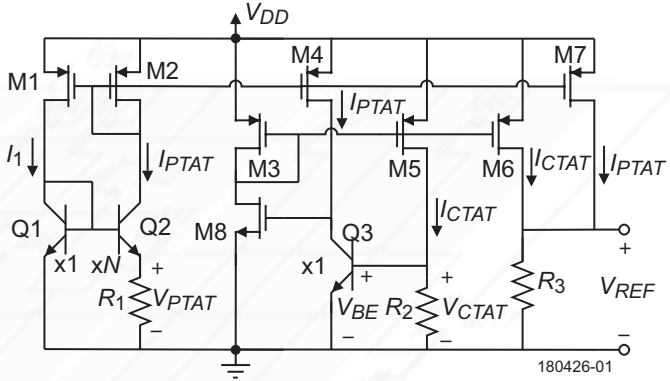


$$V_{REF} = R_3(I_{PTAT} + I_{CTAT}) = R_3\left(\frac{V_{PTAT}}{R_1} + \frac{V_{CTAT}}{R_2}\right) = \frac{R_3}{R_2}\left(\frac{R_2}{R_1}V_{PTAT} + V_{CTAT}\right)$$

Temperature and V_{DD} Independent Sources

Parallel Design Procedure BT3

Step	Design Equations	Comments
1	Select I_1, I_2, I_3, I_4, I_5, I_6, and I_7	$P_{diss} = V_{DD}\left(\sum_{i=1}^{7} I_i\right)$
2	Use Design Procedure BT1 to design Q1, Q2, M1, M2 and R_1.	
3	Let M4 and M7 equal M2.	I_{PTAT} currents equal
4	Let M3=M5=M6=M2, W_8/L_8 = 10µm/2µm, and Q3=Q1	Design of M8 is arbitrary
5	$R_2/R_1 = -\left(\frac{dV_{CTAT}/dT}{dV_{PTAT}/dT}\right) = -\left(\frac{dV_{CTAT}/dT}{200\mu V/°C}\right)$	$\frac{dV_{CTAT}}{dT} \approx$ -2mV/°C
6	$R_3 = V_{REF}R_2\left(\frac{R_2}{R_1}V_{PTAT} + V_{CTAT}\right)^{-1}$	V_{REF} specified



Example 3

Design a parallel voltage reference of 0.75V. V_{DD}=5V, and I_{Supply} 15µA.

1.) Select all currents as 2µA.

2.) From BT1, the W/L of M1, M2, M3, M4, M5, M6, and M7 = 50µm/10µm, the area of Q1 is 10µm² and Q2 = 100µm², R_1=29.93kΩ and R_2 = 10x29.93kΩ =299.3kΩ.

3.) W_8/L_8=10µm/2µm and $R_3 = V_{REF}R_2\left(\frac{R_2}{R_1}V_{PTAT} + V_{CTAT}\right)^{-1}$ =(0.75x299.3k)/1.262 = 177.9kΩ

Troubleshooting Bandgap Designs

Debugging Advice

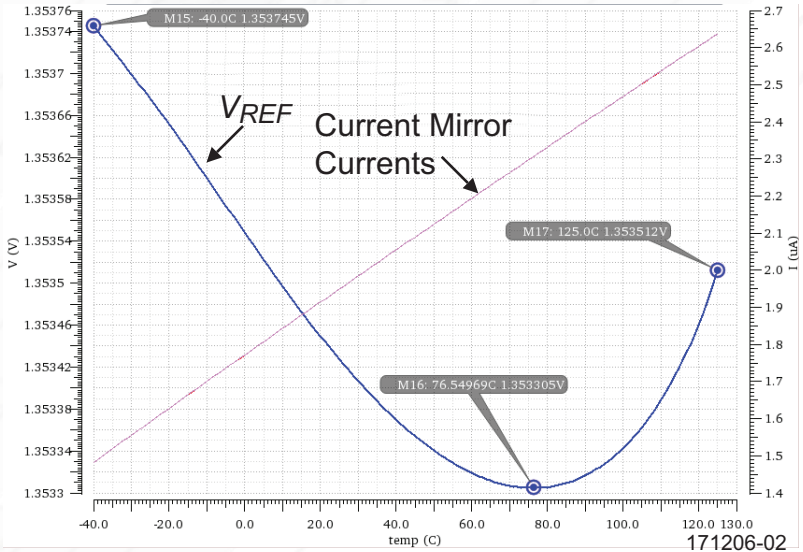
90% of the issues having to do with the bandgap not working properly have to do with how well the current mirror performs as temperature, V_{DD} or process changes.

If you are having problems, simulate currents in the current mirror and check to see that they track.

This is what they should look like:

If the currents in the current do not track, consider improving the matching of the current mirror by cascading or other means of improving the matching.

Be careful at high temperatures of leakage currents influencing the bandgap design.



Summary – Bandgap Design

Voltage and Temperature Independent Bias Design

- Objective of biasing – independence of V_{DD} and temperature
- Principle is to cancel a positive going voltage with respect to temperature with a negative going voltage
- Simple bandgap
- Brokaw bandgap
- Parallel bandgap
- Design procedures – BT1, BT2, and BT3
- Examples
- Troubleshooting bandgap designs