LECTURE 6 - HOW TO DESIGN DIFFERENTIAL OUTPUT OP AMPS

Topics:

- Introduction to differential output op amps
- Single stage differential output op amp design
- Folded cascode differential output op amp design
  - Class A
  - Class B
- Common mode stabilization
- Common mode feedback bandwidth

What will I learn?

- How to design op amps with a differential output to satisfy a given set of specifications

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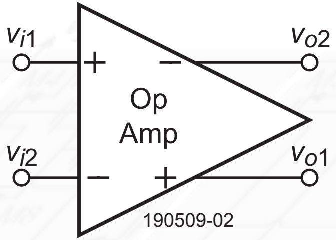
Version 190521

Differential Output Op Amp

Circuit Considerations

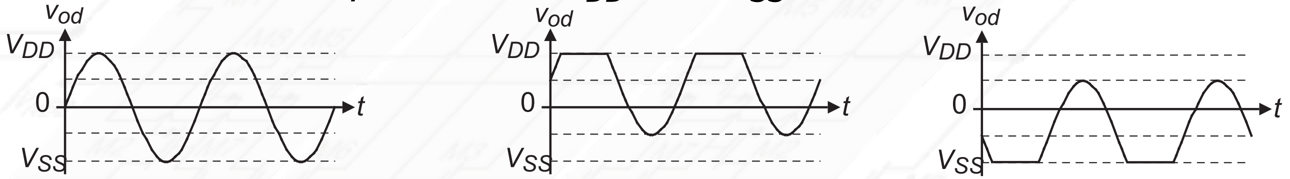
Symbol:



Definitions:

Differential input voltage = $v_{id} = v_{i1} - v_{i2}$
Differential output voltage = $v_{od} = v_{o1} - v_{o2}$
Differential in-out voltage gain = $A_{vdiff} = v_{od}/v_{id}$
Common mode input voltage = $v_{icm} = 0.5(v_{i1} + v_{i2})$
Common mode output voltage = $v_{ocm} = 0.5(v_{o1} + v_{o2})$
Common mode voltage gain = $A_{vcm} = v_{ocm}/v_{icm}$

The challenge for differential output op amps is to control the dc value of V_{ocm}. Ideally, it should be midway between V_{DD} and V_{SS}.



CM output voltage properly defined, $V_{ocm} = 0$

CM output voltage too large, $V_{ocm} = 0.5V_{DD}$

CM output voltage too small, $V_{ocm} = 0.5V_{SS}$

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Single-Ended and Differential Loads

Differential Voltage Gain

Class A Loads:

- Differential Load

$$v_{od} = \frac{g_m R_L}{2} v_{id} \Rightarrow A_{vdiff} = \frac{g_m R_L}{2}$$

- Single-ended Loads

$$v_{od} = v_{o1} - v_{o2} = \left(\frac{g_m R_L}{4} + \frac{g_m R_L}{4}\right) v_{id}$$

$$\Rightarrow A_{vdiff} = \frac{g_m R_L}{2}$$

Class B Loads (Push-pull):

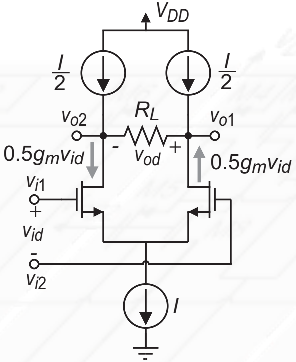
- Differential Load

$$v_{od} = g_m R_L v_{id} \Rightarrow A_{vdiff} = g_m R_L$$

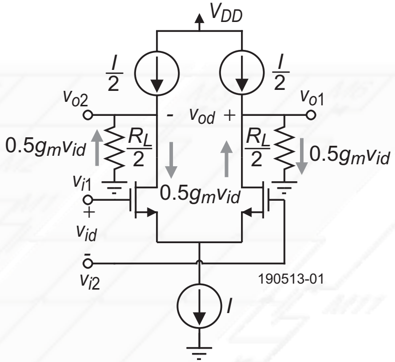
- Single-ended Loads

$$v_{od} = v_{o1} - v_{o2} = \left(\frac{g_m R_L}{2} + \frac{g_m R_L}{2}\right) v_{id}$$

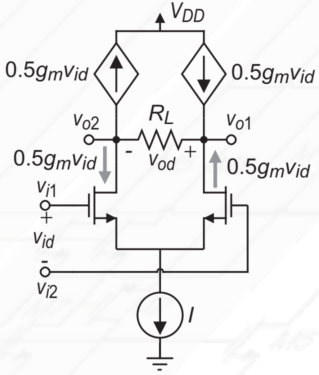
$$\Rightarrow A_{vdiff} = g_m R_L$$



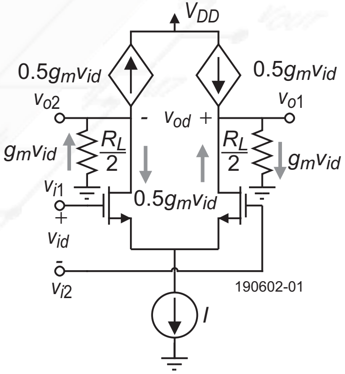
Differential Load



Single-Ended Loads



Differential Load



Single-Ended Loads

Single-Ended and Differential Loads

Slew Rate

Class A Loads:

- Differential Load

$$SR = \frac{I}{2C_L}$$

- Single-ended Loads

$$SR = SR_1 - SR_2 = \frac{I}{2}\times\frac{1}{2C_L} + \frac{I}{2}\times\frac{1}{2C_L} = \frac{I}{2C_L}$$

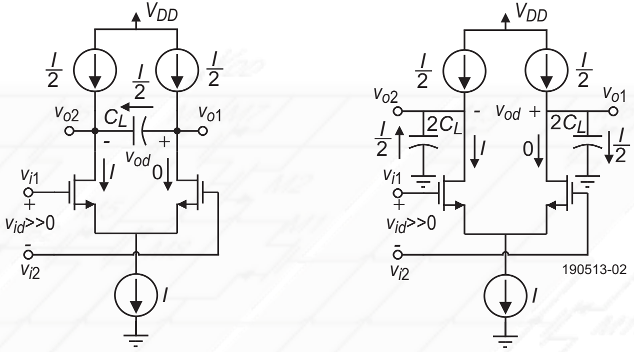
Class B Loads (Push-pull):

- Differential Load

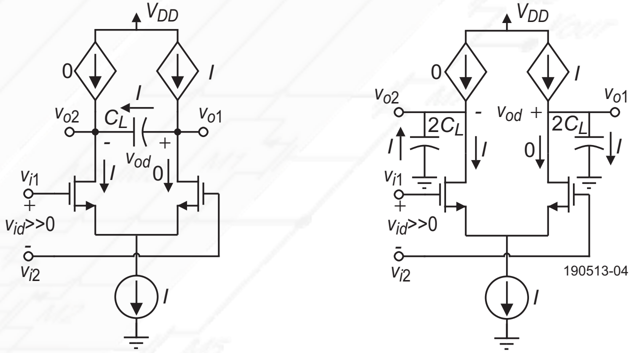
$$SR = \frac{I}{C_L}$$

- Single-ended Loads

$$SR = SR_1 - SR_2 = I\times\frac{1}{2C_L} + I\times\frac{1}{2C_L} = \frac{I}{C_L}$$



Differential Load Single-Ended Loads



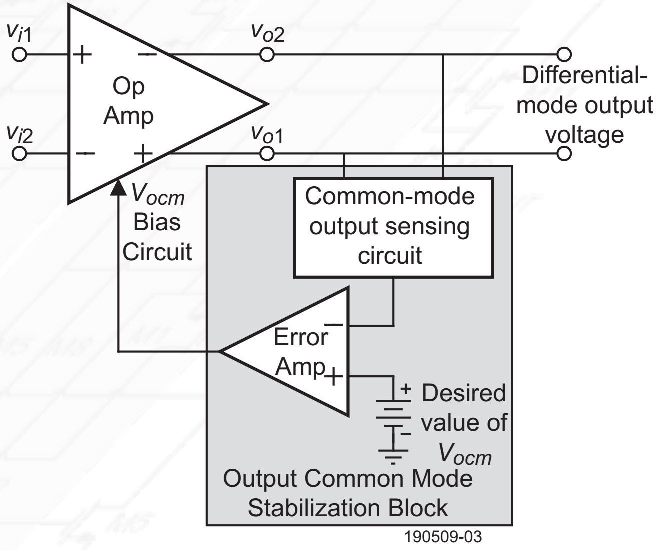
Differential Load Single-Ended Loads

Output Common Mode Stabilization

Objective

The objective of the output common mode stabilization circuit is to maintain the desired output common mode voltage.

Output Common Mode Stabilization



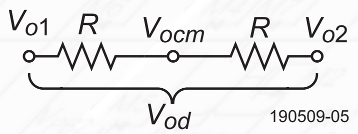
Requirements:

- The common mode stabilization is a feedback circuit and must be negative and stable
- The output differential signal should have no influence on the common mode stabilization
- The common mode stabilization should not influence the output differential voltage (such as loading it)

Output Common Mode Sensing Circuits

Approaches

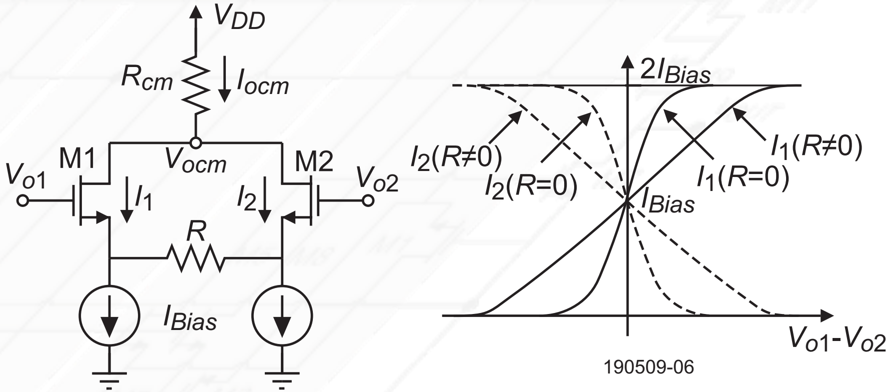
Resistive:



- If *R* is not large, it may load the op amp

Transistor:

- Does not load the op amp
- Can be NMOS or PMOS version
- The sum of I_1 and I_2 become a common mode current
- *R* allows a larger value of differential output voltage
- Can use V_{ocm} or I_{ocm} as the common mode output signal

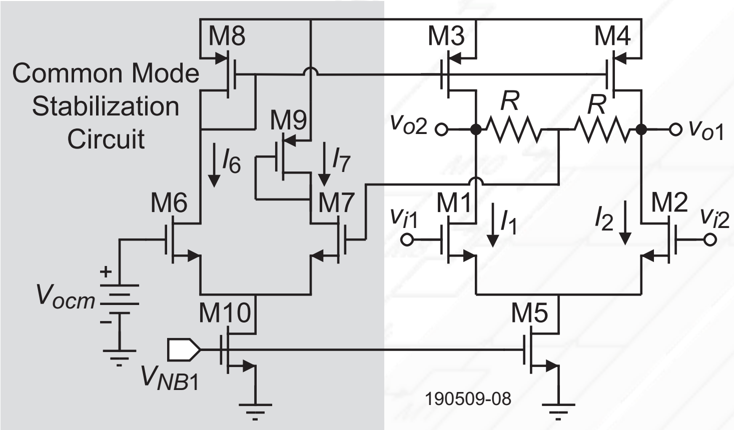


- Could split *R* in two and use a single I_{Bias} current sink

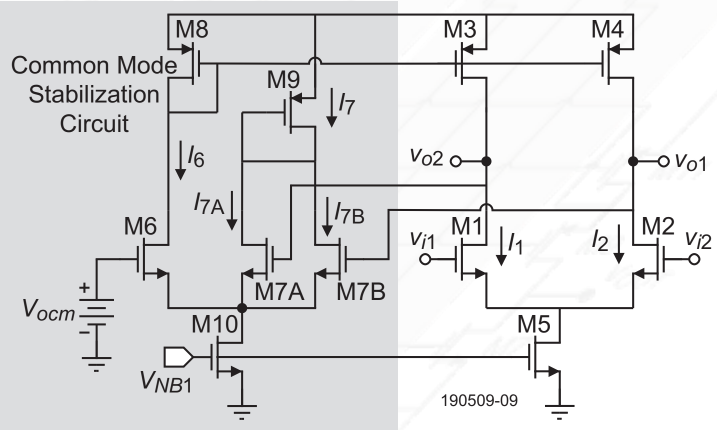
Common Mode Stabilization for a Single Stage, Class A Op Amp

Examples

Resistor CM Stabilization Circuit



Transistor CM Stabilization Circuit



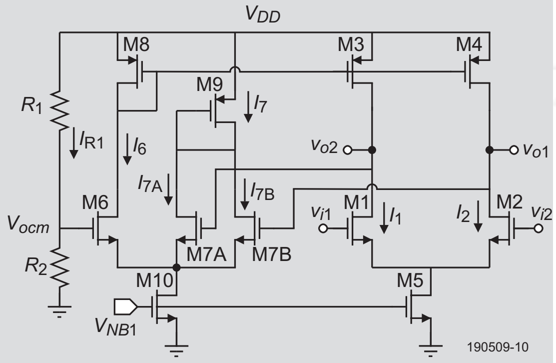
Note that both circuits are feedback circuits and must be negative and stable. The loop gain is approximately $g_{m6}R_{out}$ where R_{out} is the resistance to ground at either of the differential outputs.

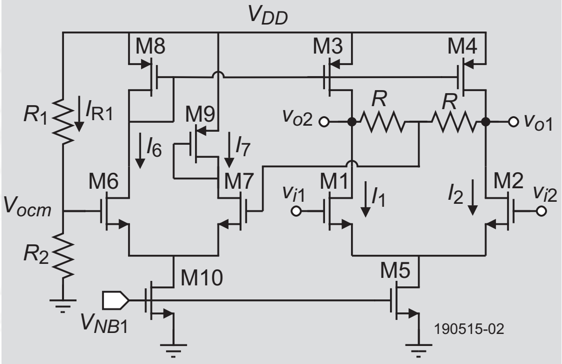
Also, the GB of the CM circuit (GB_{cm}) must be compatible with the GB of the amplifier (GB_{dm}). I.e., $GB_{dm} > GB_{cm}$, $GB_{dm} = GB_{cm}$, or $GB_{dm} < GB_{cm}$.

Single Stage, Class A, Differential Output Op Amp Design

Design Procedure – OA16

Step	Design Equations	Comments
1	Use Design Procedure OA1 to design M1-M5	M3 no longer has the gate connected to drain
2	I_5=2x($SR \times C_L$)	Max. current through C_L is $0.5I_5$
3	Let $W_{10}/L_{10}=(I_{10}/I_5)\text{x}W_5/L_5$	Choose I_{10} based on P_{diss}
4	Let $W_8/L_8=W_9/L_9=(I_6/I_1)\text{x}W_3/L_3$	Choose I_6 and I_7 based on P_{diss}
5	$g_{m6} = g_{m7}= GB_{cm} \times C_L$, $\frac{W_6}{L_6} = \frac{g_m^2}{K_6' I_{10}}$, $W_{7A}/L_{7A}=W_{7B}/L_{7B}=0.5W_6/L_6$	Choose GB_{cm}
6	$R_2=V_{ocm}/I_{R1}$	Select I_{R1} based on P_{diss}
7	$R_1=(V_{DD}/I_{R1})-R_2$	
8	If the output differential signal swing is too large, use the resistive common mode sampling circuit	

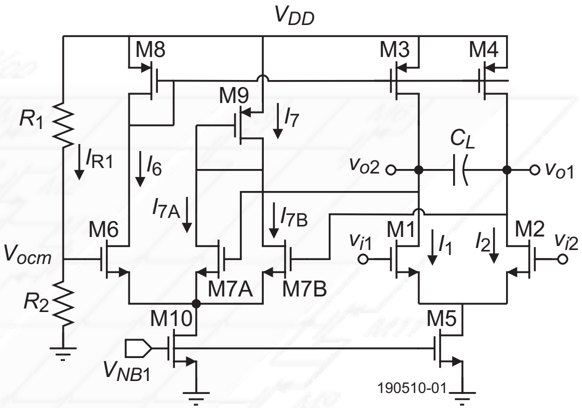




Single Stage, Class A, Differential Output Op Amp Design

Example 1:

If $K_N' = 120\mu A/V^2$, $K_P' = 25\mu A/V^2$, $V_{TN} = |V_{TP}| = 0.5V$, $\lambda_N = 0.06V^{-1}$, and $\lambda_P = 0.08V^{-1}$, use Design Procedure OA16 to design a one stage, Class A, differential output op amp. Assume that $C_L = 5pF$.



$A_{vdiff} > 50$ V/V	$V_{DD} = 2.5V$	$GB = 10MHz$	$SR > 5V/\mu s$
Phase margin ≥ 60°	$1V \le ICMR \le 2V$	$P_{diss} \le 1mW$	$V_{ocm} = 1.25V$

1.) $I_5 = 2 \times SR \times C_L = 2\text{x}5V/\mu s \times 5pF = 50\mu A$, $P_{diss} = 2.5V \times 50\mu A = 0.125mW$

2.) $g_m = g_{m1} = g_{m2} = GB_{dm} \times C_L = 100\pi\mu S$, $\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{g_m^2}{K_1' I_5} = \frac{314\mu S^2}{120\times10^{-6}\times50\mu A} = 16.43 \rightarrow 16$

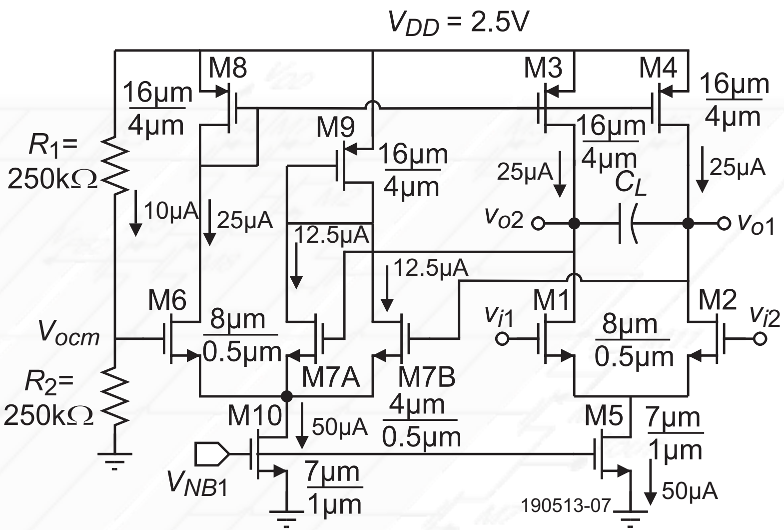
3.) $\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{I_5}{K'_3[V_{DD} - ICMR^+ - |V_{T3}| + V_{T1}]^2} = \frac{50\mu A}{25\times10^{-6}[2.5-2-0.5+0.5]} = 4$

4.) $V_{GS1} = \sqrt{\frac{50\mu A}{120\times10^{-6}\times16.43}} + 0.5 = 0.659$, $\frac{W_5}{L_5} = \frac{100\mu A}{120\times10^{-6}(1-0.659)^2} = 7.166 \rightarrow 7$

5.) $A_o = \frac{g_m R_L}{2} = \frac{2g_m}{(\lambda_N + \lambda_P)I_5} = \frac{2\times314\mu S}{(0.06+0.08)50\mu A} = 97.42\ (39.8dB)$

Single Stage, Class A, Differential Output Op Amp Design

Example 1 - Continued:



6.) Choose I_{10} = 50µA ⇒ P_{diss} = 0.250mW

Therefore, $W_{10}/L_{10} = W_5/L_5$, and $W_8/L_8 = W_9/L_9 = W_3/L_3$.

7.) Let $GB_{cm} = GB_{dm}$. Therefore $W_6/L_6 = W_1/L_1$, $W_{7A}/L_{7A} = W_{7B}/L_{7B} = 0.5W_1/L_1$.

8.) Choose I_{R1} = 10µA ⇒ P_{diss} = 0.275mW

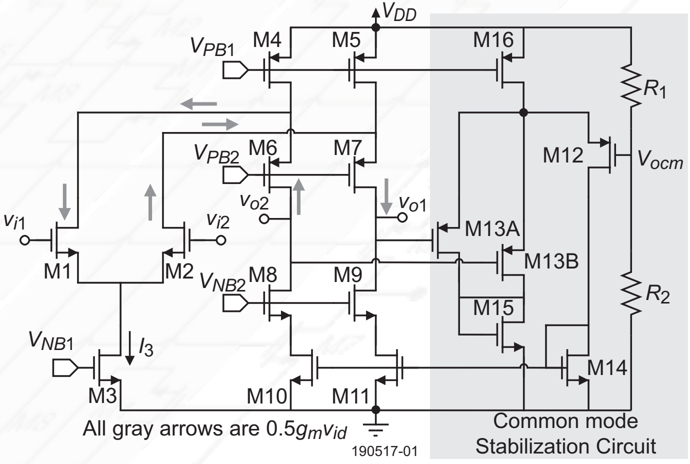
Therefore R_1=2.5/10µA = 250kΩ and R_2 = 2.5/10µA – 250kΩ =250kΩ

9.) Design L's and W's/ Pick $L_1=L_2=L_6=L_{7A}=L_{7B}$ = 0.5µm for speed. Therefore $W_1=W_2=W_6$=8µm, and $W_{7A}=W_{7B}$= 8µm. Pick $L_5=L_{10}$= 1µm which gives $W_5=W_{10}$=7µm.
For PSRR and gain, let $L_3=L_4=L_8=L_9$=4µm which gives $W_3=W_4=W_8=W_9$=16µm.

Folded Cascode, Class A, Differential Output Op Amp Design

Design Procedure – OA17

Step	Design Equations	Comments
1	Use Design Procedure OA3 to design M1-M11, $SR = 2\times I_3\times C_L$	Drain of M8 and gate of M10 are not connected
2	Let $W_{16}/L_{16}=W_5/L_5$	Let $I_{16} = I_4 = I_5$ so I_{10} and I_{11} $\geq$ maximum I_6 or I_7
3	$g_{m12} = GB_{cm}\times C_L$, $\frac{W_{12}}{L_{12}} = \frac{g_m^2}{K_1' I_{16}}$, $W_{13A}/L_{13A} = W_{13B}/L_{13B} = 0.5W_{12}/L_{12}$	Choose GB_{cm}
4	Let $W_{14}/L_{14}= W_{15}/L_{15} =W_{10}/L_{10}= W_{11}/L_{11}$	Could make $W_{14}/L_{14}= W_{15}/L_{15} > W_{10}/L_{10}$ and decrease I_9
5	$R_2=V_{ocm}/I_{R1}$ and $R_1=(V_{DD}/I_{R1})-R_2$	V_{ocm} known
6	If the output differential signal swing is too large, use the resistive common mode sampling circuit	



Folded Cascode, Class A, Differential Output Op Amp Design

Example 2

Design a common mode stabilization circuit for the op amp designed in Example 3 of Lecture 1 (Single-Stage Op Amp Design) of Module 4 assuming C_L = 5pF.

1.) The design from Example 3 of Lecture 1 is shown.

2.) Choose I_{16} = 100μA and I_{R1} = 10μA, therefore P_{diss} = 2.5V× (250μA+100μA+10μA) =0.9mW

3.) W_{16}/L_{16}=(100μA/125μA)×160=128 → 64μm/0.5μm

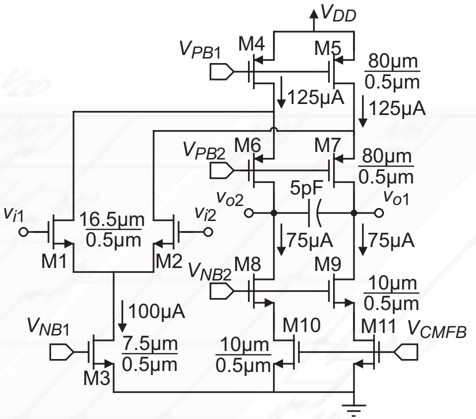
4.) Choose GB_{cm} = 1MHz ⇒ 20πx10[6]

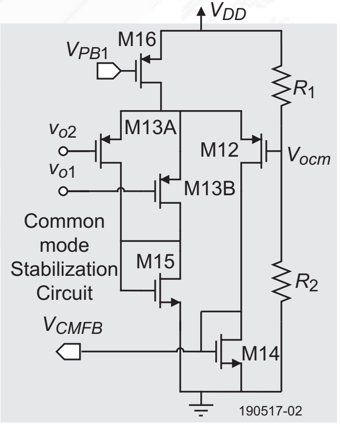
Therefore $\frac{W_{12}}{L_{12}} = \frac{g_m^2}{K_1' I_{16}} = \frac{(62.8)^2}{25\times 100} = 1.58 \rightarrow 2, \frac{W_{13A}}{L_{13A}} = \frac{W_{13B}}{L_{13B}} = 1$

5.) Let W_{14}/L_{14}=W_{15}/L_{15}=(75μA/50μA)W_{10}/L_{10}=30

6.) R_1=V_{OCM}/I_{R1} = 125kΩ, R_2 = 250kΩ – 125kΩ = 125kΩ

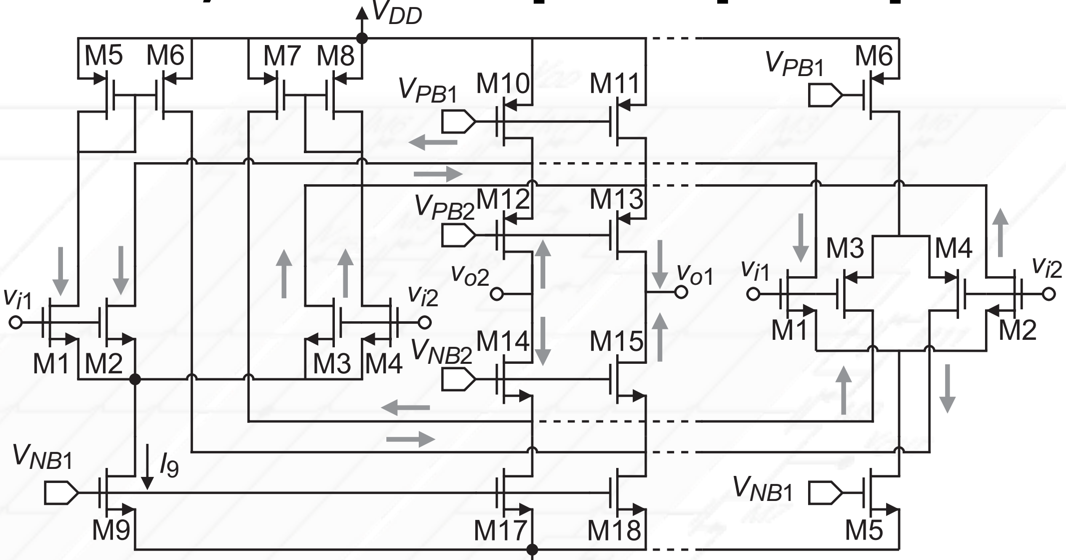
7.) Design W's and L's. Choose L_{12} and L_{13} as 1μm giving W_{12}=1μm and W_{13A}=W_{13B}=0.5μm. Choose L_{14} and L_{15} as 1μm which gives W_{14}=W_{15}=15μm.





Folded Cascode, Class B, Diff. Output Op Amp

Comments



Each gray arrow is $0.5g_m v_{id}$

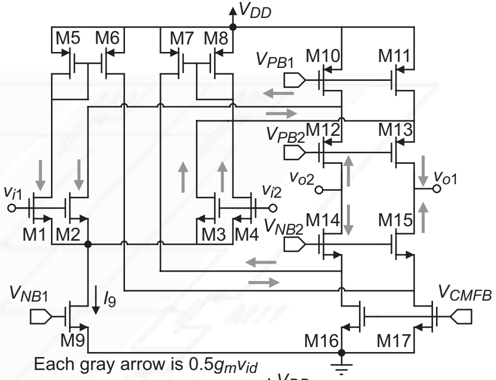
- The folded-cascode op amp is desirable for class B implementation
- Two possible input circuits are shown
  - The one on the left has the advantage of a potentially large ICMR but the *p*-channel and *n*-channel inputs must be designed so the effective g_m is constant over the ICMR*
  - The one on the right is preferable if large ICMR is not needed.
- The previous CM stabilization circuits for Class A, folded-cascode op amp are applicable for the Class B, folded-cascode op amp

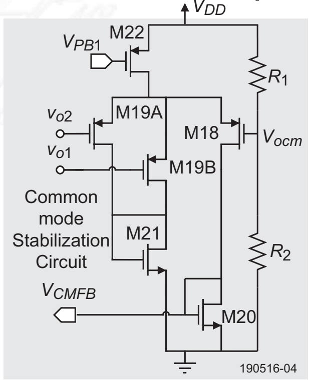
* R. Hogervorst et al., "CMOS Low-Voltage Operational Amplifiers with Constant-g_m Rail-to-Rail Input Stage," *Analog Integrated Circuits and Signal Processing*, Vol. 5, No. 4, pp. 135-146, March 1994.

Folded Cascode, Class B, Diff. Output Op Amp Design

Design Procedure – OA18

Step	Design Equations	Comments
1	$I_9 \geq 2 \cdot SR \cdot C_L$	Defines minimum current
2	$I_{10} = I_{11} = I_{16} = I_{17} = 0.5(1.1I_9 \text{ to } 1.5I_9) = 0.55I_9 \text{ to } 0.75I_9$	Avoids cascode current = 0
3	$W_{10}/L_{10} = W_{11}/L_{11} = 2I_{11}/[K'_P V_{SD4}(\text{sat})^2]$	$V_{SD11}(\text{sat})=0.5[V_{DD}-V_{out}(\text{max})]$
4	$W_{12}/L_{12} = W_{13}/L_{13} = 2I_{11}/[K'_P V_{SD6}(\text{sat})^2]$	$V_{SD13}(\text{sat})=0.5[V_{DD}-V_{out}(\text{max})]$
5	$\frac{W_{14}}{L_{14}} = \frac{W_{15}}{L_{15}} = \frac{W_{16}}{L_{16}} = \frac{W_{17}}{L_{17}} = \frac{2I_{17}}{K'_N V_{DS17}(sat)^2}$	$V_{DS16}(\text{sat})=0.5[V_{out}(\text{min})-V_{SS}]$
6	$g_{m1}=GB_{dm} \times C_L \rightarrow W_1/L_1=W_2/L_2=W_3/L_3=W_4/L_4=\frac{4GB^2C_L^2}{K'_N I_9}$	GB_{dm} is in rads/sec
7	$\frac{W_9}{L_9} = \frac{2I_9}{K'_N(ICMR^- - V_{GS1})^2}$, $V_{GS1} = \sqrt{i_9/2K'_N(\frac{W_1}{L_1})} + V_{T1}$	Note that $ICMR^-$ must be greater than V_{GS1}
8	$\frac{W_5}{L_5} = \frac{W_6}{L_6} = \frac{W_7}{L_7} = \frac{W_8}{L_8} = \frac{I_5}{K'_5[V_{DD} - ICMR^+ - \lvert V_{T5}\rvert + V_{T1}]^2}$	$ICMR^+ = V_{in}(\text{max})$ specified, M5 = M6=M7=M8
9	Design the common stabilization circuit using steps 2-6 of Design Procedure OA17	
10	Check gain and power dissipation and iterate if necessary $A_o = g_{m1}R_{out}$ and $P_{diss} = (V_{DD}-V_{SS})(I_4 + I_5 + I_{22} + I_{R1})$	

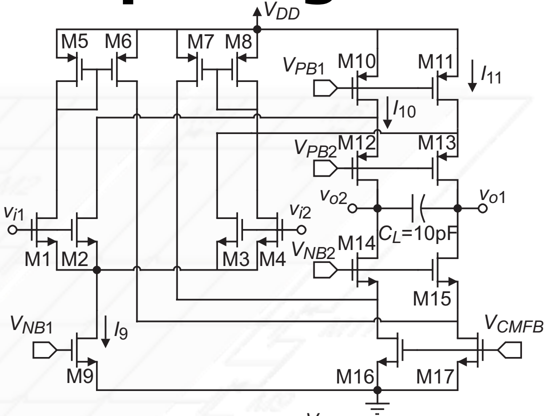




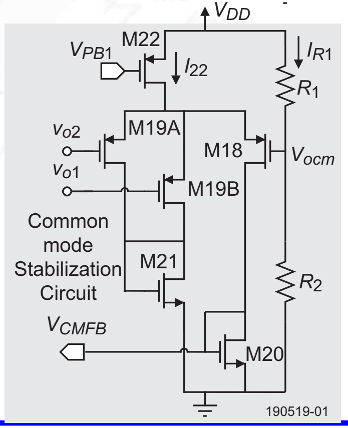
Folded Cascode, Class B, Diff. Output Op Amp Design

Example 3:

If $K_N' = 120\mu A/V^2$, $K_P' = 25\mu A/V^2$, $V_{TN} = |V_{TP}| = 0.5V$, $\lambda_N = 0.06V^{-1}$, and $\lambda_P = 0.08V^{-1}$, use Design Procedure OA18 to design a folded-cascode, Class B, differential output op amp. Assume that $C_L = 10pF$.



A_{vdiff} > 5000 V/V	V_{DD} = 2.5V	GB = 10MHz	SR > 5V/µs	P_{diss} ≤ 1mW
PM ≥ 60°	1V≤$ICMR$≤2V	V_{ocm}= 1.25V	V_o(max)=2V	V_o(min)=0.5V



1.) $I_9 = 2\times SR\times C_L = 2\text{x}5\text{V/µs}\times 10\text{pF} = 100\mu A$,

2.) Select $I_{10} = I_{11} = I_{16} = I_{17} = 125\mu A$, $P_{diss} = 2.5V\times 250\mu A = 0.250mW$

3.) V_{DSat} of M10 and M11=0.25V for gives $\frac{W_{10}}{L_{10}} = \frac{W_{11}}{L_{11}} = \frac{2\times 125}{25\times 0.25^2} = \underline{160}$

4.) Assuming $I_{12} = 125\mu A$ gives $\underline{160}$ for W_{12}/L_{12} and W_{13}/L_{13}.

5.) $V_{DS16}(\text{sat}) = 0.25V \rightarrow \frac{W_{14}}{L_{14}} = \frac{W_{15}}{L_{15}} = \frac{W_{16}}{L_{16}} = \frac{W_{17}}{L_{17}} = \frac{2I_{16}}{K_N' V_{DS16}(sat)^2} = \frac{2\times 125}{120\times 0.25^2} = \underline{20}$

6.) $\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{4GB^2C_L^2}{K_N' I_9} = \frac{4(20\pi)^2\times 10^2}{120\times 100} \approx \underline{132}$

7.) $V_{DS9}(\text{sat}) = 0.5 - \sqrt{\frac{50}{120\times 132}} = 0.444V \rightarrow \frac{W_9}{L_9} = \frac{2\times 100}{120\times 0.444^2} \approx \underline{9}$

Folded Cascode, Class B, Diff. Output Op Amp Design

Example 3 - Continued

8.) $\frac{W_5}{L_5} = \frac{W_6}{L_6} = \frac{W_7}{L_7} = \frac{W_8}{L_8} = \frac{I_5}{K'_5[V_{DD}-ICMR^+-|V_{T5}|+V_{T1}]^2} = \frac{25}{25\times[2.5-2]^2} = 4$

9.) Choose I_{22} = 100μA and I_{R1} = 10μA, therefore P_{diss} = 2.5V× (250μA+100μA+10μA) =0.9mW

10.) W_{22}/L_{22}=(100μA/125μA)×160=128 → 64μm/0.5μm

11.) Choose GB_{cm} = 1MHz ⇒ 20πx10^6

Therefore $\frac{W_{18}}{L_{18}} = \frac{g_m^2}{K_1' I_{22}} = \frac{(62.8)^2}{25\times 100} = 1.58 \to 2,\ \frac{W_{19A}}{L_{19A}} = \frac{W_{19B}}{L_{19B}} = 1$

12.) Let W_{20}/L_{20}=W_{21}/L_{21}=(125μA/50μA)W_{16}/L_{16}=50

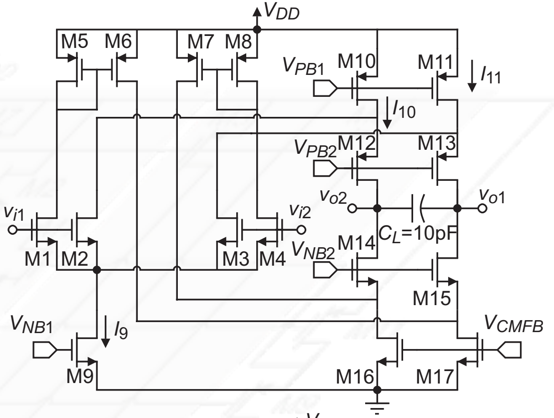
13.) R_1=V_{OCM}/I_{R1} = 125kΩ, R_2 = 250kΩ – 125kΩ = 125kΩ

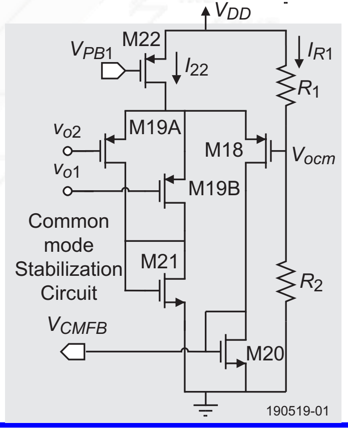
14.) Design W's and L's. Choose L_{18} and L_{19} as 1μm giving W_{18}=1μm and W_{19A}=W_{19B}=0.5μm. Choose L_{20} and L_{21} as 1μm which gives W_{20}=W_{21}=50μm.

15.) Find the gain: g_m=200πμS, $g_{mp} = \sqrt{2\times 25\times 160\times 125} = 1mS$,

$r_{dsp} = 1/\lambda_p I_{10} = 100k\Omega,\ g_{mn} = \sqrt{2\times 120\times 20\times 125} = 775\mu S, and\ r_{dsn} =$

$1/\lambda_n I_{16} = 133k\Omega \to R_L = 2\times\left(\frac{g_{mp}}{\lambda_p^2 I^2} \parallel \frac{g_{mn}}{\lambda_n^2 I^2}\right) = 11.6M\Omega \to A_{vd} = 7{,}288V/V$

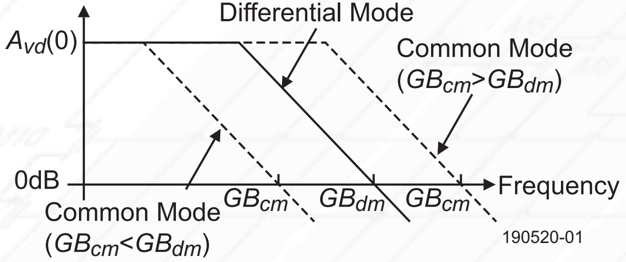




CM Feedback Circuit Frequency Response

CM Feedback GB vs Differential GB:

Should the *GB* of the common mode feedback stabilization circuit (GB_{cm}) be greater or less than the *GB* of the differential mode (GB_{dm})?



- $GB_{dm} > GB_{cm}$ means that common mode stabilization circuit is slower than the differential mode circuit
  - Common mode stabilization does not respond to quick changes in the differential mode circuit
- $GB_{dm} < GB_{cm}$ means that common mode stabilization circuit is faster than the differential mode circuit
  - Common mode stabilization circuit can respond to fast changes in the differential mode circuit and possibly create nonlinearity in the differential mode response

Differential Output Op Amp Design

Summary:

- Differential output op amps
  - Single-ended loads
  - Differential loads
- Output common mode stabilization
- Single stage, class A, differential output op amp
  - Design Procedure OA16
  - Example 1
- Folded cascode, class A, differential output op amp
  - Design Procedure OA17
  - Example 2
- Folded cascode, class B, differential output op amp
  - Design Procedure OA18
  - Example 3