LAB05 – LOW NOISE OP AMP DESIGN

Overview:

The objective of this laboratory is to design low-noise op amp that will meet a given set of specifications.

The steps in the laboratory are:

- Specifications
- Approach
- Simulation/Test Benches

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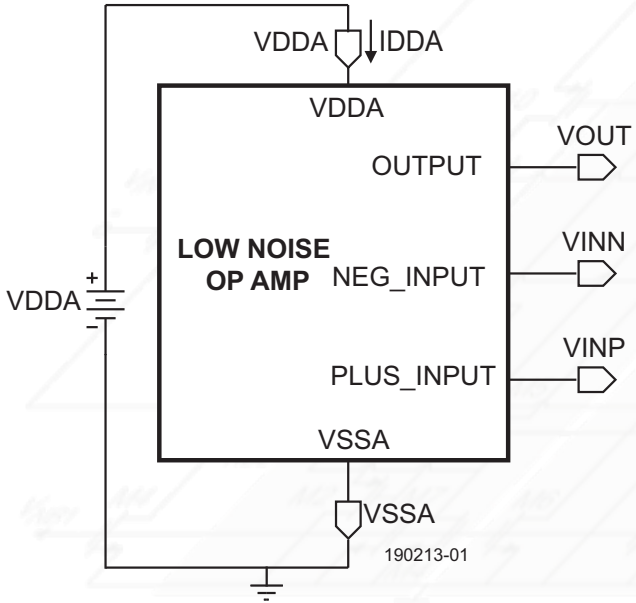
Version 190324

Lab05 - Specifications

Specifications

Technology - xFab XH035B

Block diagram:



Parameter	Symbol	Min	Typ	Max	Units
Power Supply Voltage	VDDA	3	3.3	3.6	V
Ground	VSSA	0	0	0	V
Bulk Bias Voltage	VBBA	0	0	0	V
Junction Temperature	TJ	-40	27	175	°C

Note: You are only responsible for the circuits within the box labelled **LOW NOISE OP AMP**

Lab05 - Specifications

Specifications – Continued

(VDDA = 3.3V, TJ = 27°C, C_L = 5pF unless otherwise specified below)

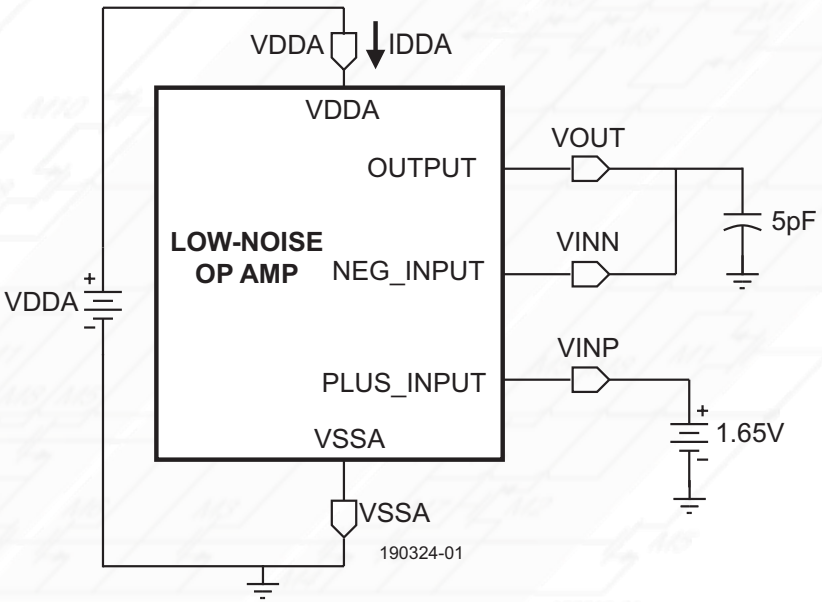
Parameter	Symbol	Condition	Min	Typ	Max	Units
Bias Current for total circuit	IDDA	VDDA = 3.3V, VINP=1.65V			50	µA
Eq. Input rms noise voltage	VINRMS	VDDA = 3.3V, VINP=1.65V, 1Hz to 1MHz			10	µV(rms)
Low frequency open loop gain	AVD	VDDA = 3.3V, VINP=1.65V	80			dB
Gain-bandwidth	GB	VDDA = 3.3V, VINP=1.65V, CL = 5pF	5			MHz
Phase Margin	PM	VDDA = 3.3V, VINP=1.65V	60			Deg
Power supply rejection ratio	PSRR	VINP=1.65V, f=1kHz	60			dB

Test Bench 1

IDDA - DC OP

This Test Bench does the following:

1.) Determines IDDA for nominal model, tm

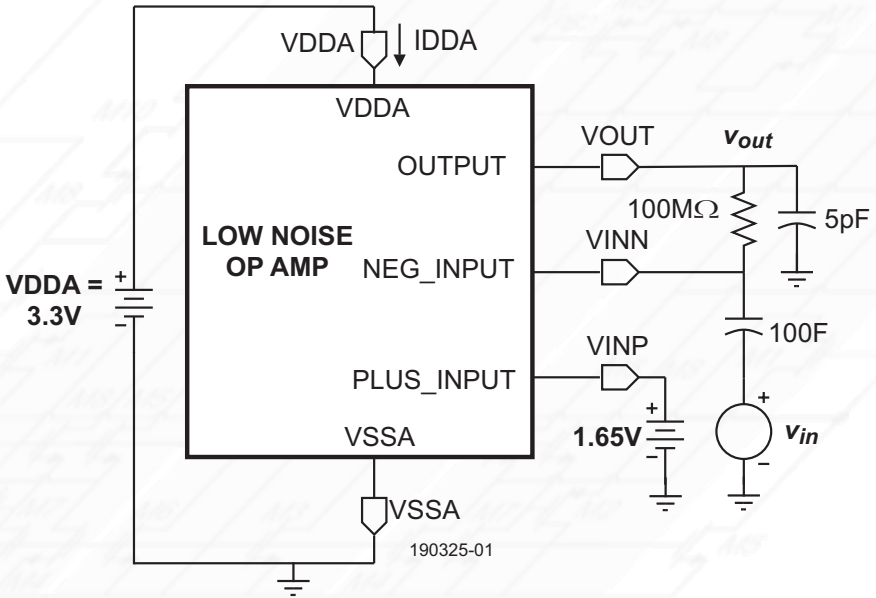


Test Bench 2

AVD, GB, and PM – AC

This Test Bench does the following:

1.) Measures the open loop gain when VDDA = 3.3V, VINP=1.65V.

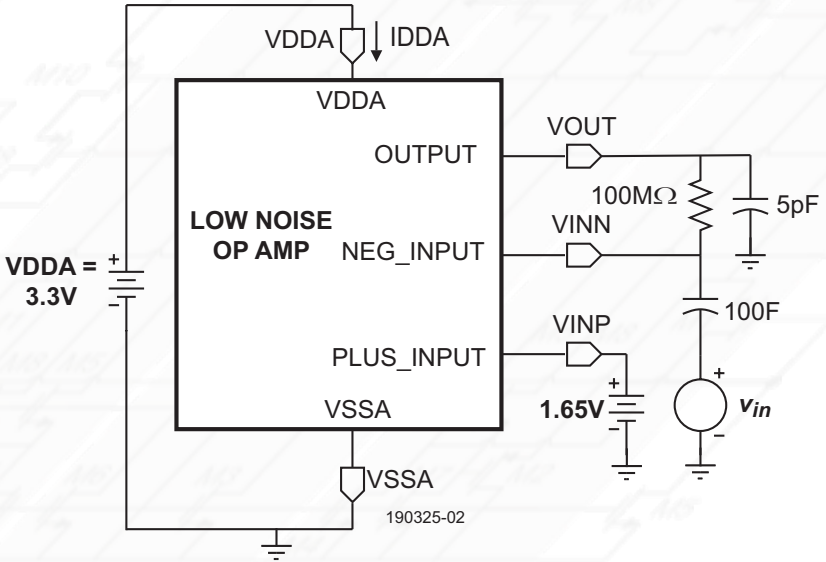


Test Bench 3

EQ. RMS NOISE VOLTAGE (1Hz to 1MHz) - NOISE

This Test Bench does the following:

1.) Measures the equivalent rms input noise voltage from 1Hz to 1MHz when VDDA = 3.3V.

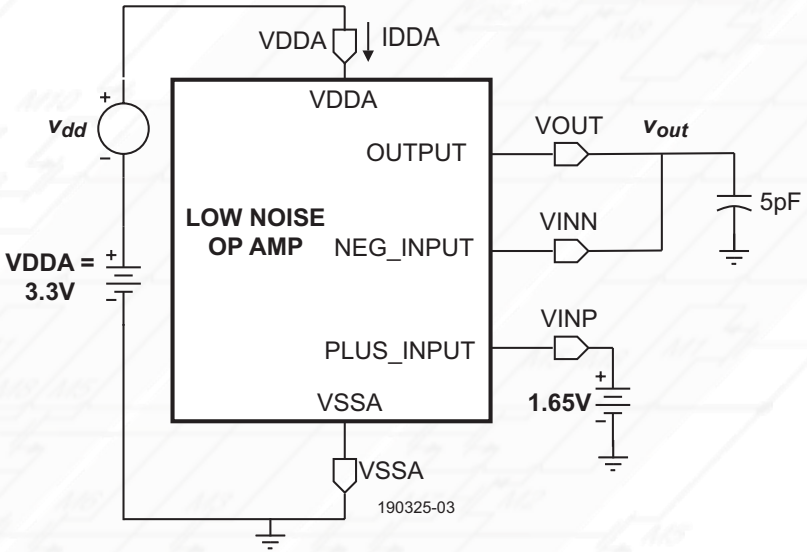


Test Bench 4

PSRR – AC

This Test Bench does the following:

1.) Puts the op amp in unity gain configuration and applies a ac signal on VDDA.



Electrical Design

Steps

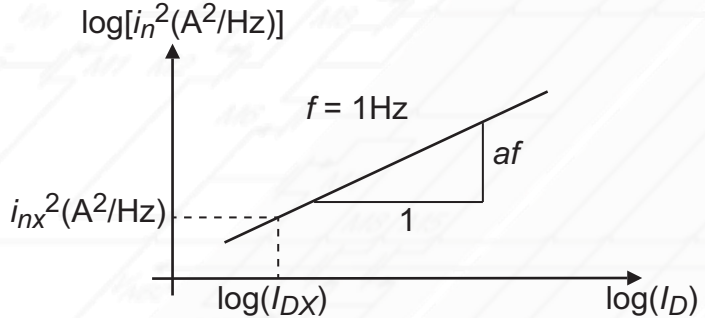
1. Choose one of the appropriate design procedures
2. Hand design using the design procedure
3. Use the test benches to determine the performance of your design keeping your design constant from test bench to test bench
4. After you have used the test benches provided to simulate your circuit, a specification sheet will be generated to indicate how well your circuit meets the specifications.
5. If you did not meet specifications, you are encouraged to modify your circuit in an attempt to meet specifications

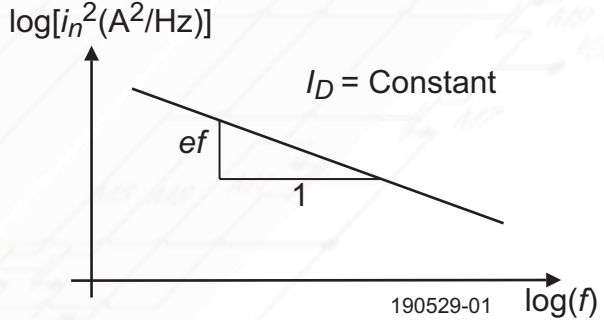
Extraction of 1/f Noise Parameters

Procedure

Normally, the 1/*f* parameters will be incorporated in the BSIM model. If not, then the following can be used for the simple 1/*f* noise model:

$$i_n^2 = \frac{kf}{C_{ox}L^2}\frac{I_D^{af}}{f^{ef}}\ (\text{A}^2/\text{Hz}) \Longrightarrow log(i_n^2) = log\frac{kf}{C_{ox}L^2} + af \times log(I_D) - ef \times \log(f)$$





$$log\left(\frac{kf}{C_{ox}L^2}\right) = log(i_{nx}^2) - af \times log(I_{DX})$$

Tips and Tricks

Helpful Ideas for Lab05

1. The equivalent input rms noise emphasizes the noise at high frequencies as it is equal to:

$$V_{eq}(rms) = \sqrt{\int_{1Hz}^{1MHz} v_{eq}^2(f)df}$$

Therefore, when you look at the spectrum of v_{eq}^2, you want an op amp with lower values of v_{eq}^2 at high frequencies.

2. If the gain of your op amp is at the input, the design of the remainder of the op amp will not influence the noise performance.

Summary – Lab05

Low Noise Op Amp Design

- Understand the lab specifications
- Selection of an appropriate design procedure and topology
- Develop the design using the design procedure
- Use test benches to simulate and determine performance
- Modify as necessary