LECTURE 2 - HOW TO DESIGN LOW NOISE OP AMPS

Topics:

- Noise concepts and models
- Low-noise, one-stage op amp design
- Low-noise, folded cascode op amp design
- Low-noise, two-stage op amp design

What will I learn?

- How to do noise analysis using noise models
- How to minimize the equivalent input noise of an op amp

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Noise Models

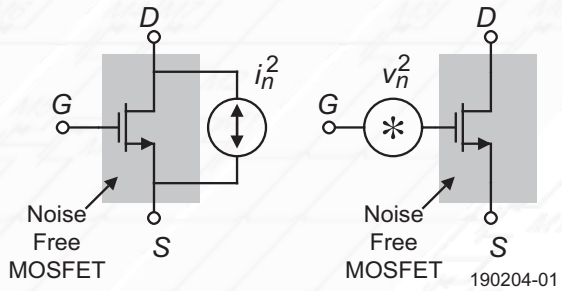
MOSFET Thermal Noise Models

Mean-square-current noise in drain

Active region:

$$i_n^2(act) = \frac{4kT}{(K'W/L)(V_{GS}-V_T)} = 4kTg_m(sat)\,(\text{A}^2/\text{Hz})$$

$$v_n^2(act) = \frac{4kTg_m(sat)}{g_m^2(act)} = \frac{4kT(V_{GS}-V_T)}{(K'W/L)V_{DS}^2}\,(\text{V}^2/\text{Hz})$$



Saturation region:

$$i_n^2(sat) = \frac{8kTg_m(sat)}{3}\,(\text{A}^2/\text{Hz}) \quad \text{or} \quad v_n^2(sat) = \frac{8kT}{3g_m(sat)}\,(\text{V}^2/\text{Hz})$$

If the bulk is not connected to the source, replace g_m with $g_m + g_{mbs}$.

MOSFET 1/F Noise Models:

$$i_n^2 = \frac{kf}{C_{ox}L^2}\frac{I_D^{af}}{f^{ef}}\,(\text{A}^2/\text{Hz}) \quad \text{or} \quad v_n^2 = \frac{kf}{2C_{ox}K'WL}\frac{I_D^{af-1}}{f^{ef}}\,(\text{V}^2/\text{Hz})$$

1/f corner frequency is where the thermal noise equals the 1/f noise

Noise Models - Continued

Resistor Thermal Noise Model

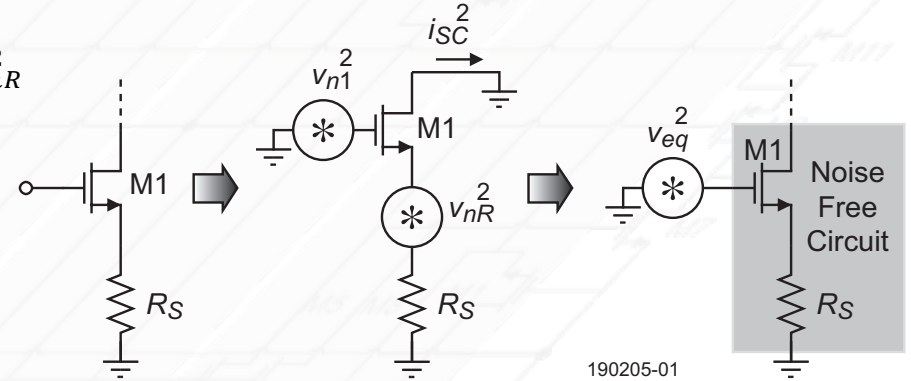
The noise voltage spectral density of a resistor R is $v_n^2 = 4kTR$ (V²/Hz)

The noise current spectral density of a resistor R is $i_n^2 = \frac{4kT}{R}$ (A²/Hz)

Noise in a Degenerated MOSFET

$$i_{SC}^2 = \left(\frac{g_{m1}}{1+g_{m1}R_S}\right)^2 v_{n1}^2 + \left(\frac{g_{m1}}{1+g_{m1}R_S}\right)^2 v_{nR}^2$$

$$v_{eq}^2 = \frac{i_{SC}^2}{\left(\frac{g_{m1}}{1+g_{m1}R_S}\right)^2} = v_{n1}^2 + v_{nR}^2$$



Noise Analysis and Minimization

Noise Analysis:

1.) Insert a noise generator for each transistor that contributes to the noise. (Generally ignore the current source transistor of source-coupled pairs.)

2.) Find the output noise voltage across an open-circuit or output noise current into a short circuit.

3.) Reflect the total output noise back to the input resulting in the equivalent input noise voltage

Noise Minimization:

- Maximize the signal gain as close to the input as possible. (As a consequence, only the input stage will contribute to the noise of the op amp.)
- To minimize the 1/f noise:
  - Use PMOS input transistors with appropriately selected dc currents and *W* and *L* values.
  - Use BJTs to eliminate the 1/*f* noise.
  - Use chopper stabilization to reduce the 1/*f* noise.

One-Stage Op Amp

Thermal Noise Analysis:

1.) Insert noise model for each MOSFET

2.) Find the short-circuit output noise spectral current density.

$$i_{SC}^2 = g_{m1}^2 v_{n1}^2 + g_{m2}^2 v_{n2}^2 + g_{m3}^2 v_{n3}^2 + g_{m4}^2 v_{n4}^2$$
$$= 2(g_{m1}^2 v_{n1}^2 + g_{m3}^2 v_{n3}^2)$$

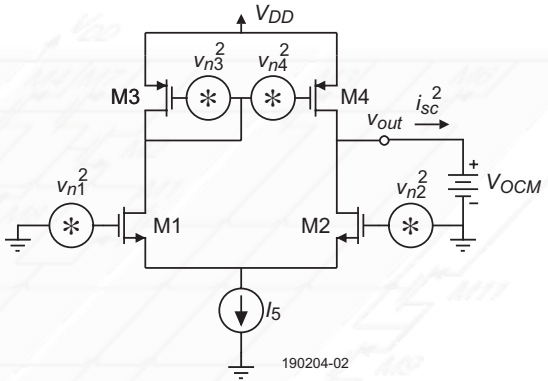
3.) Reflect i_{sc}^2 to the input by dividing by g_{m1}^2.

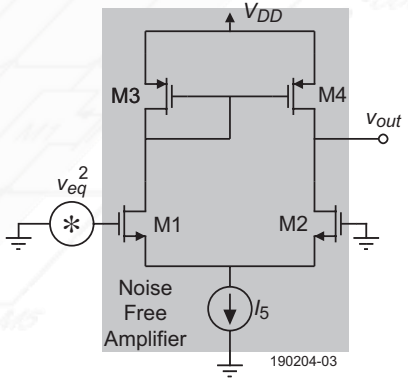
$$v_{eq}^2 = \frac{i_{SC}^2}{g_{m1}^2} = 2\left(v_{n1}^2 + \frac{g_{m3}^2}{g_{m1}^2} v_{n3}^2\right) = 2v_{n1}^2\left(1 + \frac{g_{m3}^2}{g_{m1}^2}\frac{v_{n3}^2}{v_{n1}^2}\right)$$

$$= 2v_{n1}^2\left(1 + \frac{g_{m3}^2}{g_{m1}^2}\frac{v_{n3}^2}{v_{n1}^2}\right) = 2v_{n1}^2\left(1 + \sqrt{\frac{K_p'(W_3/L_3)}{K_n'(W_1/L_1)}}\right)$$

4.) Minimize v_{eq}^2 by making $K_n'\frac{W_1}{L_1} > K_p'\frac{W_3}{L_3}$.

5.) The lowest v_{eq}^2 can be is $2v_{n1}^2$. To further reduce v_{eq}^2 make g_{m1} as large as possible.





One-Stage Op Amp

1/f Noise Analysis:

1.) Insert noise model for each MOSFET

2.) From the previous slide we get,

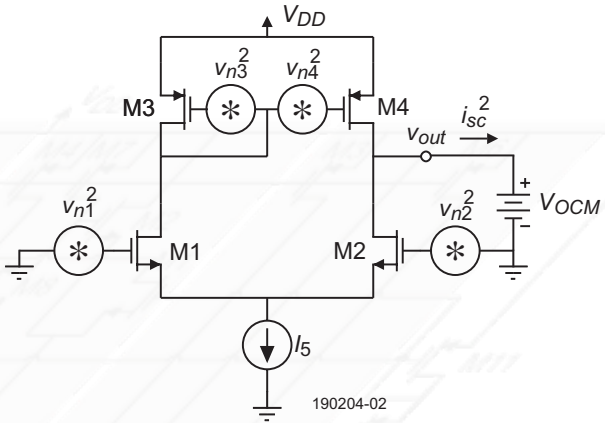
$$v_{eq}^2 = 2v_{n1}^2\left(1 + \frac{g_{m3}^2}{g_{m1}^2}\frac{v_{n3}^2}{v_{n1}^2}\right)$$

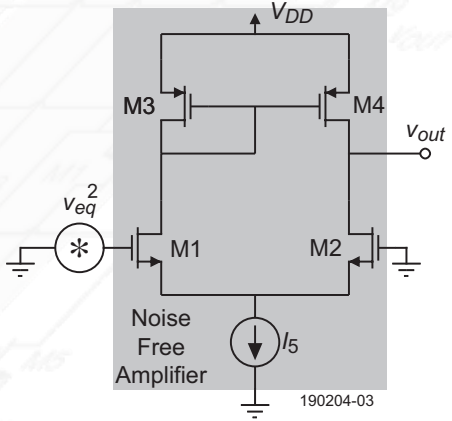
3.) Substituting the 1/f voltage noise spectral density gives assuming af = 1 and ef = 1,

$$v_{eq}^2 = 2v_{n1}^2\left(1 + \frac{kf_p}{kf_n}\frac{L_1^2}{L_3^2}\right)$$

4.) Minimize v_{eq}^2 by making $L_1 < L_3$.

5.) The lowest v_{eq}^2 can be is $2v_{n1}^2$. To further reduce v_{eq}^2 make W_1L_1 (W_2L_2)as large as possible.

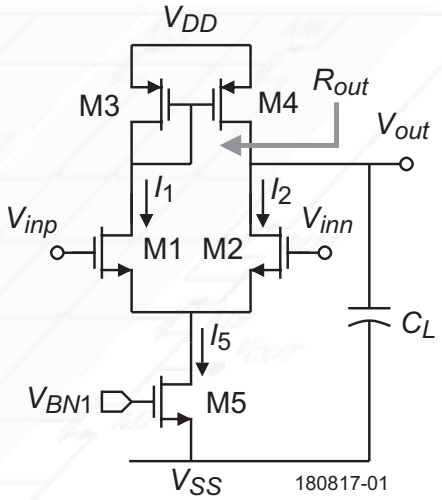




One-Stage, Low-Noise Op Amp Design

Design Procedure – OA10

Step	Design Equations	Comments
1	Use Design Procedure OA1 to design the currents and W/Ls of the one-stage op amp	Use specs for DP OA1
2	Choose $L_3 = L_4 >> L_1 = L_2$	Satisfies $K_n' \frac{W_1}{L_1} > K_p' \frac{W_3}{L_3}$
3	Increase $W_1/L_1 = W_2/L_2$ to minimize thermal noise further	Assumes the voltage gain and GB can be increased
4	To reduce the 1/f noise, make $L_1 << L_3$, $W_1 \times L_1$ large, and increase the dc current	This will decrease the voltage gain and increase *GB*



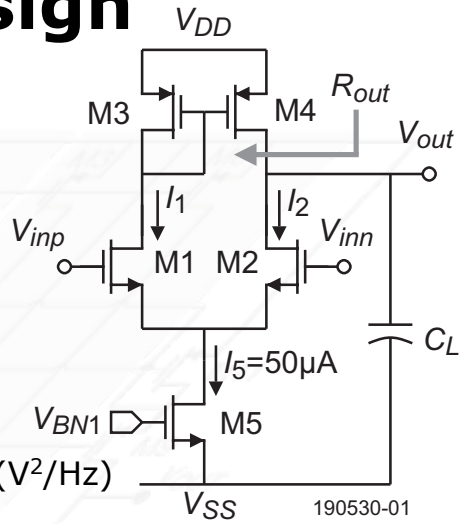
The goal of low noise design is to decrease the thermal and 1/*f* noise of the input transistors and make the voltage gain that occurs immediately after the input transistors as large as possible.

One-Stage Low-Noise Op Amp Design

Example 1:

Minimize the thermal and 1/f noise in the one-stage op amp designed in Example 1 of Lesson 1, Module 4. Assume $kf_n = 4kf_p = 4\text{x}10^{-28}$ F·A, $ef = af = 1$,and $C_{ox}=25\times10^{-4}$ F/m^2. The designed W/L's are given below:

W_1/L_1	W_2/L_2	W_3/L_3	W_4/L_4	W_5/L_5
65.73	65.73	4	4	4.72



1.) Choose $L_1 = L_2 = 1\mu m$ and $L_3 = L_4 = 10\mu m$

2.) The resulting input equivalent thermal voltage noise spectral density is

$$v_{eq}^2 = 2v_{n1}^2\left(1+\sqrt{\frac{K_p'(W_3/L_3)}{K_n'(W_1/L_1)}}\right) = 2v_{n1}^2(1.113) = 2.226\left(\frac{8\times1.38\times10^{-23}\times300}{3\times200\pi\times10^{-6}}\right) = 3.91\times10^{-17}\,(\text{V}^2/\text{Hz})$$

$$v_{eq} = 6.26nV/\sqrt{Hz}$$

3.) The input equivalent 1/f voltage noise spectral density is

$$v_{eq}^2 = 2v_{n1}^2\left(1+\frac{kf_p}{kf_n}\frac{L_1^2}{L_3^2}\right) = 2v_{n1}^2(1.0025) = \frac{2.005}{f}\left(\frac{4\times10^{-28}}{2\times25\times10^{-4}\times120\times10^{-6}\times65.73\times10^{-6}\times1\times10^{-6}}\right) = \frac{1.014\times10^{-11}}{f}\,(\text{V}^2/\text{Hz})$$

$$v_{eq} = \frac{3.185}{\sqrt{f}}\mu V/\sqrt{Hz} \;\Rightarrow\; 1/f \text{ noise corner} = \frac{1.014\times10^{-11}}{3.91\times10^{-17}} = 259kHz$$

4.) Further reduction in noise would come if the dc currents are increased. This would increase the *GB* and decrease the voltage gain. The voltage gain decrease could be made up by an increase in W_1/L_1.

Folded-Cascode, Op Amp

Noise Analysis

Thermal:

$$i_{SC}^2 \cong g_{m1}^2 v_{n1}^2 + g_{m2}^2 v_{n2}^2 + \frac{v_{n6}^2}{r_{ds4}^2} + \frac{v_{n7}^2}{r_{ds5}^2} + \frac{v_{n8}^2}{r_{ds10}^2} + \frac{v_{n9}^2}{r_{ds11}^2}$$
$$+ g_{m10}^2 v_{n10}^2 + g_{m11}^2 v_{n11}^2 + \frac{4kT}{r_{ds4}} + \frac{4kT}{r_{ds5}}$$

Note: $g_{m6}(eff) = \frac{g_{m6}}{1+g_{m6}r_{ds4}} \cong \frac{1}{r_{ds4}}$

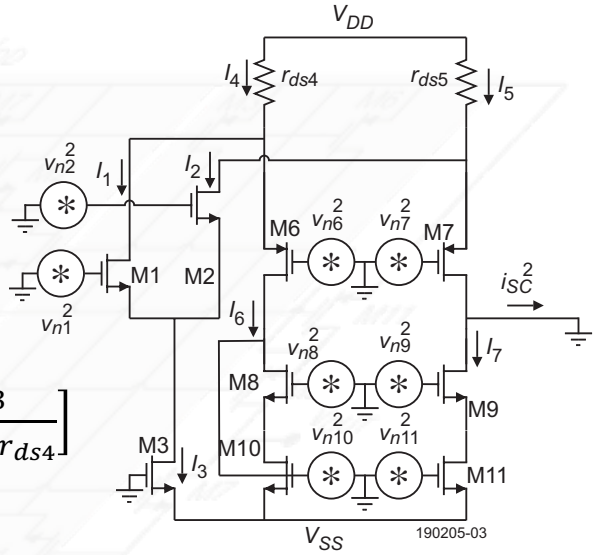
$$v_{eq}^2 = \frac{i_{SC}^2}{g_{m1}^2} = 2v_{n1}^2 + 2\left(\frac{v_{n6}^2}{g_{m1}^2 r_{ds4}^2}\right) + 2\left(\frac{v_{n8}^2}{g_{m1}^2 r_{ds10}^2}\right) + 2\left(\frac{g_{m10}^2}{g_{m1}^2} v_{n10}^2\right) + \frac{8kT}{g_{m1}^2 r_{ds4}}$$

$$v_{eq}^2 \cong 2v_{n1}^2\left[1 + \left(\frac{g_{m10}^2}{g_{m1}^2}\frac{v_{n10}^2}{v_{n1}^2}\right) + \frac{8kT}{v_{n1}^2 g_{m1}^2 r_{ds4}}\right] = 2v_{n1}^2\left[1 + \frac{g_{m10}}{g_{m1}} + \frac{3}{g_{m1}r_{ds4}}\right]$$

$$= 2v_{n1}^2\left[1 + \sqrt{\frac{W_{10}/L_{10}}{W_1/L_1}} + 3\sqrt{\frac{\lambda_p^2 I_4}{2K_p'(W_4/L_4)}}\right]$$

1/f:

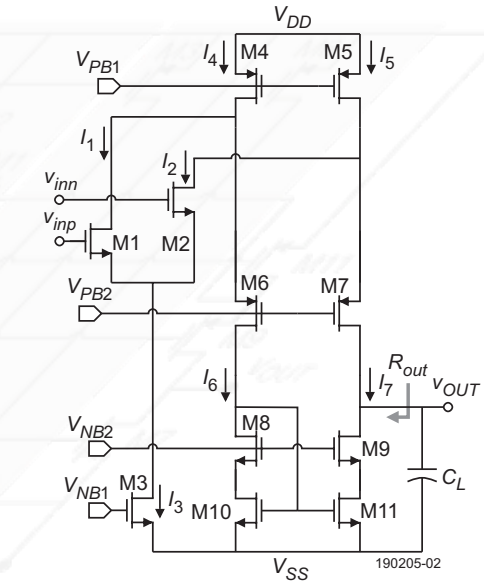
$$v_{eq}^2 \cong 2v_{n1}^2\left[1 + \left(\frac{g_{m10}^2}{g_{m1}^2}\frac{v_{n10}^2}{v_{n1}^2}\right)\right] = 2v_{n1}^2\left(1 + \frac{L_1^2}{L_{10}^2}\right)$$



Folded-Cascode, Low-Noise Op Amp Design

Design Procedure – OA11

Step	Design Equations	Comments
1	Use Design Procedure OA3 to design the currents and *W*/*L*s of the folded-cascode op amp	Use specs for DP OA3
2	Choose $L_{10} = L_{11} >> L_1 = L_2$	Satisfies $\frac{W_1}{L_1} > \frac{W_{10}}{L_{10}}$
3	Increase $W_1/L_1 = W_2/L_2$ to minimize thermal noise further	Assumes the voltage gain and GB can be increased
4	Increase W_4/L_4 and W_5/L_5	Reduces the 4kTR noise of M4 and M5
5	To reduce the 1/f noise, make $L_1 << L_{10}$, $W_1 \times L_1$ large, and increase I_3	This decreases the voltage gain and increases *GB*



The goal of low noise design is to decrease the thermal and 1/*f* noise of the input transistors and make the voltage gain that occurs immediately after the input transistors as large as possible.

Folded Cascode, Low Noise Op Amp Design

Example 2:

Minimize the thermal and 1/f noise in the folded cascode op amp designed in Example 3 of Lesson 1, Module 4. Assume $kf_n = 4kf_p = 4\text{x}10^{-28}$ F·A, $ef = af = 1$,and $C_{ox}=25\times10^{-4}$ F/m^2. The designed W/L's are given in the table below:

W_1/L_1	W_2/L_2	W_3/L_3	W_4/L_4	W_5/L_5	W_6/L_6	W_7/L_7	W_8/L_8	W_9/L_9	W_{10}/L_{10}	W_{11}/L_{11}
33	33	15	160	160	160	160	20	20	20	20

1.) Choose $L_1 = L_2 = 1\mu m$ and $L_{10} = L_{11} = 10\mu m$

2.) The resulting input equivalent thermal voltage noise spectral density is

$$v_{eq}^2 = 2v_{n1}^2\left[1+\sqrt{\frac{W_{10}/L_{10}}{W_1/L_1}}+3\sqrt{\frac{\lambda_p^2 I_4}{2K_p'(W_4/L_4)}}\right] = 2v_{n1}^2(1+.77+0.0137) = 1.878\times10^{-16}\ (\text{V}^2/\text{Hz})$$

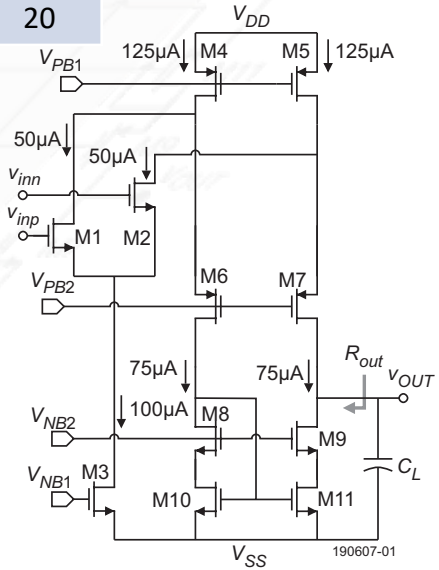
$$v_{eq} = 13.7nV/\sqrt{Hz}$$

3.) The thermal noise has increased due to the contribution of M10 and M11. We could minimize it by increasing the W/L of M1 and M2 to a 1000. This should increase the voltage gain and GB roughly by a factor of 5.5. With this value we get, $v_{eq}^2 = 7.362\times10^{-18}\ (V^2/Hz)\ or\ v_{eq}^2 = 2.71nV/\sqrt{Hz}$.

4.) For the 1/f noise,

$$v_{eq}^2 \cong 2v_{n1}^2\left(1+\frac{L_1^2}{L_{10}^2}\right) = \frac{2.02}{f}\left(\frac{4\times10^{-28}}{2\times25\times10^{-4}\times120\times10^{-6}\times33\times10^{-6}\times1\times10^{-6}}\right) = \frac{2.02\times10^{-11}}{f}\ (\text{V}^2/\text{Hz})$$

$$v_{eq} = \frac{4.495}{\sqrt{f}}\mu V/\sqrt{Hz} \Rightarrow 1/f \text{ noise corner} = \frac{2.02\times10^{-11}}{1.878\times10^{-16}} = 107kHz$$



Two-Stage Op Amp

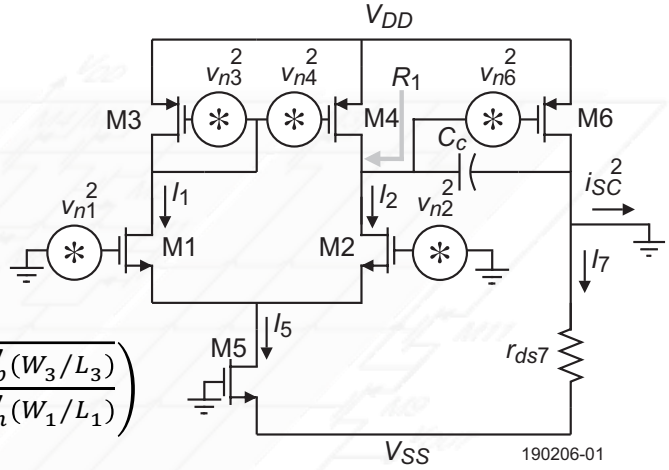
Noise Analysis

Thermal:

$$i_{SC}^2 \cong g_{m1}^2 R_1^2 g_{m6}^2 v_{n1}^2 + g_{m2}^2 R_1^2 g_{m6}^2 v_{n2}^2 + g_{m3}^2 R_1^2 g_{m6}^2 v_{n3}^2 + g_{m4}^2 R_1^2 g_{m6}^2 v_{n4}^2 + g_{m6}^2 v_{n6}^2 + 4kTr_{ds7}$$

$$v_{eq}^2 = \frac{i_{SC}^2}{g_{m1}^2 R_1^2 g_{m6}^2} = 2v_{n1}^2 + 2v_{n3}^2 + \frac{v_{n6}^2}{g_{m1}^2 R_1^2} + \frac{8kTr_{ds7}}{g_{m1}^2 R_1^2 g_{m6}^2}$$

$$v_{eq}^2 \cong 2v_{n1}^2\left[1 + \left(\frac{g_{m3}^2}{g_{m1}^2}\frac{v_{n3}^2}{v_{n1}^2}\right)\right] = 2v_{n1}^2\left[1 + \frac{g_{m3}}{g_{m1}}\right] = 2v_{n1}^2\left(1 + \sqrt{\frac{K_p'(W_3/L_3)}{K_n'(W_1/L_1)}}\right)$$



1/f:

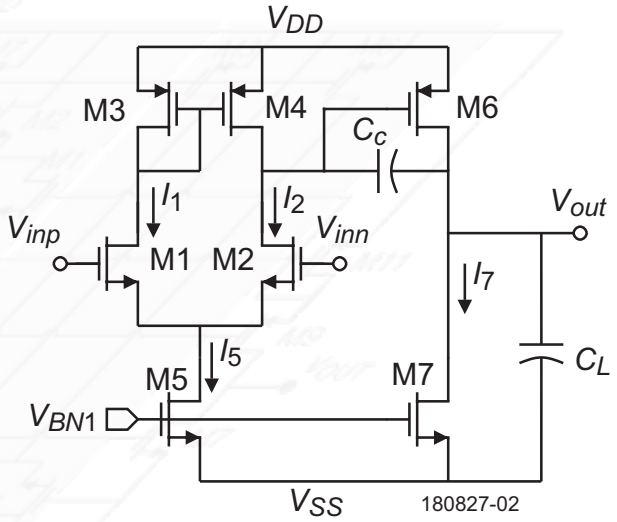
$$v_{eq}^2 \cong 2v_{n1}^2\left[1 + \left(\frac{g_{m3}^2}{g_{m1}^2}\frac{v_{n3}^2}{v_{n1}^2}\right)\right] = v_{eq}^2 = 2v_{n1}^2\left(1 + \frac{kf_p}{kf_n}\frac{L_1^2}{L_3^2}\right)$$

If the gain of the first stage is reasonably large, the noise performance is identical with the one-stage op amp in slide 5. Therefore, the design procedure developed on the next slide for the two-stage op amp noise design will be similar to the Design Procedure OA10.

Two-Stage, Low-Noise Op Amp Design

Design Procedure – OA12

Step	Design Equations	Comments
1	Use Design Procedure OA4 to design the currents and W/Ls of the two-stage op amp	Designs all W/L's and currents
2	Choose $L_3 = L_4 >> L_1 = L_2$	Satisfies $K_n' \frac{W_1}{L_1} > K_p' \frac{W_3}{L_3}$
3	Increase $W_1/L_1 = W_2/L_2$ to minimize thermal noise further	Assumes the voltage gain and GB can be increased
4	To reduce the 1/f noise, make $L_1 << L_3$, $W_1 \times L_1$ large, and increase the dc current	This will decrease the voltage gain and increase GB



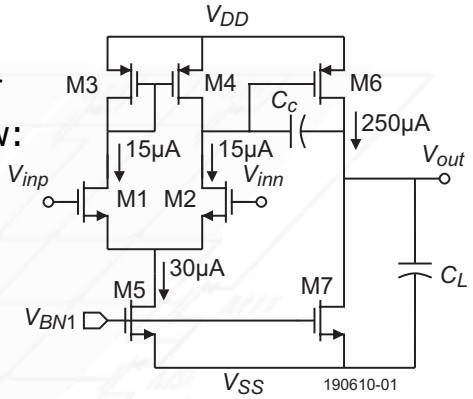
The goal of low noise design is to decrease the thermal and 1/f noise of the input transistors and make the voltage gain that occurs immediately after the input transistors as large as possible.

Two-stage Low Noise Op Amp Design

Example 3:

Minimize the thermal and 1/f noise in the two-stage op amp designed in Example 1 of Lesson 2, Module 4. Assume $kf_n = 4kf_p = 4\text{x}10^{-28}$ F·A, $ef = af = 1$,and $C_{ox}=25\times10^{-4}$ F/m^2. The designed W/L's are given in the table below:

W_1/L_1	W_2/L_2	W_3/L_3	W_4/L_4	W_5/L_5	W_6/L_6	W_7/L_7
9.87	9.87	2.4	2.4	4.3	284	35.8



1.) Choose $L_1 = L_2 = 1\mu m$ and $L_3 = L_4 = 10\mu m$

2.) The resulting input equivalent thermal voltage noise spectral density is

$$v_{eq}^2 = 2v_{n1}^2\left(1+\sqrt{\frac{K_p'(W_3/L_3)}{K_n'(W_1/L_1)}}\right) = 2v_{n1}^2(1.225) = 2.45\left(\frac{8\times1.38\times10^{-23}\times300}{3\times60\pi\times10^{-6}}\right) = 14.35\times10^{-17}\,(\text{V}^2/\text{Hz})$$

$$v_{eq} = 11.98nV/\sqrt{Hz}$$

3.) The input equivalent 1/f voltage noise spectral density is

$$v_{eq}^2 = 2v_{n1}^2\left(1+\frac{kf_p}{kf_n}\frac{L_1^2}{L_3^2}\right) = 2v_{n1}^2(1.0025) = \frac{2.005}{f}\left(\frac{4\times10^{-28}}{2\times25\times10^{-4}\times120\times10^{-6}\times9.87\times1\times10^{-12}}\right) = \frac{6.754\times10^{-11}}{f}\,(\text{V}^2/\text{Hz})$$

$$v_{eq} = \frac{8.218}{\sqrt{f}}\mu V/\sqrt{Hz} \;\Rightarrow\; 1/f \text{ noise corner} = \frac{6.754\times10^{-11}}{14.35\times10^{-17}} = 471kHz$$

4.) Further reduction in noise would come if the dc currents are increased. This would increase the GB and decrease the voltage gain. The voltage gain decrease could be made up by an increase in $W_1/L_1 = W_2/L_2$ or W_6/L_6.

Low Noise Op Amps

RMS Noise

Up to this point, we have considered just the noise spectral density of the op amps. In practice, the op amp has a bandwidth and the rms noise of the op amp is the noise spectral density times the bandwidth.

Example

Consider the spectral noise of the previous two-stage op amp. The low-frequency gain was 4834 V/V and the *GB* was 10MHz. The dominant pole was 10MHz/4834 = 2069Hz. To find the rms noise voltage, we will assume the thermal noise remains flat as frequency increases and integrate the 1/f noise from 1Hz to the 1/f frequency (471kHz) and the thermal noise from 471kHz to 10MHz.

$$V_{eq}^2(rms) = \int_1^{471kHz}\left(\frac{6.754\times10^{-11}}{f}\right)df + \int_{471kHz}^{10MHz}(14.35\times10^{-17})df$$

$$= 6.754\times10^{-11}[\ln(471kHz) - \ln(1)] + 14.35\times10^{-17}(9.53MHz)$$

$$= 6.754\times10^{-11}(13.066) + 1.367\times10^{-9} = 2.25\times10^{-9}\ V^2(rms)$$

$$V_{eq}(rms) = 47.43\mu V(rms)$$

Simulation gives 52.7μV(rms) for the rms noise 1Hz to 10MHz and 32.41x10^{-17} V^2/Hz for the thermal noise

Low Noise Op Amp Design

Summary:

- Noise models and noise analysis techniques
- Simple one-stage op amp
  - Noise analysis
  - Design procedure OA10
  - Example 1
- Folded cascode op amp
  - Noise analysis
  - Design procedure OA11
  - Example 2
- Two-stage op amp
  - Noise analysis
  - Design procedure OA12
  - Example 3
- Equivalent input RMS noise voltage of op amps