HOW TO DESIGN BIAS CIRCUITS INDEPENDENT OF V_{DD} AND PROCESS

Topics:

- How process influences circuit performance
- Bias voltages independent of V_{DD} (V) and process (P)
- Bias currents independent of V_{DD} and process minimization
- Design procedures
- Examples

What will I learn?

- The principles of V_{DD} (V) and process (P) influence
- How to design voltage and current bias circuits that are independent of voltage and minimize process influence

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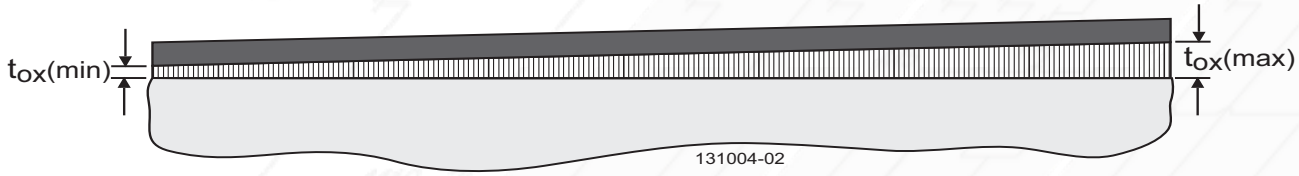
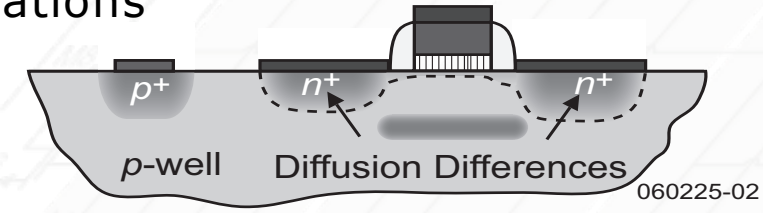
Process Influence (*P*) on Bias Circuits

How does technology vary?

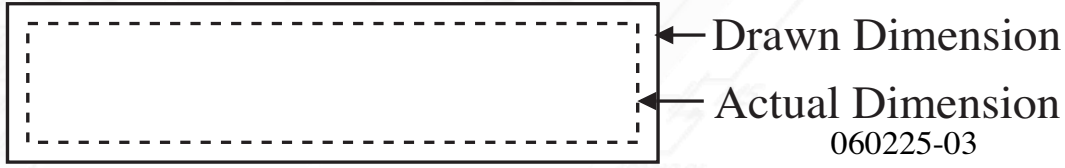
1. Thickness variations in layers (dielectrics and conductors)



2. Doping variations



3. Process biases – differences between the drawn and actual dimensions due to etching, lateral diffusion, etc.



Process Influence on Bias Circuits

Influence on Circuits:

- Transistors
  - MOS: K' and V_T all a function of process
  - BJT: β, n, and I_S all a function of process
- Resistors
  - R a function of process
- Capacitors
  - C a function of process

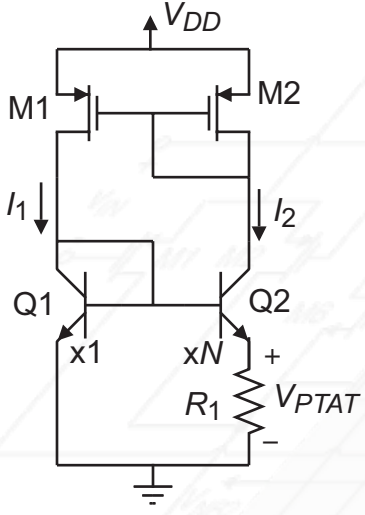
Simulation:

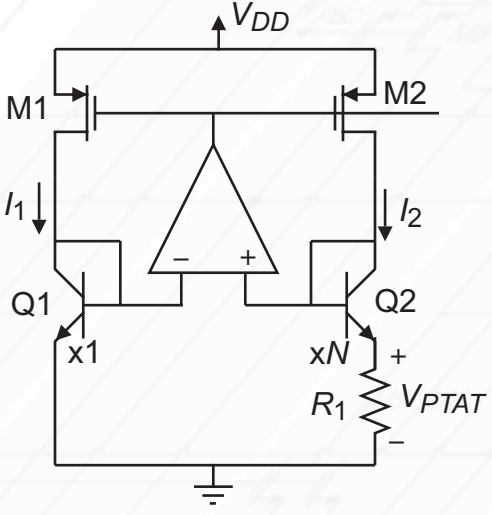
Use worst case model parameters or Monte Carlo to simulate the influence of process variation on the circuit performance

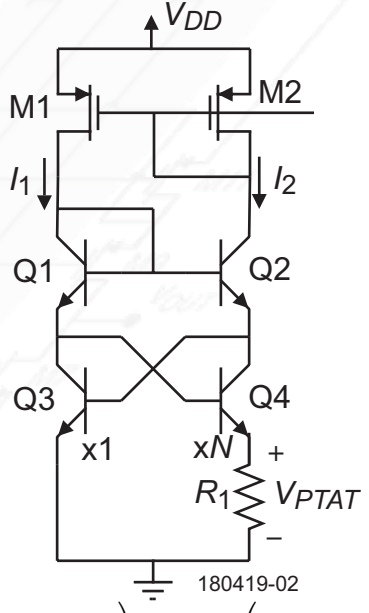
Bias Voltages Independent of *V* and *P*

VPTAT:

The familiar *VPTAT* circuit results in a voltage truly independent of V_{DD} and process.







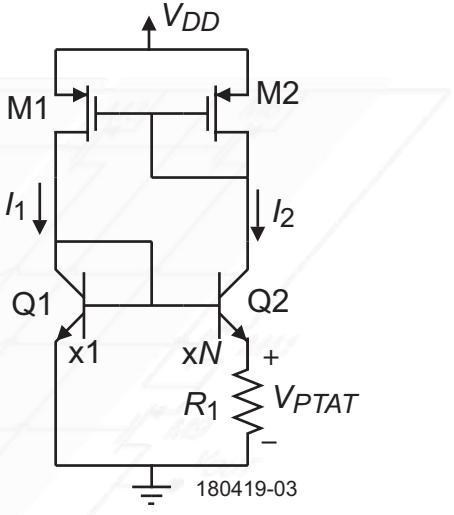
$$V_{PTAT} = V_t \ln\left(\frac{I_1}{I_{S1}} \times \frac{I_{S2}}{I_2}\right) = \frac{kT}{q}\ln\left(\frac{I_{S2}}{I_{S1}}\right) = \frac{kT}{q}\ln\left(\frac{A_{E2}}{A_{E1}}\right) \quad \text{if } I_1 = I_2$$

$$V_{PTAT} = V_t \ln\left(\frac{I_{S1}}{I_{S2}}\frac{I_{S4}}{I_{S3}}\right) = V_t \ln\left(\frac{A_{E1}}{A_{E2}}\frac{A_{E4}}{A_{E3}}\right)$$

Design Procedure for Bias Voltage Independent of *V* and *P*

Design Procedure, BP1:

Step	Design Equations	Comments
1	Select I_1 and I_2	$P_{diss}=V_{DD}(I_1+I_2)$
2	Choose $W_1/L_1 = W_2/L_2$	Let $W_1/L_1 = W_2/L_2 > 1$ and choose L_1 and L_2 long for good matching and PSRR
3	Choose A_{E1} and A_{E2}	Current density of emitter
4	$R = \frac{V_t \times \ln(A_{E2}/A_{E1})}{I_2}$	Resistor design, R. Assume $A_{E2} = 10A_{E1}$



Example 1:

Design a V_{PTAT} voltage bias assuming P_{diss} = 30μW, V_{DD} = 5V and the BJTs have a current rating of 1μA/μm².

1.) 30μW/5V = 6μA. Choose $I_1 = I_2 = 2\mu A$.

2.) Choose $W_1 = W_2 = 50\mu m$ and $L_1 = L_2 = 10\mu m$.

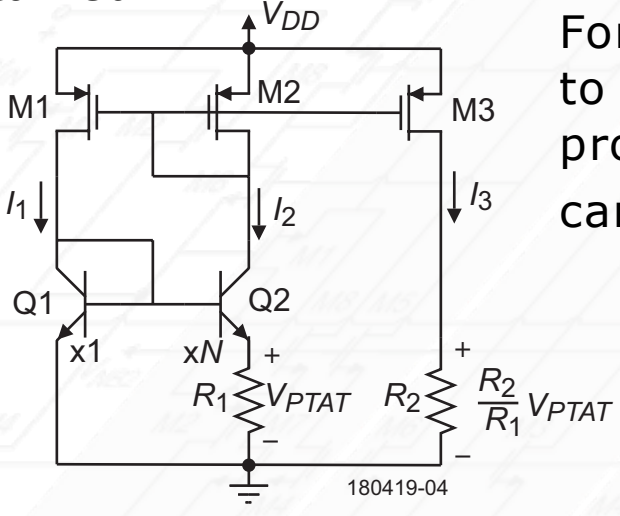
3.) For 2μA, the emitter area should be 2μm². Choose 10μm².

4.) R=0.026xln(10)/2μA=29.93kΩ.

Adjusting the Value of V_{PTAT}

Values of V_{PTAT} other than $V_t\ ln(N)$:

- Normally, the value of V_{PTAT} is approximately 60mV depending on the temperature and the value of N.
- The following technique allows different values of V_{PTAT} to be obtained.



For this circuit to work, $R1$ and $R2$ have to the same type of resistor so that the process dependence (P) of the resistor cancels out.

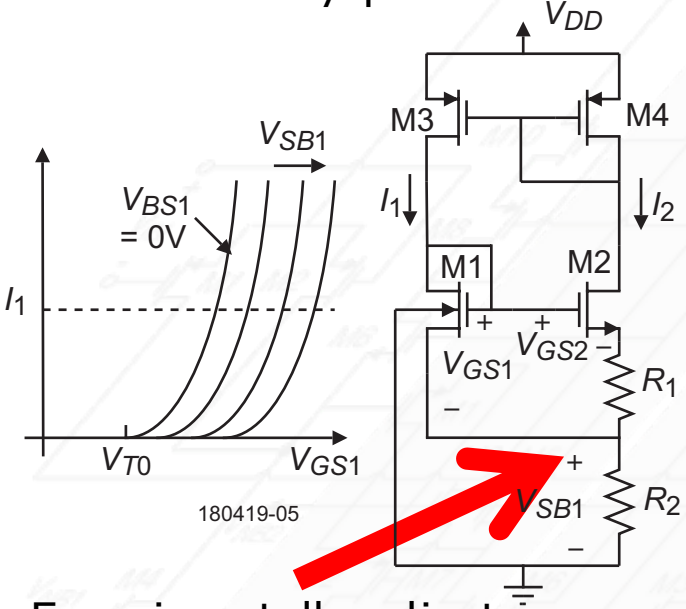
$$V_{Bias} = \frac{R_2}{R_1} V_{PTAT} \rightarrow \frac{dV_{Bias}}{dP} = \left(\frac{1}{R_1}\frac{dR_2}{dP} - \frac{R_2}{R_1^2}\frac{dR_1}{dP} \right) V_{PTAT}$$

$$= \frac{R_2}{R_1}\left(\frac{1}{R_2}\frac{dR_2}{dP} - \frac{1}{R_1}\frac{dR_1}{dP} \right) V_{PTAT} = \frac{R_2}{R_1} V_{PTAT}$$

Current Bias with Minimum *P* Influence

Backgate Bias Technique:

Principle – Balance the components determining the current that are influenced by process so that they oppose each other.



Experimentally adjust split for best results

$$I_1 = I_2 = \frac{\Delta V_{GS}}{R_1} \rightarrow \frac{1}{I}\frac{dI}{dP} = \frac{1}{\Delta V_{GS}}\frac{d(\Delta V_{GS})}{dP} - \frac{1}{R_1}\frac{dR_1}{dP}$$

where $I_1 = I_2 = I$ and $\Delta V_{GS} = V_{GS1} - V_{GS2}$

$$\Delta V_{GS} \approx K_1 + K_2\sqrt{R_2} \rightarrow \frac{d(\Delta V_{GS})}{dP} \approx \frac{K_2}{\sqrt{R_2}}\frac{dR_2}{dP}$$

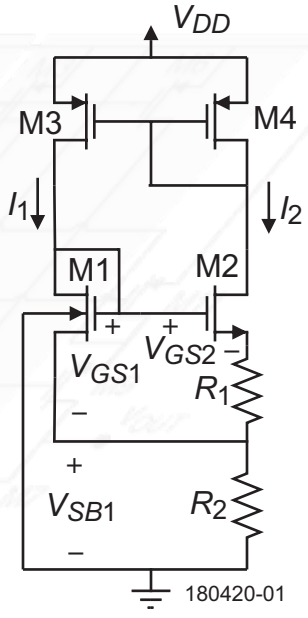
So that, $$\frac{1}{I}\frac{dI}{dP} = \frac{K_2}{\Delta V_{GS}\sqrt{R_2}}\frac{dR_2}{dP} - \frac{1}{R_1}\frac{dR_1}{dP}$$

Note that when R_1 and R_2 increase, V_{GS1} increases because of $V_{SB1} = I_2R_2$ increases which causes ΔV_{GS} to increase which opposes the decrease in I_2 due to the increase in R_1 and R_2 .

Design Procedure for Current Bias with Minimum *P* Dependence using Backgate Bias

Design Procedure, BP2:

Step	Design Equations	Comments
1	Design M1, M2, M3, M4, and R_1	Use BV1 design procedure
2	Choose $R_1 = R_2$	R is from BV1 design procedure
3	Experimentally adjust the value of R_2 for best process independence	Use worst case or Monte Carlo simulation



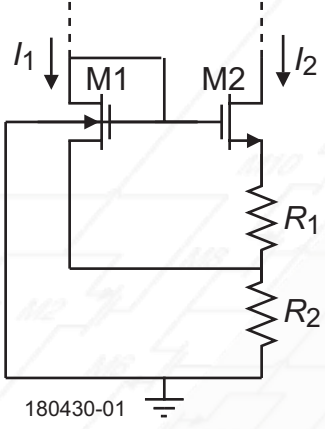
Example 2:

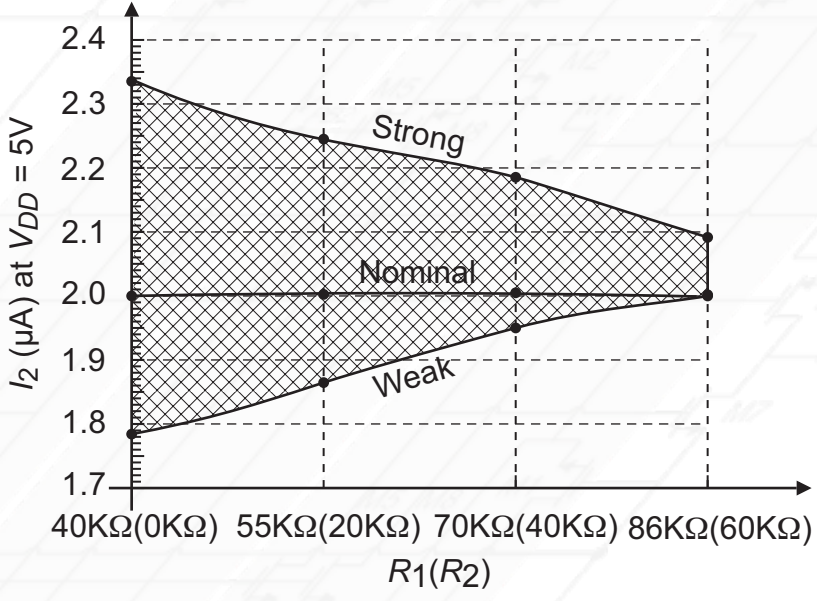
1. From Example 1 of Bias Design Independent of V_{DD}†,
   $I_1 = I_2 = 2\mu A$, $W_1/L_1 = 10\mu m/1\mu m$, $W_2/L_2 = 40\mu m/1\mu m$, $W_3/L_3 = W_4/L_4 = 20\mu m/1\mu m$, and $R_2 = 11.18k\Omega$.
2. $R_1 = R_2 = 11.18k\Omega$.
3. Experimentally adjust the value of R_2 for best results (see next slide)

† How to design Bias Currents Independent of V_{DD}

Design Procedure for Current Bias with Minimum *P* Dependence using Backgate Bias

Experimental Adjustment of R_2:

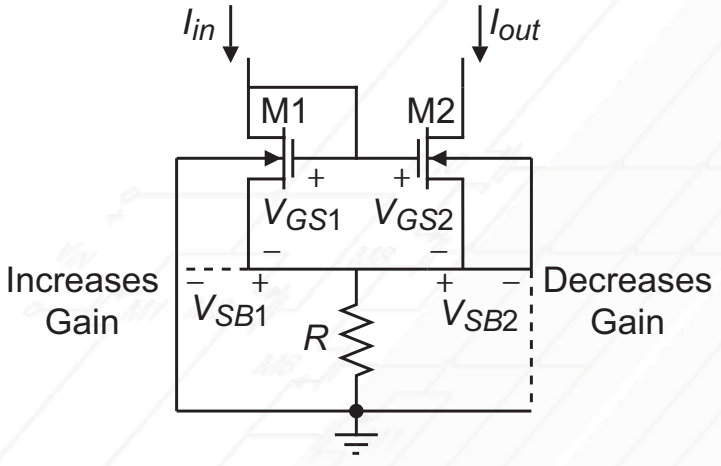


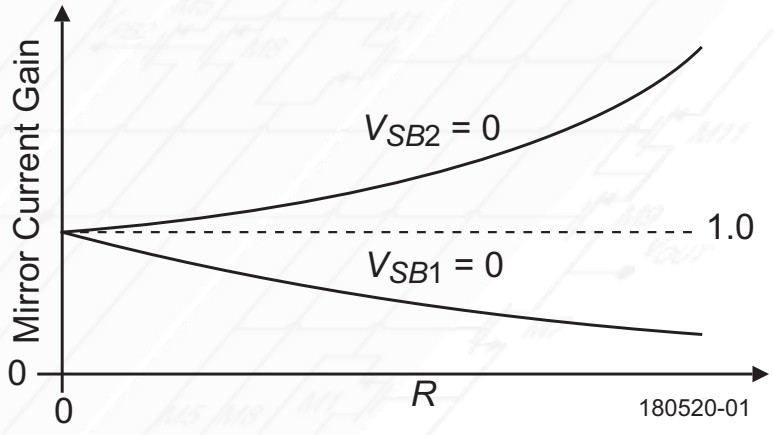


As R_2 becomes larger, the voltage drop it creates will increase the minimum power supply voltage at which the bias circuit works properly.

Current Mirror Gains Dependent on Process

The previous concept can be used to create current mirrors whose gain depends on resistance.





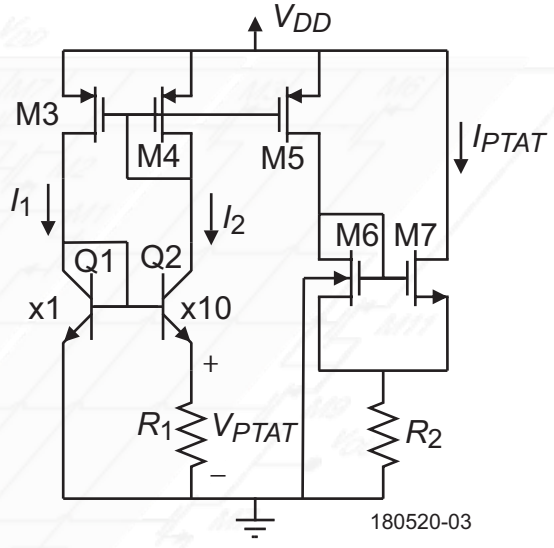
Note the positive feedback loop ($V_{GS2}\uparrow \rightarrow I_{out}\uparrow \rightarrow V_{SB1}\uparrow \rightarrow V_{GS1}\uparrow \rightarrow V_{GS2}\uparrow$) with a loop gain of $LG = \frac{g_{m2}}{g_{m1}}\left(\frac{g_{mbs1}r_{ds2}R}{r_{ds2}+R}\right)$ which becomes greater than 1 as R increases.

Cannot use R greater than the value which causes the loop gain to become unity.

Design Procedure for Current Bias with Minimum *P* Dependence

Design Procedure, BP3:

Step	Design Equations	Comments
1	Design Q1, Q2, M3, M4, and R_1	Use BP1 design procedure
2	Let M5 = M4	
3	Chose $W_6/L_6 = W_7/L_7$	Large *WxL* for good matching
4	Experimentally adjust the value of R_2 for best process independence	Use worst case or Monte Carlo simulation



Example 3:

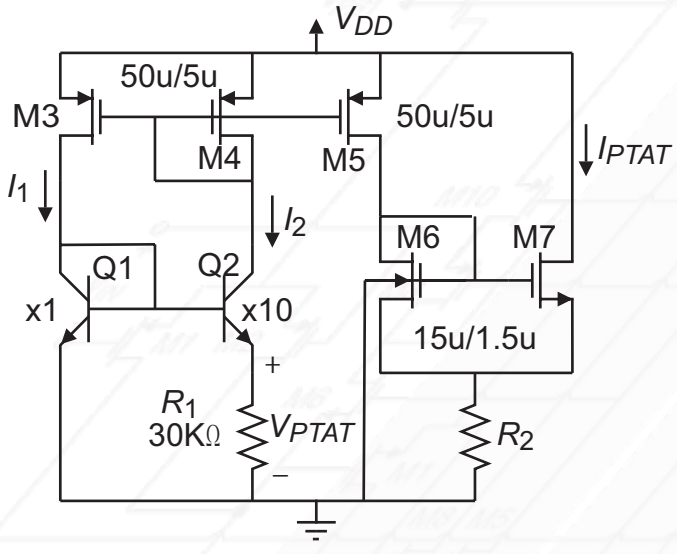
1. From Example 1 of design procedure BP1,

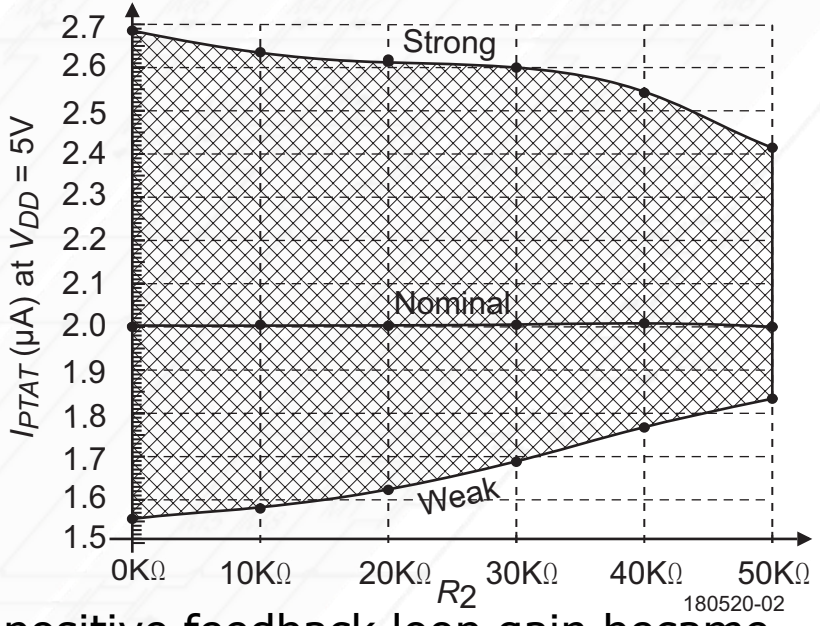
   $I_1 = I_2 = 2\mu A$, $A_{E1} = 6.3\mu m \times 6.3\mu m$, $A_{E2} = 10\,A_{E1}$,

   $W_3/L_3 = W_4/L_4 = W_5/L_5 = 50\mu m/5\mu m$, and $W_6/L_6 = W_7/L_7 = 15\mu m/1.5\mu m$.
2. $R_1 = 60mV/2\mu A = 30k\Omega$.
3. Experimentally adjust the value of R_2 for best results (see next slide)

I_{PTAT} with Minimum P Influence

Circuit:





In this circuit (0.35μm BiCMOS) the positive feedback loop gain became greater than unity for the Weak model at 60KΩ.

Summary – Process and V_{DD} Independent Design

Voltage and Process Temperature Independent Bias Design:

- Objective of biasing – independence of V_{DD}, and process
- Simple V_{PTAT} circuit
- Reducing process influence for CMOS current bias circuits
- Reducing process influence for I_{PTAT} current bias circuits
- Design procedures – BP1, BP2, and BP3
- Examples