

LECTURE 2 - HOW TO DESIGN CASCODE BIAS CIRCUITS INDEPENDENT OF V_{DD}

Topics:

- Biasing of cascode circuits
- Design procedures
 - Cascode bias circuits
 - BJT cascode bias circuits
- Examples

What will I learn?

- How to design cascode bias circuits that are independent of V_{DD}

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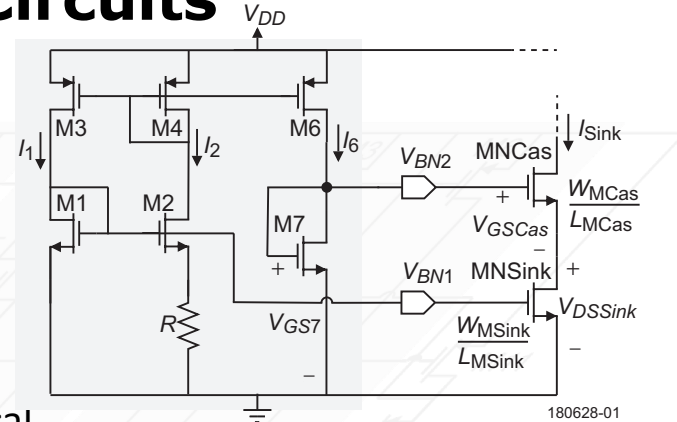
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Biasing Cascode Circuits

Cascode Circuits

- Cascode circuits increase output resistance and improve current mirror matching
- Bias must optimize signal swing by biasing the cascoded transistor at $V_{DS}(sat)$

Designing V_{BN2} and V_{BP2} :



Assume the K_N' and V_T of M7, MCas, and Msink are identical.

$$V_{GS7} = V_{GSCas} + V_{DSSink}(sat) \rightarrow \sqrt{\frac{2I_6}{K_N' W_7/L_7}} + V_T = \sqrt{\frac{2I_{Sink}}{K_N' W_{Cas}/L_{Cas}}} + V_T + \sqrt{\frac{2I_{Sink}}{K_N' W_{Sink}/L_{Sink}}}$$

$$\sqrt{\frac{2I_6}{K_N' W_7/L_7}} = \sqrt{\frac{2I_{Sink}}{K_N' W_{Cas}/L_{Cas}}} + \sqrt{\frac{2I_{Sink}}{K_N' W_{Sink}/L_{Sink}}} \rightarrow \frac{W_7}{L_7} = \frac{I_6}{I_{Sink}(\sqrt{L_{Cas}/W_{Cas}} + \sqrt{L_{Sink}/W_{Sink}})^2}$$

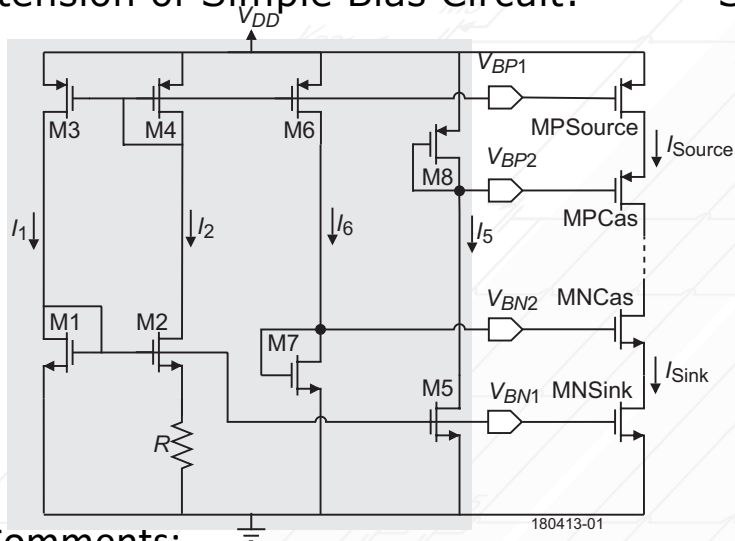
If $W_{CAS}/L_{CAS} = W_{Sink}/L_{Sink}$,

$$\frac{W_7}{L_7} = \frac{I_6}{4I_{Sink}} \frac{W_{Sink}}{L_{Sink}} = \frac{I_6}{4I_{Sink}} \frac{W_{Cas}}{L_{Cas}}$$

V_{DD} Independent Cascode Bias Design

Bias Circuits

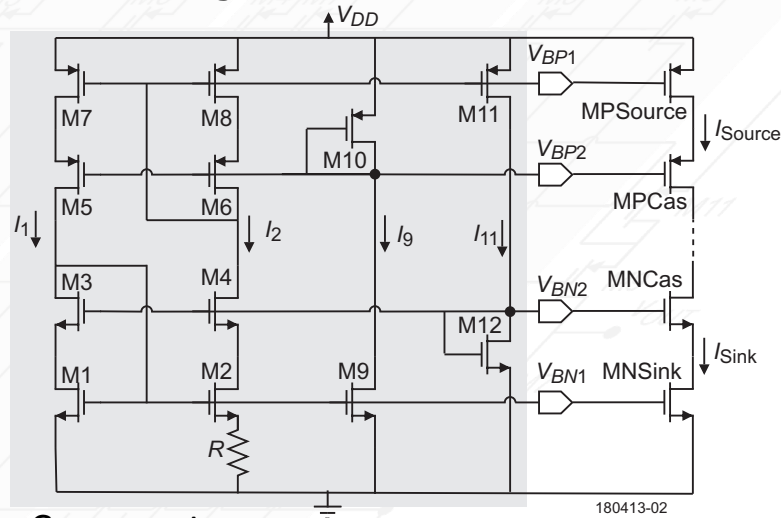
Extension of Simple Bias Circuit:



Comments:

- Straight-forward extension of previous bias circuit
- Current mirrors not accurate

Self-Bias using Positive Feedback:



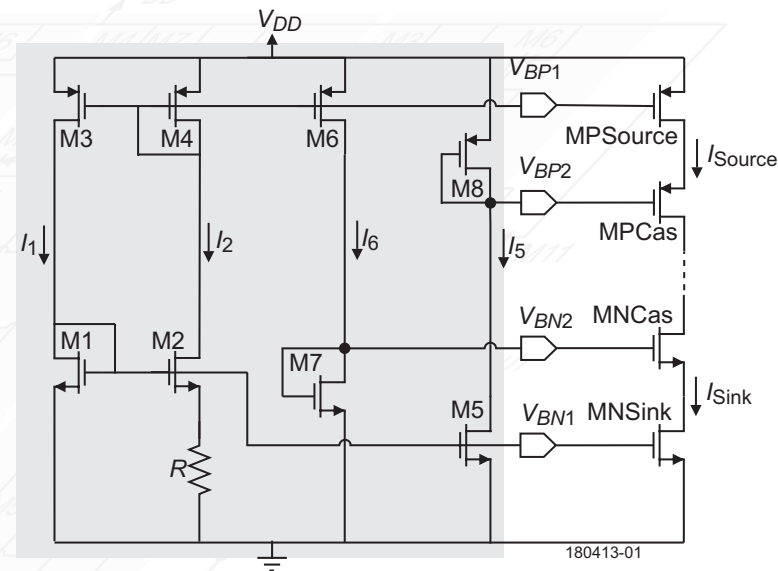
Comments:

- Uses positive feedback with loop gains less than unity
- Current mirrors accurate

V_{DD} Independent Cascode Bias Design Procedure

Design Procedure for Simple Cascode Bias, BV3

Step	Design Equations	Comments
1	Select $I_1 = I_2$ and I_5 and I_6	$P_{diss} = V_{DD}(I_1 + I_2 + I_5 + I_6)$
2	Follow BV1 design procedure	
	V_{BN2} – Use I_6 with gate-drain connected NMOS (M7)	
3	$W_6/L_6 = (I_2/I_6)(W_4/L_4)$	I_6 known (Step 1)
4	$W_7/L_7 = I_6/4I_{Sink} \times W_{Sink}/L_{Sink}$	Assume $W_{NCas}/L_{NCas} = W_{NSink}/L_{NSink}$
	V_{BP2} – Use I_5 with gate-drain connected PMOS (M8)	
5	$W_5/L_5 = (I_1/I_5)(W_1/L_1)$	I_5 known (Step 1)
6	$W_8/L_8 = (I_5/4I_{Source}) \times W_{PSource}/L_{PSource}$	Assume $W_{PCas}/L_{PCas} = W_{PSource}/L_{PSource}$

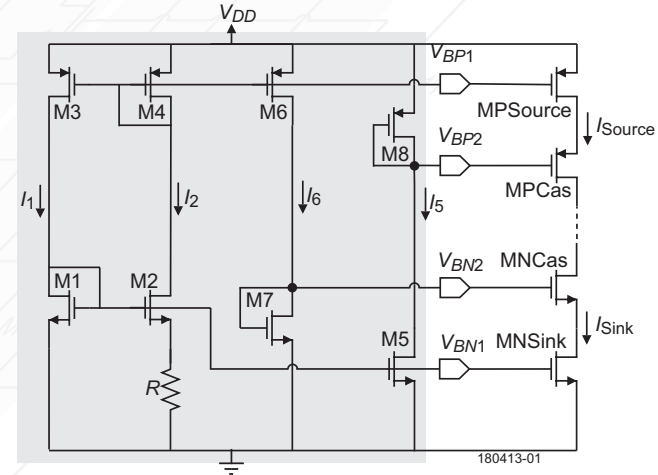


V_{DD} Independent Cascode Bias Design Procedure

Example 1

Use the Design Procedure BV3 to design the bias circuit for an NMOS and PMOS cascode circuit where $I_{Sink} = I_{Source} = 10\mu A$ if $P_{diss} = 40\mu W$, $W_{NCas}/L_{NCas} = W_{NSink}/L_{NSink} = 50\mu m/1\mu m$, $W_{PCas}/L_{Pas} = W_{PSource}/L_{PSource} = 100\mu m/1\mu m$, and $K_N' = 100\mu A/V^2$.

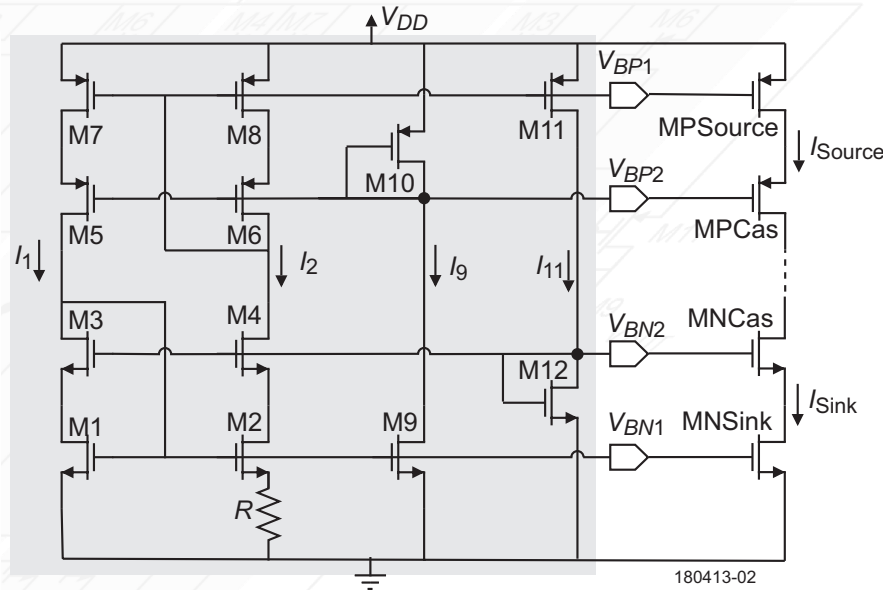
- 1.) Choose $I_1 = I_2 = I_5 = I_6 = 2\mu A$ ($P_{diss} = 40\mu W$)
- 2.) From Design Procedure BV1 we get $L_3 = L_4 = L_{Source} = 1\mu m$, $W_3 = W_4 = (I_2/I_{Source}) \times W_{Source} = 20\mu m$, $L_1 = L_2 = L_{Sink} = 1\mu m$, and $W_1 = W_2/4 = (I_1/I_{Sink}) \times W_{Sink} = 10\mu m$, and $R = 11.18k\Omega$.
- 3.) $W_6/L_6 = (I_2/I_6)(W_4/L_4) = 20\mu m/1\mu m$
- 4.) $W_7/L_7 = (I_6/4I_{Sink})(W_{NSink}/L_{NSink}) = (2/40)(50) = 2.5\mu m/1\mu m$
- 5.) $W_5/L_5 = (I_1/I_5)(W_1/L_1) = 20\mu m/1\mu m$
- 6.) $W_8/L_8 = (I_5/4I_{Source})(W_{NSource}/L_{NSource}) = (2/40)(100) = 5\mu m/1\mu m$



V_{DD} Independent Cascode Bias Design Procedure

Design Procedure for Self-Biased Cascode Bias, BV4

Step	Design Equations	Comments
1	Select $I_1 = I_2$ and I_9 and I_{11}	$P_{diss} = V_{DD}(I_1 + I_2 + I_9 + I_{11})$
2	Follow BV1 design procedure	
3	Let $M5 \text{ \& } M6 = M7 \text{ \& } M8$	$M7 \text{ \& } M8$ are $M3 \text{ \& } M4$ of BV1
4	Let $M3 \text{ \& } M4 = M1$	$M1$ of BV1
5	Follow BV3 to design $M9$ through $M12$	

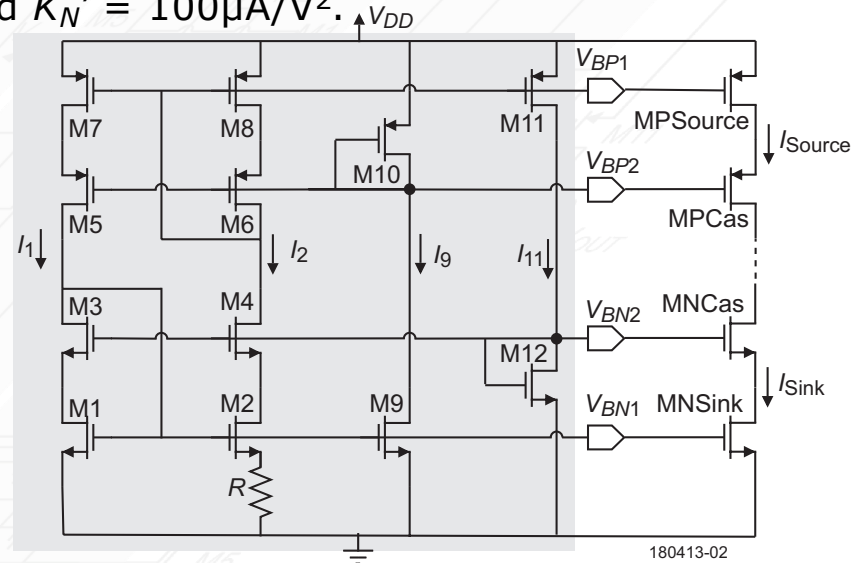


V_{DD} Independent Cascode Bias Design Procedure

Example 2

Use the Design Procedure BV4 to design the self-biased cascode circuit if $V_{DD} = 5V$, $P_{diss} = 40\mu W$, $I_{Sink} = I_{Source} = 10\mu A$, $W_{Sink}/L_{Sink} = W_{NCas}/L_{NCas} = 50\mu m/1\mu m$, $W_{Source}/L_{Source} = W_{PCas}/L_{PCas} = 100\mu m/1\mu m$, and $K_N' = 100\mu A/V^2$.

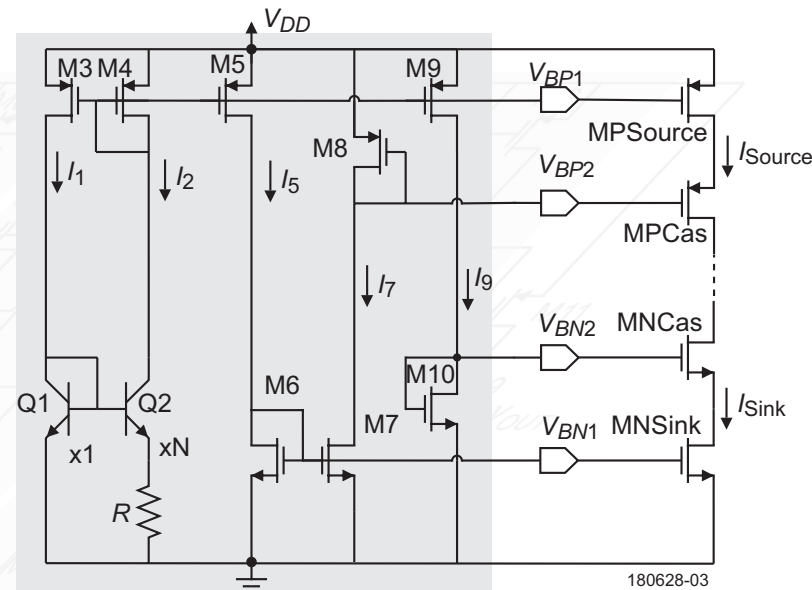
- 1.) Choose $I_1 = I_2 = I_9 = I_{11} = 2\mu A$ ($P_{diss} = 40\mu W$)
- 2.) From DP BV1, we get, $W_7/L_7 = W_8/L_8 = W_5/L_5 = W_6/L_6 = 20\mu m/1\mu m$ and $W_1/L_1 = W_2/4L_2 = W_3/L_3 = W_4/L_4 = 10\mu m/1\mu m$, and $R = 11.18k\Omega$.
- 3.) $W_9/L_9 = W_1/L_1$ and $W_{11}/L_{11} = W_8/L_8$
- 4.) $W_{12}/L_{12} = (I_{11}/4I_{Sink})(W_{NSink}/L_{NSink}) = (2/40)(50) = 2.5\mu m/1\mu m$
- 5.) $W_{10}/L_{10} = (I_9/4I_{Source})(W_{NSource}/L_{NSource}) = (2/40)(100) = 5\mu m/1\mu m$



V_{DD} Independent Bias Design Procedure using BJTs

Design Procedure using BJTs, BV5

Step	Design Equations	Comments
1	Select $I_1 = I_2, I_5, I_6,$ and I_9	$P_{diss} = V_{DD}(I_1 + I_2 + I_5 + I_6 + I_9)$
2	$L_3 = L_4 = L_5 = L_9 = L_{Source}$ and $W_3 = W_4 = (I_2/I_{Source})W_{Source}$	$W_{Source}, L_{Source},$ and I_{Source} known
3	Choose A_{E1} and A_{E2}	Current density of emitter
4	$R = \frac{V_t \times \ln(A_{E2}/A_{E1})}{I_2}$	Resistor design, R . Assume $A_{E2} = 10A_{E1}$
5	$W_5 = (I_2/I_5)(W_4/L_4) L_5$	I_5 and L_5 known (step 1)
6	$W_9 = (I_2/I_9)(W_4/L_4) L_9$	I_9 and L_9 known (step 1)
7	$L_6 = L_7 = L_{Sink}$ & $W_6 = (I_5/I_{Sink})(W_{Sink})$ and $W_7 = (I_7/I_{Sink})(W_{Sink})$	$W_{Sink}, L_{Sink},$ and I_{Sink} known
V_{NB2} – Use I_9 with gate-drain connected NMOS (M10)		
8	$\frac{W_{10}}{L_{10}} = \frac{I_9}{4I_{Sink}} \times \frac{W_{Sink}}{L_{Sink}}$	Assume both cascode and cas-coded transistors have same W/L
V_{PB2} – Use I_5 with gate-drain connected PMOS (M8)		
9	$\frac{W_8}{L_8} = \frac{I_7}{4I_{Source}} \times \frac{W_{Source}}{L_{Source}}$	Assume both cascode and cas-coded transistors have same W/L

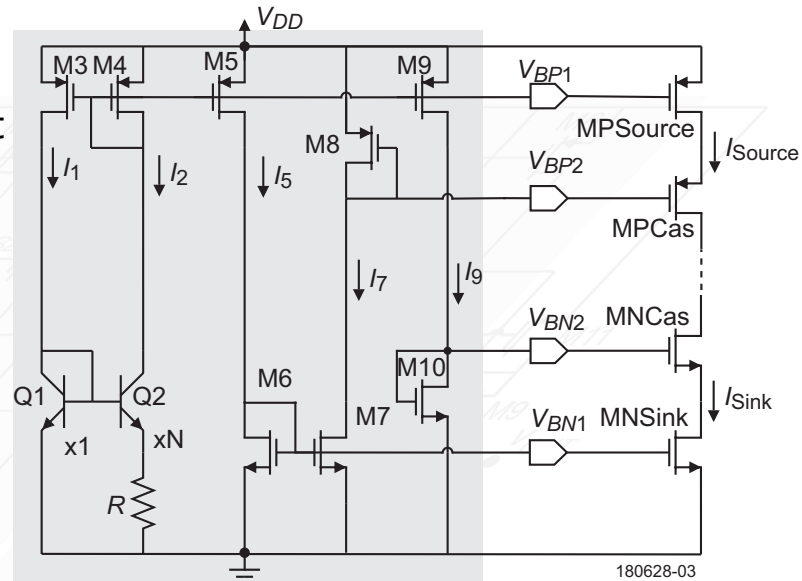


V_{DD} Independent Bias Design Procedure using BJTs

Example 3

Design the bias current generator and the cascode biases. Assume the BJTs have a current rating of $1\mu\text{A}/\mu\text{m}^2$ and $V_{DD} = 5\text{V}$, $P_{diss} = 50\mu\text{W}$, $I_{Sink} = I_{Source} = 10\mu\text{A}$, $W_{Sink}/L_{Sink} = W_{NCas}/L_{NCas} = 50\mu\text{m}/1\mu\text{m}$, $W_{Source}/L_{Source} = W_{PCas}/L_{PCas} = 100\mu\text{m}/1\mu\text{m}$.

- 1.) Let $I_1 = I_2 = I_5 = I_7 = I_9 = 2\mu\text{A}$
- 2.) $L_3=L_4 = L_5=L_9 = L_{Source} = 1\mu\text{m}$ & $W_3=W_4=(I_2/I_{Source})W_{Source} = 20\mu\text{m}$
- 3.) Let the area of Q1 and Q2 be $10\mu\text{m}^2$
- 4.) $R = \frac{V_t \times \ln(A_{E2}/A_{E1})}{I_2} = \frac{0.026 \times \ln(10)}{2\mu\text{A}} = 29.934\text{k}\Omega$
- 5.) $W_5 = W_9 = W_4 = 20\mu\text{m}$
- 6.) $L_6=L_7=L_{Sink} = 1\mu\text{m}$ and $W_6 = (I_5/I_{Sink})(W_{Sink}) = 10\mu\text{m}$ and $W_7 = (I_7/I_{Sink})(W_{Sink}) = 10\mu\text{m}$
- 7.) $W_{10}/L_{10} = I_9/(4I_{Sink}) \times (W_{Sink}/L_{Sink}) = (2/40)(50/1) = 2.5\mu\text{m}/1\mu\text{m}$
- 8.) $W_8/L_8 = I_7/(4I_{Source}) \times (W_{Source}/L_{Source}) = (2/40)(100/1) = 5\mu\text{m}/1\mu\text{m}$



Summary – Cascode Bias Circuit Design

Cascode Bias Circuit Design Independent of V_{DD}

- Biasing cascode circuits
- V_{DD} independent biasing for cascode circuits using MOSFETs
- V_{DD} independent biasing using BJTs (and MOSFETs)
- Design procedures – BV3, BV4, and BV5
- Examples
- All other *How to Design Analog Circuit* lectures will use these bias circuits in one form or another to achieve bias currents in MOSFETs that are independent of V_{DD}