# LECTURE 39 – OVERSAMPLING ADCS – PART I

## LECTURE ORGANIZATION

**Outline**

- Introduction
- Delta-sigma modulators
- Summary

***CMOS Analog Circuit Design*, 3rd Edition Reference**

Pages 589-596

# INTRODUCTION

## What is an oversampling converter?

An oversampling converter uses a noise-shaping modulator to reduce the in-band quantization noise to achieve a high degree of resolution.

- What is the range of oversampling?
  The oversampling ratio, called *M*, is a ratio of the sampling frequency to the Nyquist frequency of the input signal. The Nyquist frequency is twice the bandwidth of the input signal. This oversampling ratio can vary from 8 to 256.
  - The resolution of the oversampled converter is proportional to the oversampled ratio.
  - The bandwidth of the input signal is inversely proportional to the oversampled ratio.
- What are the advantages of oversampling converters?
  Very compatible with VLSI technology because most of the converter is digital
  High resolution
  Single-bit quantizers use a one-bit DAC which has no INL or DNL errors
  Provide an excellent means of trading precision for speed (16-18 bits with a signal bandwidth of 50kHz to 8-10 bits with a signal bandwidth of 5-10MHz).
- What are the disadvantages of oversampling converters?
  Difficult to model and simulate
  Limited in bandwidth to the clock frequency divided by the oversampling ratio

## Nyquist Versus Oversampled ADCs

Conventional Nyquist ADC Block Diagram:

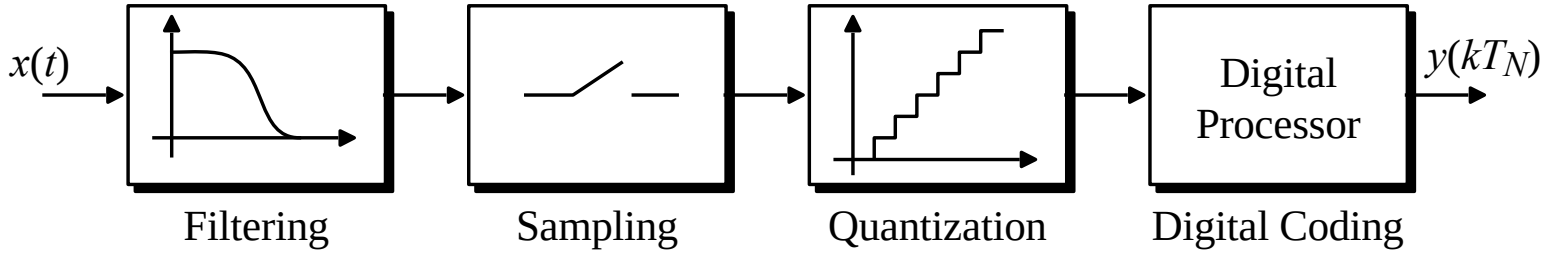



Fig.10.9-01

Oversampled ADC Block Diagram:

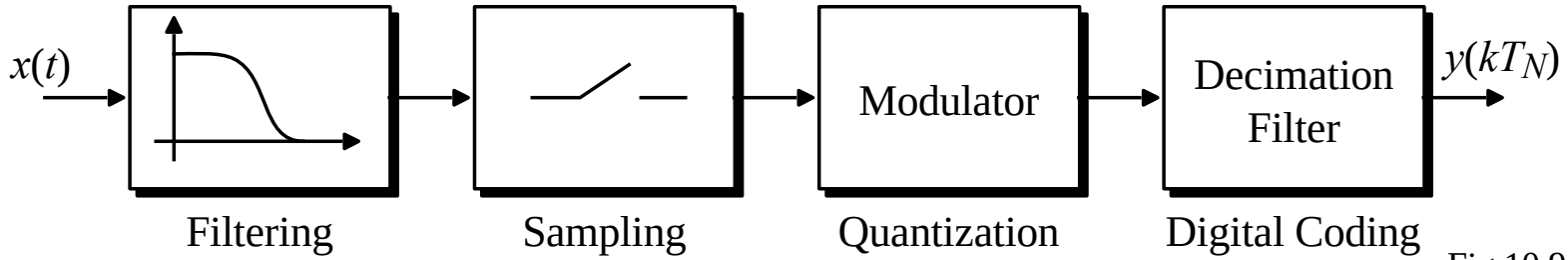



Fig.10.9-02

Components:

- Filter - Prevents possible aliasing of the following sampling step.
- Sampling - Necessary for any analog-to-digital conversion.
- Quantization - Decides the nearest analog voltage to the sampled voltage (determines the resolution).
- Digital Coding - Converts the quantizer information into a digital output signal.

# Frequency Spectrum of Nyquist and Oversampled Converters

Definitions:

$f_B$ = analog signal bandwidth

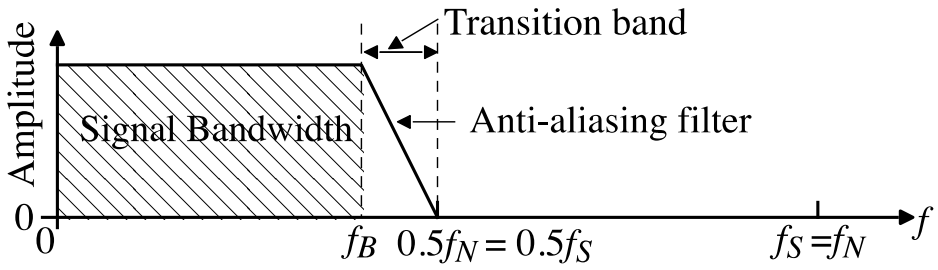
$f_N$ = Nyquist frequency (two times $f_B$)

$f_S$ = sampling or clock frequency

$M = \frac{f_S}{f_N} = \frac{f_S}{2f_B}$ = oversampling ratio

Frequency prespective:

Conventional ADC with $f_B \approx 0.5f_N = 0.5f_S$.




Oversampled ADC with $f_B \approx 0.5f_N << f_S$.

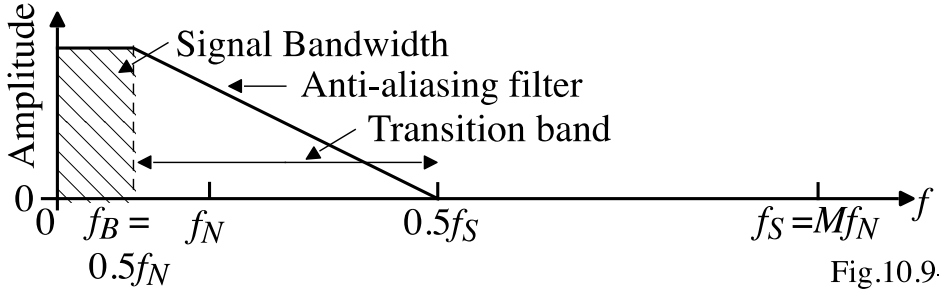



Fig.10.9-03

## Quantization Noise of a Conventional (Nyquist) ADC

Multilevel Quantizer:

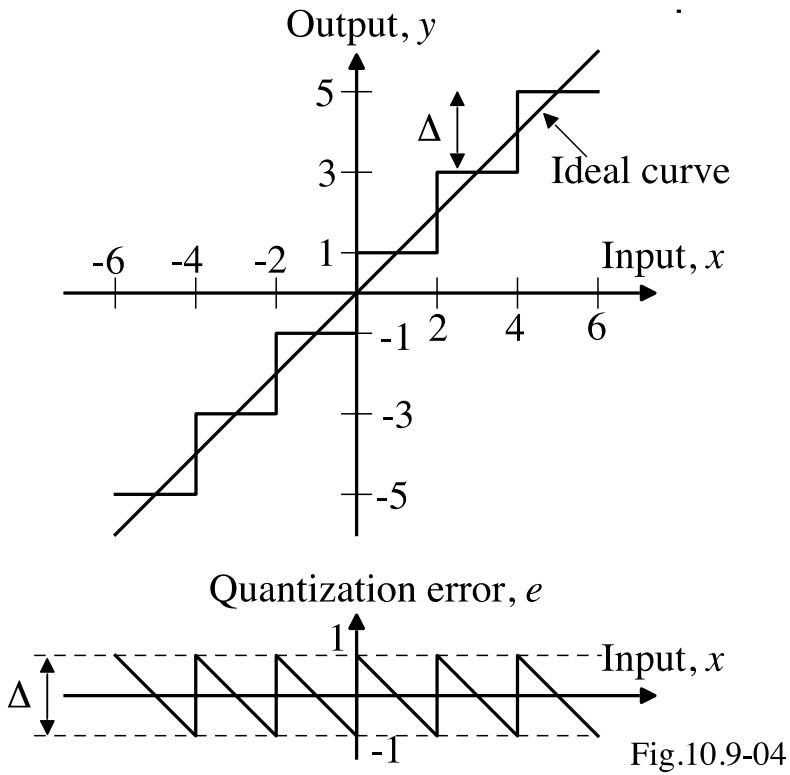



Fig.10.9-04

The quantized signal $y$ can be represented as,

$$y = Gx + e$$

where

$G$ = gain of the ADC, normally 1

$e$ = quantization error

The mean square value of the quantization error is

$$e_{rms}^2 = S_Q = \frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2} e(x)^2 dx = \frac{\Delta^2}{12}$$

## Quantization Noise of a Conventional (Nyquist) ADC - Continued

Spectral density of the sampled noise:

When a quantized signal is sampled at $f_S$ (= $1/\tau$), then all of its noise power folds into the frequency band from 0 to $0.5f_S$. Assuming that the noise power is white, the spectral density of the sampled noise is,

$$E(f) = e_{rms}\sqrt{\frac{2}{f_S}} = e_{rms}\sqrt{2\tau}$$

where $\tau = 1/f_S$ and $f_S$ = sampling frequency. The inband noise energy $n_o$ is

$$n_o^2 = \int_0^{f_B} E^2(f)df = e_{rms}^2\ (2f_B\tau) = e_{rms}^2\left(\frac{2f_B}{f_S}\right) = \frac{e_{rms}^2}{M} \qquad \Rightarrow \qquad n_o = \frac{e_{rms}}{\sqrt{M}}$$

What does all this mean?

- One way to increase the resolution of an ADC is to make the bandwidth of the signal, $f_B$, less than the clock frequency, $f_S$. In otherwords, give up bandwidth for precision.
- However, it is seen from the above that a doubling of the oversampling ratio $M$, only gives a decrease of the inband noise, $n_o$, of $1/\sqrt{2}$ which corresponds to -3dB decrease or an increase of resolution of 0.5 bits.

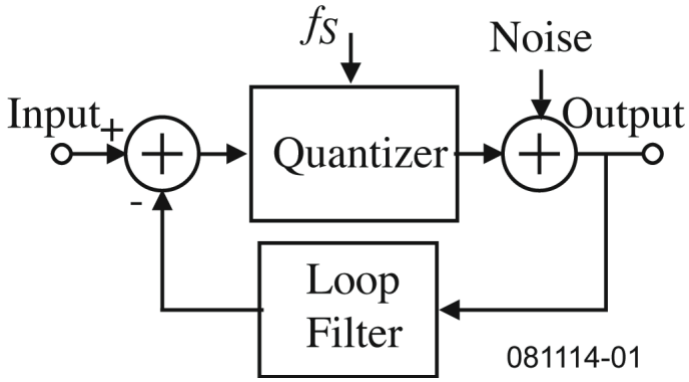
*As a result, increasing the oversampling ratio of a Nyquist analog-digital converter is not a very good method of increasing the resolution.*

## Oversampled Analog-Digital Converters

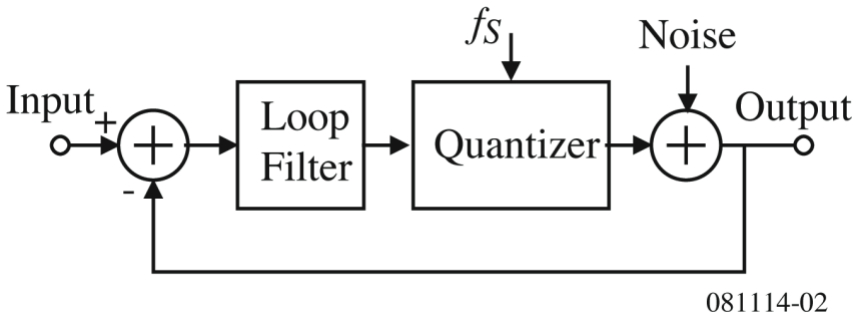
Classification of oversampled ADCs:

1.) Straight-oversampling - The quantization noise is assumed to be equally distributed over the entire frequency range of dc to $0.5f_S$. This type of converter is represented by the Nyquist ADC.

2.) Predictive oversampling - Uses noise shaping plus oversampling to reduce the inband noise to a much greater extent than the straight-oversampling ADC. Both the signal and noise quantization spectrums are shaped.




3.) Noise-shaping oversampling - Similar to the predictive oversampling except that only the noise quantization spectrum is shaped while the signal spectrum is preserved.




The noise-shaping oversampling ADCs are also known as *delta-sigma* ADCs. We will only consider the delta-sigma type oversampling ADCs.

# DELTA-SIGMA MODULATORS

## General block diagram of an oversampled ADC

Components of the Oversampled ADC:

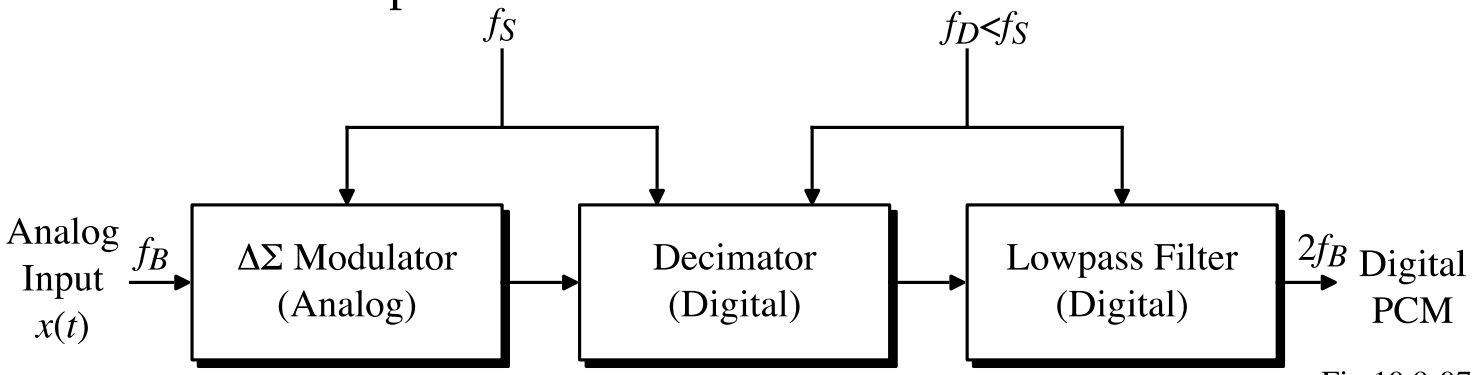



Fig.10.9-07

1.) ΔΣ Modulator - Also called the noise shaper because it can shape the quantization noise and push the majority of the inband noise to higher frequencies. It modulates the analog input signal to a simple digital code, normally a one-bit serial stream using a sampling rate much higher than the Nyquist rate.

2.) Decimator - Also called the down-sampler because it down samples the high frequency modulator output into a low frequency output and does some pre-filtering on the quantization noise.

3.) Digital Lowpass Filter - Used to remove the high frequency quantization noise and to preserve the input signal.

Note: Only the modulator is analog, the rest of the circuitry is digital.

# First-Order, Delta-Sigma Modulator

Block diagram of a first-order, delta-sigma modulator:

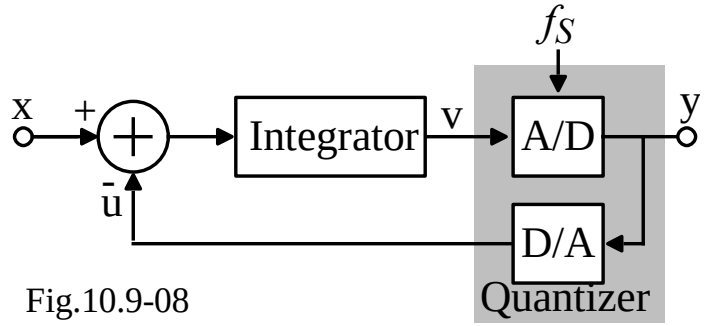



Fig.10.9-08

Components:

- Integrator (continuous or discrete time)
- Coarse quantizer (typically two levels)
  - A/D which is a comparator for two levels
  - D/A which is a switch for two levels

First-order modulator output for a sinusoidal input:

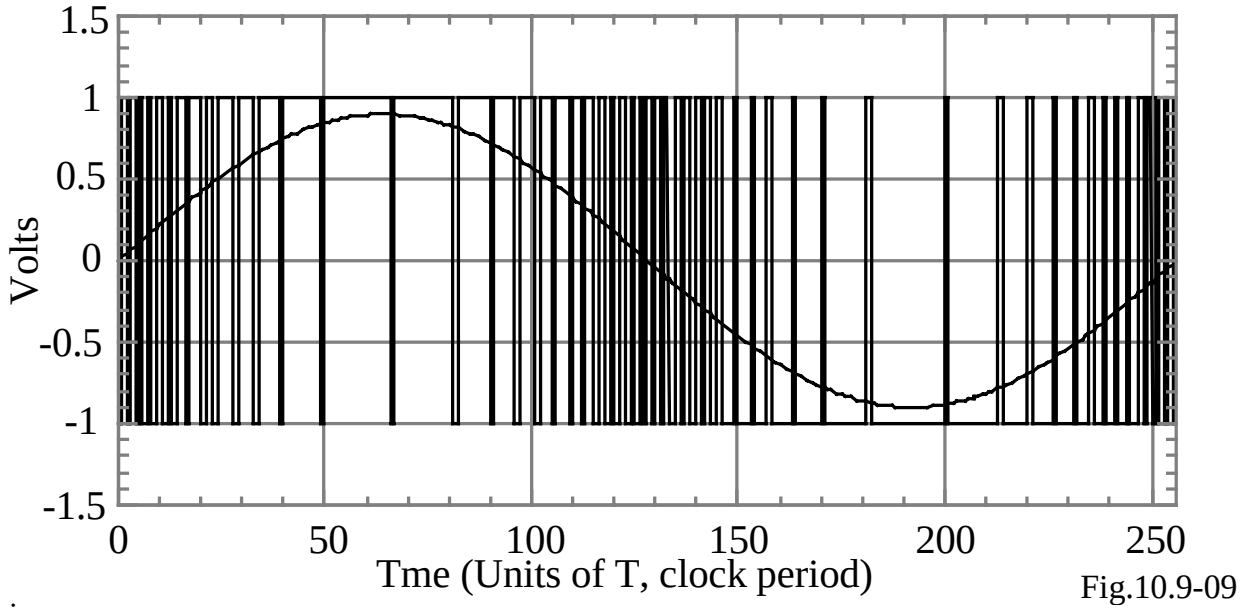



Fig.10.9-09

# Sampled-Data Model of a First-Order ΔΣ Modulator

Writing the following relationships,

$$y[nT_S] = q[nT_S] + v[nT_S]$$

$$v[nT_S] = w[(n\text{-}1)T_S] + v[(n\text{-}1)T_S]$$

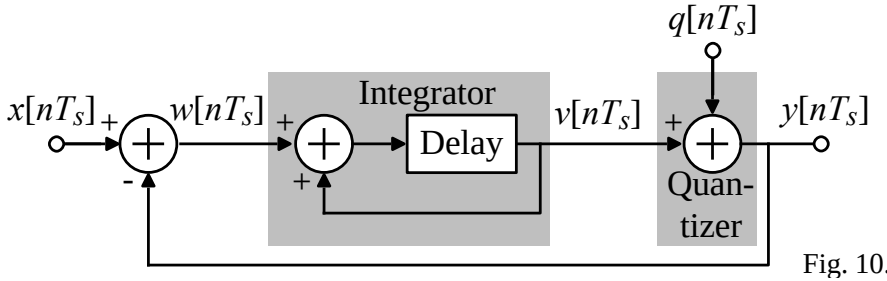



Fig. 10.9-10

$$\therefore \quad y[nT_S] = q[nT_S]+w[(n\text{-}1)T_S]+v[(n\text{-}1)T_S] = q[nT_S]+\{x[(n\text{-}1)T_S]-y[(n\text{-}1)T_S]\}+v[(n\text{-}1)T_S]$$

But the first equation can be written as

$$y[(n\text{-}1)T_S] = q[(n\text{-}1)T_S] + v[(n\text{-}1)T_S] \quad \rightarrow \quad q[(n\text{-}1)T_S] = y[(n\text{-}1)T_S]\} - v[(n\text{-}1)T_S]$$

Substituting this relationship into the above gives,

$$y[nT_S] = x[(n\text{-}1)T_S] + q[nT_S] - q[(n\text{-}1)T_S]$$

Converting this expression to the $z$-domain gives,

$$Y(z) = z^{-1}X(z) + (1\text{-}z^{-1})Q(z)$$

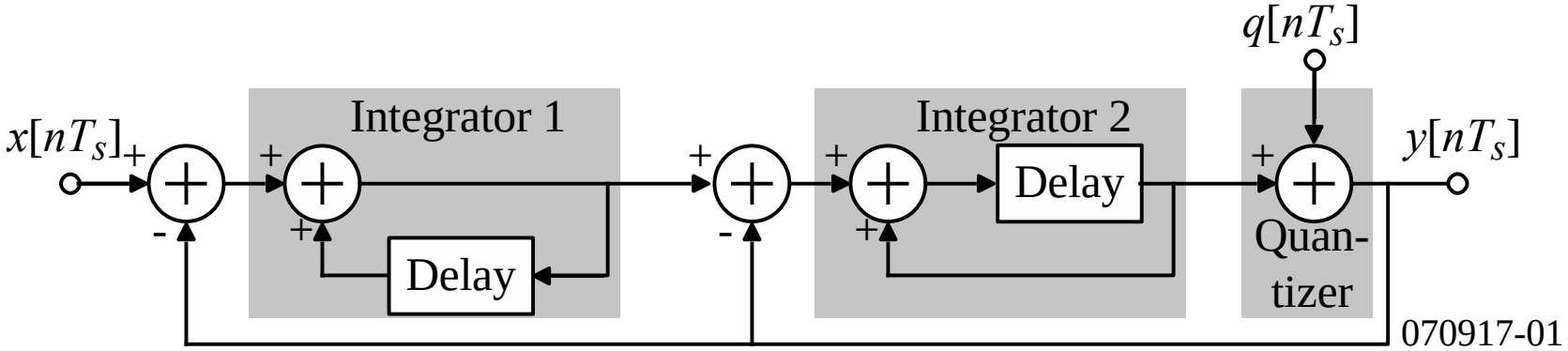
Definitions:

$$\text{Signal Transfer Function} = STF = \frac{Y(z)}{X(x)} = z^{-1}$$

$$\text{Noise Transfer Function} = NTF = \frac{Y(z)}{Q(x)} = 1\text{-}z^{-1}$$

## Higher-Order ΔΣ Modulators

A second-order, ΔΣ modulator:




It can be shown that the *z*-domain output is,

$$Y(z) = z^{-1}X(z) + (1-z^{-1})^2Q(z)$$

The general, *L*-th order ΔΣ modulator has the following form,

$$Y(z) = z^{-K}X(z) + (1-z^{-1})^LQ(z)$$

Note that noise transfer function, *NTF*, has *L*-zeros at the origin resulting in a high-pass transfer function. *K* depends on the architecture where $K \leq L$.

*This high-pass characteristic reduces the noise at low frequencies which is the key to extending the dynamic range within the bandwidth of the converter.*

## Noise Transfer Function

The noise transfer function can be written as,

$$NTF_Q(z) = (1-z^{-1})^L$$

Evaluate $(1-z^{-1})$ by replacing $z$ by $e^{j\omega T_s}$ to get

$$(1-z^{-1}) = \left(1 - e^{-j\omega T_s}\right)\left(\frac{2j}{2j}\right)\frac{e^{j\pi f/f_s}}{e^{j\pi f/f_s}} = \left(\frac{e^{j\pi f/f_s} - e^{-j\pi f/f_s}}{2j}\right) 2j\, e^{-j\pi f/f_s} = \sin(\pi f T_s)\, 2j\, e^{-j\pi f/f_s}$$

$$|1-z^{-1}| = (2\sin\pi f T_s) \quad \rightarrow \quad |NTF_Q(f)| = (2\sin\pi f T_s)^L$$

Magnitude of the noise transfer function,

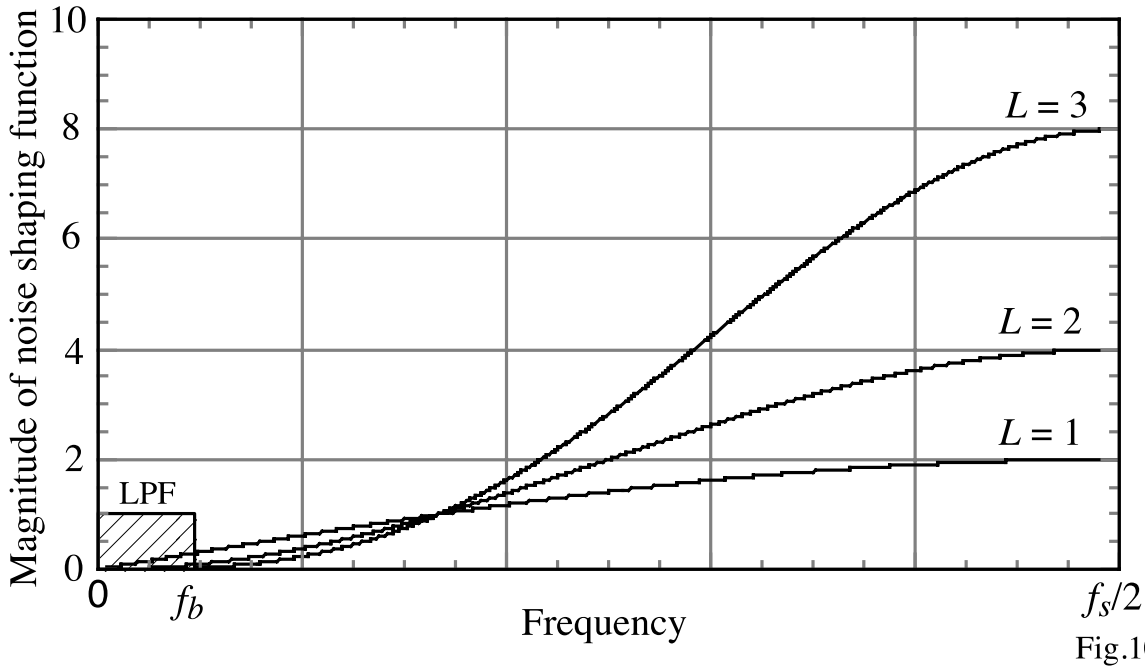



Fig.10.9-12

Note: Single-loop modulators having noise shaping characteristics of the form $(1-z^{-1})^L$ are unstable for $L>2$ unless an $L$-bit quantizer is used.

## In-Band Rms Noise of Single-Loop ΔΣ Modulator

Assuming noise power is white, the power spectral density of the ΔΣ modulator, $S_E(f)$, is

$$S_E(f) = |NTF_Q(f)|^2 \frac{|S_Q(f)|}{f_s}$$

Next, integrate $S_E(f)$ over the signal band to get the inband noise power using $S_Q = \frac{\Delta^2}{12}$

$$\therefore \quad S_B = \frac{1}{f_s}\int_{-f_b}^{f_b} (2\sin\pi f T_s)^{2L} \frac{\Delta^2}{12} df \approx \left(\frac{\pi^{2L}}{2L+1}\right)\left(\frac{1}{M^{2L+1}}\right)\left(\frac{\Delta^2}{12}\right) \quad \text{where } \sin\pi f T_s \approx \pi f T_s \text{ for } M>>1.$$

Therefore, the in-band, rms noise is given as

$$n_0 = \sqrt{S_B} = \left(\frac{\pi^L}{\sqrt{2L+1}}\right)\left(\frac{1}{M^{L+0.5}}\right)\left(\frac{\Delta}{\sqrt{12}}\right) = \left(\frac{\pi^L}{\sqrt{2L+1}}\right)\left(\frac{1}{M^{L+0.5}}\right) e_{rms}$$

Note that the ΔΣ is a much more efficient way of achieving resolution by increasing $M$.

$$n_0 \propto \frac{e_{rms}}{M^{L+0.5}} \Rightarrow \text{ Doubling of } M \text{ leads to a } 2^{L+0.5} \text{ decrease of in-band noise}$$

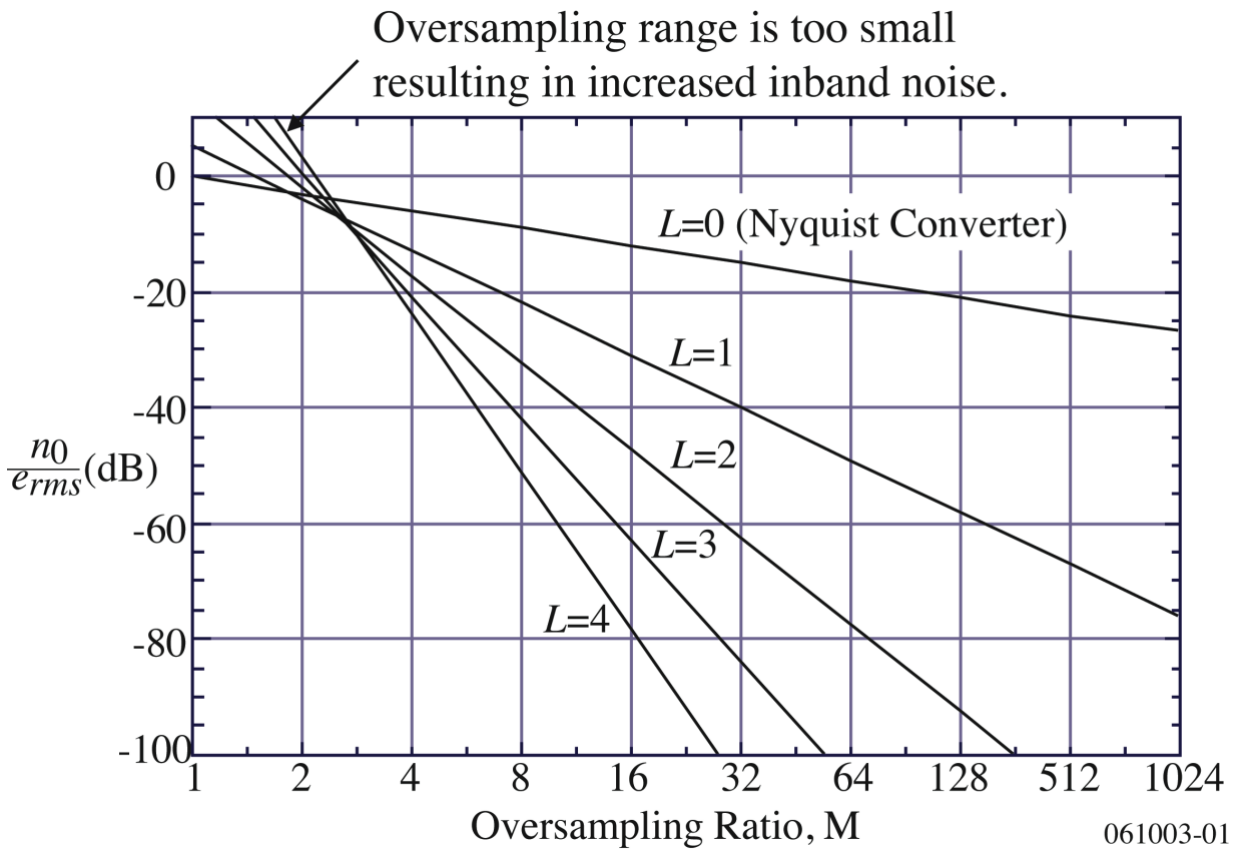
resulting in an extra L+0.5 bits of resolution!

∴ *The increase of the oversampling ratio is an excellent method of increasing the resolution of a ΔΣ oversampling analog-digital converter.*

# Illustration of RMS Noise Versus Oversampling Ratio for Single Loop ΔΣ Modulators

Plotting $n_0/e_{rms}$ gives,

$$\frac{n_0}{e_{rms}} = \left(\frac{\pi^L}{\sqrt{2L+1}}\right)\left(\frac{1}{M^{L+0.5}}\right)$$



## Dynamic Range of ΔΣ Analog-Digital Converters

Oversampled $\Delta\Sigma$ Converter:

The dynamic range, $DR$, for a 1 bit-quantizer with level spacing $\Delta = V_{REF}$, is

$$DR^2 = \frac{\text{Maximum signal power}}{S_B(f)} = \frac{\left(\frac{\Delta}{2\sqrt{2}}\right)^2}{\left(\frac{\pi^{2L}}{2L+1}\right)\left(\frac{1}{M^{2L+1}}\right)\left(\frac{\Delta^2}{12}\right)} = \frac{3}{2}\frac{2L+1}{\pi^{2L}}M^{2L+1}$$

Nyquist Converter:

The dynamic range of a $N$-bit Nyquist rate ADC is (now $\Delta$ becomes $\approx V_{REF}$ for large $N$),

$$DR^2 = \frac{\text{Maximum signal power}}{S_Q} = \frac{(V_{REF}/2\sqrt{2})^2}{\Delta^2/12} = \frac{3}{2}2^{2N} \quad \rightarrow \quad DR = \sqrt{1.5}\,2^N$$

Expressing $DR$ in terms of dB ($DR_{dB}$) and solving for $N$, gives

$$N = \frac{DR_{dB} - 1.7609}{6.0206} \quad \text{or} \quad DR_{dB} = (6.0206N + 1.7609)\ \text{dB}$$

Example: A 16-bit ΔΣ ADC requires about 98dB of dynamic range. For a second-order modulator, $M$ must be 153 or 256 since we must use powers of 2.

Therefore, if the bandwidth is 20kHz, then the clock frequency must be 10.24MHz.

## Multibit Quantizers

A single-bit quantizer:

$$\Delta = V_{REF}$$

Advantage is that the DAC is inherently linear.

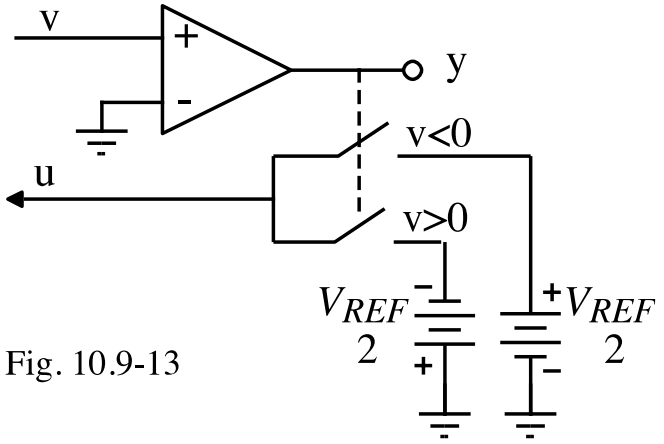



Fig. 10.9-13

Multi-bit quantizer:

Consists of an ADC and DAC of B-bits.

$$\Delta = \frac{V_{REF}}{2^B - 1}$$

Disadvantage is that the DAC is no longer perfectly linear. To get large resolution delta-sigma ADCs requires highly precise DACs.

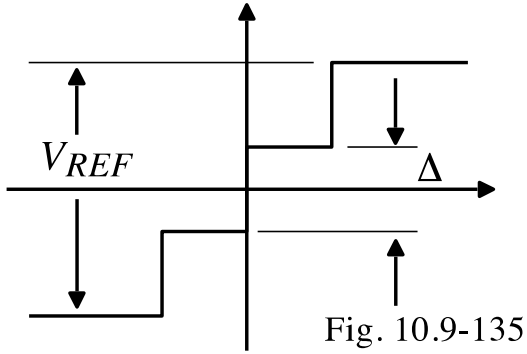



Fig. 10.9-135

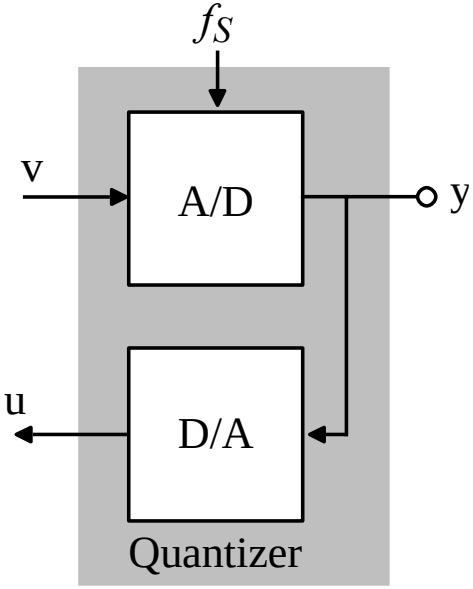



Fig. 10.9-14

Dynamic range of a multibit ΔΣ ADC:

$$DR^2 = \frac{3}{2}\frac{2L+1}{\pi^{2L}} M^{2L+1}\left(2^B - 1\right)^2$$

## Example 39-1 - Tradeoff Between Signal Bandwidth and Accuracy of ΔΣ ADCs

Find the minimum oversampling ratio, $M$, for a 16-bit oversampled ADC which uses (a.) a 1-bit quantizer and third-order loop, (b.) a 2-bit quantizer and third-order loop, and (c.) a 3-bit quantizer and second-order loop. For each case, find the bandwidth of the ADC if the clock frequency is 10MHz.

*Solution*

We see that 16-bit ADC corresponds to a dynamic range of approximately 98dB. (a.) Solving for $M$ gives

$$M = \left(\frac{2}{3}\frac{DR^2}{2L+1}\frac{\pi^{2L}}{(2^{B-1})^2}\right)^{1/(2L+1)}$$

Converting the dynamic range to 79,433 and substituting into the above equation gives a minimum oversampling ratio of $M$ = 48.03 which would correspond to an oversampling rate of 64. Using the definition of $M$ as $f_C/2f_B$ gives $f_B$ as 10MHz/2·64 = 78kHz.

(b.) and (c.) For part (b.) and (c.) we obtain a minimum oversampling rates of $M$ = 32.53 and 96.48, respectively. These values correspond to oversampling rates of 32 and 128, respectively. The bandwidth of the converters is 312kHz for (b.) and 78kHz for (c.).

## Z-Domain Equivalent Circuits

The modulator structures are much easier to analyze and interpret in the z-domain.

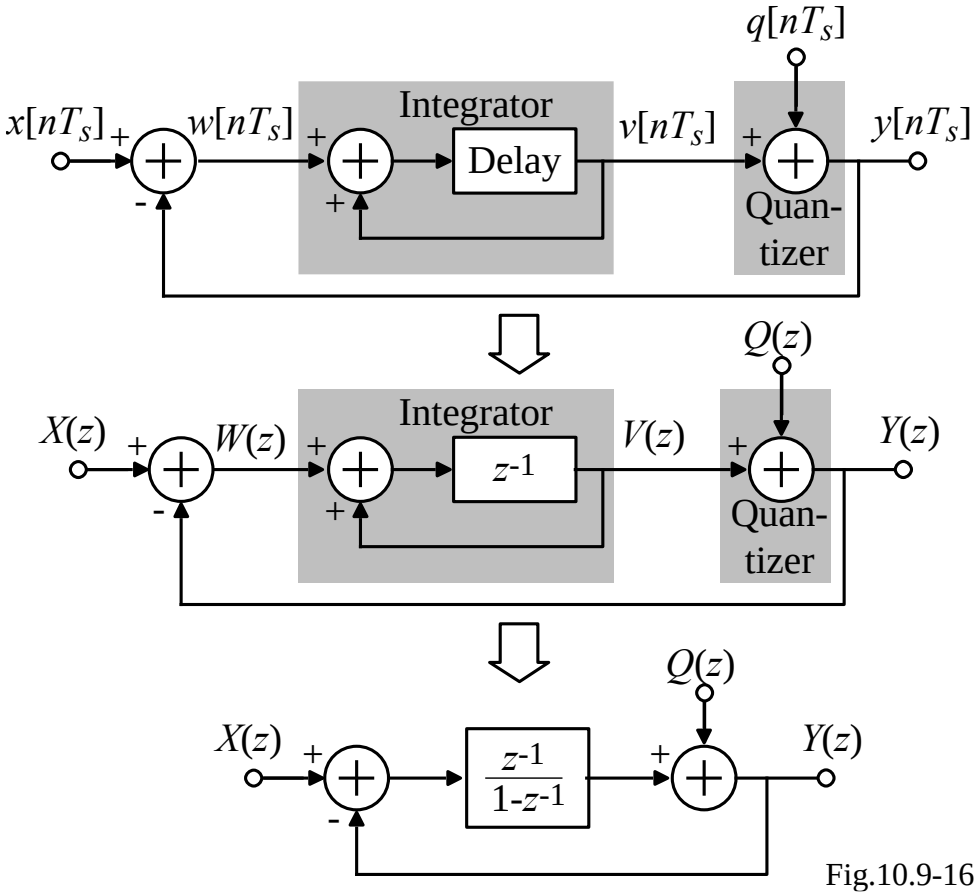



Fig.10.9-16

$$Y(z) = Q(z) + \left(\frac{z^{-1}}{1-z^{-1}}\right)[X(z) - Y(z)] \quad \rightarrow \quad Y(z)\left(\frac{1}{1-z^{-1}}\right) = Q(z) + \left(\frac{z^{-1}}{1-z^{-1}}\right)X(z)$$

$$\therefore \quad Y(z) = (1-z^{-1})Q(z) + z^{-1}X(z) \quad \rightarrow \quad NTF_Q(z) = (1-z^{-1}) \quad \text{for } L = 1$$

## Cascaded, Second-Order ΔΣ Modulator

Since the single-loop architecture with order higher than 2 are unstable, it is necessary to find alternative architectures that allow stable higher order modulators.

A cascaded, second-order structure:

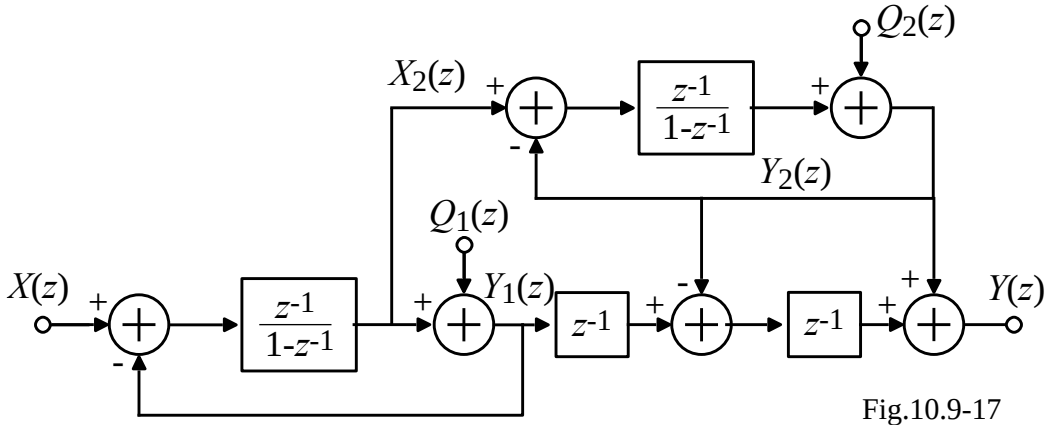



Fig.10.9-17

$$Y_1(z) = (1-z^{-1})Q_1(z) + z^{-1}X(z)$$

$$X_2(z) = \left(\frac{z^{-1}}{1-z^{-1}}\right)(X(z) - Y_1(z)$$

$$= \left(\frac{z^{-1}}{1-z^{-1}}\right)X(z) - \left(\frac{z^{-1}}{1-z^{-1}}\right)[(1-z^{-1})Q_1(z) + z^{-1}X(z)]$$

$$Y_2(z) = (1-z^{-1})Q_2(z) + z^{-1}X_2(z) = (1-z^{-1})Q_2(z) + \left(\frac{z^{-2}}{1-z^{-1}}\right)X(z) - z^{-2}Q_1(z) - \left(\frac{z^{-2}}{1-z^{-1}}\right)X(z)$$

$$= (1-z^{-1})Q_2(z) - z^{-2}Q_1(z)$$

$$Y(z) = Y_2(z) - z^{-1}Y_2(z) + z^{-2}Y_1(z) = (1-z^{-1})Y_2(z) + z^{-2}Y_1(z)$$

$$= (1-z^{-1})^2Q_2(z) - (1-z^{-1})z^{-2}Q_1(z) + (1-z^{-1})z^{-2}Q_1(z) + z^{-3}X(z) = (1-z^{-1})^2Q_2(z) + z^{-3}X(z)$$

$$\therefore \quad Y(z) = (1-z^{-1})^2Q_2(z) + z^{-3}X(z)$$

# Third-Order, MASH ΔΣ Modulator

It can be shown that

$$Y(z) = X(z) + (1-z^{-1})^3 Q_3(z)$$

This results in a 3rd-order noise shaping and no delay between the input and output.

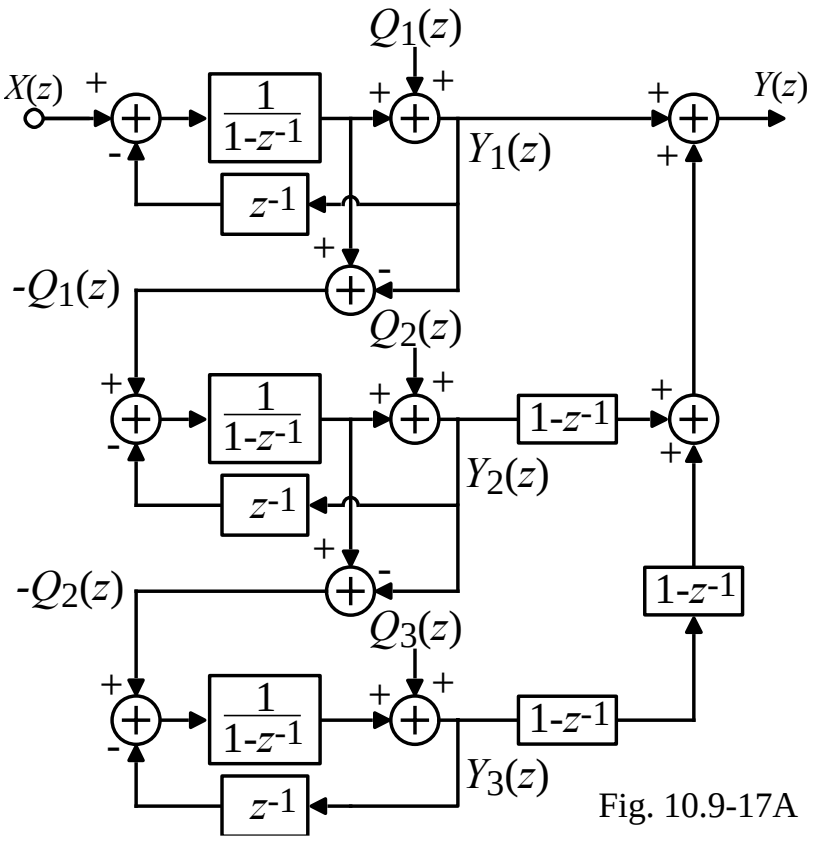
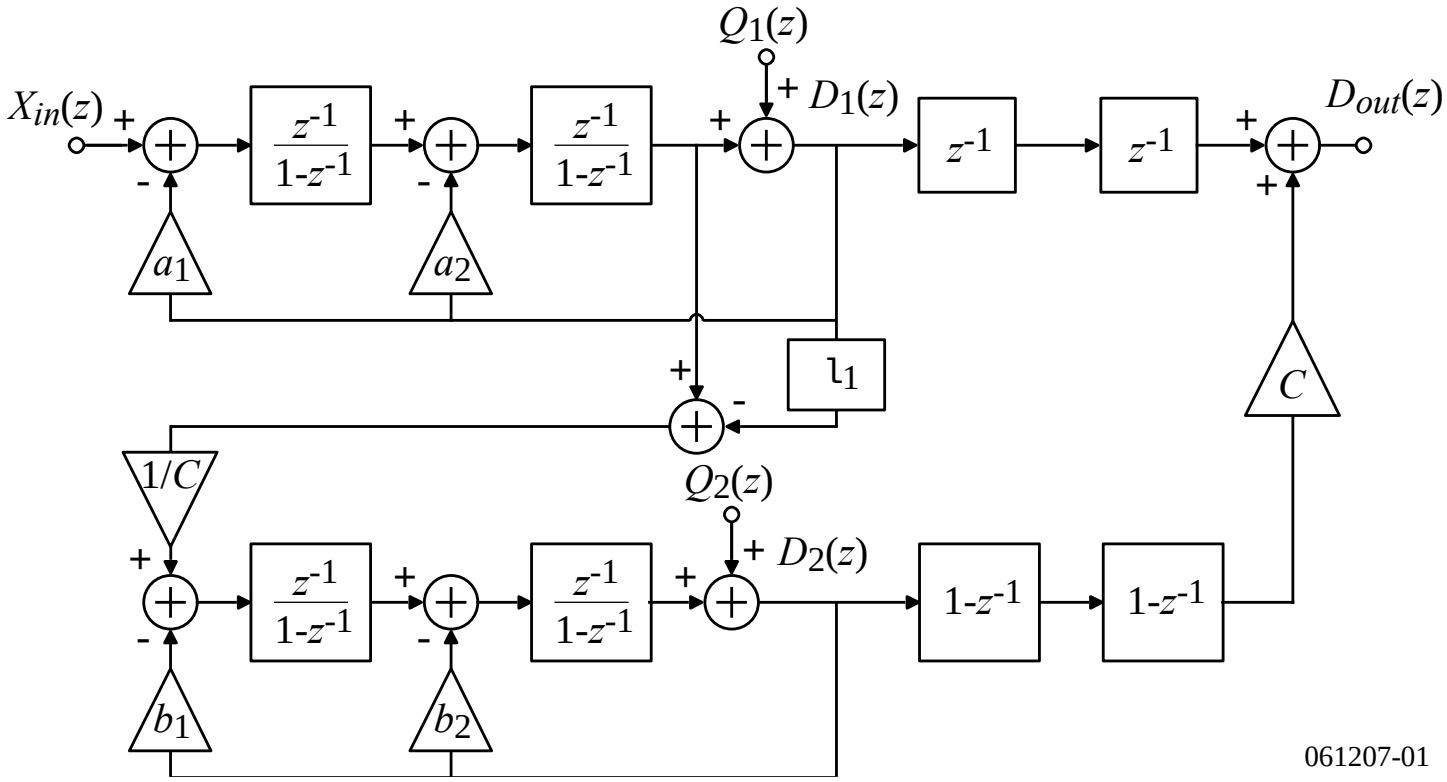



Fig. 10.9-17A

Comments:

- The above structures that eliminate the noise of all quantizers except the last are called *MASH* or multistage architectures.
- Digital error cancellation logic is used to remove the quantization noise of all stages, except that of the last one.

# A Fourth-Order, MASH-type Modulator using Scaling of Error Signals†




The signal is divided by $1/C$ as it passes from the first 2nd-order modulator to the second 2nd-order modulator. The digital output of the second 2nd-order modulator is then multiplied by the inverse factor of $C$.

The various transfer functions are ($a_1$=1, $a_2$=2, $b_1$=1, $b_2$=2, $\lambda_1$=2 and $C$ = 4) :

$$D_1(z) = X_{in}(z) + (1-z^{-1})^2\, Q_1(z) \quad \text{and} \quad D_2(z) = (1/C)(-Q_1(z)) + (1-z^{-1})^2\, Q_2(z)$$

Giving $$D_{out}(z) = X_{in}(z) + (1-z^{-1})^4\, Q_2(z)$$

† U.S. Patent 5,061,928, Oct. 29, 1991.

# Distributed Feedback ΔΣ Modulator - Fourth-Order

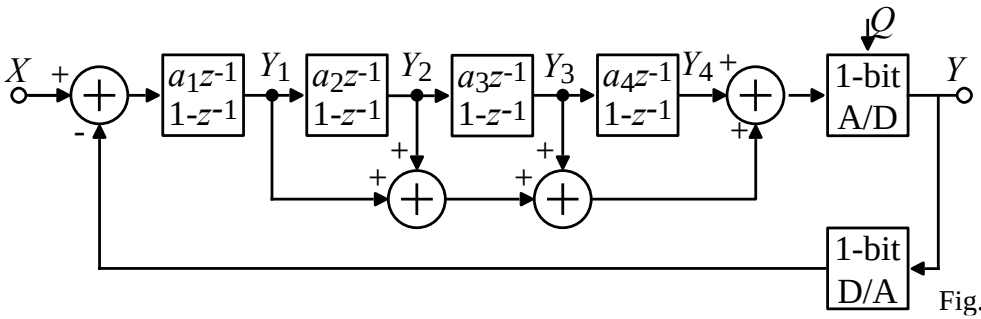
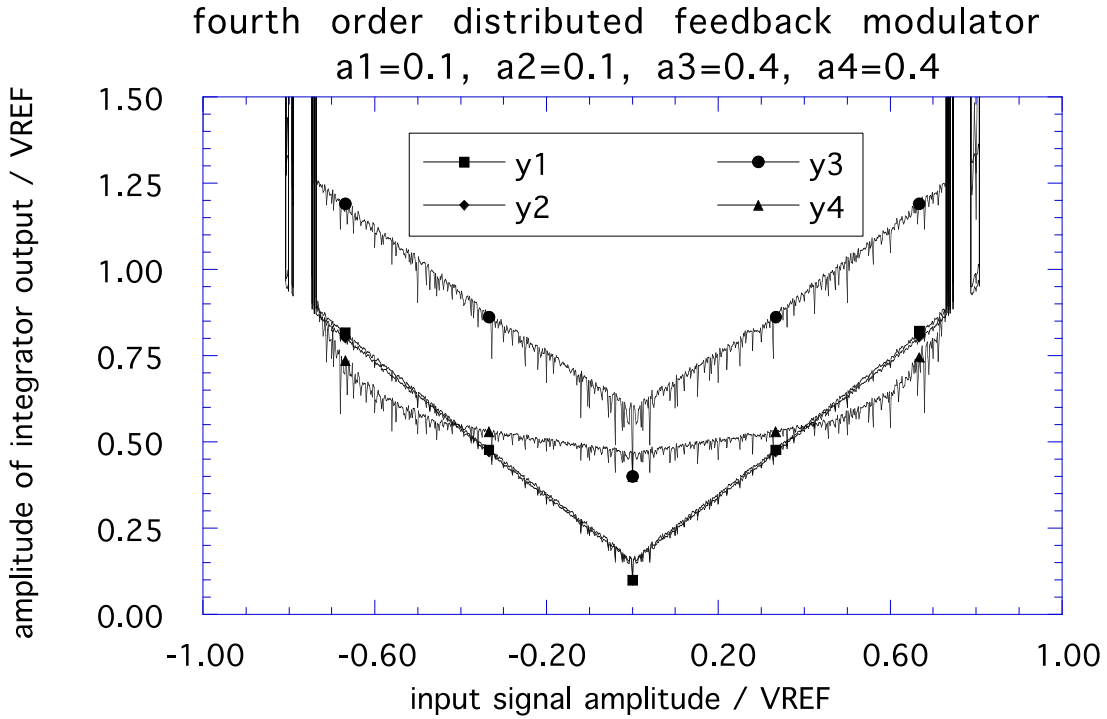



Fig.10.9-20

Amplitude of integrator outputs:



# Distributed Feedback ΔΣ Modulator - Fourth-Order – Continued

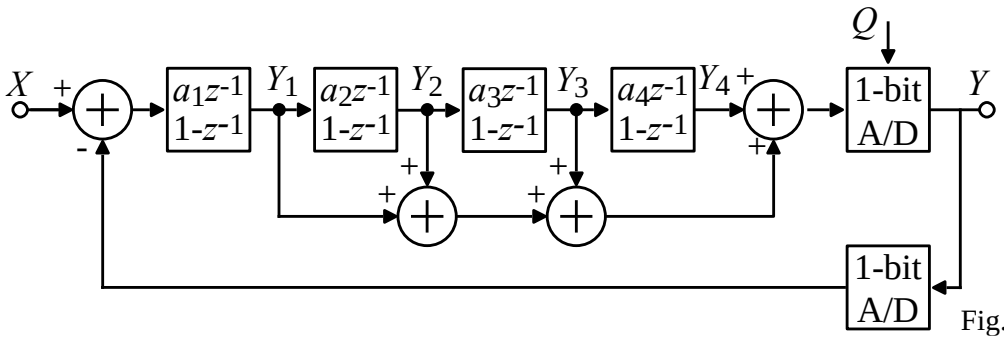
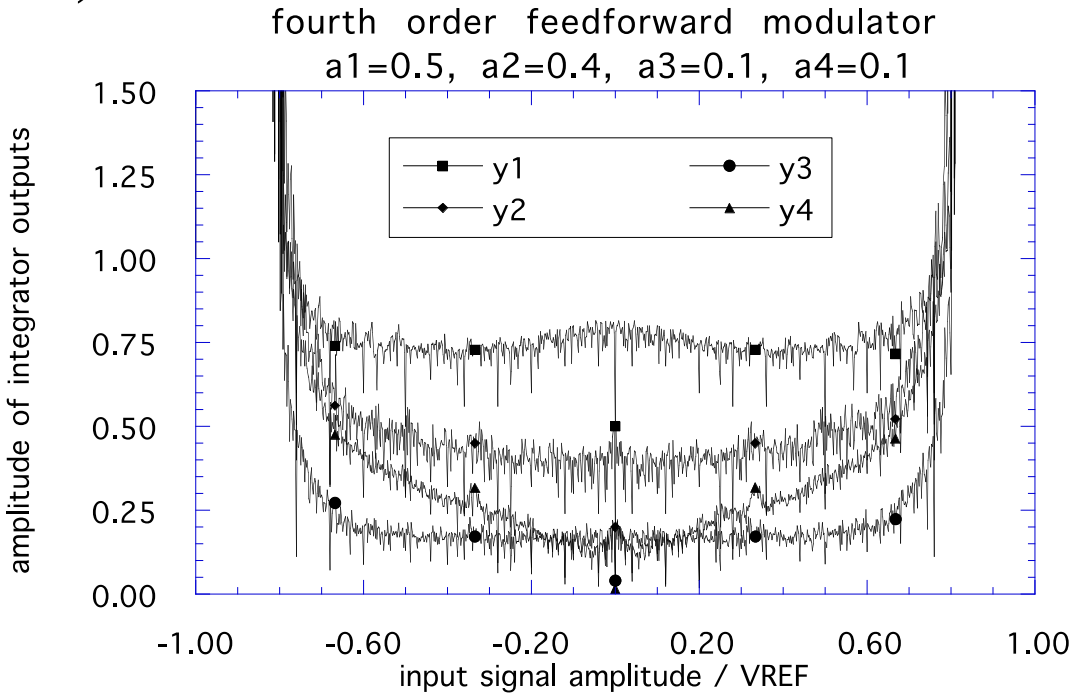



Fig.10.9-20

Amplitude of integrator outputs (Integrator constants have been optimized to minimize the integrator outputs):



# Cascaded of a Second-Order Modulator with a First-Order Modulator

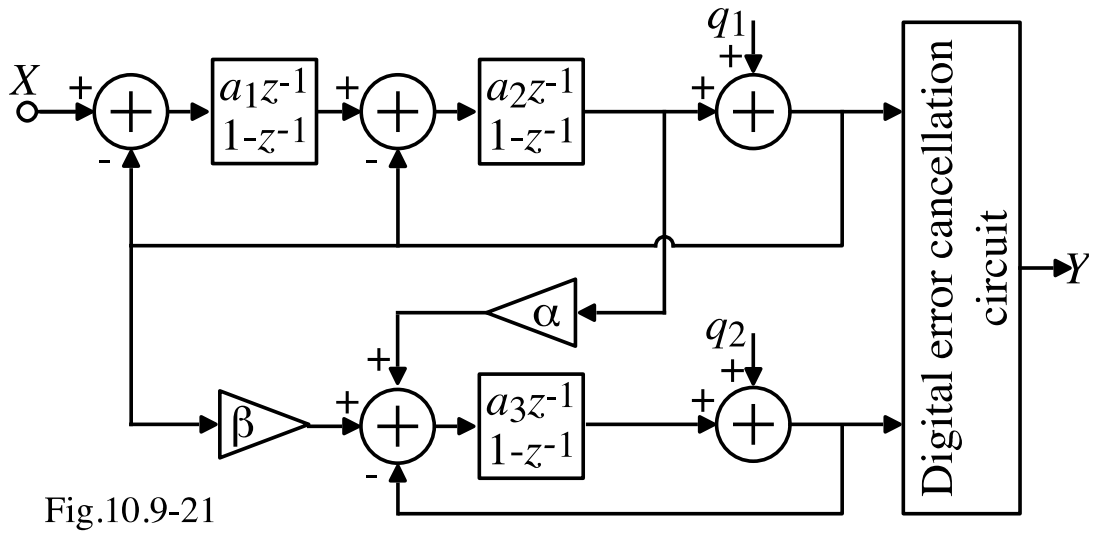



Fig.10.9-21

Comments:

- The stability is guaranteed for cascaded structures
- The maximum input range is almost equal to the reference voltage level for the cascaded structures
- All structures are sensitive to the circuit imperfection of the first stages
- The output of cascaded structures is multi-bit requiring a more complex digital decimator

## Integrator Circuits for ΔΣ Modulators

Fundamental block of the ΔΣ modulator:

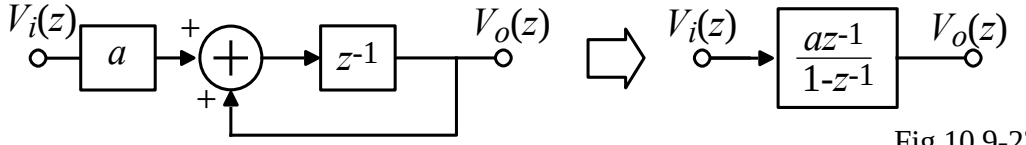



Fig.10.9-22

Fully-Differential, Switched Capacitor Implementation:

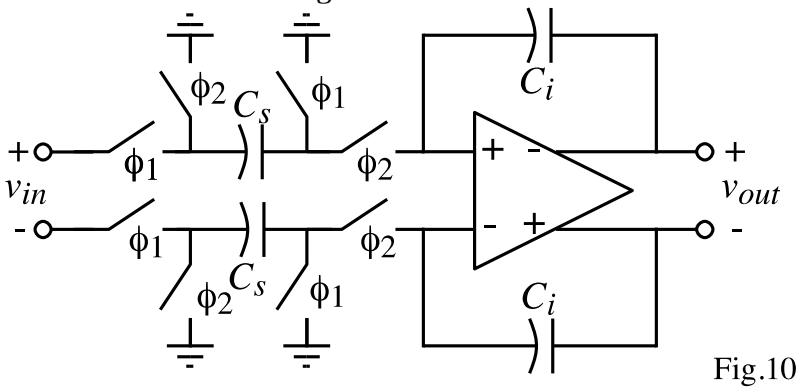



Fig.10.9-23

It can be shown that (Chapter 9 of the second edition or Appendix E of the third edition) that,

$$\frac{V_{out}(z)}{V_{in}(z)} = \left(\frac{C_s}{C_i}\right)\left(\frac{z^{-1}}{1-z^{-1}}\right)$$

becomes,

$$\frac{V_{out}^{o}(e^{j\omega T})}{V_{in}^{o}(e^{j\omega T})} = \left(\frac{C_1}{C_2}\right)\frac{e^{-j\omega T/2}}{j2\sin(\omega T/2)}\left(\frac{\omega T}{\omega T}\right) = \left(\frac{C_1}{j\omega T C_2}\right)\left(\frac{\omega T/2}{\sin(\omega T/2)}\right)\left(e^{-j\omega T/2}\right)$$

or

$$\frac{V_{out}^{o}(e^{j\omega T})}{V_{in}^{o}(e^{j\omega T})} = \text{(Ideal)x(Magnitude error)x(Phase error) where } \omega_I = \frac{C_1}{TC_2} \Rightarrow \text{Ideal} = \frac{\omega_I}{j\omega}$$

## Power Dissipation versus Supply Voltage and Oversampling Ratio

The following is based on the above switched-capacitor integrator:

1.) Dynamic range:

The noise in the band $[-f_S,f_S]$ is $kT/C$ while the noise in the band $[-f_S/2M,f_S/2M]$ is $kT/MC$. We must multiply this noise by 4; x2 for the sampling and integrating phases and x2 for differential operation. The dynamic range is then $V_{DD}$ divided by this noise,

$$\therefore \qquad DR = \frac{V_{DD}^2/2}{4kT/MC_S} = \frac{V_{DD}^2 MC_S}{8kT}$$

2.) Lower bound on the sampling capacitor, $C_S$, can be written as: $C_S = \dfrac{8kT\cdot DR}{V_{DD}^2 M}$

3.) Static power dissipation of the integrator: $P_{int} = I_b V_{DD}$

4.) Settling time for a step input of $V_{o,max}$:

$$I_b = C_i\frac{V_{o,max}}{T_{settle}} = \left(\frac{C_i}{T_{settle}}\right)\left(\frac{C_S}{C_i}V_{DD}\right) = \frac{C_S V_{DD}}{T_{settle}} = C_S V_{DD}(2f_S) = 2Mf_N C_S V_{DD}$$

$$\therefore \qquad P_{int} = 2Mf_N C_S V_{DD}^2 = 16kT\cdot DR\cdot f_N$$

Because of additional feedback to the 1st integrator, power is increased by a factor of 2.

$$\therefore \qquad P_{1st\text{-}int} = 32kT\cdot DR\cdot f_N$$

## SUMMARY

- Oversampled ADCs allow signal bandwidth to be efficiently traded for resolution
- Noise shaping oversampled ADCs preserve the signal spectrum and shape the noise quantization spectrum
- The modulator shapes the noise quantization spectrum with a high pass filter
- The quantizer can be single or multiple bit
  - Single bit quantizers do not require linear DACs because a 1 bit DAC cannot be nonlinear
  - Multiple bit quantizers require ultra linear DACs
- Modulators consist of combined integrators with the goal of high-pass shaping of the noise spectrum and cancellation of all quantizer noise but the last quantizer