LECTURE 38 – HIGH SPEED NYQUIST ADCS

LECTURE ORGANIZATION

Outline

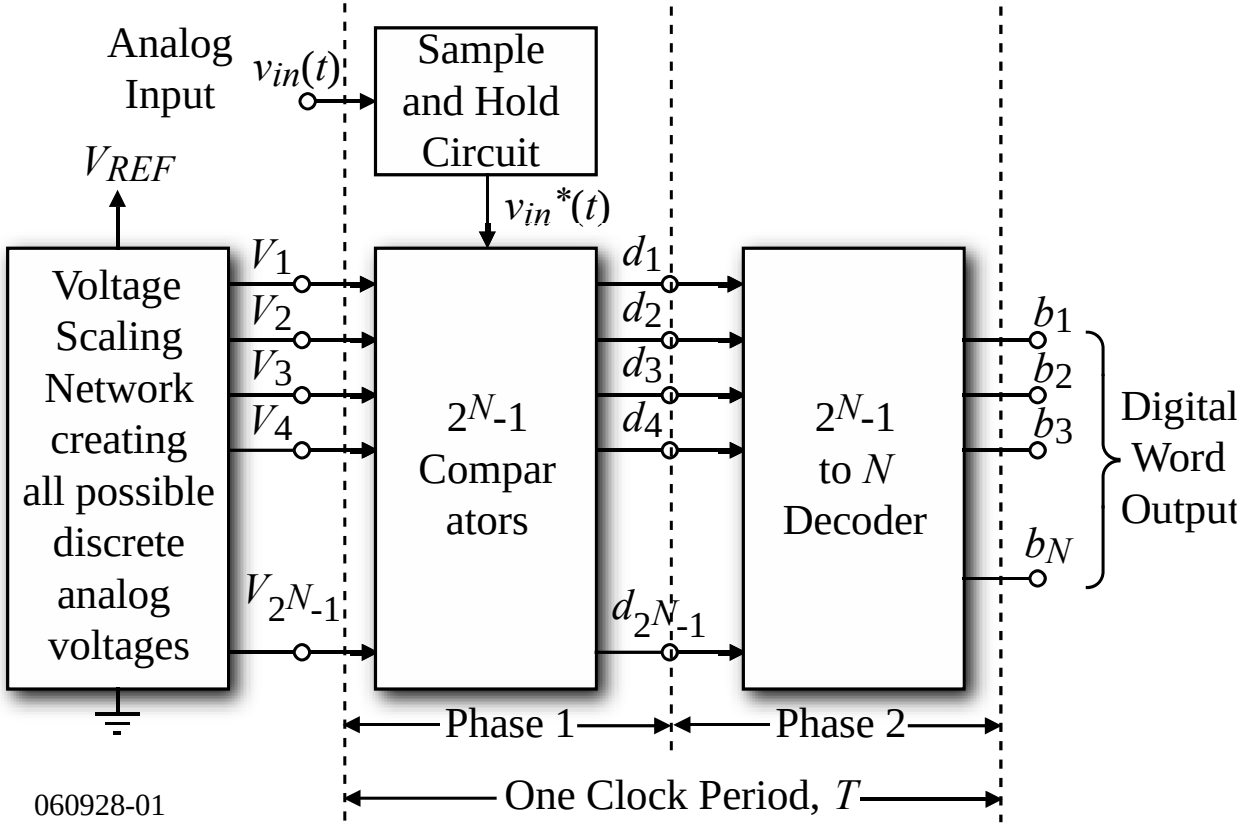
- Parallel/flash ADCs
- Interpolating and averaging
- Folding
- High-speed, high-resolution ADCs
- Time-interleaved ADCs

***CMOS Analog Circuit Design*, 3rd Edition Reference**

Pages 573-588

PARALLEL/FLASH ADCs

Parallel/Flash ADC Architecture



- The notation, $v_{in}^*(t)$, means the signal is sampled and held.
- The sample and hold function can be incorporated into the comparators
- The digital words designated as d_i form a thermometer code

A 3-bit, parallel ADC

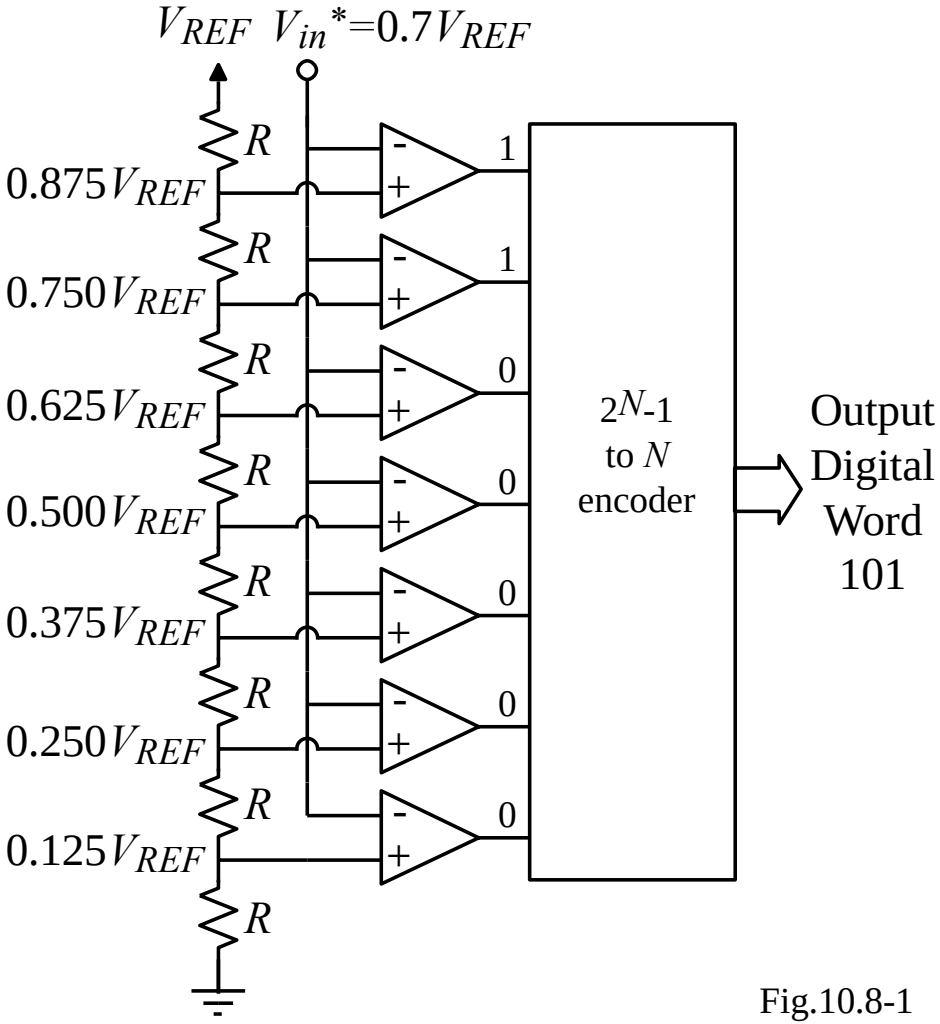


Fig.10.8-1

General Comments:

- Fast, in the first phase of the clock the analog input is sampled and applied to the comparators. In the second phase, the digital encoding network determines the correct output digital word.
- Number of comparators required is 2^N-1 which can become large if N is large
- The offset of the comparators must be less than $\pm V_{REF}/2^{N+1}$
- Errors occur as "bubbles" in the thermometer code and can be corrected with additional circuitry
- Typical sampling frequencies can be as high as 1000MHz for 6-bits in sub-micron CMOS technology.

Example 38-1 - Comparator Bandwidth Limitations on the Flash ADC

The comparators of a 6-bit, flash ADC have a dominant pole at 10^4 radians/sec, a dc gain of 10^4 a slew rate of 10V/μs, and a binary output voltage of 1V and 0V. Assume that the conversion time is the time required for the comparator to go from its initial state to halfway to its final state. What is the maximum conversion rate of this ADC if V_{REF} = 1V? Assume the resistor ladder is ideal.

Solution:

The output of the *i*-th comparator can be found by taking the inverse Laplace transform of,

$$\mathcal{L}^{-1}\left[\text{Vout}(s) = \left(\frac{A_o}{(s/10^4)+1}\right)\cdot\left(\frac{V_{in}^{*}-V_{Ri}}{s}\right)\right] \rightarrow v_{out}(t) = A_o(1 - e^{-10^4 t})(V_{in}^{*} - V_{Ri}).$$

The worst case occurs when

$$V_{in}^{*}-V_{Ri} = 0.5V_{LSB} = V_{REF}/2^7 = 1/128$$

$$\therefore \quad 0.5\text{V} = 10^4(1 - e^{-10^4 T})(1/128) \rightarrow 64\text{x}10^{-4} = 1 - e^{-10^4 T}$$

$$\text{or,} \quad e^{-10^4 T} = 1 - 64\text{x}10^{-4} = 0.9936 \rightarrow T = 10^{-4}\ln(1.0064) = 0.6421\mu\text{s}$$

$$\therefore \quad \text{Maximum conversion rate} = \frac{1}{0.6421\mu\text{s}} = 1.557\text{x}10^6 \text{ samples/second}$$

Checking the slew rate shows that it does not influence the maximum conversion rate.

$$\text{SR} = 10\text{V}/\mu\text{s} \rightarrow \frac{\Delta V}{\Delta T} = 10\text{V}/\mu\text{s} \rightarrow \Delta V = 10\text{V}/\mu\text{s}(0.6421\mu\text{s}) = 6.421\text{V} > 1\text{V}$$

Signal Delay in High Speed Converters

Assume that clocked comparators are used in a 500MHz sampling frequency ADC of 8-bits. If the input frequency is 250MHz with a peak-to-peak value of V_{REF}, the clock accuracy must be

$$\Delta t \le \frac{\Delta V}{\omega V_p} = \frac{V_{REF}/2^{N+1}}{2\pi f(0.5V_{REF})} = \frac{1}{2^9 \cdot \pi \cdot f} \approx 2.5\text{ps}$$

Since electrical signals travel at approximately 50μm/ps for metal on an IC, each metal path from the clock to each comparator must be equal to within 125μm to avoid LSB errors due to clock skew. Therefore, must use careful layout to avoid ADC inaccuracies at high frequencies.

An equal-delay clock distribution system for a 4-bit parallel ADC:

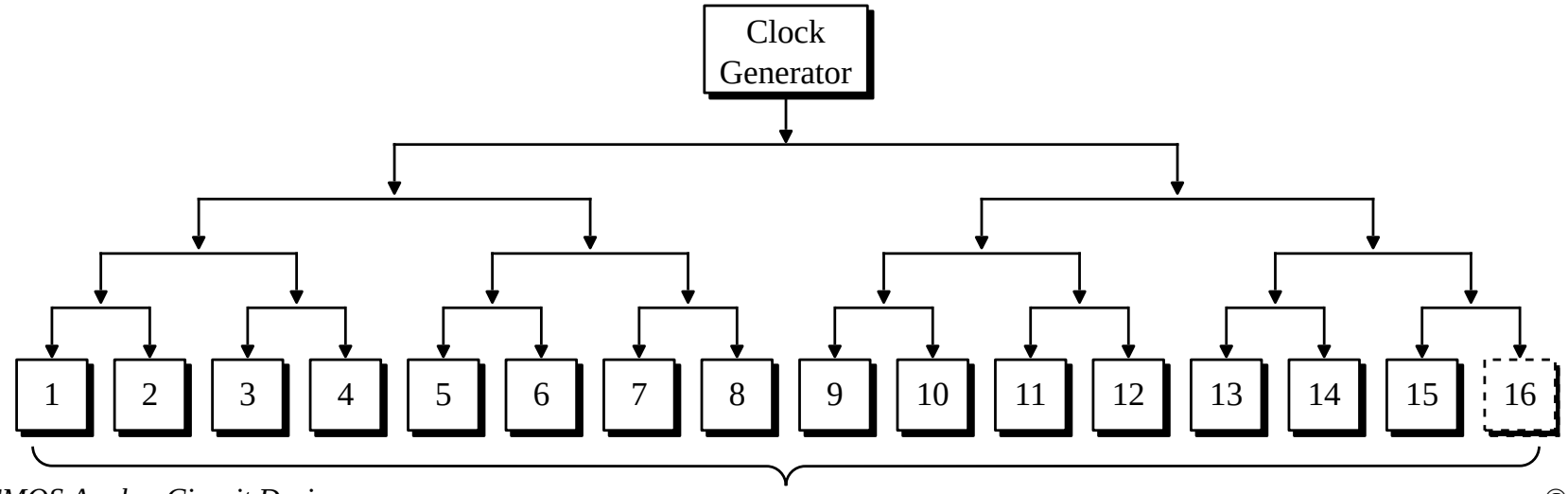


Fig.10.8-2B

Other Errors of the Parallel ADC

- Resistor string error - if current is drawn from the taps to the resistor string this will create a "bowing" effect on the voltage. This can be corrected by applying the correct voltage to various points of the resistor string.
- Input common mode range of the comparators - the comparators at the top of the string must operate with the same performance as the comparators at the bottom of the string.
- Kickback or flashback - influence of rapid transition changes occurring at the input of a comparator. Can be solved by using a preamplifier or buffer in front of the comparator.
- Metastability - uncertainty of the comparator output causing the transition of the thermometer code to be undetermined.

INTERPOLATING AND AVERAGING

Illustration of a 3-bit interpolating ADC using a factor of 4 interpolation

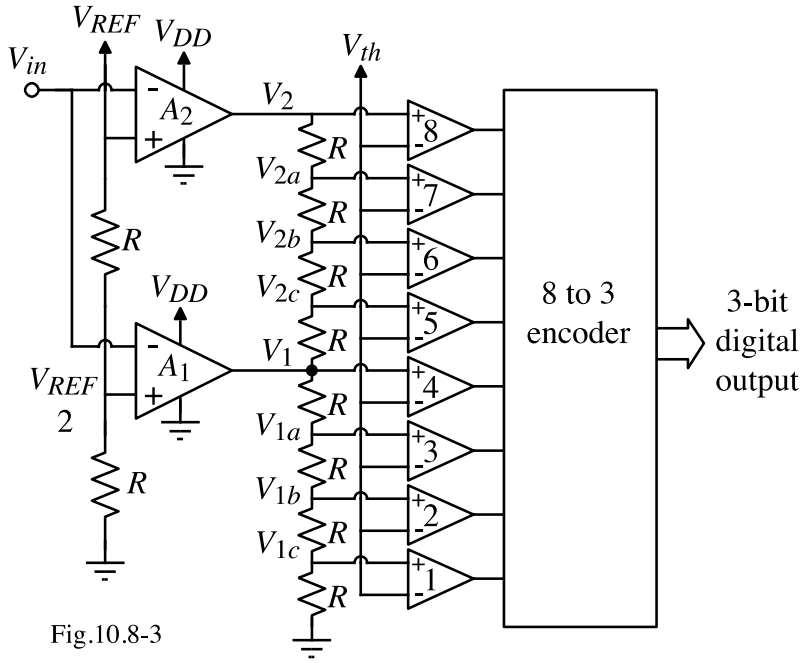


Fig.10.8-3

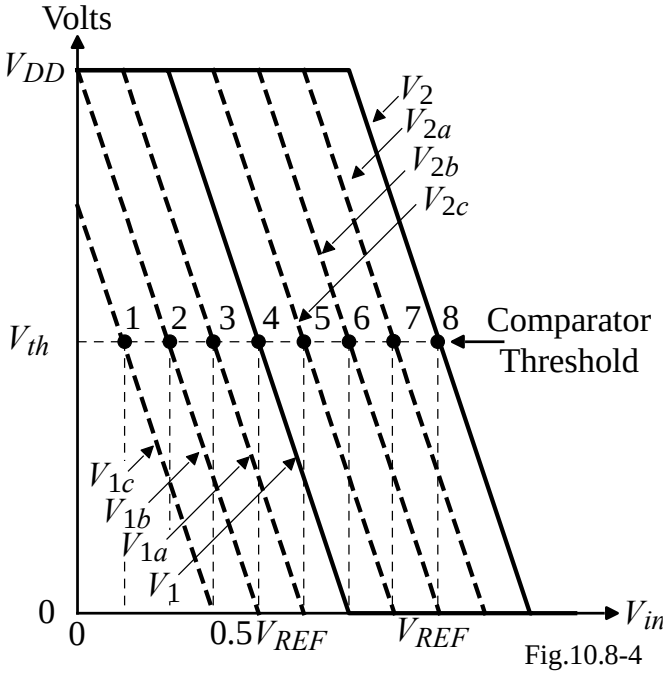


Fig.10.8-4

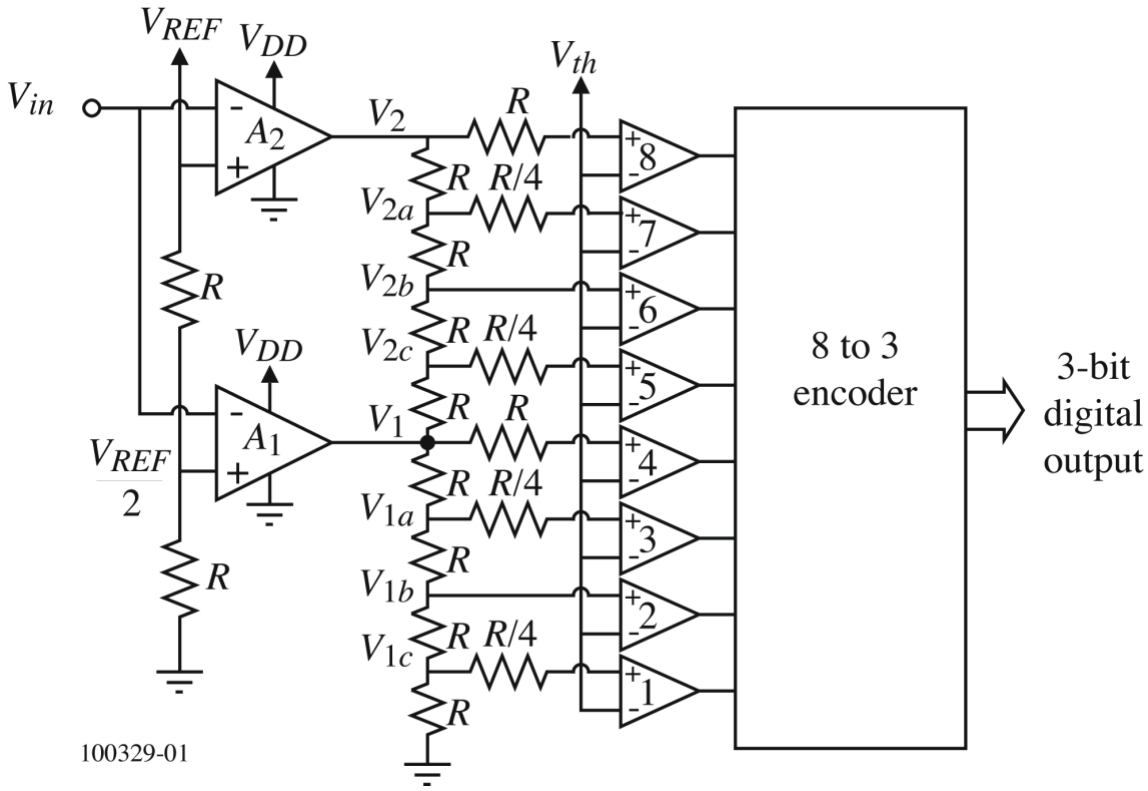
Comments:

- Capacitive loading at the input is reduced from 8 comparators to two amplifiers.
- The comparators no longer need a large *ICMR*
- V_1 and V_2, are interpolated through the resistor string and applied to the comparators.
- Because of the amplification of the input amplifiers and a single threshold, the comparators can be simple and are often replaced by a latch.
- If the dots in Fig. 10.8-4 are not equally spaced, *INL* and *DNL* will result.

A 3-Bit Interpolating ADC with Equalized Comparator Delays

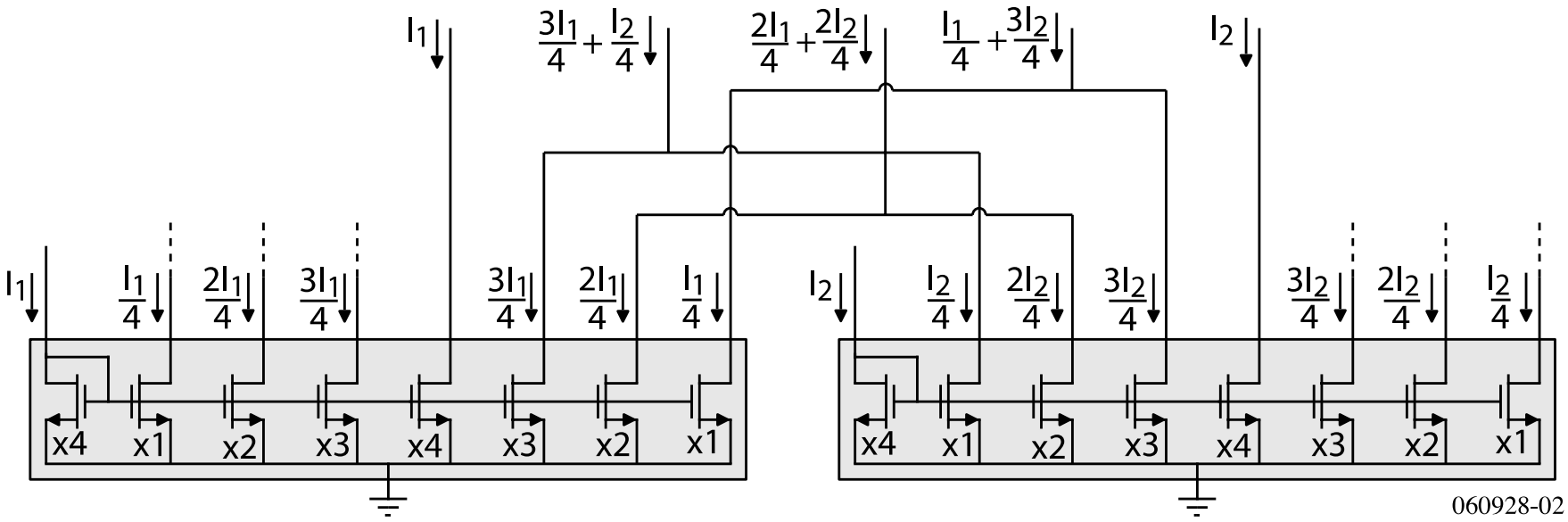
One of the problems in voltage (passive) interpolation is that the delay from the amplifier output to each comparator can be different due to different source resistance.

Solution:



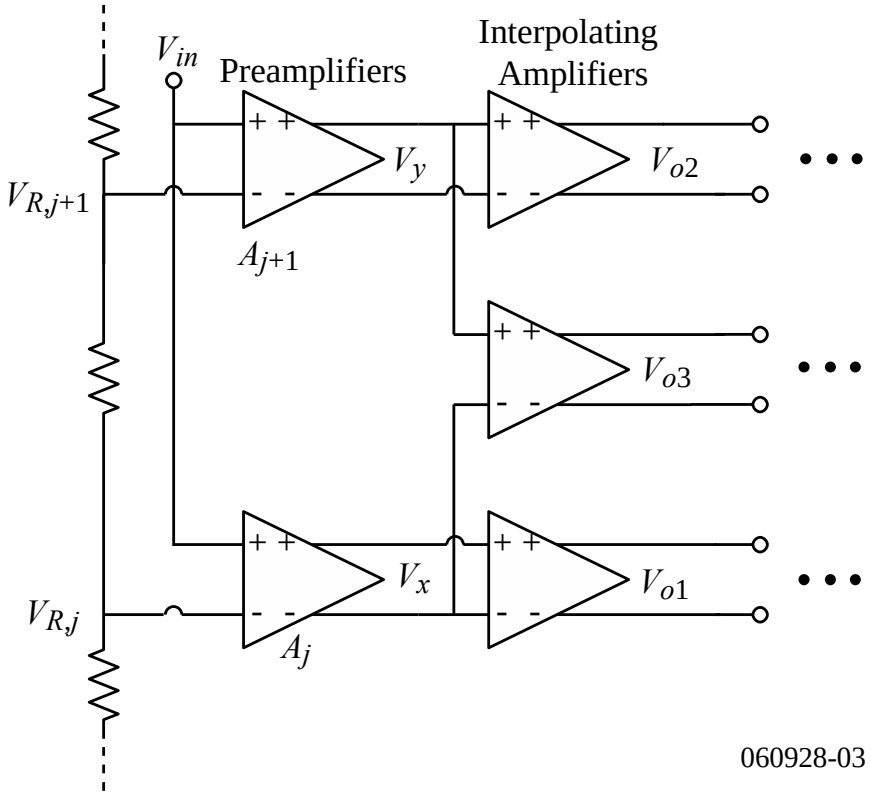
Active Interpolation

Example of a 3 level current interpolation:



This type of interpolation works well with current processing, i.e., current comparators.

Interpolation using Amplifiers

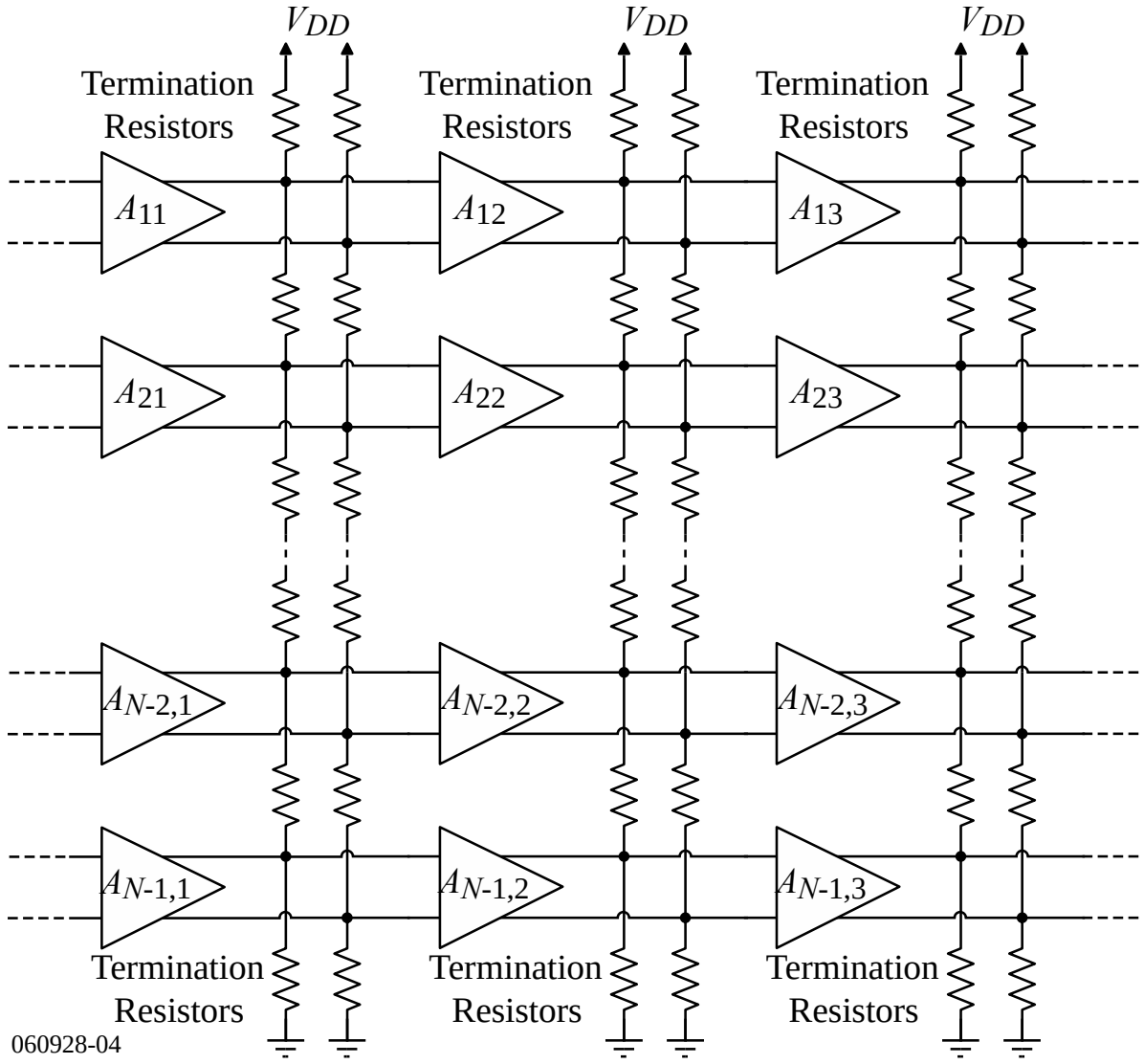


$V_{o3} = K(V_y - V_x)$ which is between V_y and V_x.

Averaging†

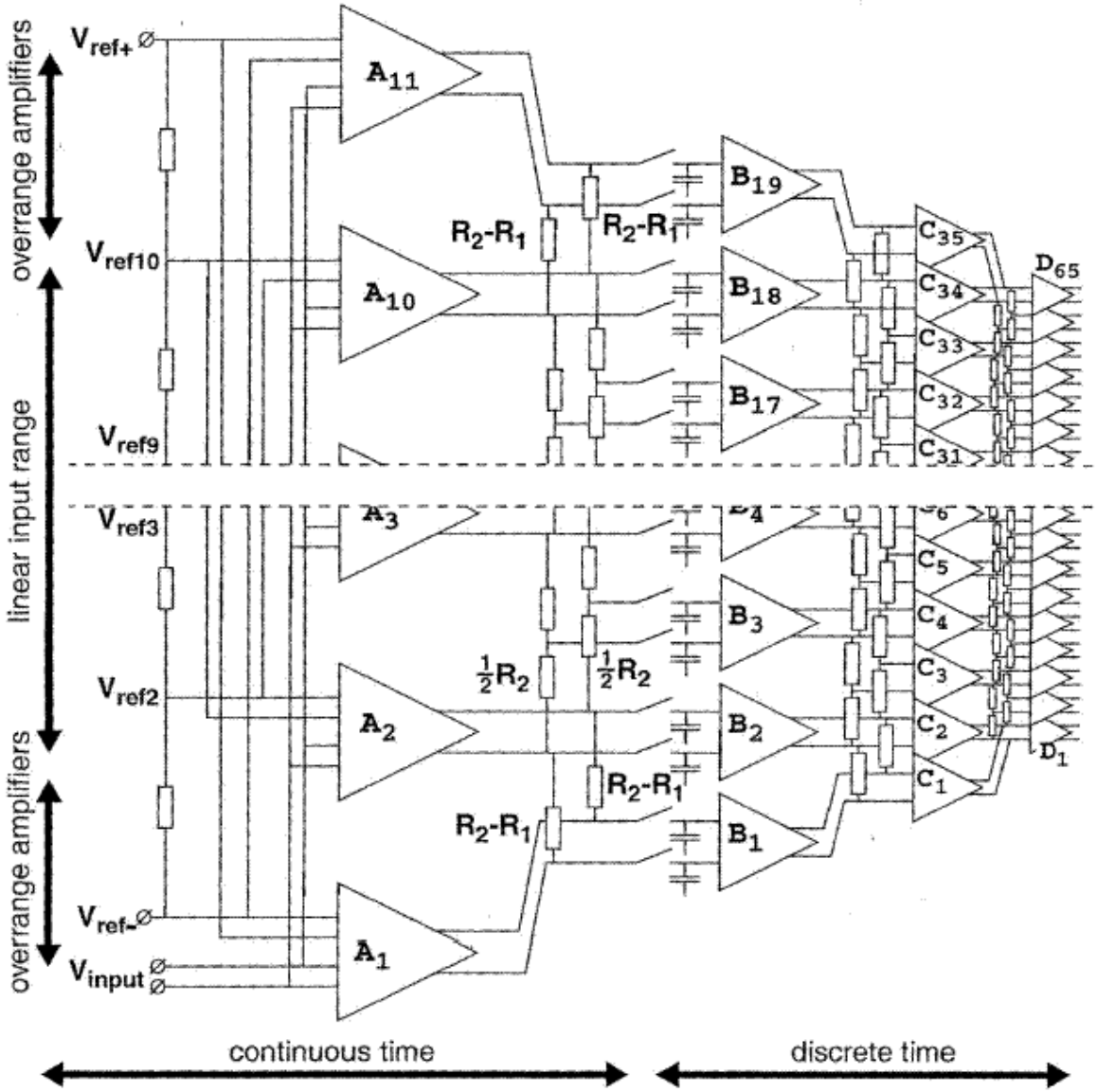
In many cases, the comparators consist of a number of pre-amplifiers followed by a latch. Averaging is the result of interconnecting the outputs of each stage of amplifiers so that the errors in one amplifier chain are balanced out by adjacent amplifier chains.

Result: The offsets are reduced allowing the transistors to be made smaller and therefore reducing the parasitics increasing the speed of the ADC.



† P.C.S. Scholtens and M. Vertregt, "A 6-b 1.6-Gsample/s Flash ADC in 0.18 µm CMOS Using Averaging Termination, *IEEE J. of Solid-State Circuits*, vol. 37, no. 12, Dec. 2002, pp. 1599-1609.

Analog Front End of an ADC using Averaging

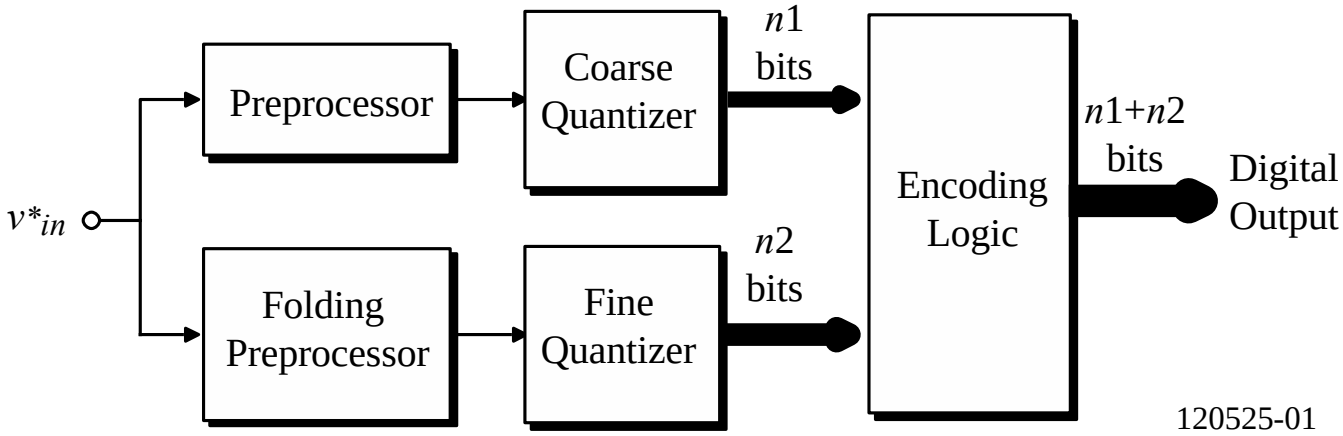


FOLDING

Folding Analog-Digital Converters

Allows the number of comparators to be reduced below the value of 2^N-1.

Architecture for a folded ADC:



Operation:

The input is split into two or more parallel paths.

- First path uses a coarse quantizer to quantize the signal into 2^{n1} values
- The second path maps all of the 2^{n1} subranges onto a single subrange and applies this analog signal to a fine quantizer of 2^{n2} subranges.

Thus, the total number of comparators is 2^{n1}-1 + 2^{n2}-1 compared with 2^{n1+n2}-1 for a parallel ADC.

I.e., if $n1$ = 2 and $n2$ = 4, the folding ADC requires 3 + 15 = 18 compared with 63 comparators.

Example of a Folding Preprocessor

Folding characteristic for $n1 = 2$ and $n2 = 3$.

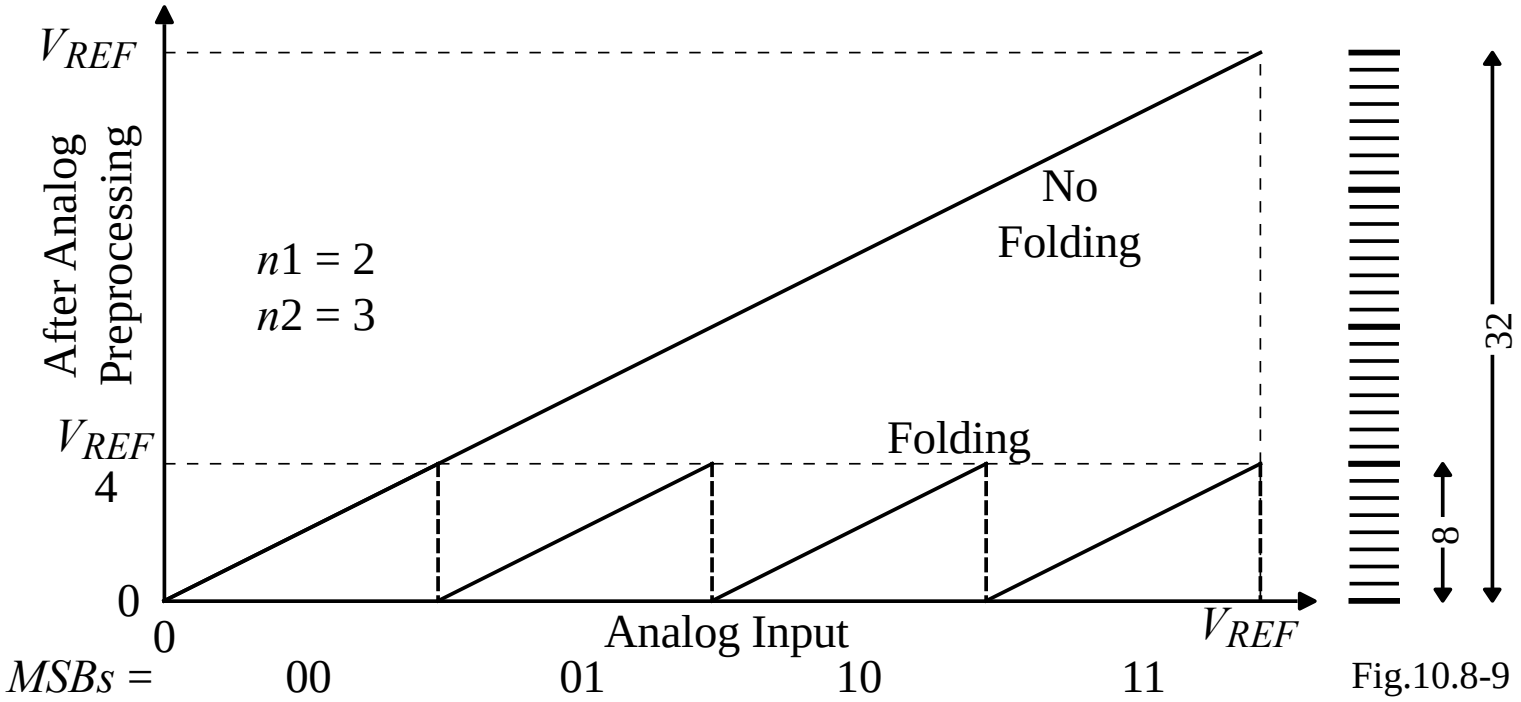


Fig.10.8-9

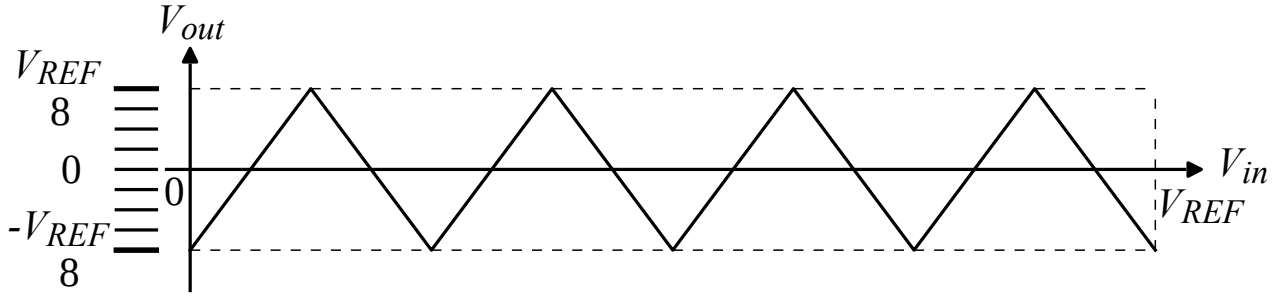
Problems:

- The sharp discontinuities of the folder are difficult to implement at high speeds.
- Fine quantizer must work at voltages ranging from 0 to $V_{REF}/4$ (subranging).
- The actual frequency of the folding signal is F times the input frequency where F is the number of folds

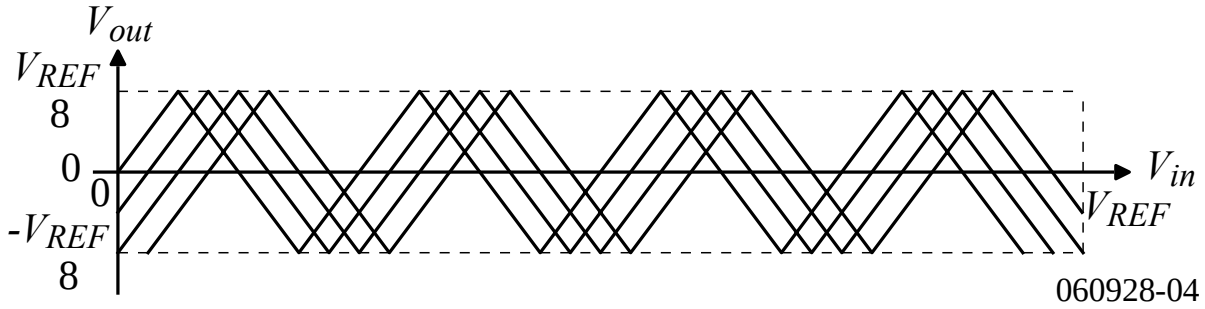
Modified Folding Preprocessors

The discontinuity problem can be removed by the following folding preprocessors:

Folder that removes discontinuity problem.



Multiple folders shifted in voltage.



In the second case, the reference voltage for all comparators is identical which removes any ICMR problems.

A 5-Bit Folding ADC Using 1-Bit Quantizers (Comparators)

Block diagram:

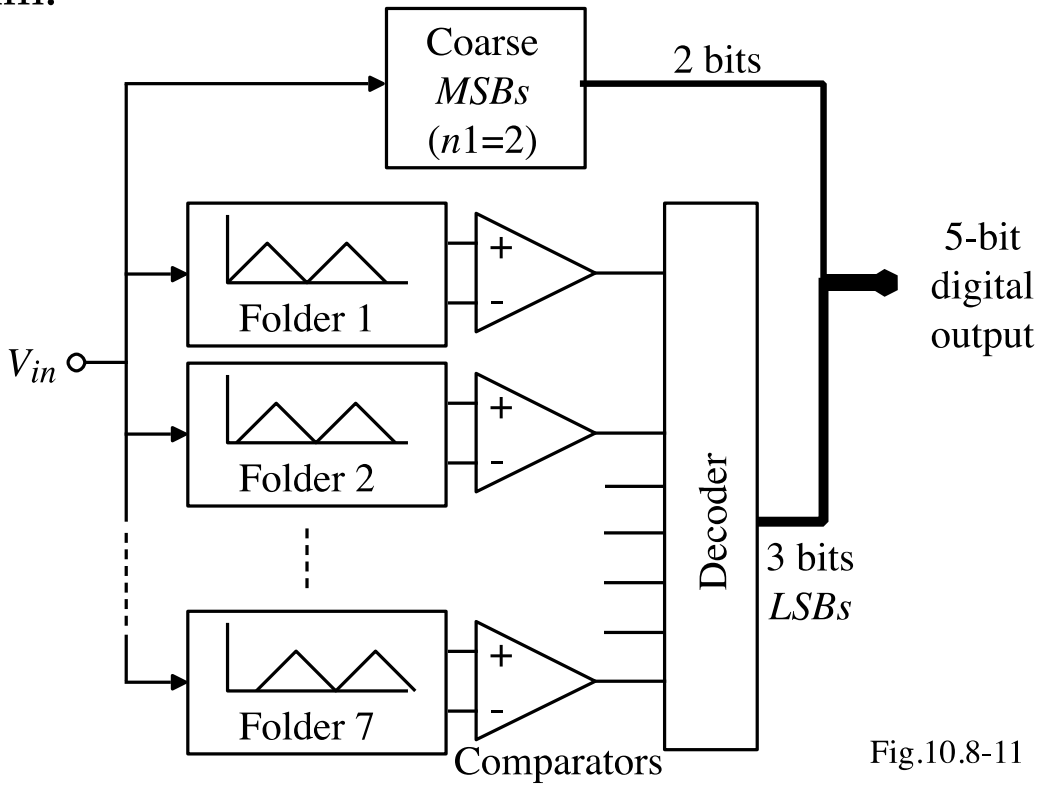


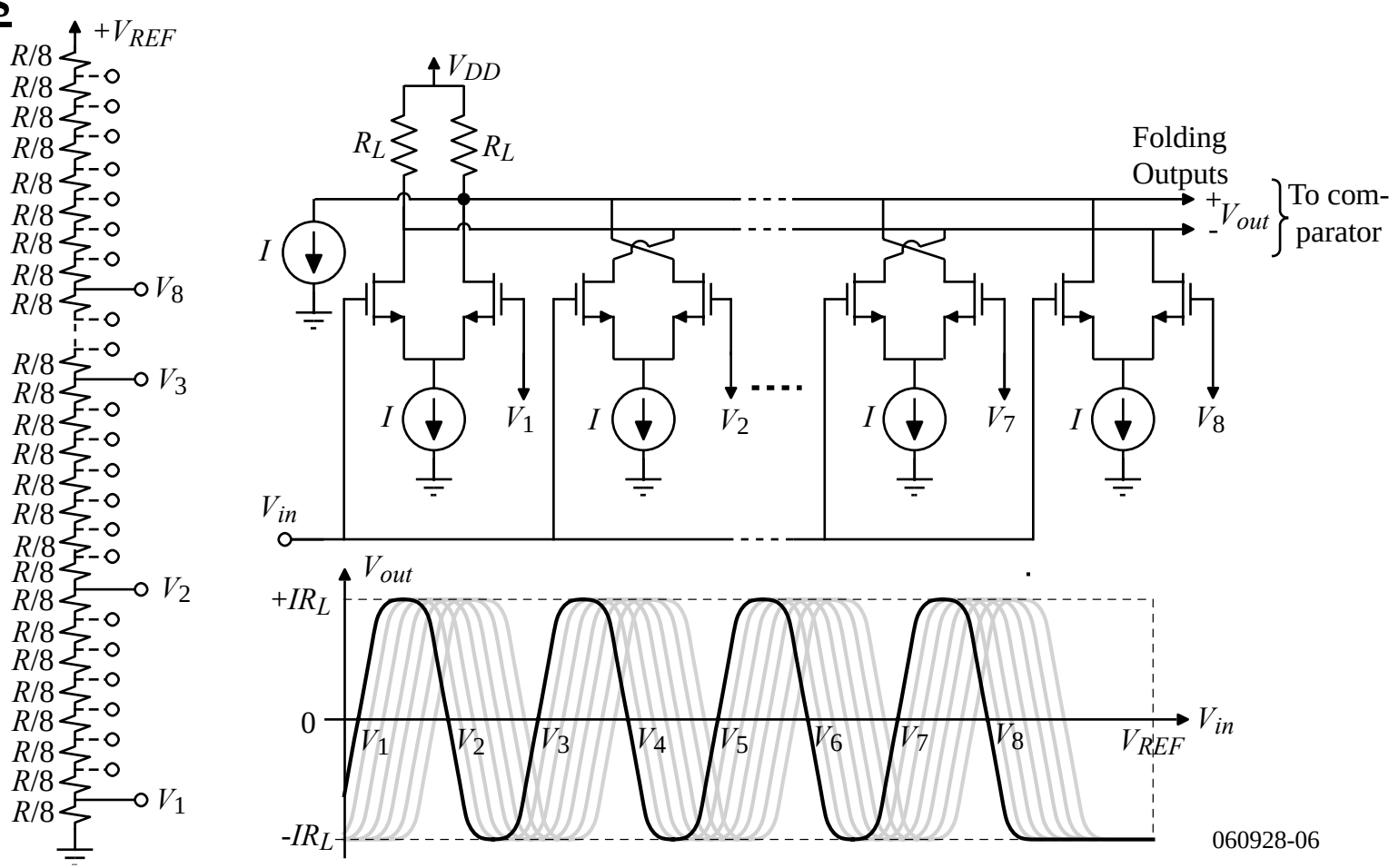
Fig.10.8-11

Comments:

- Number of comparators is 7 for the fine quantizer and 3 for the coarse quantizer
- The zero crossings of the folders must be equally spaced to avoid linearity errors
- The number of folders can be reduced and the comparators simplified by use of interpolation

Folding Circuits

Implementation of a times 4 folder used in a 3-bit quantizer:



Comments:

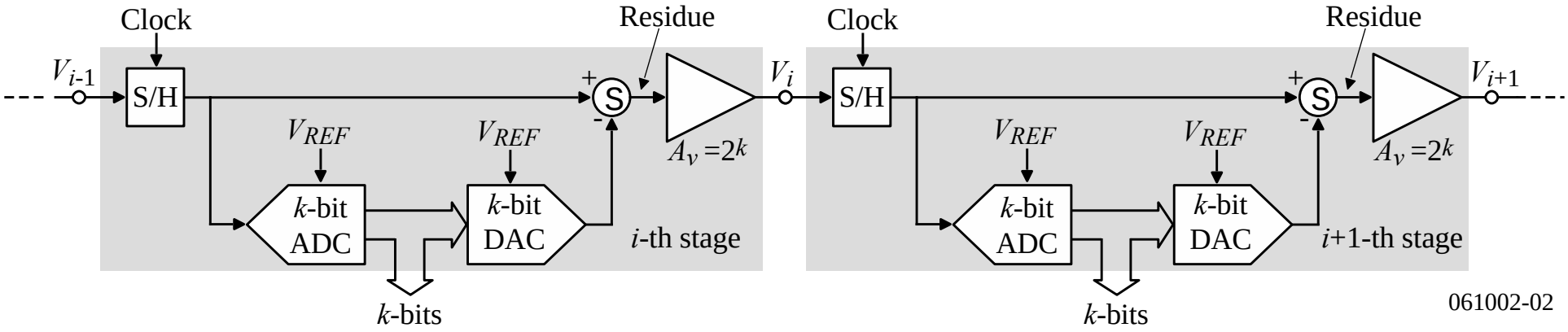
- Horizontal shifting is achieved by connecting V_1 through V_8 to different points on the voltage scaling resistor string.
- Folding and interpolation ADCs offer the most resolution at high speeds (≈8 bits at 500MHz)

HIGH-SPEED, HIGH-RESOLUTION ADCs

Multiple-Bit, Pipeline Analog-Digital Converters

A compromise between speed and resolution is to use a pipeline ADC with multiple bits/stage.

i-th stage of a *k*-bit per stage pipeline ADC with residue amplification:



$$\text{Residue voltage} = V_{i\text{-}1} - \left(\frac{b_0}{2} + \frac{b_1}{2^2} + \cdots + \frac{b_{k\text{-}2}}{2^{k\text{-}1}} + \frac{b_{k\text{-}1}}{2^k}\right) V_{REF}$$

Potential specifications range from 100-300 Msps and 10 to 14 bits.

A 3-Stage, 3-Bit Per Stage Pipeline ADC

Illustration of the operation:

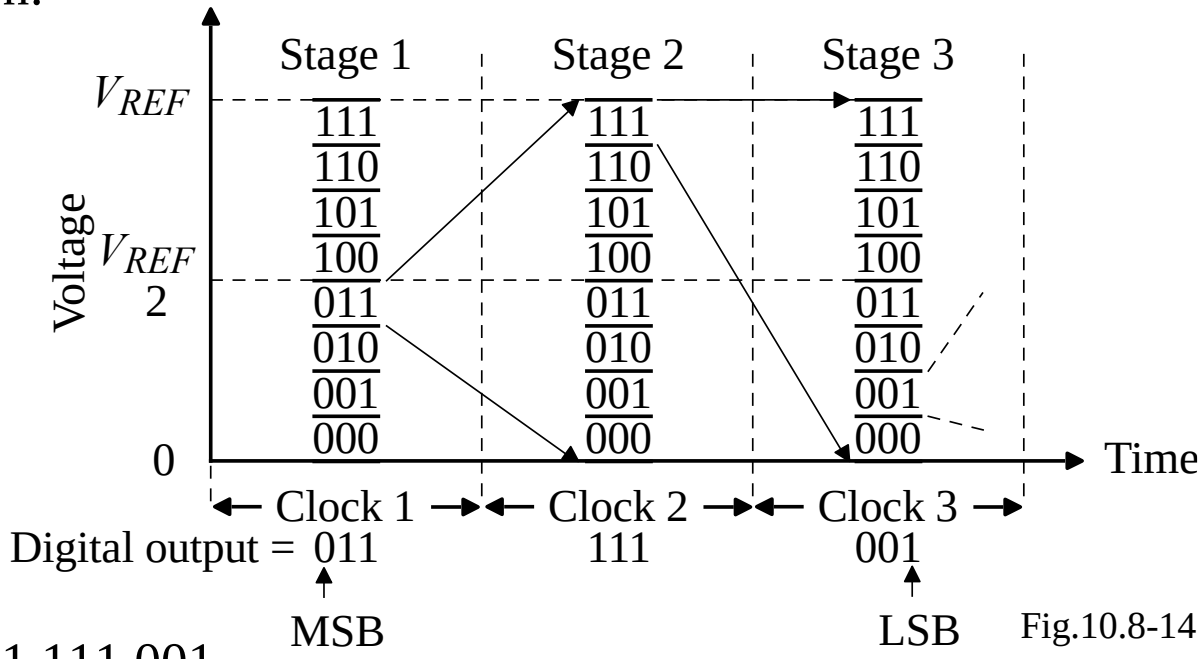


Fig.10.8-14

Converted word is 011 111 001

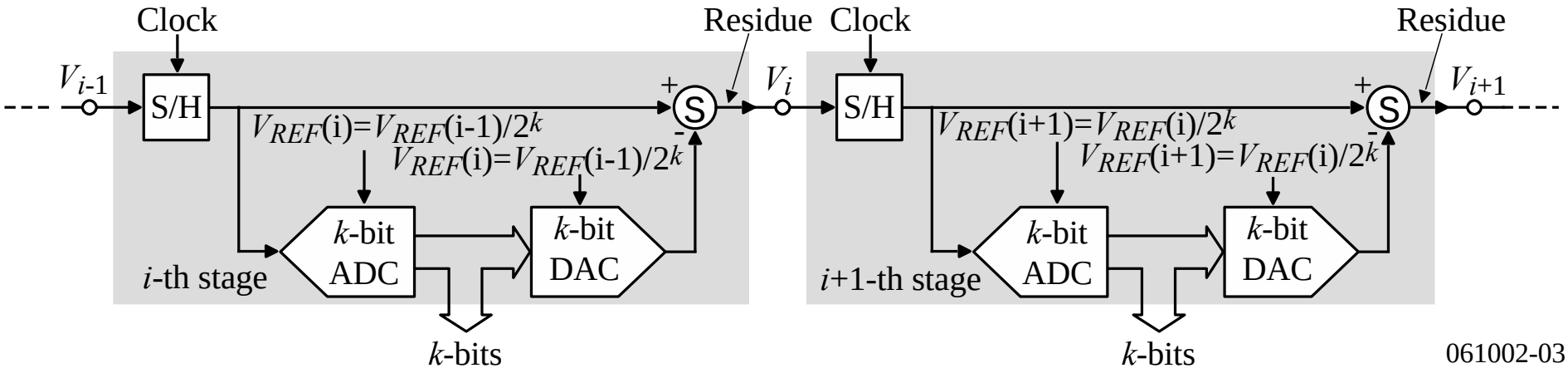
Comments:

- Only 21 comparators are required for this 9-bit ADC
- Conversion occurs in three clock cycles
- The residue amplifier will cause a bandwidth limitation,

$$GB = 50\text{MHz} \rightarrow f_{\text{-3dB}} = \frac{50\text{MHz}}{2^3} \approx 6\text{MHz}$$

Multiple-Bit, Pipeline Analog-Digital Converters - Subranging

The amplification of $A_V = 2^k$ for each stage places a bandwidth limitation on the converter. The subranging technique shown below eliminates this problem.



Note: the reference voltage of the previous stage (i-1) is divided by 2^k to get the reference voltage for the present stage (i), $V_{REF}(i)$, and so forth.

Subranging, Multiple-Bit, Pipeline ADCs

Illustration of a 2-stage, 2-bits/stage pipeline ADC:

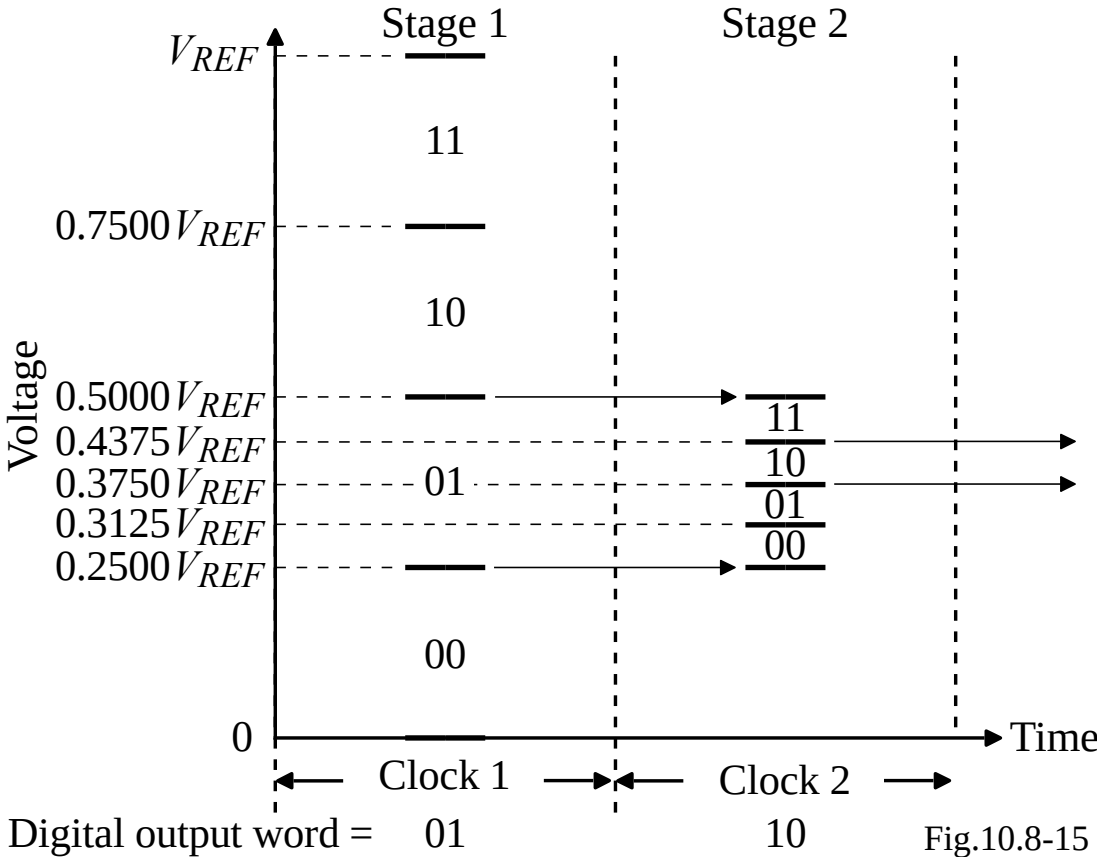


Fig.10.8-15

Comments:

- Resolution of the comparators for the following stages increases but fortunately, the tolerance of each stage decreases by 2^k for every additional stage.
- Removes the frequency limitation of the amplifier

Implementation of the DAC in the Multiple-Bit, Pipeline ADC

Circuit:

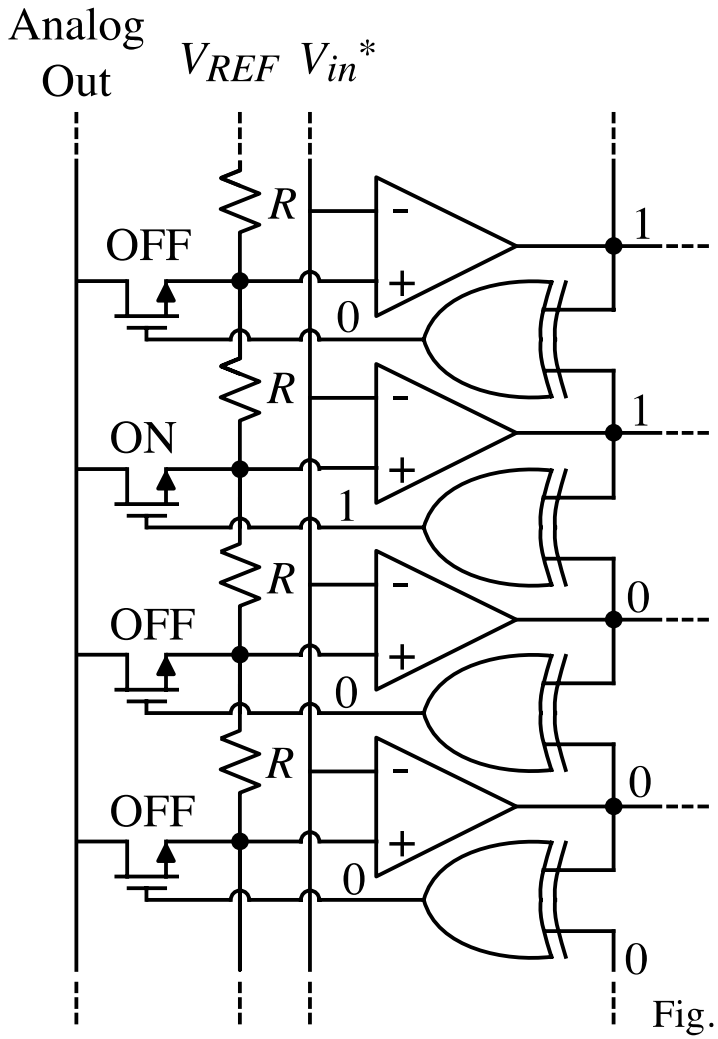


Fig.10.8-16

Comments:

- A good compromise between area and speed
- The ADC does not need to be a flash or parallel if speed is not crucial
- Typical performance is 10 bits at 50Msamples/sec

Example 38-2 - Examination of error in subranging for a 2-stage, 2-bits/stage pipeline ADC

The stages of the 2-stage, 2-bits/stage pipeline ADC shown below are ideal. However, the second stage divides V_{REF} by 2 rather than 4. Find the $\pm INL$ and $\pm DNL$ for this ADC.

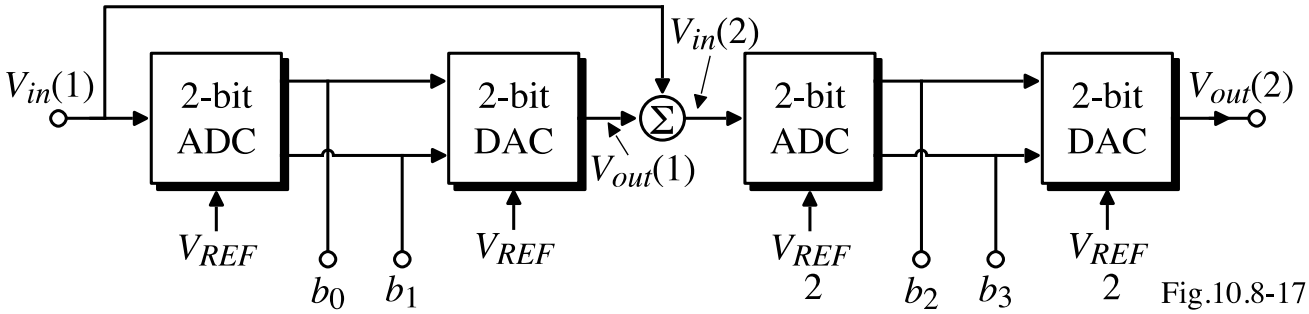


Fig.10.8-17

Solution

Examination of the first stage shows that its output, $V_{out}(1)$ changes at

$$\frac{V_{in}(1)}{V_{REF}} = \frac{1}{4}, \frac{2}{4}, \frac{3}{4}, \text{ and } \frac{4}{4}.$$

The output of the first stage will be

$$\frac{V_{out}(1)}{V_{REF}} = \frac{b_0}{2} + \frac{b_1}{4}.$$

The second stage changes at

$$\frac{V_{in}(2)}{V_{REF}} = \frac{1}{8}, \frac{2}{8}, \frac{3}{8}, \text{ and } \frac{4}{8}$$

where

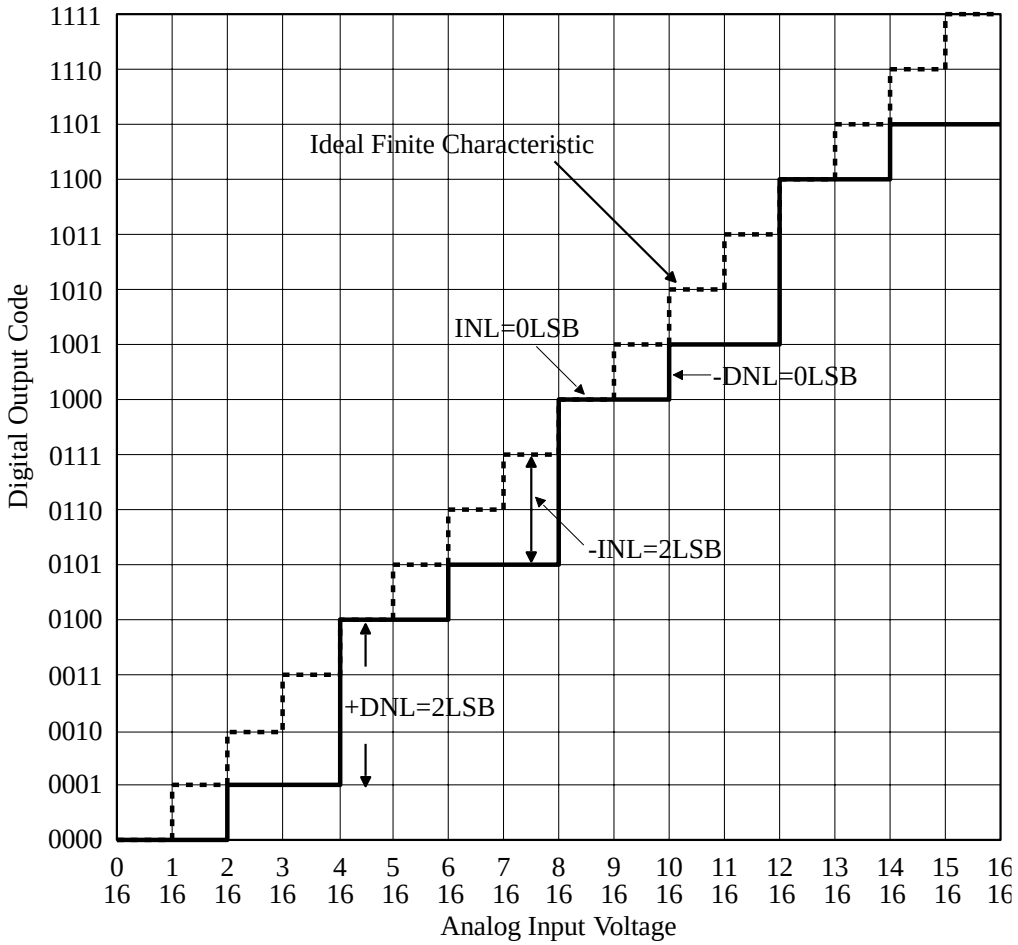
$$V_{in}(2) = V_{in}(1) - V_{out}(1).$$

The above relationships permit the information given in the following table.

Example 38-2 - Continued

Output digital word for Ex. 38-2:

$\frac{V_{in}(1)}{V_{REF}}$	b_0	b_1	$\frac{V_{out}(1)}{V_{REF}}$	$\frac{V_{in}(2)}{V_{REF}}$	b_2	b_3	Ideal Ouput $b_0\ b_1\ b_2\ b_3$			
0	0	0	0	0	0	0	0	0	0	0
1/16	0	0	0	1/16	0	0	0	0	0	1
2/16	0	0	0	2/16	0	1	0	0	1	0
3/16	0	0	0	3/16	0	1	0	0	1	1
4/16	0	1	4/16	0	0	0	0	1	0	0
5/16	0	1	4/16	1/16	0	0	0	1	0	1
6/16	0	1	4/16	2/16	0	1	0	1	1	0
7/16	0	1	4/16	3/16	0	1	0	1	1	1
8/16	1	0	8/16	0	0	0	1	0	0	0
9/16	1	0	8/16	1/16	0	0	1	0	0	1
10/16	1	0	8/16	2/16	0	1	1	0	1	0
11/16	1	0	8/16	3/16	0	1	1	0	1	1
12/16	1	1	12/16	0	0	0	1	1	0	0
13/16	1	1	12/16	1/16	0	0	1	1	0	1
14/16	1	1	12/16	2/16	0	1	1	1	1	0
15/16	1	1	12/16	3/16	0	1	1	1	1	1



Comparing the actual digital output word with the ideal output word gives the following: $+INL = 0LSB$, $-INL$ = 0111-0101 = $-2LSB$, $+DNL$ = (1000-0101) - $1LSB$ = $+2LSB$, and $-DNL$ = (0101-0100) - $1LSB$ = $0LSB$.

Example of a Multiple-Bit, Pipeline ADC

Two-stages with 5-bits per stage resulting in a 10-bit ADC with a sampling rate of 5Msamples/second.

Architecture:

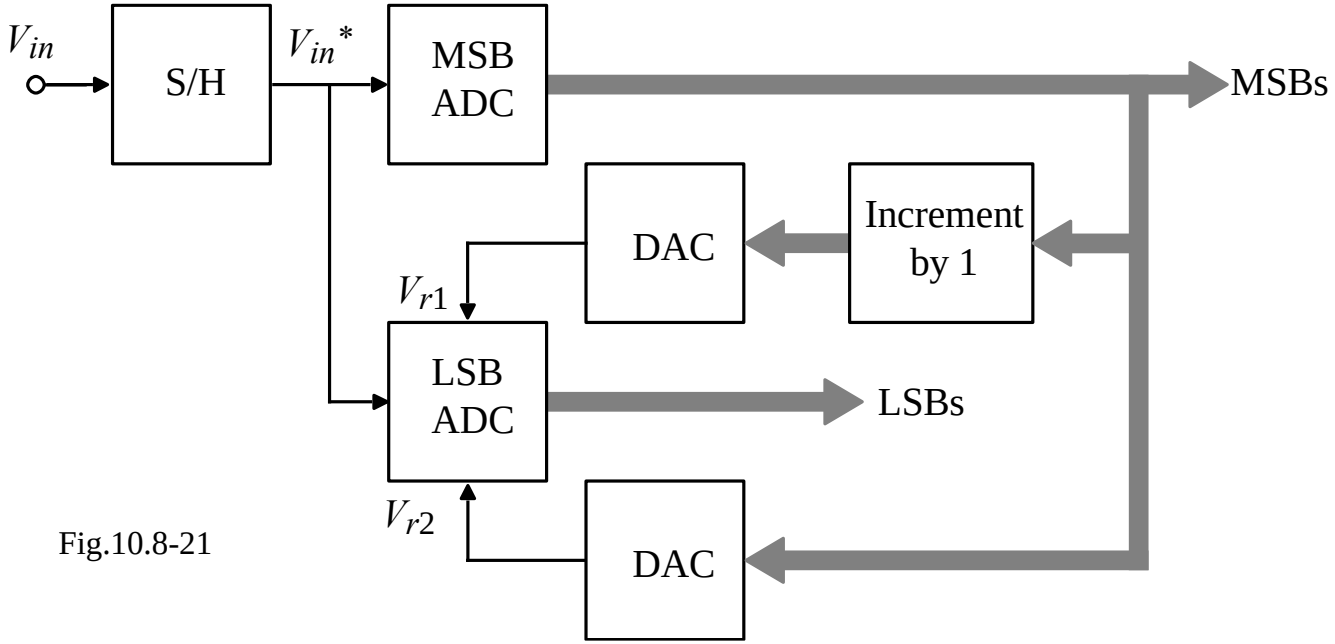


Fig.10.8-21

Features:

- Requires only $2^{n/2}$-1 comparators
- *LSBs* decoded using 31 preset charge redistribution capacitor arrays
- Reference voltages used in the *LSBs* are generated by the *MSB* ADC
- No op amps are used

Example of a Multiple-Bit, Pipeline ADC - Continued

MSB Conversion:

Operation:

1.) Sample V_{in}^* on each $32C$ capacitance autozeroing the comparators

2.) Connect each comparator to a node of the resistor string generating a thermometer code.

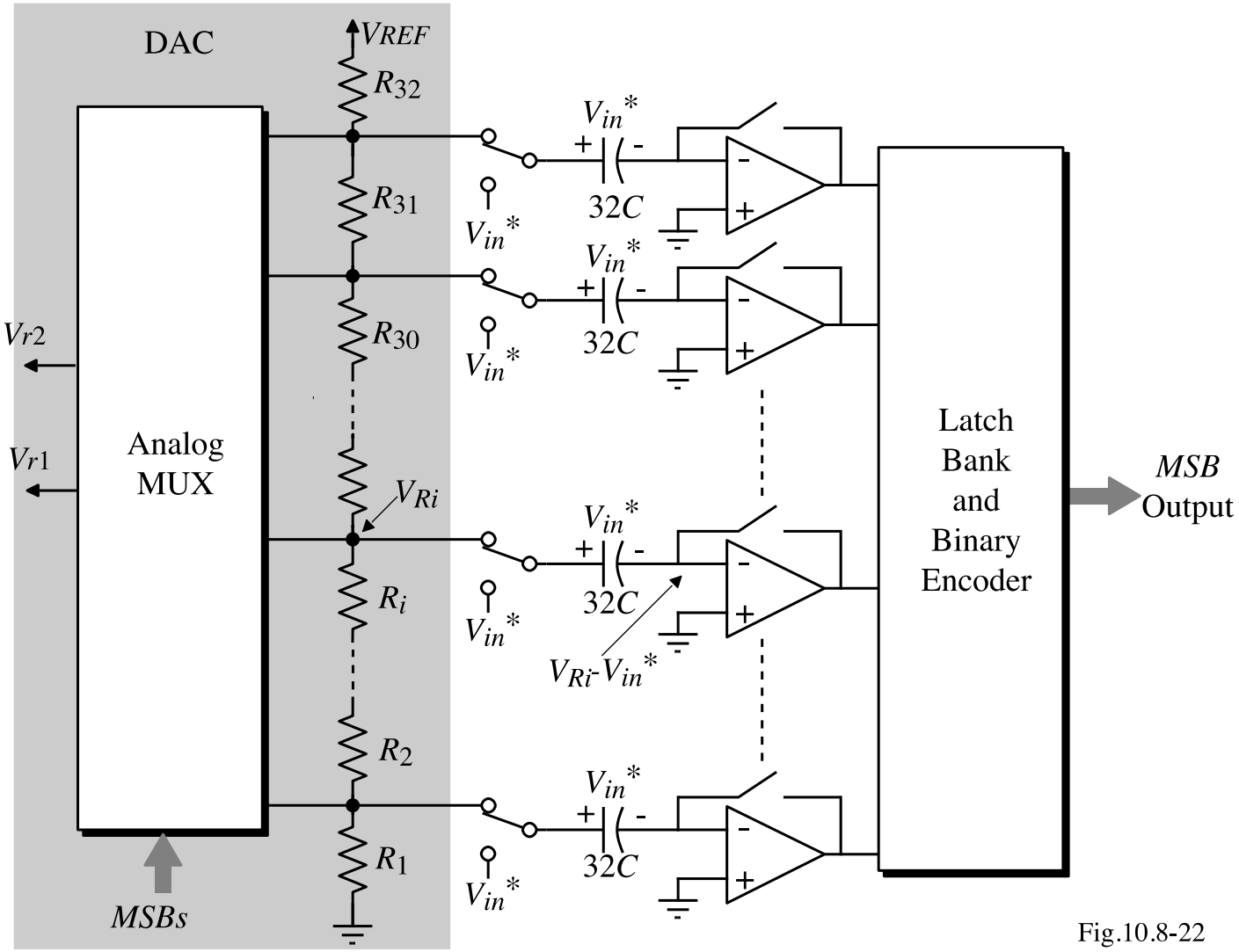


Fig.10.8-22

Example of a Multiple-Bit, Pipeline ADC - Continued

LSB Conversion:

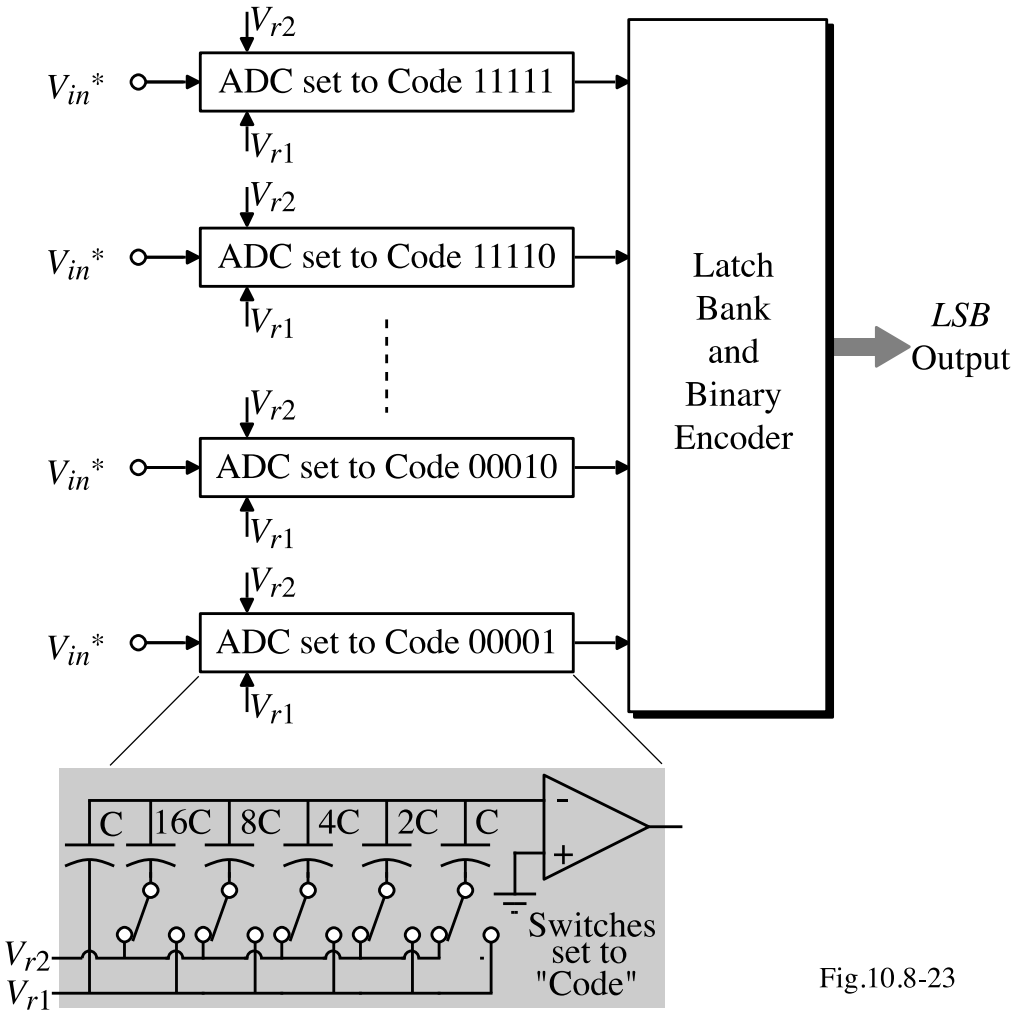


Fig.10.8-23

Operation:

1.) *MSB* comparators are preset to each of the 31 possible digital codes.

2.) V_{r1} and V_{r2} are derived from the *MSB* conversion.

3.) Preset comparators will produce a thermometer code to the encoder.

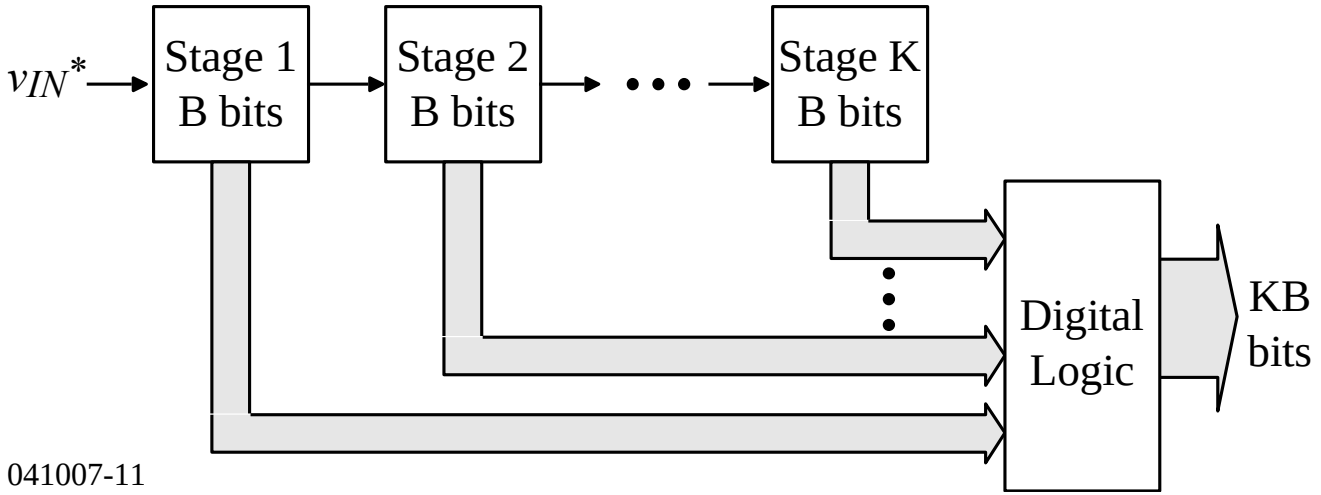
Comments:

- Requires two full clock cycles
- Reuses the comparators
- Accuracy limited by resistor string and its dynamic loading
- Accuracy also limited by the capacitor array
- Comparator is a 3-stage, low-gain, wide-bandwidth, using internal autozeroing

Digital Error Correction

Like many of the accuracy enhancing techniques, there are particular applications where certain correcting techniques are useful. In the pipeline, analog-digital converter, a technique called digital error correction is used to remove the imperfections of the components.

Pipeline ADC:



Operation:

1.) Stage 1 resolves the analog input signal to within one of *B* subranges which determines the first *B* bits.

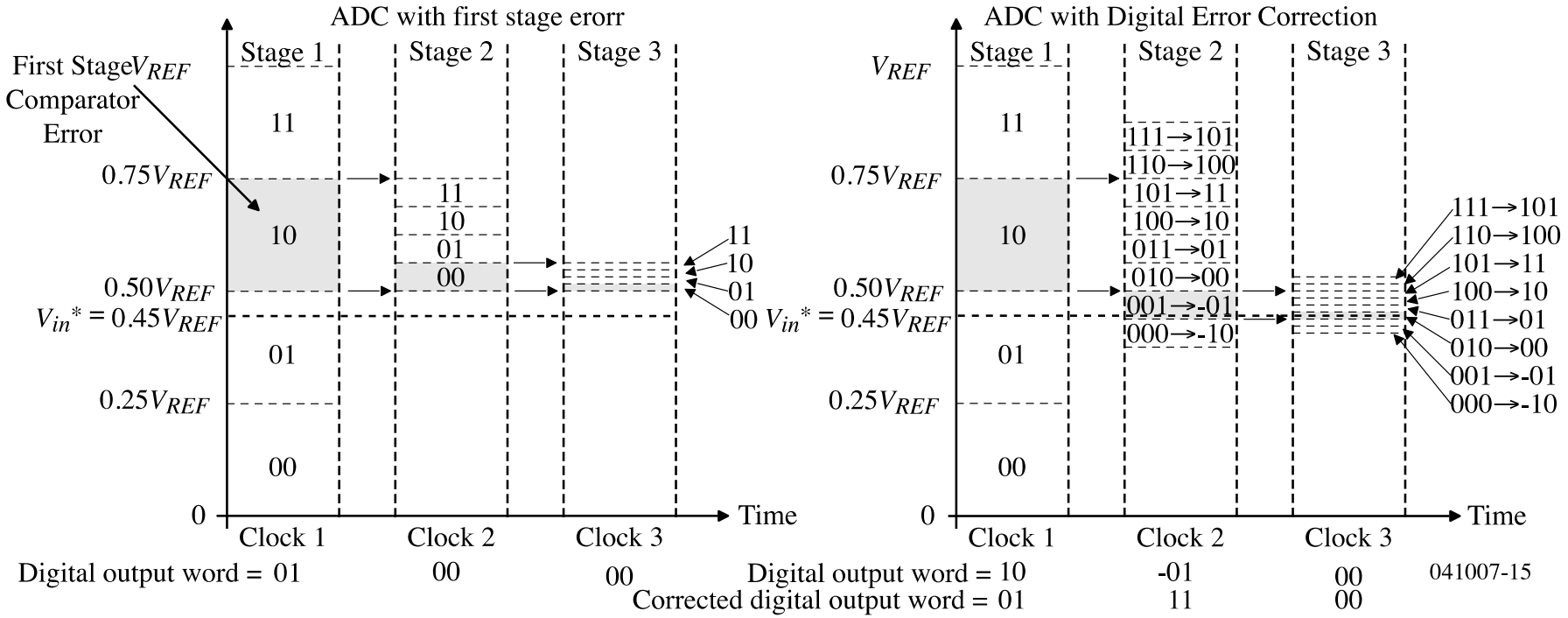
2.) Stage 1 then creates the analog residue (analog input – quantized analog output) and passes on to Stage 2 by either amplifying or subranging.

3.) Stage 2 repeats this process which ends with Stage K.

Example of Digital Error Correction in a Pipeline ADC

Subranging Pipeline ADC Example (B =2, K = 3) using Digital Error Correction.

No correction (error in first comparator): Digital error correction (extra bit in stage 2):



Comments:

- Adds a correcting bit to the following stage to correct for errors in the previous stage.
- The subranging or amplification of the next stage does not include the correcting bit.
- Correction can be done after all stages of the pipeline ADC have converted or after each individual stage.

12-Bit Pipeline ADC with Digital Error Correction & Self-Calibration†

Digital Error Correction:

- Avoids saturation of the next stage
- Reduces the number of missing codes
- Relaxed specifications for the comparators
- Compensates for wrong decisions in the coarse quantizers

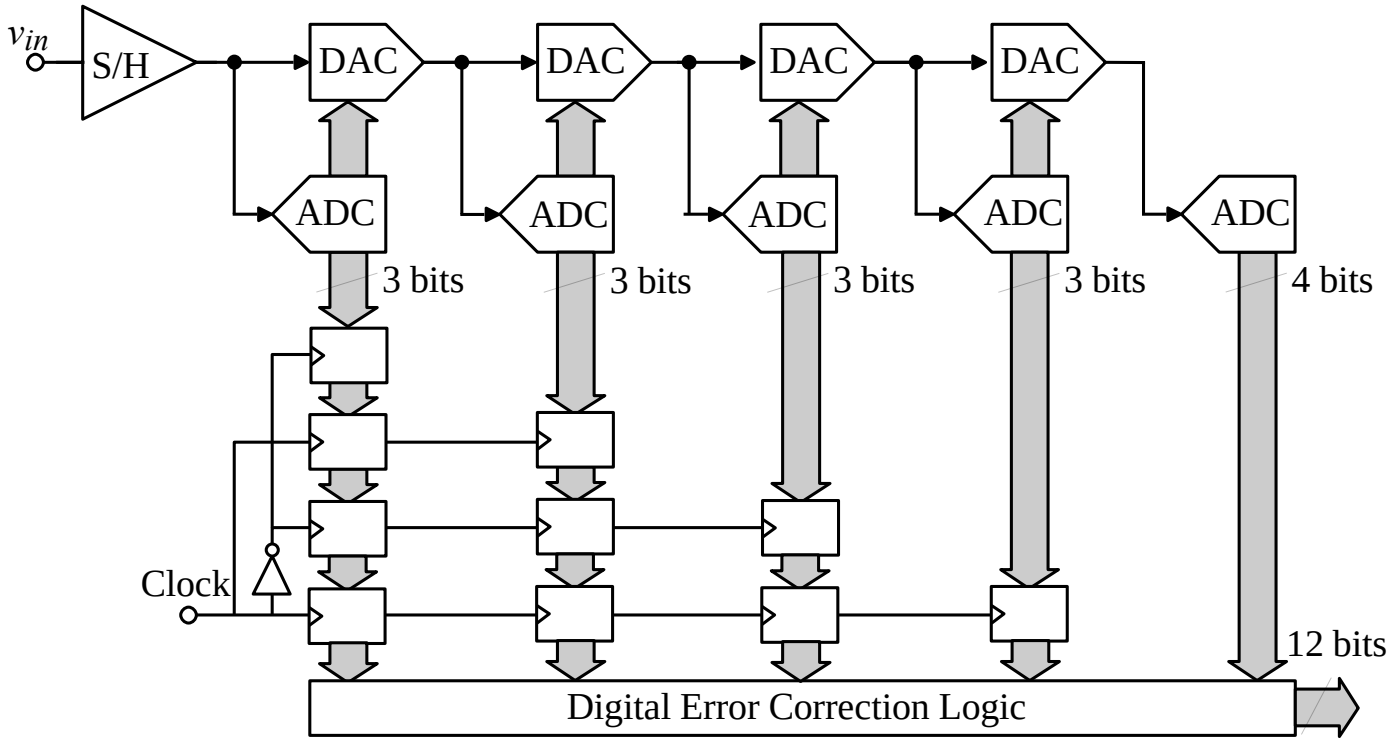


Fig. 11-30

Self-Calibration:

- Can calibrate the effects of the DAC nonlinearity and gain error
- Can be done by digital or analog methods or both

† J. Goes, et. al., *CICC'96*

TIME-INTERLEAVED ADC CONVERTERS

Time-Interleaved Analog-Digital Converters

Slower ADCs are used in parallel for area reduction or fast ADCs in parallel for speed.

Illustration:

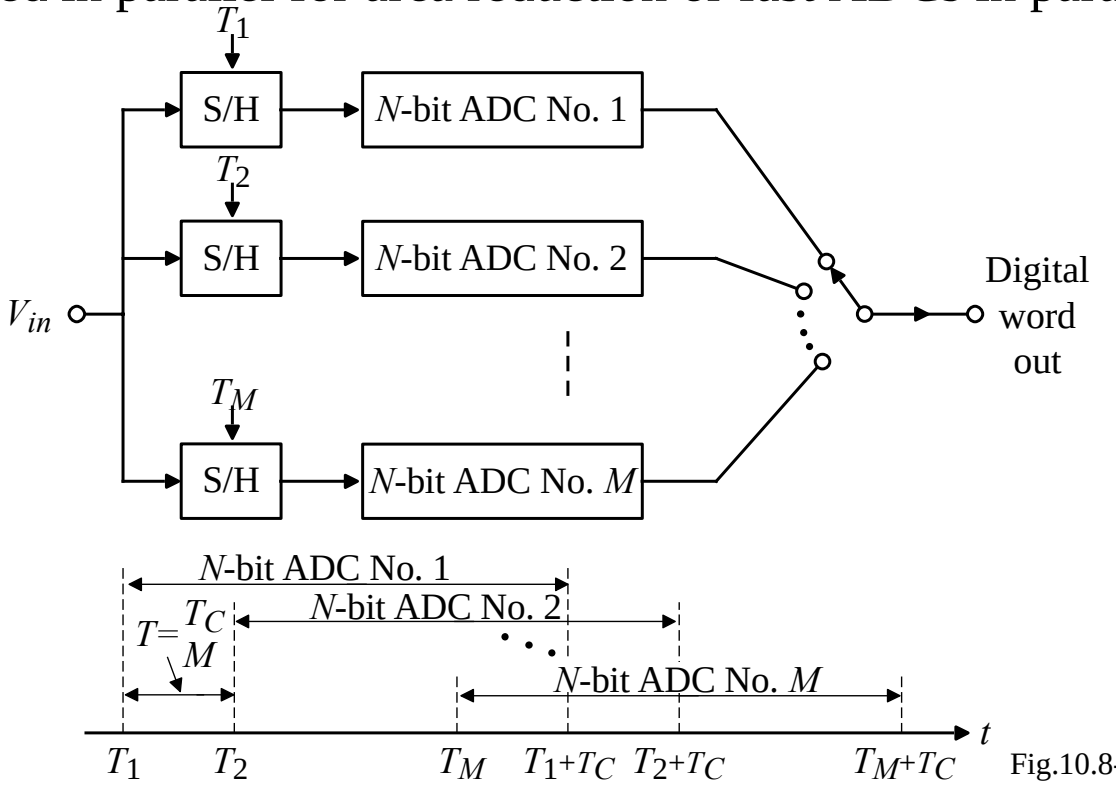


Fig.10.8-20

Comments:

- Can get the same throughput with less chip area
- If $M = N$, then a digital word is converted at every clock cycle
- Multiplexer and timing become challenges at high speeds
- Channels must be matched with ±0.5LSB for delay, gain, and offset.

SUMMARY

Type of ADC	Primary Advantage	Primary Disadvantage
Flash or parallel	Fast	Area is large if $N > 6$
Interpolating	Fast	Requires accurate interpolation
Folding	Fast	Bandwidth increases if no S/H used
Multiple-Bit, Pipeline	Increased number of bits	Slower than flash
Time-interleaved	Small area with large throughput	Precise timing and fast multiplexer

Typical Performance:

- 6-8 bits
- 500-2000 Msamples/sec.
- The *ENOB* at the Nyquist frequency is typically 1-2 bits less that the *ENOB* at low frequencies.
- Power is approximately 0.3 to 1W