LECTURE 35 – PARALLEL DACS, IMPROVED DAC RESOLUTION AND SERIAL DACS

LECTURE ORGANIZATION

Outline

- Charge scaling DACs
- Extending the resolution of parallel DACs
- Serial DACs
- Summary

***CMOS Analog Circuit Design*, 3rd Edition Reference**

Pages 517-539

CHARGE SCALING DIGITAL-ANALOG CONVERTERS

General Charge Scaling Digital-Analog Converter

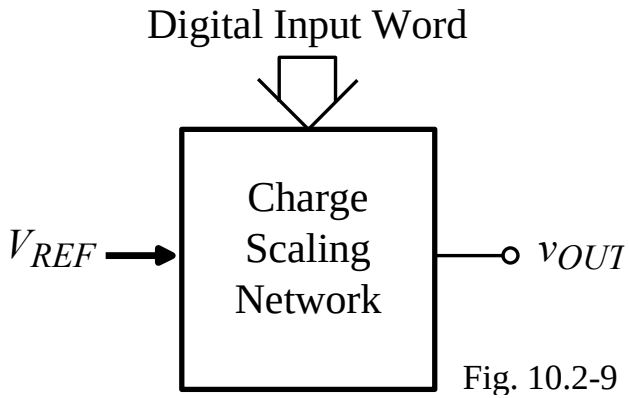


Fig. 10.2-9

General principle is to capacitively attenuate the reference voltage. Capacitive attenuation is simply:

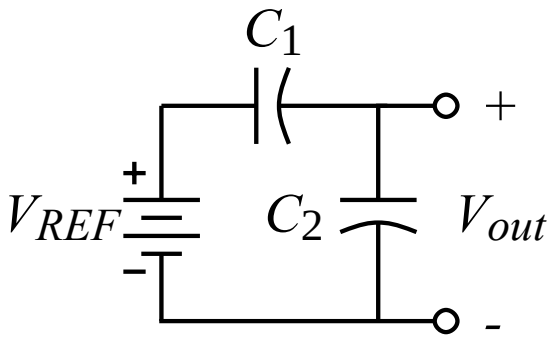


Fig. 10.2-9b

Calculate as if the capacitors were resistors. For example,

$$V_{out} = \frac{\frac{1}{C_2}}{\frac{1}{C_1}+\frac{1}{C_2}} V_{REF} = \frac{C_1}{C_1 + C_2} V_{REF}$$

Binary-Weighted, Charge Scaling DAC

Circuit:

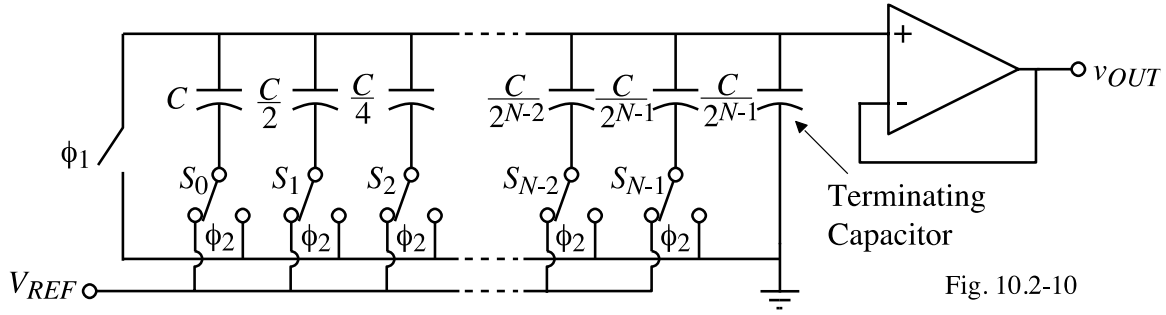


Fig. 10.2-10

Operation:

1.) All switches connected to ground during ϕ_1.

2.) Switch S_i closes to V_{REF} if $b_i = 1$ or to ground if $b_i = 0$.

Equating the charge in the capacitors gives,

$$V_{REF}C_{eq} = V_{REF}\left(b_0C + \frac{b_1C}{2} + \frac{b_2C}{2^2} + \ldots + \frac{b_{N-1}C}{2^{N-1}}\right) = C_{tot}\,v_{OUT} = 2C\,v_{OUT}$$

which gives

$$v_{OUT} = [b_0 2^{-1} + b_1 2^{-2} + b_2 2^{-3} + \ldots + b_{N-1}2^{-N}]V_{REF}$$

Equivalent circuit of the binary-weighted, charge scaling DAC is:

Attributes:

- Accurate
- Sensitive to parasitics
- Not monotonic
- Charge feedthrough occurs at turn on of switches

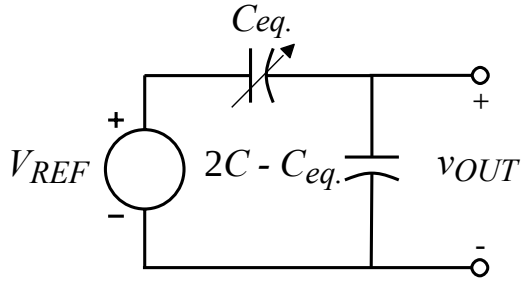


Fig. 10.2-11

Integral Nonlinearity of the Charge Scaling DAC

Again, we use a worst case approach. Assume an n-bit charge scaling DAC with the MSB capacitor of C and the LSB capacitor of $C/2^{n-1}$ and the capacitors have a tolerance of $\Delta C/C$.

The ideal output when the i-th capacitor only is connected to V_{REF} is

$$v_{OUT}\,(\text{ideal}) = \frac{C/2^{i-1}}{2C} V_{REF} = \frac{V_{REF}}{2^i}\left(\frac{2^n}{2^n}\right) = \frac{2^n}{2^i} LSBs$$

The maximum and minimum capacitance is $C_{max} = C + \Delta C$ and $C_{min} = C - \Delta C$. Therefore, the actual worst case output for the i-th capacitor is

$$v_{OUT}(\text{actual}) = \frac{(C\pm\Delta C)/2^{i-1}}{2C} V_{REF} = \frac{V_{REF}}{2^i} \pm \frac{\Delta C \cdot V_{REF}}{2^i C} = \frac{2^n}{2^i} \pm \frac{2^n \Delta C}{2^i C} LSBs$$

Now, the INL for the i-th bit is given as

$$INL(i) = v_{OUT}(\text{actual}) - v_{OUT}(\text{ideal}) = \frac{\pm 2^n \Delta C}{2^i C} = \frac{2^{n-i}\Delta C}{C} LSBs$$

Typically, the worst case value of i occurs for $i = 1$. Therefore, the worst case INL is

$$\boxed{INL = \pm 2^{n-1}\frac{\Delta C}{C} LSBs}$$

Differential Nonlinearity of the Charge Scaling DAC

The worst case *DNL* for the binary weighted capacitor array is found when the *MSB* changes. The output voltage of the binary weighted capacitor array can be written as

$$v_{OUT} = \frac{C_{eq.}}{(2C\text{-}C_{eq.}) + C_{eq.}} V_{REF}$$

where C_{eq} are capacitors whose bits are 1 and $(2C - C_{eq})$ are capacitors whose bits are 0.

The worst case *DNL* can be expressed as

$$DNL = \frac{v_{\text{step}}(\text{worst case})}{v_{\text{step}}(\text{ideal})} - 1 = \left(\frac{v_{OUT}(1000....) - v_{OUT}(0111....)}{1\ LSB} - 1 \right) LSBs$$

The worst case choice for the capacitors is to choose C_1 larger by ΔC and the remaining capacitors smaller by ΔC giving,

$$C_1 = C + \Delta C,\ C_2 = \frac{1}{2}(C - \Delta C), \ldots, C_{n-1} = \frac{1}{2^{n-2}}(C - \Delta C),\ C_n = \frac{1}{2^{n-1}}(C - \Delta C), \text{ and } C_{term} = \frac{1}{2^{n-1}}(C - \Delta C)$$

Note that $\sum_{i=2}^{n} C_i + C_{term} = C_2 + C_3 + \cdots + C_{n-1} + C_n + C_{term} = C - \Delta C$

Differential Nonlinearity of the Charge Scaling DAC - Continued

$$\therefore \quad v_{OUT}(1000...) = \left(\frac{C+\Delta C}{(C+\Delta C)+(C-\Delta C)}\right)V_{REF} = \left(\frac{C+\Delta C}{2C}V_{REF}\right)$$

$$= \left(\frac{C+\Delta C}{2C}V_{REF}\right)\frac{2^n}{2^n} = 2^n\left(\frac{C+\Delta C}{2C}\right) LSBs$$

and

$$v_{OUT}(0111...) = \left(\frac{(C-\Delta C) - C_{term}}{(C+\Delta C)+(C-\Delta C)}\right)V_{REF} = \frac{(C-\Delta C) - \frac{1}{2^{n-1}}(C-\Delta C)}{(C+\Delta C)+(C-\Delta C)}V_{REF}$$

$$= \left(\frac{C-\Delta C}{2C}\right)\left(1 - \frac{2}{2^n}\right)V_{REF} = \frac{2^n}{2^n}\left(\frac{C-\Delta C}{2C}\right)\left(1 - \frac{2}{2^n}\right)V_{REF} = 2^n\left(\frac{C-\Delta C}{2C}\right)\left(1 - \frac{2}{2^n}\right) LSBs$$

$$\therefore \left(\frac{v_{OUT}(1000...) - v_{OUT}(0111...)}{1\ LSB} - 1\right) LSBs = 2^n\left(\frac{C+\Delta C}{2C}\right) - 2^n\left(\frac{C-\Delta C}{2C}\right)\left(1-\frac{2}{2^n}\right) - 1 = (2^n-1)\frac{\Delta C}{C} LSBs$$

Therefore, $\boxed{DNL = (2^n - 1)\frac{\Delta C}{C} LSBs}$

Example 35-1 - *DNL* and *INL* of a Binary Weighted Capacitor Array DAC

If the tolerance of the capacitors in an 8-bit, binary weighted, charge scaling DAC are ±0.5%, find the worst case *INL* and *DNL*.

Solution

For the worst case *INL*, we get from above that

$$INL = (2^7)(\pm 0.005) = \pm 0.64\ LSBs$$

For the worst case *DNL*, we can write that

$$DNL = (2^8\text{-}1)(\pm 0.005) = \pm 1.275\ LSBs$$

Example 35-2 - Influence of Capacitor Ratio Accuracy on Number of Bits

Use the data shown to estimate the number of bits possible for a charge scaling DAC assuming a worst case approach for *INL* and that the worst conditions occur at the midscale (1 *MSB*).

Solution

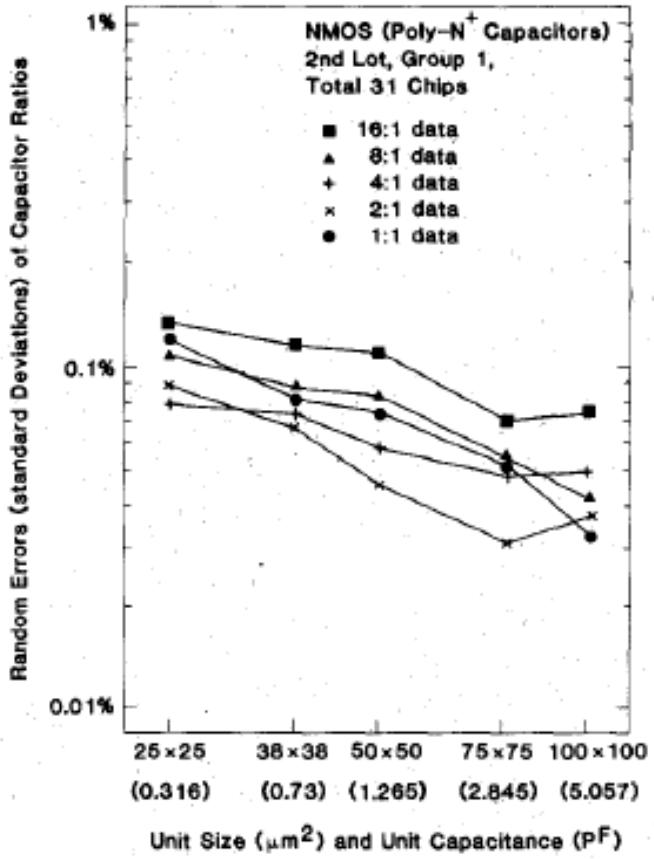
Assuming an *INL* of ±0.5 *LSB*, we can write that

$$INL = \pm 2^{N-1}\frac{\Delta C}{C} \leq \pm\frac{1}{2} \quad \rightarrow \quad \left[\frac{\Delta C}{C}\right] = \frac{1}{2^N}$$

Let us assume a unit capacitor of 50 μm by 50 μm and a relative accuracy of approximately ±0.1%. Solving for *N* in the above equation gives approximately 10 bits. However, the ±0.1% figure corresponds to ratios of 16:1 or 4 bits. In order to get a solution, we estimate the relative accuracy of capacitor ratios as

$$\frac{\Delta C}{C} \approx 0.001 + 0.0001N$$

Using this approximate relationship, a 9-bit digital-analog converter should be realizable.



Binary Weighted, Charge Amplifier DAC

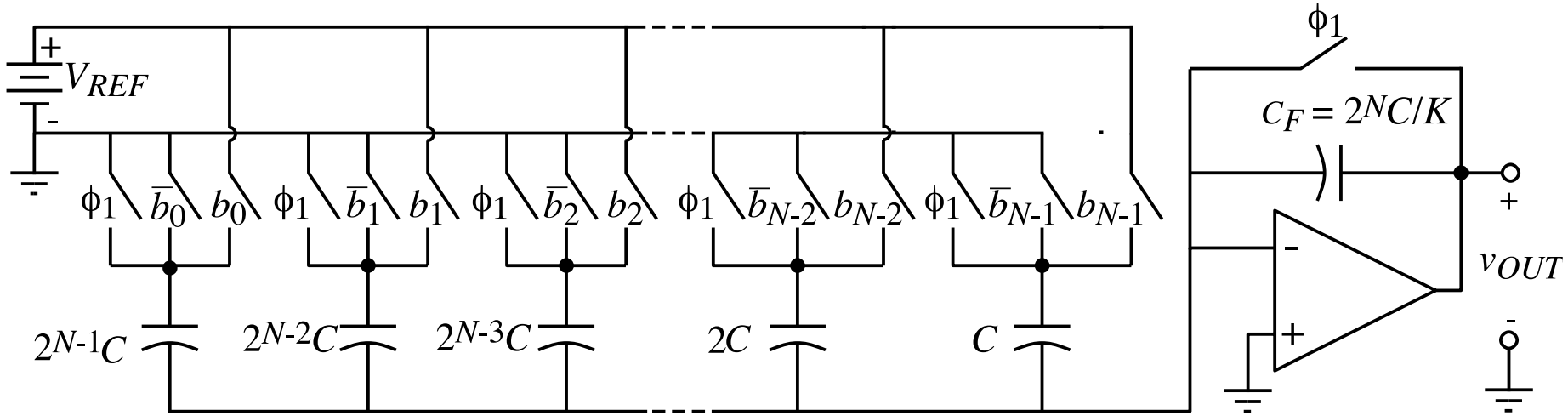


Fig. 10.2-12

Attributes:

- No floating nodes which implies insensitive to parasitics and fast
- No terminating capacitor required
- With the above configuration, charge feedthrough will be $\Delta V_{error} \approx -(C_{OL}/2C^N)\Delta V$
- Can totally eliminate parasitics with parasitic-insensitive switched capacitor circuitry but not the charge feedthrough

EXTENDING THE RESOLUTION OF PARALLEL DIGITAL-ANALOG CONVERTERS

Background

Technique:

Divide the total resolution N into k smaller sub-DACs each with a resolution of $\frac{N}{k}$.

Result:

Smaller total area.

More resolution because of reduced largest to smallest component spread.

Approaches:

- Combination of similarly scaled subDACs
  - Divider approach (scale the analog output of the subDACs)
  - Subranging approach (scale the reference voltage of the subDACs)
- Combination of differently scaled subDACs

COMBINATION OF SIMILARLY SCALED SUBDACs

Analog Scaling - Divider Approach

Example of combining a *m*-bit and *k*-bit subDAC to form a *m*+*k*-bit DAC.

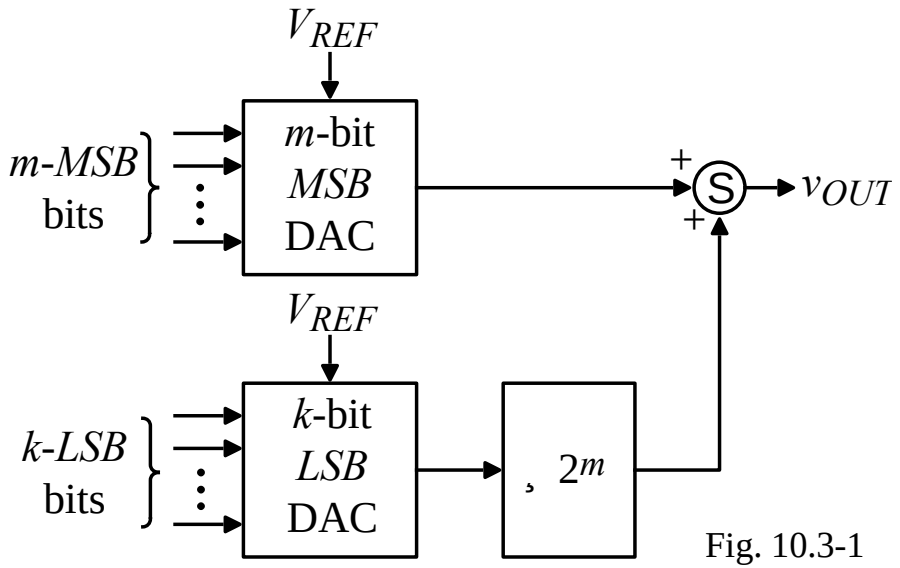


Fig. 10.3-1

$$v_{OUT} = \left(\frac{b_0}{2} + \frac{b_1}{4} + \cdots + \frac{b_{m\text{-}1}}{2^m}\right)V_{REF} + \left(\frac{1}{2^m}\right)\left(\frac{b_m}{2} + \frac{b_{m+1}}{4} + \cdots + \frac{b_{m+k\text{-}1}}{2^k}\right)V_{REF}$$

$$v_{OUT} = \left(\frac{b_0}{2} + \frac{b_1}{4} + \cdots + \frac{b_{m\text{-}1}}{2^m} + \frac{b_m}{2^{m+1}} + \frac{b_{m+1}}{2^{m+2}} + \cdots + \frac{b_{m+k\text{-}1}}{2^{m+k}}\right)V_{REF}$$

Example 35-3 - Illustration of the Influence of the Scaling Factor

Assume that $m = 2$ and $k = 2$ in Fig. 10.3-1 and find the transfer characteristic of this DAC if the scaling factor for the *LSB* DAC is 3/8 instead of 1/4. Assume that $V_{REF} =$ 1V. What is the $\pm INL$ and $\pm DNL$ for this DAC? Is this DAC monotonic or not?

Solution

The ideal DAC output is given as

$$v_{OUT} = \frac{b_0}{2} + \frac{b_1}{4} + \frac{1}{4}\left(\frac{b_2}{2} + \frac{b_3}{4}\right) = \frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \frac{b_3}{16}.$$

The actual DAC output can be written as

$$v_{OUT}(\text{act.}) = \frac{b_0}{2} + \frac{b_1}{4} + \frac{3b_2}{16} + \frac{3b_3}{32} = \frac{16b_0}{32} + \frac{8b_1}{32} + \frac{6b_2}{32} + \frac{3b_3}{32}$$

The results are tabulated in the following table for this example.

Example 35-3 - Continued

Ideal and Actual Analog Output for the DAC in Ex. 35-3,

Input Digital Word	v_{OUT}(act.)	v_{OUT}	v_{OUT}(act.) - v_{OUT}	Change in v_{OUT}(act) - 2/32
0000	0/32	0/32	0/32	-
0001	3/32	2/32	1/32	1/32
0010	6/32	4/32	2/32	1/32
0011	9/32	6/32	3/32	1/32
0100	8/32	8/32	0/32	-3/32
0101	11/32	10/32	1/32	1/32
0110	14/32	12/32	2/32	1/32
0111	17/32	14/32	3/32	1/32
1000	16/32	16/32	0/32	-3/32
1001	19/32	18/32	1/32	1/32
1010	22/32	20/32	2/32	1/32
1011	25/32	22/32	3/32	1/32
1100	24/32	24/32	0/32	-3/32
1101	27/32	26/32	1/32	1/32
1110	30/32	28/32	2/32	1/32
1111	33/32	30/32	3/32	1/32

The table contains all the information we are seeking. An LSB for this example is 1/16 or 2/32. The fourth column gives the +*INL* as 1.5*LSB* and the -INL as 0*LSB*. The fifth column gives the +*DNL* as 0.5*LSB* and the -*DNL* as -1.5*LSB*. Because the -*DNL* is greater than -1*LSB*, this DAC is not monotonic.

Reference Scaling - Subranging Approach

Example of combining a *m*-bit and *k*-bit subDAC to form a *m*+*k*-bit DAC.

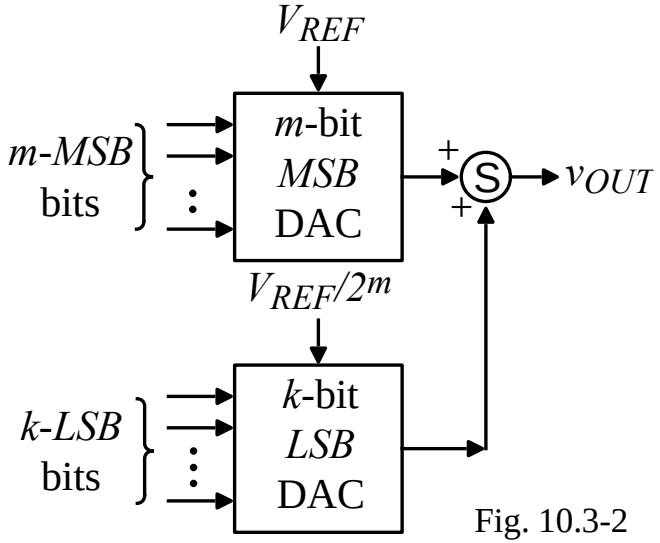


Fig. 10.3-2

$$v_{OUT} = \left(\frac{b_0}{2} + \frac{b_1}{4} + \cdots + \frac{b_{m\text{-}1}}{2^m}\right)V_{REF} + \left(\frac{b_m}{2} + \frac{b_{m+1}}{4} + \cdots + \frac{b_{m+k\text{-}1}}{2^k}\right)\left(\frac{V_{REF}}{2^m}\right)$$

$$v_{OUT} = \left(\frac{b_0}{2} + \frac{b_1}{4} + \cdots + \frac{b_{m\text{-}1}}{2^m} + \frac{b_m}{2^{m+1}} + \frac{b_{m+1}}{2^{m+2}} + \cdots + \frac{b_{m+k\text{-}1}}{2^{m+k}}\right)V_{REF}$$

Accuracy considerations of this method are similar to the analog scaling approach.

Advantage: There are no dynamic limitations associated with the scaling factor of $1/2^m$.

Current Scaling Dac Using Two SubDACs

Implementation:

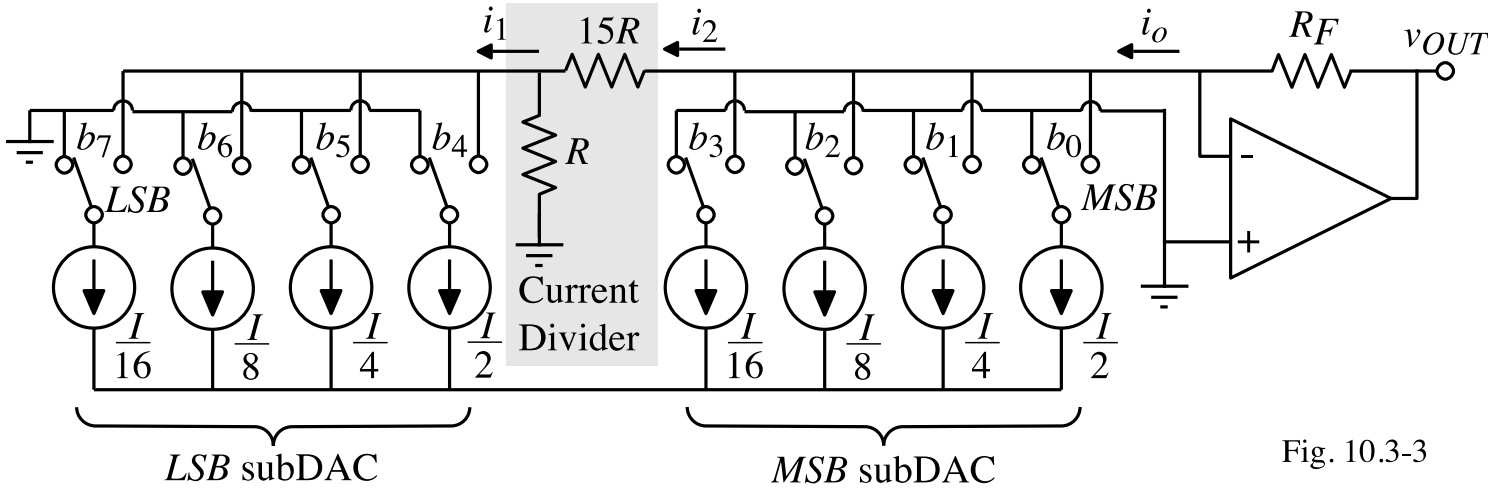
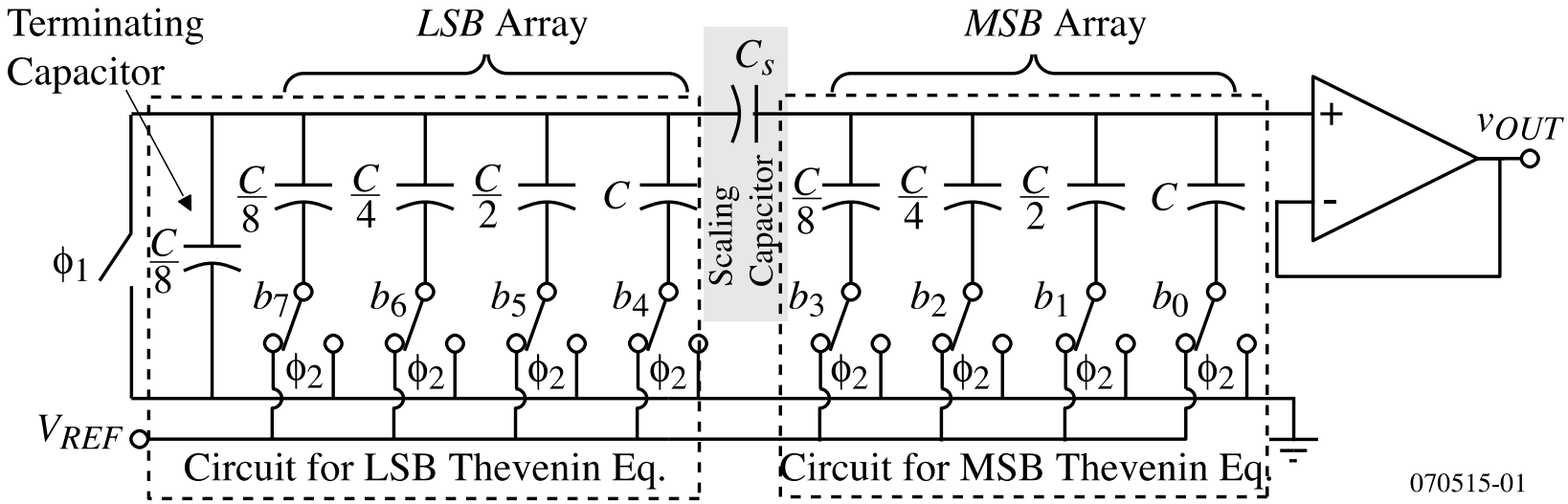


Fig. 10.3-3

$$v_{OUT} = R_F I\left[\left(\frac{b_0}{2}+\frac{b_1}{4}+\frac{b_2}{8}+\frac{b_3}{16}\right)+\frac{1}{16}\left(\frac{b_4}{2}+\frac{b_5}{4}+\frac{b_6}{8}+\frac{b_7}{16}\right)\right]$$

Charge Scaling DAC Using Two SubDACs

Implementation:



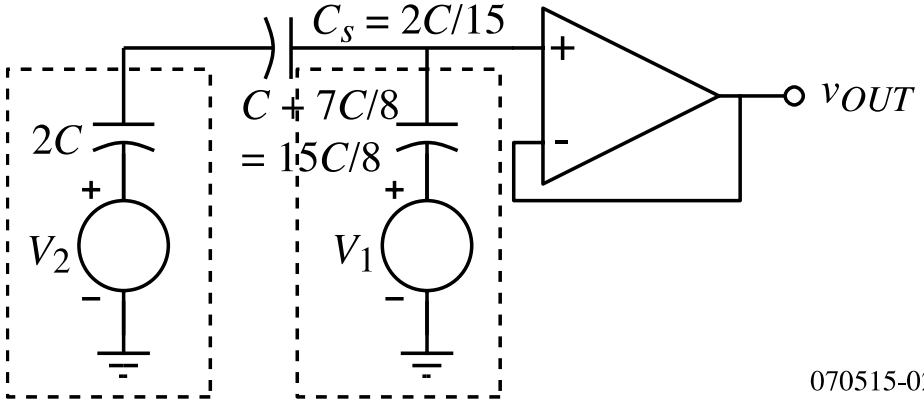
Design of the scaling capacitor, C_S:

The series combination of C_s and the *LSB* array must terminate the *MSB* array or equal $C/8$. Therefore, we can write

$$\frac{C}{8} = \frac{1}{\frac{1}{C_s} + \frac{1}{2C}} \quad \text{or} \quad \frac{1}{C_S} = \frac{8}{C} - \frac{1}{2C} = \frac{16}{2C} - \frac{1}{2C} = \frac{15}{2C}$$

Equivalent Circuit of the Charge Scaling Dac Using Two SubDACs

Simplified equivalent circuit:



where the Thevenin equivalent voltage of the *MSB* array is

$$V_1 = \left[\left(\frac{1}{15/8}\right)b_0 + \left(\frac{1/2}{15/8}\right)b_1 + \left(\frac{1/4}{15/8}\right)b_2 + \left(\frac{1/8}{15/8}\right)b_3\right]V_{REF} = \frac{16}{15}\left(\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \frac{b_3}{16}\right)V_{REF}$$

and the Thevenin equivalent voltage of the *LSB* array is

$$V_2 = \left[\left(\frac{1/1}{2}\right)b_4 + \left(\frac{1/2}{2}\right)b_5 + \left(\frac{1/4}{2}\right)b_6 + \left(\frac{1/8}{2}\right)b_7\right]V_{REF} = \left(\frac{b_4}{2} + \frac{b_5}{4} + \frac{b_6}{8} + \frac{b_7}{16}\right)V_{REF}$$

Combining the elements of the simplified equivalent circuit above gives

$$v_{OUT} = \left(\frac{\frac{1}{2}+\frac{15}{2}}{\frac{1}{2}+\frac{15}{2}+\frac{8}{15}}\right)V_1 + \left(\frac{\frac{8}{15}}{\frac{1}{2}+\frac{15}{2}+\frac{8}{15}}\right)V_2 = \left(\frac{15+15\cdot 15}{15+15\cdot 15+16}\right)V_1 + \left(\frac{16}{15+15\cdot 15+16}\right)V_2 =$$

$$\frac{15}{16}V_1 + \frac{1}{16}V_2$$

$$v_{OUT} = \left(\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \frac{b_3}{16} + \frac{b_4}{32} + \frac{b_5}{64} + \frac{b_6}{128} + \frac{b_7}{256}\right)V_{REF} = \sum_{i=0}^{7} \frac{b_i V_{REF}}{2i+1}$$

Charge Amplifier DAC Using Two Binary Weighted Charge Amplifier SubDACs

Implementation:

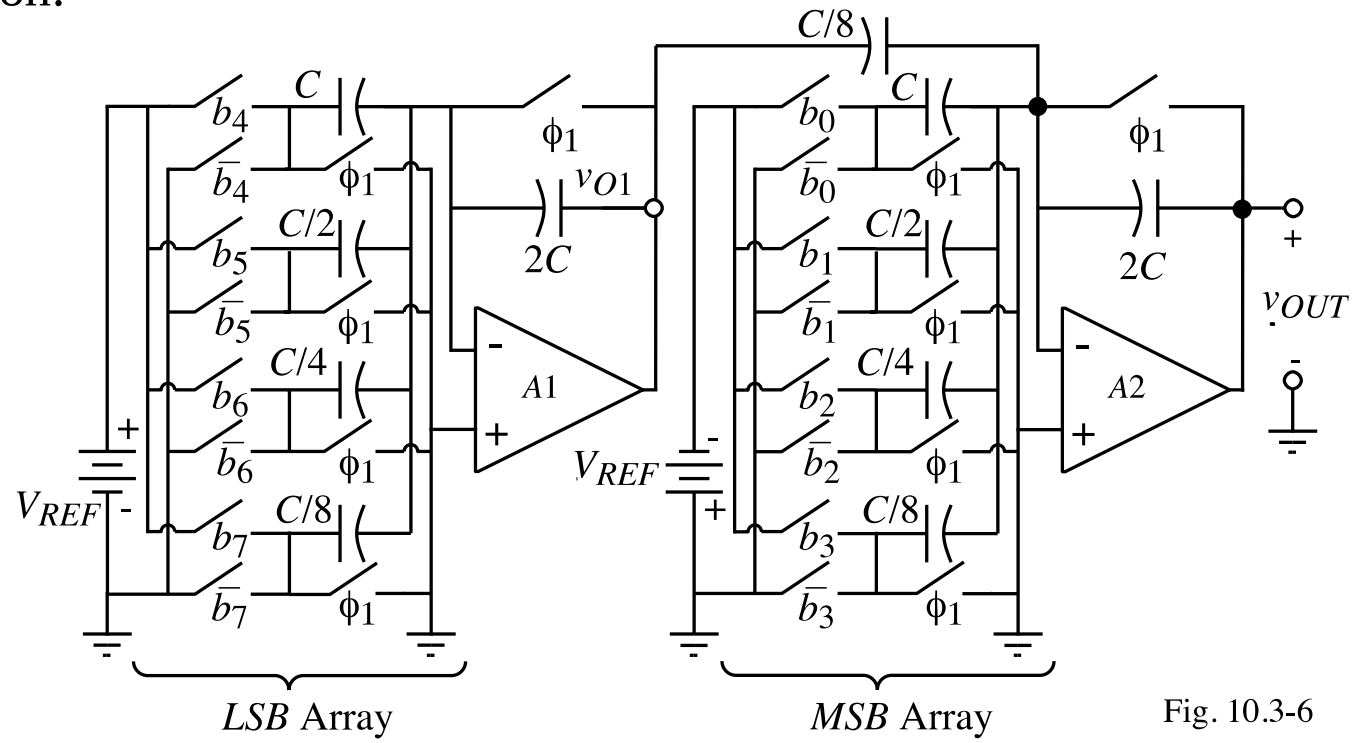


Fig. 10.3-6

Attributes:

- *MSB* subDAC is not dependent upon the accuracy of the scaling factor for the *LSB* subDAC.
- Insensitive to parasitics, fast
- Limited to op amp dynamics (*GB*)
- No ICMR problems with the op amp

COMBINATION OF DIFFERENTLY SCALED SUBDACs

Voltage Scaling *MSB* SubDAC And Charge Scaling *LSB* SubDAC

Implementation:

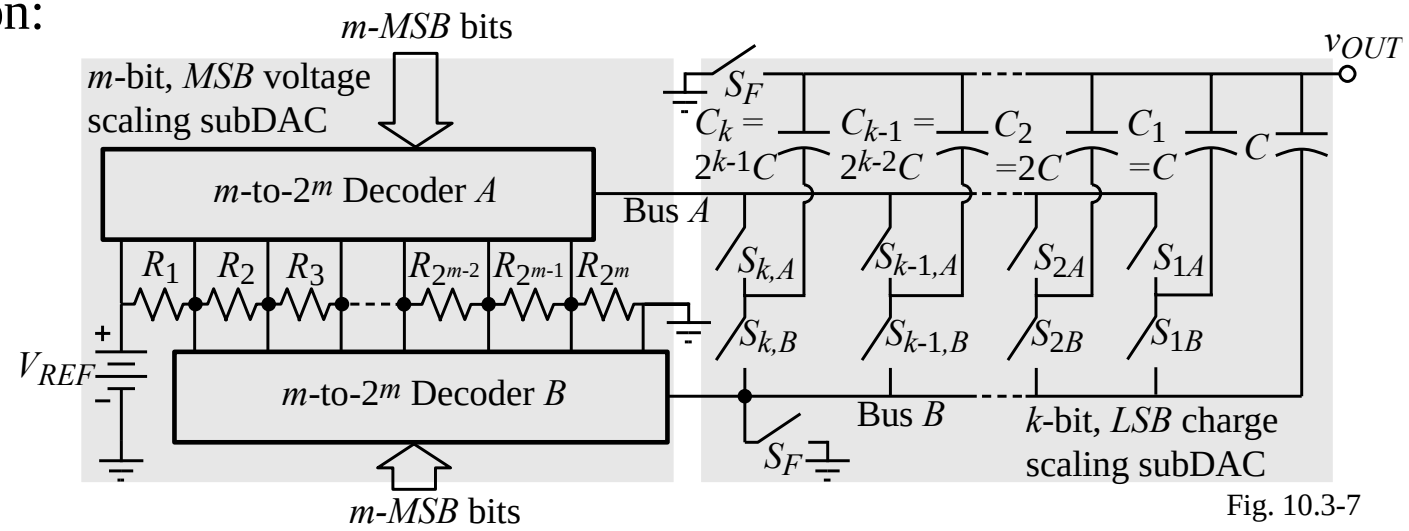


Fig. 10.3-7

Operation:

1.) Switches S_F and S_{1B} through $S_{k,B}$ discharge all capacitors.

2.) Decoders *A* and *B* connect Bus *A* and Bus *B* to the top and bottom, respectively, of the appropriate resistor as determined by the *m*-bits.

3.) The charge scaling subDAC divides the voltage across this resistor by capacitive division determined by the *k*-bits.

Attributes:

- *MSB's* are monotonic but the accuracy is poor
- Accuracy of *LSBs* is good

Voltage Scaling *MSB* SubDAC And Charge Scaling *LSB* SubDAC - Continued

Equivalent circuit of the voltage scaling (*MSB*) and charge scaling (*LSB*) DAC:

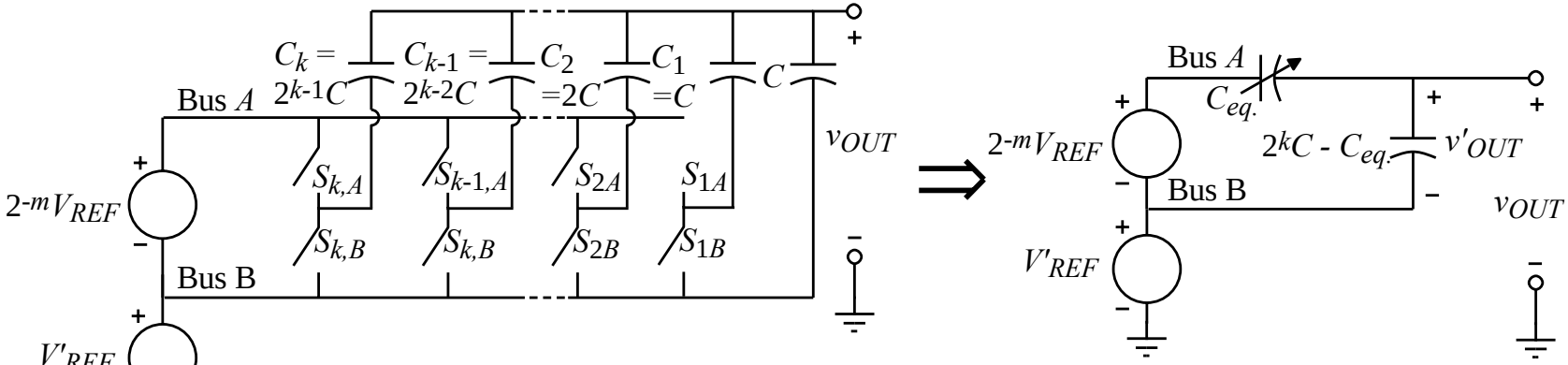


Fig. 10.3-8

where,

$$V'_{REF} = V_{REF}\left(\frac{b_0}{2^1} + \frac{b_1}{2^2} + \cdots + \frac{b_{m-2}}{2^{m-1}} + \frac{b_{m-1}}{2^m}\right)$$

and

$$v'_{OUT} = \frac{V_{REF}}{2^m}\left(\frac{b_m}{2} + \frac{b_{m+1}}{2^2} + \cdots + \frac{b_{m+k}}{2^{k-1}} + \frac{b_{m+k-1}}{2^k}\right) = V_{REF}\left(\frac{b_m}{2^{m+1}} + \frac{b_{m+1}}{2^{m+2}} + \cdots + \frac{b_{m+k}}{2^{m+k-1}} + \frac{b_{m+k-1}}{2^{m+k}}\right)$$

Adding V'_{REF} and v'_{OUT} gives the DAC output voltage as

$$v_{OUT} = V'_{REF} + v'_{OUT} = V_{REF}\left(\frac{b_0}{2^1}+\frac{b_1}{2^2}+\cdots+\frac{b_{m-2}}{2^{m-1}}+\frac{b_{m-1}}{2^m}+\frac{b_m}{2^{m+1}}+\frac{b_{m+1}}{2^{m+2}}+\cdots+\frac{b_{m+k}}{2^{m+k-1}}+\frac{b_{m+k-1}}{2^{m+k}}\right)$$

which is equivalent to an $m+k$ bit DAC.

Charge Scaling *MSB* SubDAC and Voltage Scaling *LSB* SubDAC

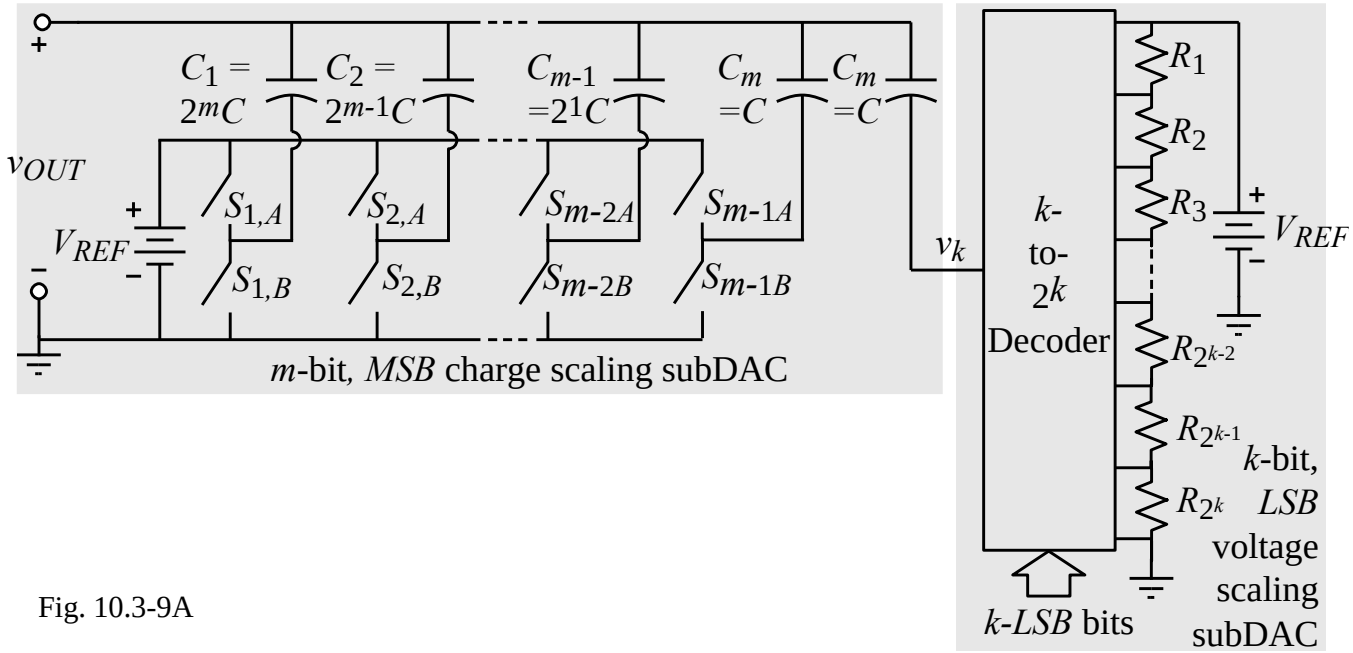


Fig. 10.3-9A

$$v_{OUT} = \left(\frac{b_0}{2^1}+\frac{b_1}{2^2}+\cdots+\frac{b_{m-2}}{2^{m-1}}+\frac{b_{m-1}}{2^m}\right)V_{REF}+\frac{v_k}{2^m} \quad \text{where} \quad v_k = \left(\frac{b_m}{2^1}+\frac{b_{m+1}}{2^2}+\cdots+\frac{b_{m+k}}{2^{k-1}}+\frac{b_{m+k-1}}{2^k}\right)V_{REF}$$

$$\therefore \quad v_{OUT} = \left(\frac{b_0}{2^1}+\frac{b_1}{2^2}+\cdots+\frac{b_{m-2}}{2^{m-1}}+\frac{b_{m-1}}{2^m}+\frac{b_m}{2^{m+1}}+\frac{b_{m+1}}{2^{m+2}}+\cdots+\frac{b_{m+k}}{2^{m+k-1}}+\frac{b_{m+k-1}}{2^{m+k}}\right)V_{REF}$$

Attributes:

- *MSBs* have good accuracy
- *LSBs* are monotonic, have poor accuracy - require trimming for good accuracy

Tradeoffs in SubDAC Selection to Enhance Linearity Performance

Assume a *m*-bit *MSB* subDAC and a *k*-bit *LSB* subDAC.

MSB Voltage Scaling SubDAC and *LSB* Charge Scaling SubDAC ($n = m+k$)

INL and *DNL* of the *m*-bit *MSB* voltage-scaling subDAC:

$$INL(R) = 2^{m-1}\left(\frac{2^n}{2^m}\right)\frac{\Delta R}{R} = 2^{n-1}\frac{\Delta R}{R}\,LSBs \quad \text{and} \quad DNL(R) = \frac{\pm\Delta R}{R}\left(\frac{2^n}{2^m}\right) = 2^k\frac{\pm\Delta R}{R}\,LSBs$$

INL and *DNL* of the *k*-bit *LSB* charge-scaling subDAC:

$$INL(C) = 2^{k-1}\frac{\Delta C}{C}\,LSBs \quad \text{and} \quad DNL(C) = (2^k-1)\frac{\Delta C}{C}\,LSBs$$

Combining these relationships:

$$\boxed{INL = INL(R) + INL(C) = \left(2^{n-1}\frac{\Delta R}{R} + 2^{k-1}\frac{\Delta C}{C}\right)LSBs}$$

and

$$\boxed{DNL = DNL(R) + DNL(C) = \left(2^k\frac{\Delta R}{R} + (2^k-1)\frac{\Delta C}{C}\right)LSBs}$$

MSB Charge Scaling SubDAC and *LSB* Voltage Scaling SubDAC

$$\boxed{INL = INL(R) + INL(C) = \left(2^{k-1}\frac{\Delta R}{R} + 2^{n-1}\frac{\Delta C}{C}\right)LSBs}$$

and

$$\boxed{DNL = DNL(R) + DNL(C) = \left(\frac{\Delta R}{R} + (2^n-1)\frac{\Delta C}{C}\right)LSBs}$$

Example 35-4 – DAC with Voltage Scaling for *MBSs* and Charge Scaling for *LSBs*

Consider a 12-bit DAC that uses voltage scaling for the *MSBs* charge scaling for the *LSBs*. To minimize the capacitor element spread and the number of resistors, choose m = 5 and k = 7. Find the tolerances necessary for the resistors and capacitors to give an *INL* and *DNL* equal to or less than 2 *LSB* and 1 *LSB*, respectively.

Solution

Substituting n = 12 and k = 7 into the previous equations gives

$$2 = 2^{11}\frac{\Delta R}{R} + 2^{6}\frac{\Delta C}{C} \quad \text{and} \quad 1 = 2^{7}\frac{\Delta R}{R} + (2^{7}\text{-}1)\frac{\Delta C}{C}$$

Solving these two equations simultaneously gives

$$\frac{\Delta C}{C} = \frac{2^{4}\text{-}2}{2^{11} - 2^{6} - 2^{4}} = 0.0071 \rightarrow \frac{\Delta C}{C} = 0.71\%$$

$$\frac{\Delta R}{R} = \frac{2^{8} - 2^{6} - 2}{2^{18} - 2^{13} - 2^{11}} = 0.0008 \rightarrow \frac{\Delta R}{R} = 0.075\%$$

We see that the capacitor tolerance will be easy to meet but that the resistor tolerance will require resistor trimming to meet the 0.075% requirement. Because of the 2^{n-1} multiplying $\Delta R/R$ in the relationship, we are stuck with approximately 0.075%.

Therefore, choose m = 2 (which makes the 0.075% easier to achieve) and let k = 10 which gives $\Delta R/R$ = 0.083% and $\Delta C/C$ = 0.12%.

Example 35-5 - DAC with Charge Scaling for *MBSs* and Voltage Scaling for *LSBs*

Consider a 12-bit DAC that uses charge scaling for the *MSBs* voltage scaling for the *LSBs*. To minimize the capacitor element spread and the number of resistors, choose m = 7 and k = 5. Find the tolerances necessary for the resistors and capacitors to give an *INL* and *DNL* equal to or less than 2 *LSB* and 1 *LSB*, respectively.

Solution

Substituting the values of this example into the relationships developed on a previous slide, we get

$$2 = 2^4 \frac{\Delta R}{R} + 2^{11} \frac{\Delta C}{C} \quad \text{and} \quad 1 = \frac{\Delta R}{R} + (2^{12}\text{-}1) \frac{\Delta C}{C}$$

Solving these two equations simultaneously gives

$$\frac{\Delta C}{C} = \frac{2^4\text{-}2}{2^{16}\text{-}2^{11}\text{-}2^4} = 0.000221 \rightarrow \frac{\Delta C}{C} = 0.0221\% \quad \text{and} \quad \frac{\Delta R}{R} \approx \frac{3}{2^5\text{-}1} = 0.0968 \rightarrow \frac{\Delta R}{R} = 9.68\%$$

For this example, the resistor tolerance is easy to meet but the capacitor tolerance will be difficult. To achieve accurate capacitor tolerances, we should decrease the value of m and increase the value of k to achieve a smaller capacitor value spread and thereby enhance the tolerance of the capacitors. If we choose m = 4 and k = 8, the capacitor tolerance is 0.049% and the resistor tolerance becomes 0.79% which is still reasonable. The largest to smallest capacitor ratio is 8 rather than 64 which helps to meet the capacitor tolerance requirements.

Example 35-5 – Continued

Based on the previous slide, we need to minimize the number of MSB bits as capacitors to enhance the accuracy. This puts pressure on the resistors. A good compromise is:

MSB subdac: 2 bits capacitive scaling.

LSB subdac: A 10 bit, R-2R ladder.

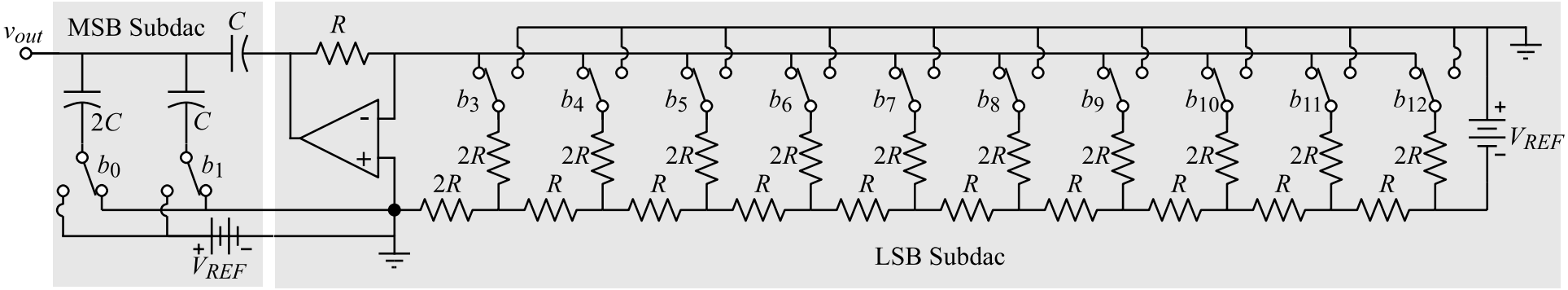
With this design, the tolerances become,

$$2 = 2^9 \frac{\Delta R}{R} + 2^{11} \frac{\Delta C}{C} \qquad \text{and} \qquad 1 = \frac{\Delta R}{R} + (2^{12}\text{-}1) \frac{\Delta C}{C}$$

giving,

$$\frac{\Delta C}{C} = \frac{1\text{-}2^{-8}}{2^{12}\text{-}1\text{-}2^{-3}} = 0.000243 \rightarrow \frac{\Delta C}{C} = 0.0243\% \text{ and } \frac{\Delta R}{R} \approx 1 - (2^{12}\text{-}1)\frac{\Delta C}{C} = 0.00388 \rightarrow \frac{\Delta R}{R} = 0.388\%$$

Possible realization:



SERIAL DIGITAL-ANALOG CONVERTERS

Serial DACs

- Typically require one clock pulse to convert one bit
- Types considered here are:
  Charge-redistribution
  Algorithmic

Charge Redistribution DAC

Implementation:

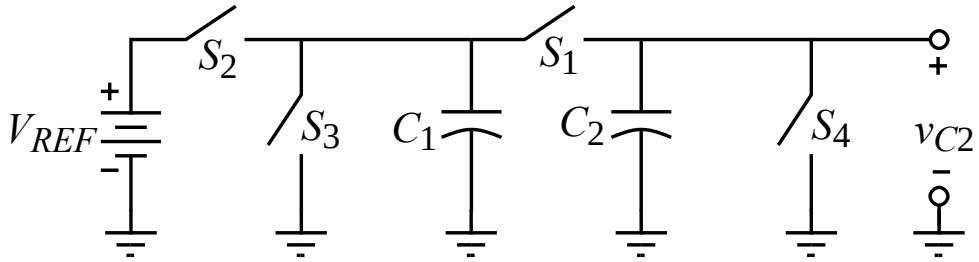


Fig. 10.4-1

Operation:

Switch S_1 is the redistribution switch that parallels C_1 and C_2 sharing their charge

Switch S_2 precharges C_1 to V_{REF} if the ith bit, b_i, is a 1

Switch S_3 discharges C_1 to zero if the ith bit, b_i, is a 0

Switch S_4 is used at the beginning of the conversion process to initially discharge C_2

Conversion always begins with the *LSB* bit and goes to the *MSB* bit.

Example 35-6 - Operation of the Serial, Charge Redistribution DAC

Assume that $C_1 = C_2$ and that the digital word to be converted is given as $b_0 = 1$, $b_1 = 1$, $b_2 = 0$, and $b_3 = 1$. Follow through the sequence of events that result in the conversion of this digital input word.

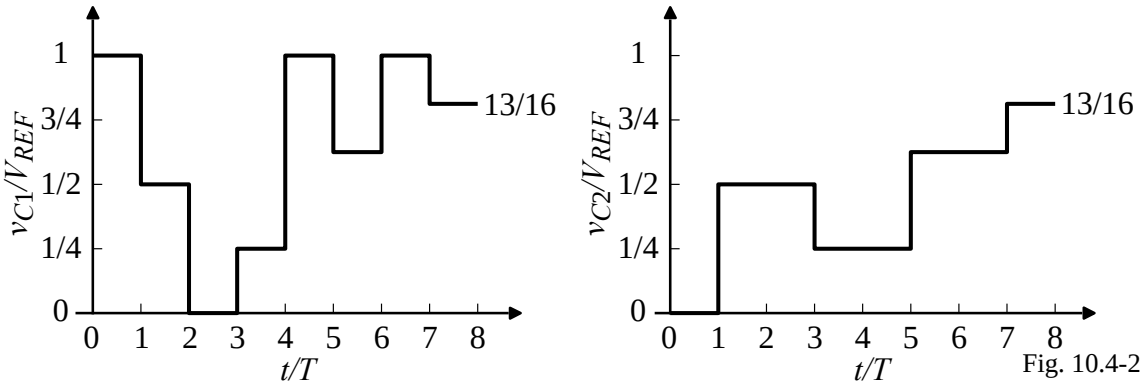


Fig. 10.4-2

Solution

1.) S_4 closes setting $v_{C2} = 0$.

2.) $b_3 = 1$, closes switch S_2 causing $v_{C1} = V_{REF}$.

3.) Switch S_1 is closed causing $v_{C1} = v_{C2} = 0.5V_{REF}$.

4.) $b_2 = 0$, closes switch S_3, causing $v_{C1} = 0$V.

5.) S_1 closes, the voltage across both C_1 and C_2 is $0.25V_{REF}$.

6.) $b_1 = 1$, closes switch S_2 causing $v_{C1} = V_{REF}$.

7.) S_1 closes, the voltage across both C_1 and C_2 is $(1+0.25)/2V_{REF} = 0.625V_{REF}$.

8.) $b_0 = 1$, closes switch S_2 causing $v_{C1} = V_{REF}$.

9.) S_1 closes, the voltage across both C_1 and C_2 is $(0.625+1)/2V_{REF} = 0.8125V_{REF} = (13/16)V_{REF}$.

Pipeline DAC

The pipeline DAC is simply an extension of the sub-DACs concept to the limit where the bits converted by each sub-DAC is 1.

Implementation:

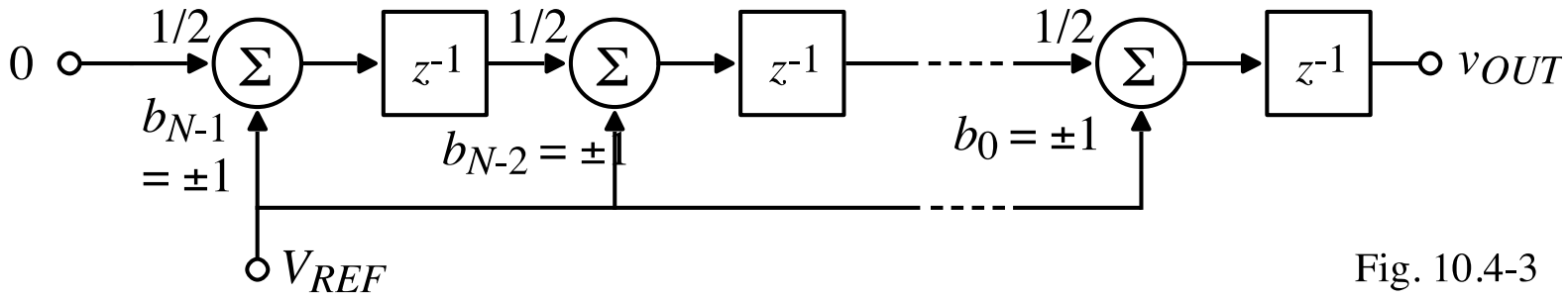


Fig. 10.4-3

$$V_{out}(z) = [b_0 z^{-1} + 2^{-1} b_1 z^{-2} + \cdots + 2^{-(N-2)} b_{N-2} z^{-(N-1)} + b_{N-1} z^{-N}] V_{REF}$$

where b_i is either ±1 if the ith bit is high or low. The z^{-1} blocks represent a delay of one clock period between the 1-bit sub-DACs.

Attributes:

- Takes N+1 clock cycles to convert the digital input to an analog output
- However, a new analog output is converted every clock after the initial N+1 clocks

Algorithmic (Iterative) DAC

Implementation:

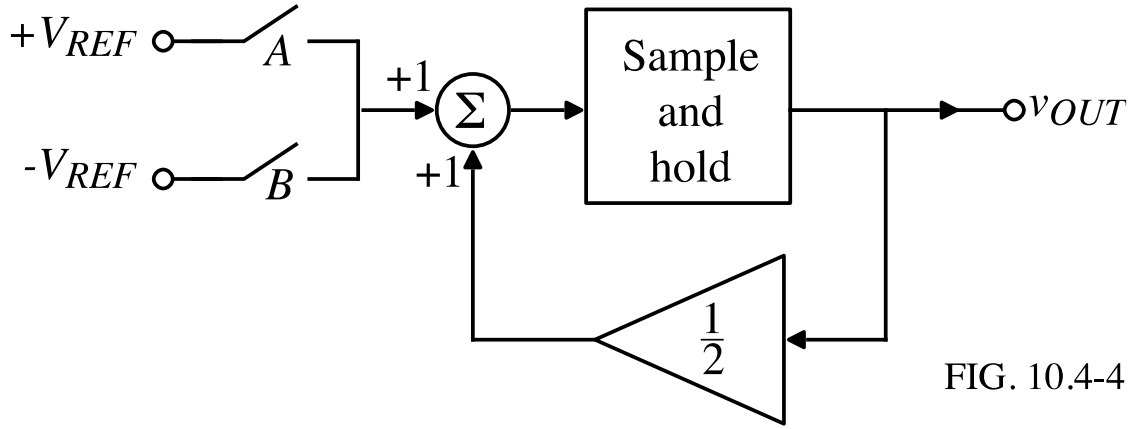


FIG. 10.4-4

Closed form of the previous series expression is,

$$V_{out}(z) = \frac{b_i z^{-1} V_{REF}}{1 - 0.5z^{-1}}$$

Operation:

Switch *A* is closed when the *i*th bit is 1 and switch *B* is closed when the *i*th bit is 0. Start with the *LSB* and work to the *MSB*.

Example 35-7 - Digital-Analog Conversion Using the Algorithmic Method

Assume that the digital word to be converted is 11001 in the order of *MSB* to *LSB*. Find the converted output voltage and sketch a plot of v_{OUT}/V_{REF} as a function of t/T, where T is the period for one conversion.

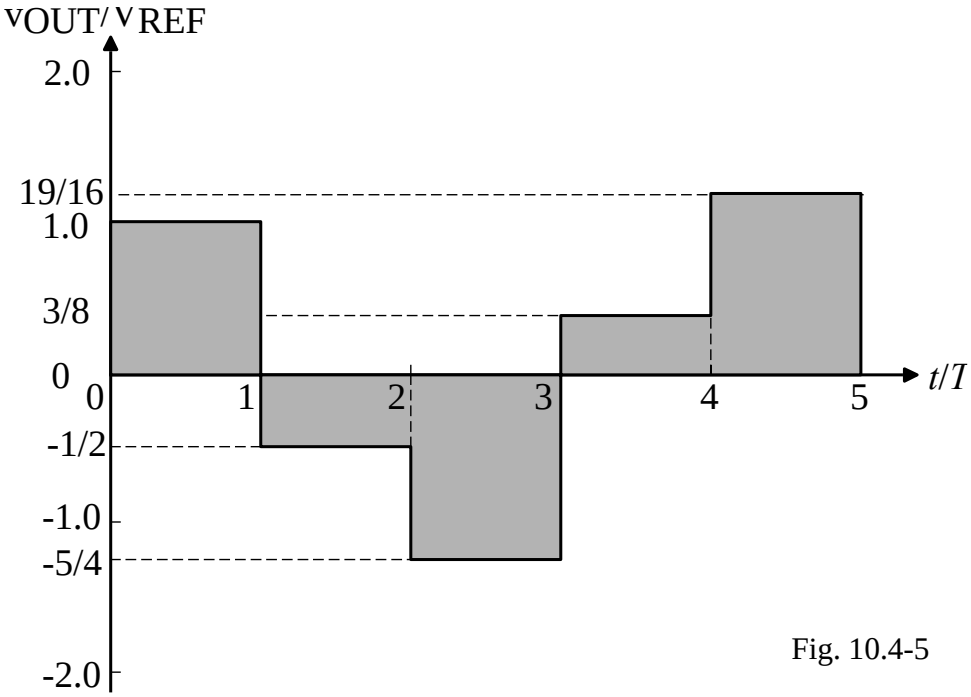


Fig. 10.4-5

Solution

1.)The conversion starts by zeroing the output (not shown on Fig. 10.4-4).

2.)The $LSB = 1$, switch A is closed and V_{REF} is summed with zero to give an output of $+V_{REF}$.

3.)The next $LSB = 0$, switch B is closed and $v_{OUT} = -V_{REF}+0.5V_{REF} = -0.5V_{REF}$.

4.)The next $LSB = 0$, switch B is closed and $v_{OUT} = -V_{REF}+0.5(-0.5V_{REF}) = -1.25V_{REF}$.

5.)The next $LSB = 1$, switch A is closed and $v_{OUT} = V_{REF}+0.5(-1.25V_{REF}) = 0.375V_{REF}$.

6.)The MSB = 1, switch *A* is closed and $v_{OUT} = V_{REF} + 0.5(0.375V_{REF}) = 1.1875V_{REF} = (19/16)V_{REF}$. (Note that because the actual V_{REF} of this example if $\pm V_{REF}$ or $2V_{REF}$, the analog value of the digital word 11001 is 19/32 times $2V_{REF}$ or $(19/16)V_{REF}$.)

SUMMARY

- Voltage scaling DACs are monotonic, use equal resistors but are sensitive to capacitve parasitics
- Charge scaling DACs are fast with good accuracy but have large element spread and are nonmonotonic
- DAC resolution can be increased by combining several subDACs with smaller resolution
- Methods of combining include scaling the output or the reference of the non-*MSB* subDACs
- SubDACs can use similar or different scaling methods
- Tradeoffs in the number of bits per subDAC and the type of subDAC allow minimization of the *INL* and *DNL*
- Serial, charge redistribution DAC is simple and requires minimum area but is slow and requires complex external circuitry
- Pipeline DAC has a latency of N+1 clock cycles but gives an analog output for each clock
- Serial, algorithmic DAC is simple and requires minimum area but is slow and requires complex external circuitry