# LECTURE 34 – CHARACTERIZATION OF DACS AND CURRENT AND VOLTAGE SCALING DACS

## LECTURE ORGANIZATION

**Outline**

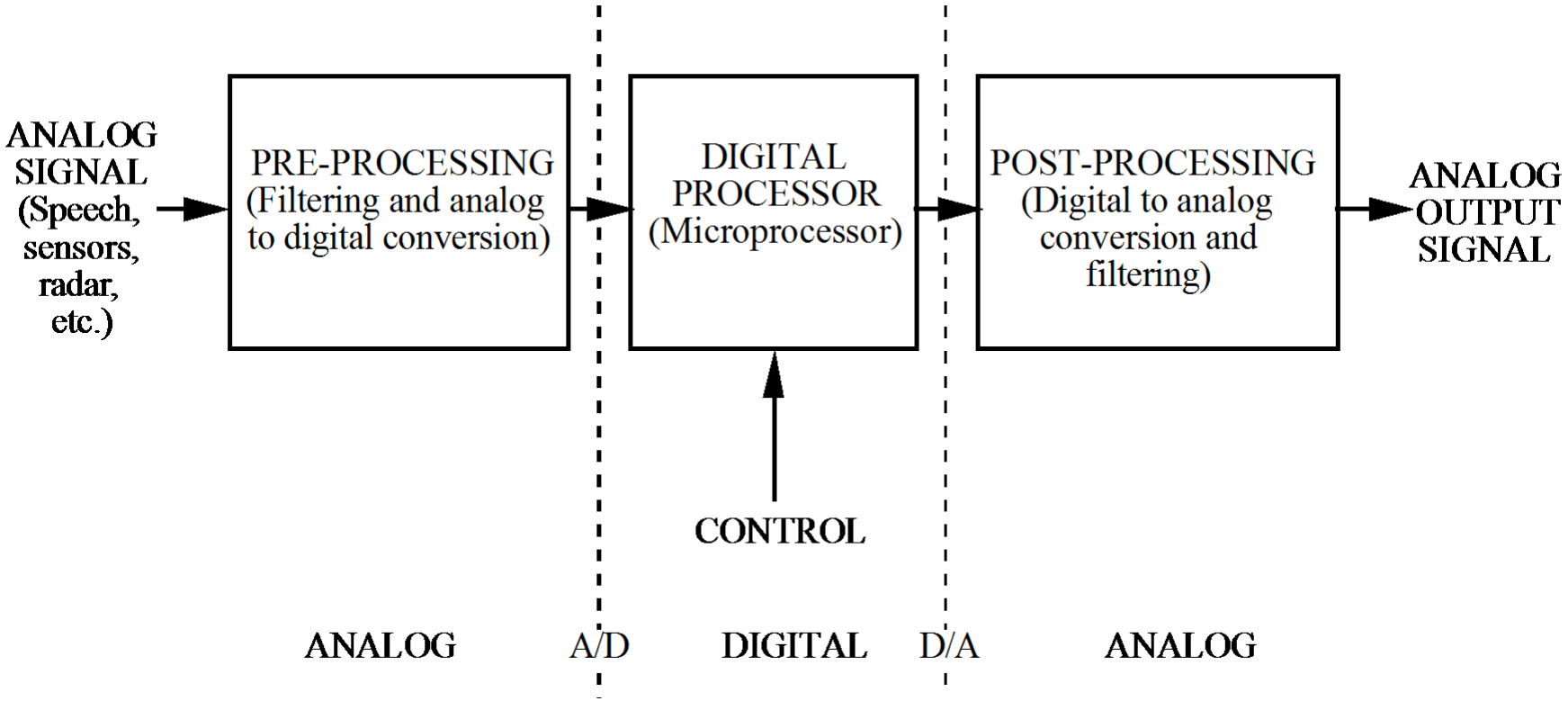
- Introduction
- Static characterization of DACs
- Dynamic characterization of DACs
- Testing of DACs
- Current scaling DACs
- Voltage scaling DACs
- Summary

***CMOS Analog Circuit Design*, 3rd Edition Reference**

Pages 499-517

# INTRODUCTION

## Importance of Data Converters in Signal Processing



# Digital-Analog Converters

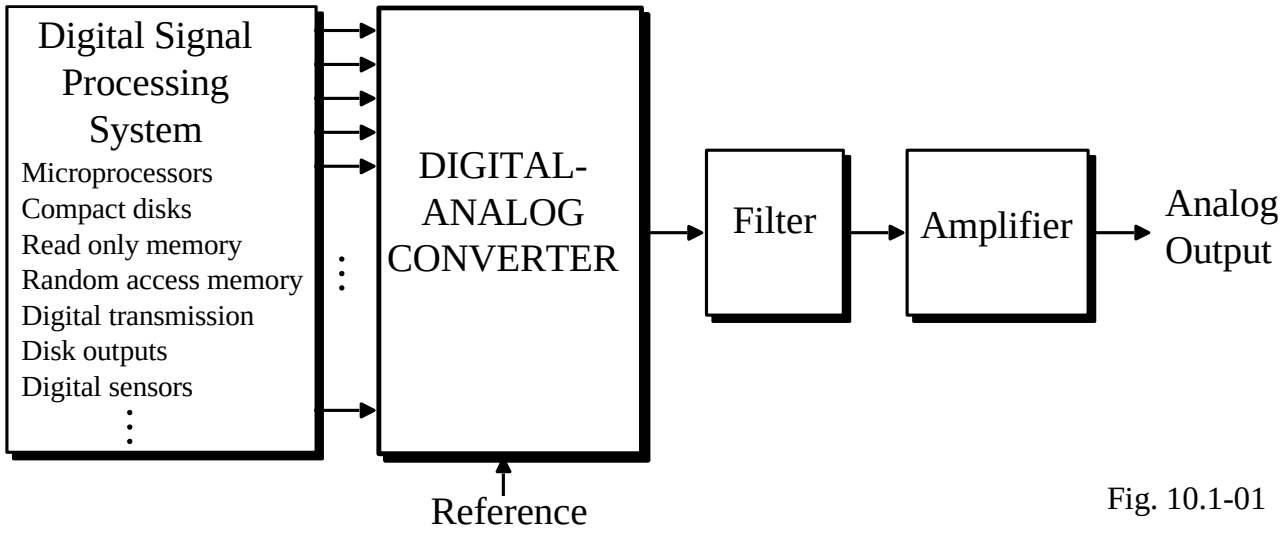
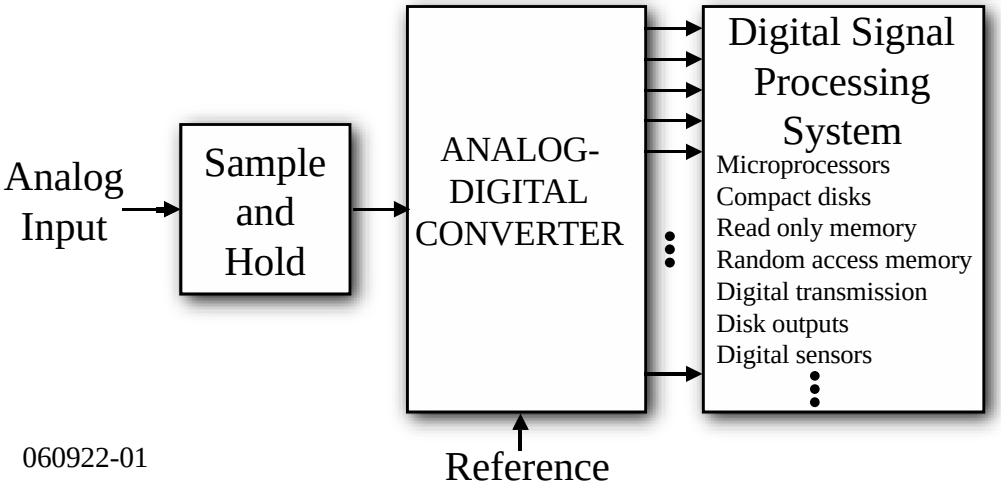



Fig. 10.1-01

Characteristics:

- Can be asynchronous or synchronous
- Primary active element is the op amp
- Conversion time can vary from fast (one clock period, $T$) to slow ($2^{\text{No. of bits}} * T$)

# Analog-Digital Converters

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Characteristics:

- Can only be synchronous (the analog signal is sampled and held during conversion)
- Primary active element is the comparator
- Conversion time can vary from fast (one clock period, $T$) to slow ($2^{\text{No. of bits}} * T$)

# STATIC CHARACTERISTICS OF DIGITAL-ANALOG CONVERTERS

## Block Diagram of a Digital-Analog Converter

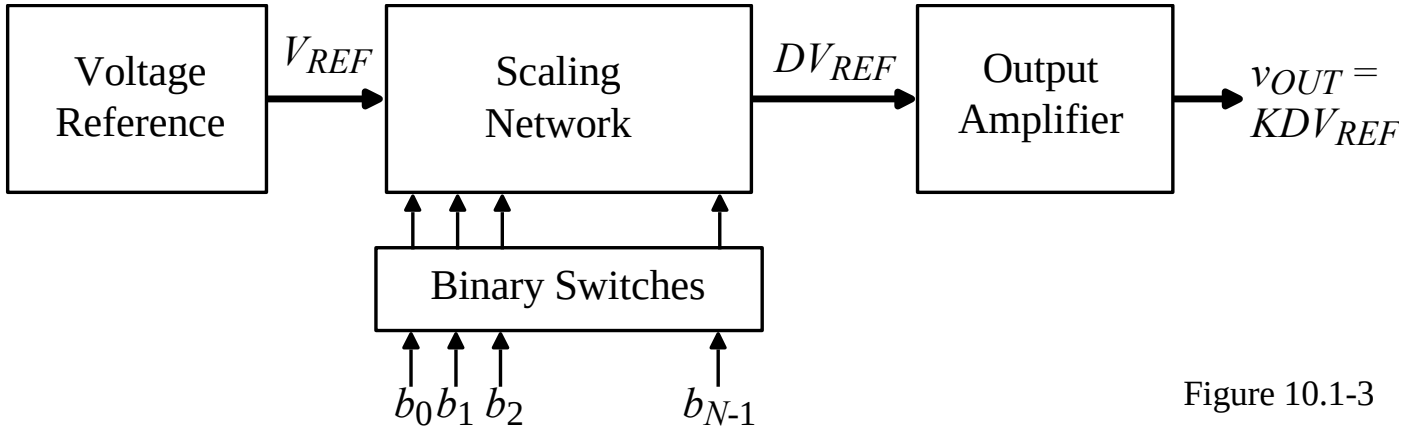



Figure 10.1-3

$b_0$ is the most significant bit (MSB)

The MSB is the bit that has the most (largest) influence on the analog output

$b_{N-1}$ is the least significant bit (LSB)

The LSB is the bit that has the least (smallest) influence on the analog output

# Input-Output Characteristics

Ideal input-output characteristics of a 3-bit DAC

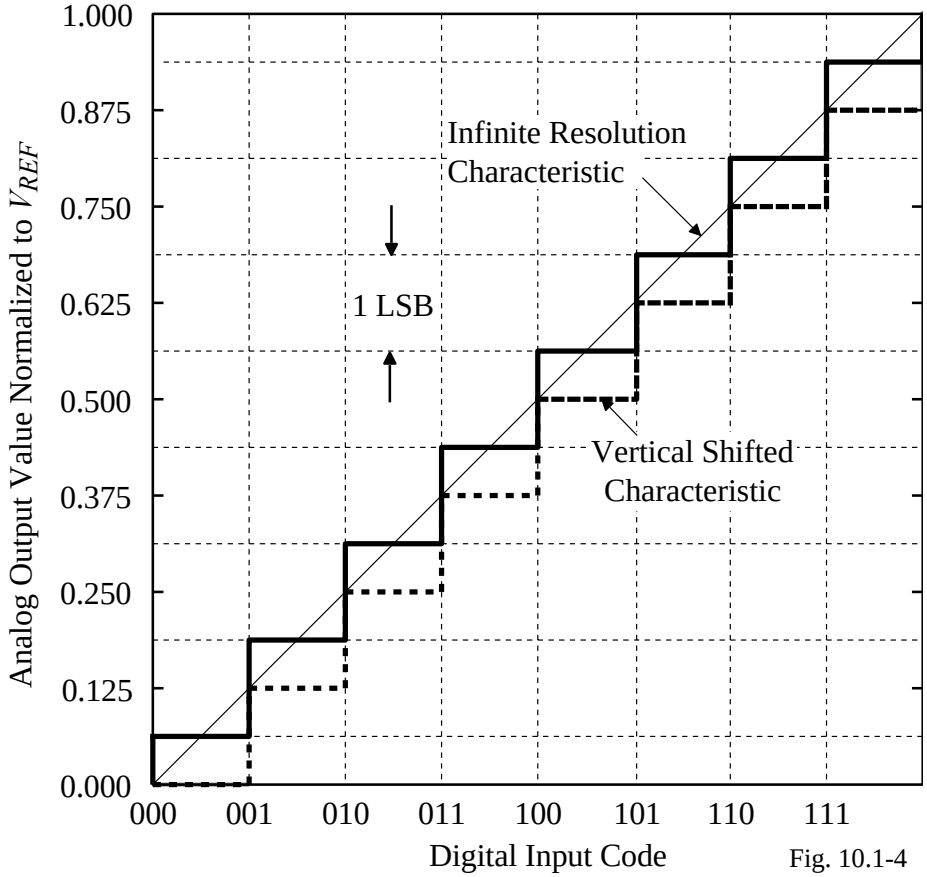



Fig. 10.1-4

## Definitions

- *Resolution* of the DAC is equal to the number of bits in the applied digital input word.
- *The full scale* (FS):

  FS = Analog output when all bits are 1 - Analog output all bits are 0

  $$FS = (V_{REF} - \frac{V_{REF}}{2^N}) - 0 = V_{REF}\left(1 - \frac{1}{2^N}\right)$$

- *Full scale range* (FSR) is defined as

  $$FSR = \lim_{N \to \infty}(FS) = V_{REF}$$

- *Quantization Noise* is the inherent uncertainty in digitizing an analog value with a finite resolution converter.

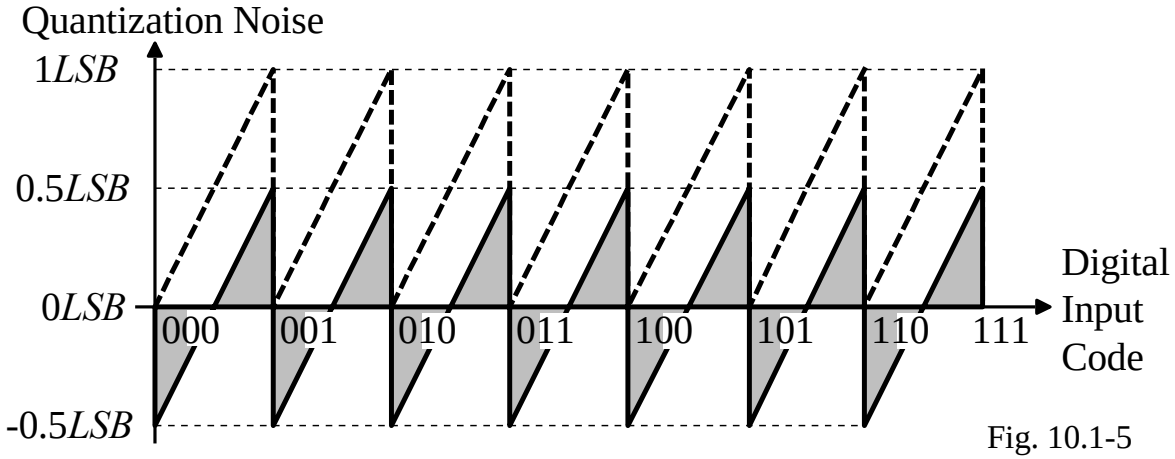



Fig. 10.1-5

## More Definitions

- *Dynamic Range* (*DR*) of a DAC is the ratio of the *FS*R to the smallest difference that can be resolved (i.e. an *LSB*)

$$DR = \frac{FSR}{LSB \text{ change}} = \frac{FSR}{(FSR/2^N)} = 2^N$$

or in terms of decibels

$$DR(\text{dB}) = 6.02N \text{ (dB)}$$

- *Signal-to-noise ratio* (*SNR*) for the DAC is the ratio of the full scale value to the *rms* value of the quantization noise.

$$rms(\text{quantization noise}) = \sqrt{\frac{1}{T}\int_0^T LSB^2\left(\frac{t}{T} - 0.5\right)^2 dt} = \frac{LSB}{\sqrt{12}} = \frac{FSR}{2^N\sqrt{12}}$$

$$\therefore \quad SNR = \frac{v_{OUT}(rms)}{(FSR/\sqrt{12}\ 2^N)}$$

- *Maximum SNR* ($SNR_{max}$) for a sinusoid is defined as

$$SNR_{max} = \frac{v_{OUT}max(rms)}{(FSR/\sqrt{12}\ 2^N)} = \frac{FSR/(2\sqrt{2})}{FSR/(\sqrt{12}\ 2^N)} = \frac{\sqrt{6}\ 2^N}{2}$$

or in terms of decibels

$$SNR_{max}(\text{dB}) = 20log_{10}\left(\frac{\sqrt{6}2^N}{2}\right) = 10\ log_{10}(6)+20\ log_{10}(2^N)-20\ log_{10}(2)= 1.76 + 6.02N \text{ dB}$$

## Even More Definitions

- *Effective number of bits (ENOB)* can be defined from the above as

$$ENOB = \frac{SNR_{Actual} - 1.76}{6.02}$$

where $SNR_{Actual}$ is the actual *SNR* of the converter.

Comment:

The *DR* is the amplitude range necessary to resolve *N* bits regardless of the amplitude of the output voltage.

However, when referenced to a given output analog signal amplitude, the *DR* required must include 1.76 dB more to account for the presence of quantization noise.

Thus, for a 10-bit DAC, the *DR* is 60.2 dB and for a full-scale, *rms* output voltage, the signal must be approximately 62 dB above whatever noise floor is present in the output of the DAC.

## Accuracy Requirements of the *i-th* Bit

- The output of the *i-th* bit of the converter is expressed as:

$$\text{The output of the } i\text{-th bit} = \frac{V_{REF}}{2^{i+1}}\left(\frac{2^n}{2^n}\right) = 2^{n-i-1}\ LSBs$$

- The uncertainty of each bit must be less than ±0.5 *LSB* (assuming all other bits are ideal. Must use ±0.25 *LSB* if each bit has a worst case error.)
- The accuracy of the *i-th* bit is equal to the uncertainty divided by the output giving:

$$\text{Accuracy of the } i\text{-th bit} = \frac{\pm 0.5\ LSB}{2^{n-i-1}\ LSB} = \frac{1}{2^{n-i}} = \frac{100}{2^{n-i}}\ \%$$

Result: The highest accuracy requirement is always the MSB ($i = 0$).

The LSB bit only needs ±50% accuracy.

Example:

What is the accuracy requirement for each of the bits of a 10 bit converter?

Assuming all other bits are ideal, the accuracy requirement per bit is given below.

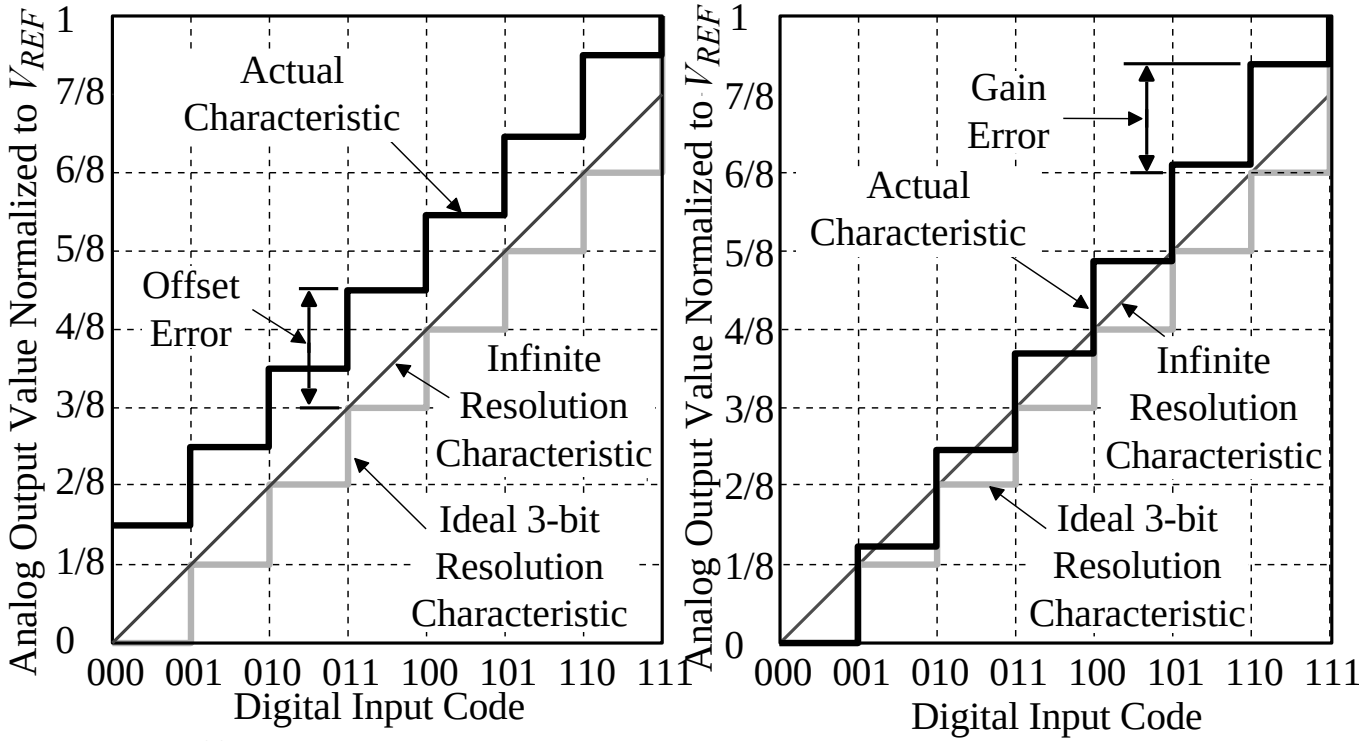
| Bit Number | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
|---|---|---|---|---|---|---|---|---|---|---|
| Accuracy % | 0.098 | 0.195 | 0.391 | 0.781 | 1.563 | 3.125 | 6.25 | 12.5 | 25 | 50 |

(If all other bits are worst case, the numbers above must be divided by 2.)

## Offset and Gain Errors

An *offset error* is a constant difference between the actual finite resolution characteristic and the ideal finite resolution characteristic measured at any vertical jump.

A *gain error* is the difference between the slope of the actual finite resolution and the ideal finite resolution characteristic measured at the right-most vertical jump.




Offset Error in a 3-bit DAC

Gain Error in a 3-bit DAC

Fig. 10.1-6

## Integral and Differential Nonlinearity

- *Integral Nonlinearity* (*INL*) is the maximum difference between the actual finite resolution characteristic and the ideal finite resolution characteristic measured vertically (% or *LSB*).
- *Differential Nonlinearity* (*DNL*) is a measure of the separation between adjacent levels measured at each vertical jump (% or *LSB*).

$$DNL = V_{cx} - V_S = \left(\frac{V_{cx} - V_S}{V_s}\right) V_S = \left(\frac{V_{cx}}{V_S} - 1\right) LSBs$$

where $V_{cx}$ is the actual voltage change on a bit-to-bit basis and $V_S$ is the ideal *LSB* change of ($V_{FSR}/2^N$)

Example of a 3-bit DAC:

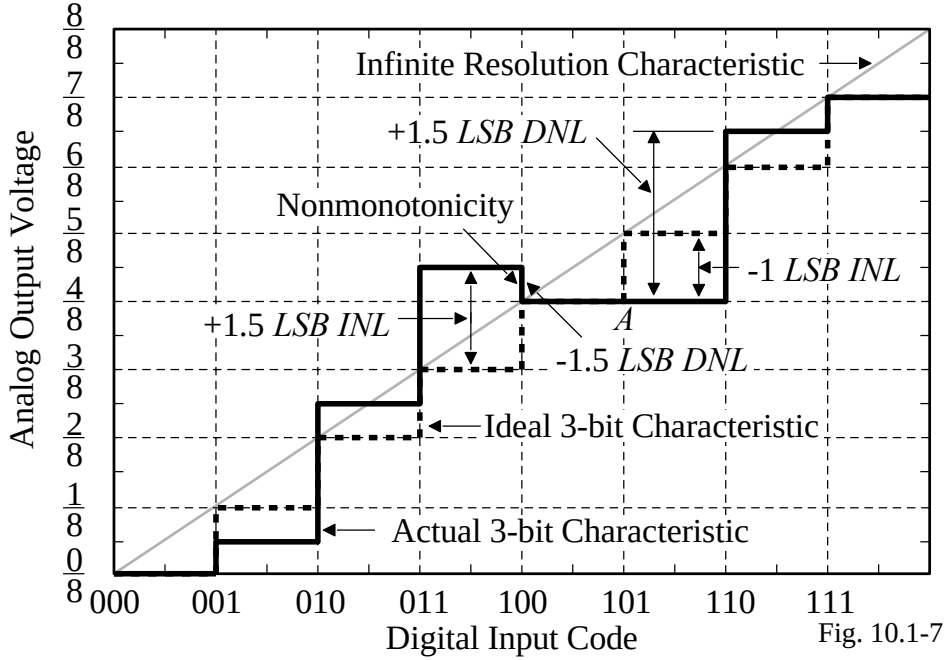



Fig. 10.1-7

# Example of INL and DNL of a Nonideal 4-Bit Dac

Find the ±*INL* and ±*DNL* for the 4-bit DAC shown.

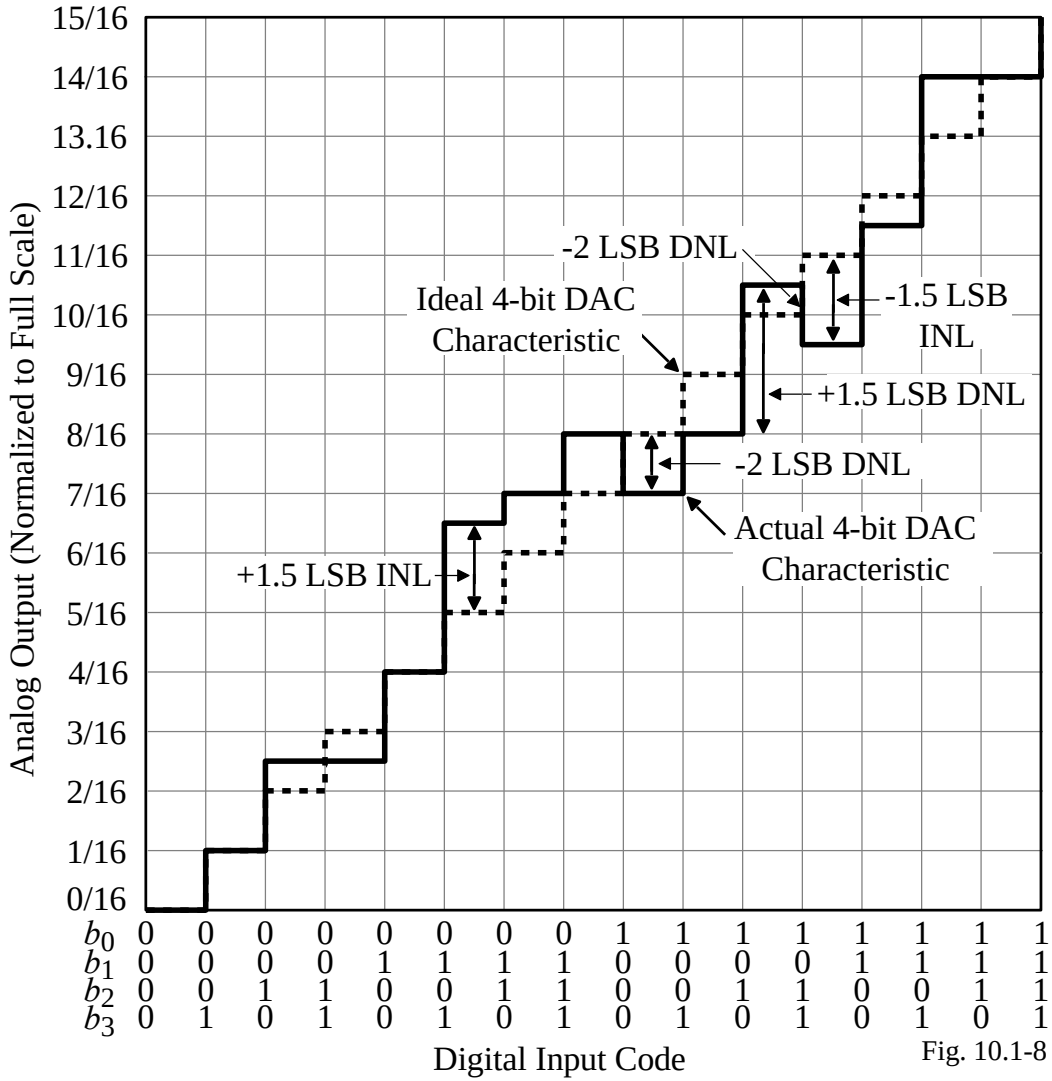



Fig. 10.1-8

# DYNAMIC CHARACTERISTICS OF DIGITAL-ANALOG CONVERTERS

Dynamic characteristics include the influence of time.

## Definitions

- *Conversion speed* is the time it takes for the DAC to provide an analog output when the digital input word is changed.

  Factor that influence the conversion speed:

  Parasitic capacitors (would like all nodes to be low impedance)

  Op amp gainbandwidth

  Op amp slew rate

- *Gain error* of an op amp is the difference between the desired and actual output voltage of the op amp (can have both a static and dynamic influence)

$$\text{Actual Gain} = \text{Ideal Gain} \times \left( \frac{\text{Loop Gain}}{1 + \text{Loop Gain}} \right)$$

$$\text{Gain error} = \frac{\text{Ideal Gain-Actual Gain}}{\text{Ideal Gain}} = \frac{1}{1+\text{Loop Gain}}$$

## Example 34-1 – Influence of Op Amp Gain Error on DAC Performance

Assume that a DAC using an op amp in the inverting configuration with $C_1 = C_2$ and $A_{vd}(0) = 1000$. Find the largest resolution of the DAC if $V_{REF}$ is 1V and assuming worst case conditions.

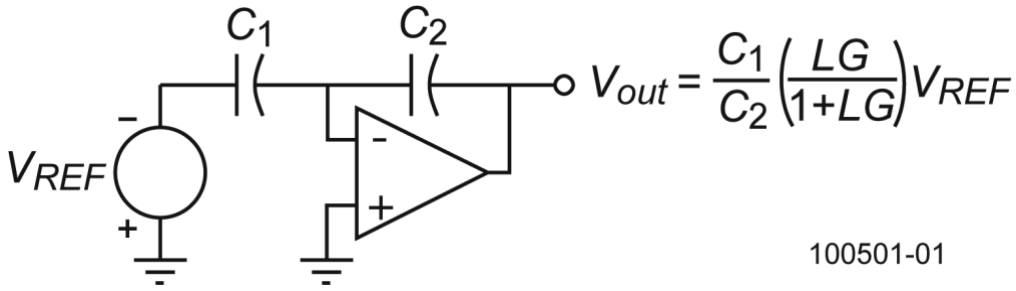
*Solution*

The loop gain of the inverting configuration is $LG = \frac{C_2}{C_1+C_2} A_{vd}(0) = 0.5 \cdot 1000 = 500.$

The gain error is therefore $1/501 \approx 0.002$. The gain error should be less than the quantization noise of $\pm 0.5LSB$ which is expressed as

$$Gain\ error\ x\ V_{REF} = \frac{V_{REF}}{501} \approx 0.002 V_{REF} \leq \frac{V_{REF}}{2^{N+1}}$$

Therefore the largest value of $N$ that satisfies this equation is $N = 7$.



## Influence of the Op Amp Gainbandwidth

Single-pole response:

$$v_{out}(t) = A_{CL}[1 - e^{-\omega_H t}]v_{in}(t)$$

where

$A_{CL}$ = closed-loop gain

$$\omega_H = GB\left(\frac{R_1}{R_1+R_2}\right) \text{ or } GB\left(\frac{C_2}{C_1+C_2}\right)$$

To avoid errors in DACs (and ADCs), $v_{out}(t)$ must be within $\pm 0.5LSB$ of the final value by the end of the conversion time.

Multiple-pole response:

Typically the response is underdamped like the following (see Appendix D of text).

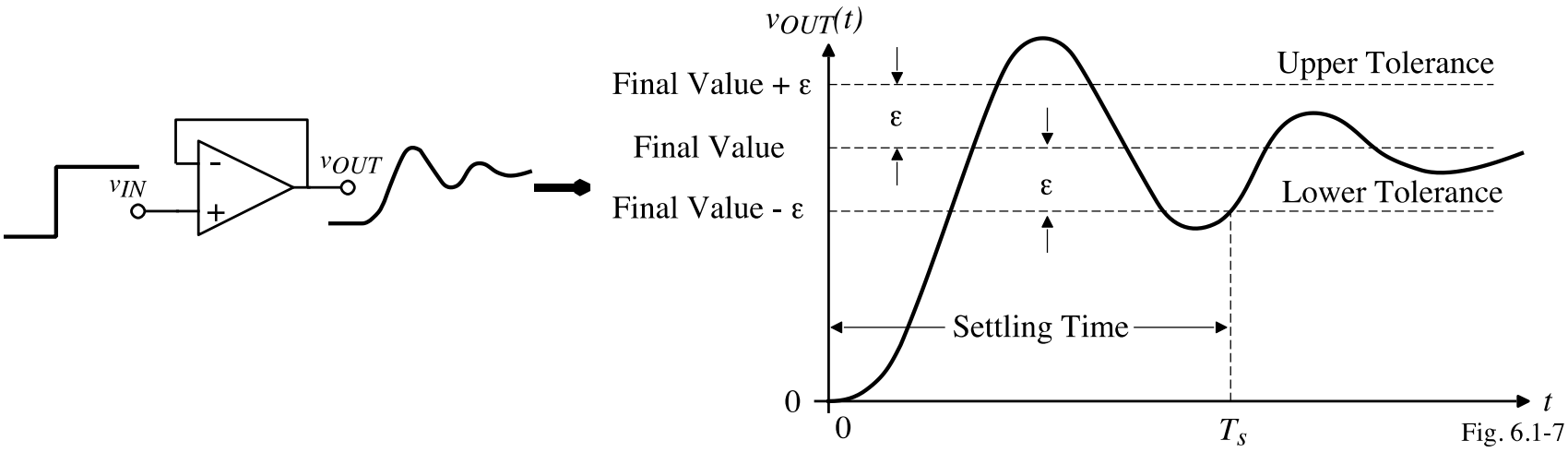



Fig. 6.1-7

## Example 34-2 – Influence of *GB* and Settling Time on DAC Performance

Assume that a DAC uses a switched capacitor noninverting amplifier with $C_1 = C_2$ using an op amp with a dominant pole and $GB$ = 1MHz. Find the conversion time of an 8-bit DAC if $V_{REF}$ is 1V.

*Solution*

From the results in Appendix E.2 of the text, we know that

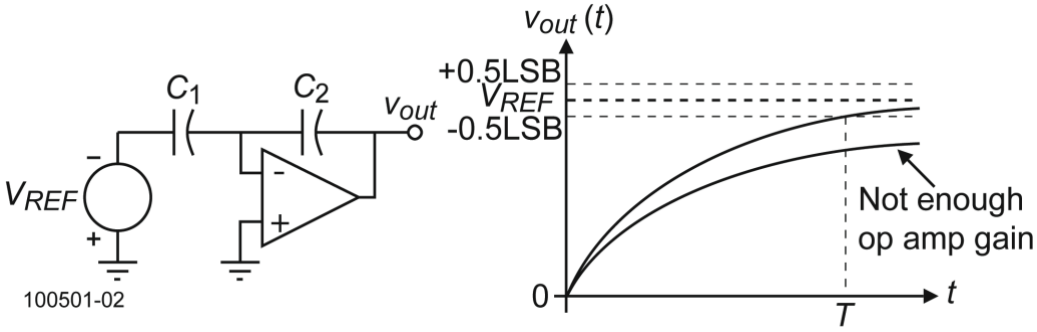
$$\omega_H = \left(\frac{C_2}{C_1+C_2}\right) GB \qquad = (2\pi)(0.5)(10^6) = 3.141\text{x}10^6$$

and $A_{CL} = 1$. Assume that the ideal output is equal to $V_{REF}$. Therefore the value of the output voltage which is 0.5LSB of $V_{REF}$ is

$$1 - \frac{1}{2^{N+1}} = 1 - e^{-\omega_H T}$$

or

$$2^{N+1} = e^{\omega_H T}$$




Solving for $T$ gives

$$T = \left(\frac{N+1}{\omega_H}\right) ln(2) = 0.693 \left(\frac{N+1}{\omega_H}\right) = \left(\frac{9}{3.141}\right) 0.693 = 1.986\mu s$$

# TESTING OF DACs

## Input-Output Test

Test setup:

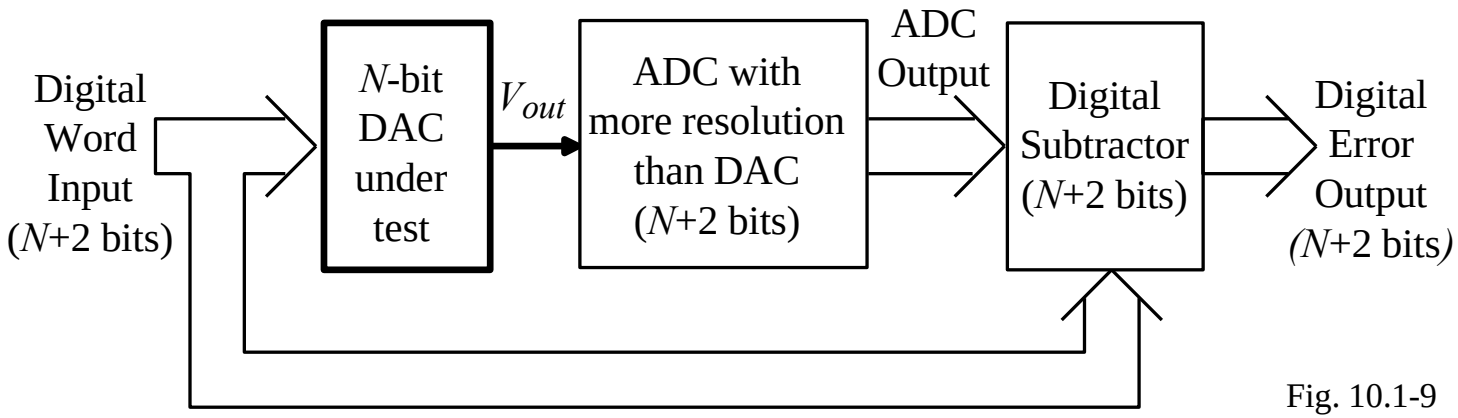



Fig. 10.1-9

Comments:

Sweep the digital input word from 000...0 to 111...1.

The ADC should have more resolution by at least 2 bits and be more accurate than the errors of the DAC

*INL* will show up in the output as the presence of 1's in any bit.

If there is a 1 in the Nth bit, the *INL* is greater than ±0.5*LSB*

*DNL* will show up as a change between each successive digital error output.

The bits which are greater than *N* in the digital error output can be used to resolve the errors to less than ±0.5*LSB*

## Spectral Test

Test setup:

Comments:

Digital input pattern is selected to have a fundamental frequency which has a magnitude of at least 6*N* dB above its harmonics.

Length of the digital sequence determines the spectral purity of the fundamental frequency.

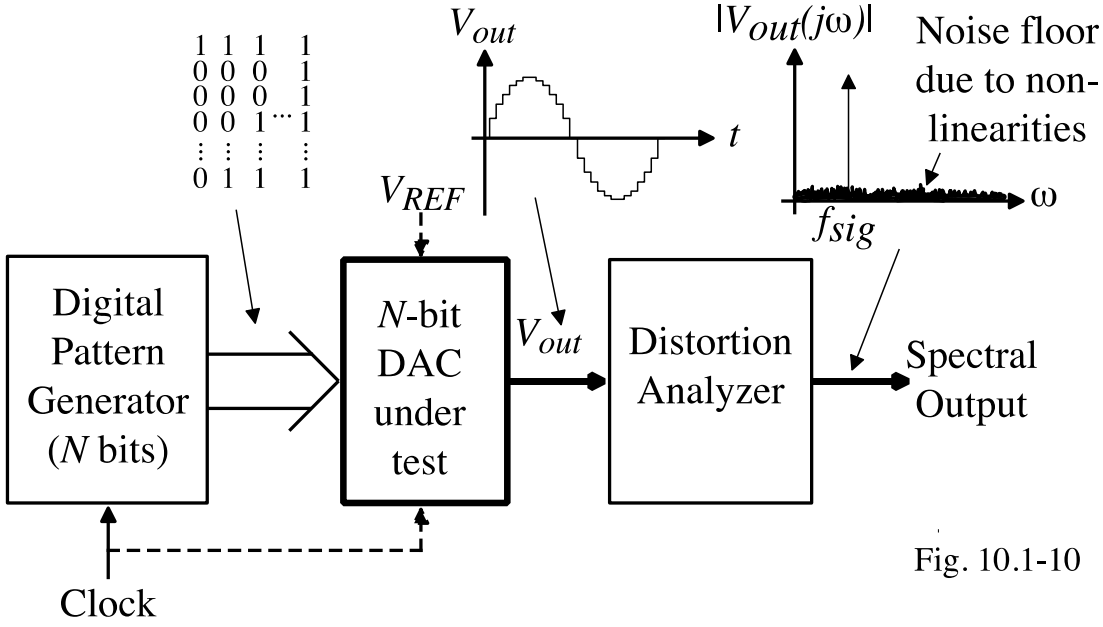



Fig. 10.1-10

All nonlinearities of the DAC (i.e. *INL* and *DNL*) will cause harmonics of the fundamental frequency

The THD can be used to determine the SNR dB range between the magnitude of the fundamental and the THD. This SNR should be at least 6*N* dB to have an *INL* of less than ±0.5*LSB* for an ENOB of *N*-bits.

Note that the noise contribution of $V_{REF}$ must be less than the noise floor due to nonlinearities.

If the period of the digital pattern is increased, the frequency dependence of *INL* can be measured.

# CURRENT SCALING DIGITAL-ANALOG CONVERTERS

## Classification of Digital-Analog Converters

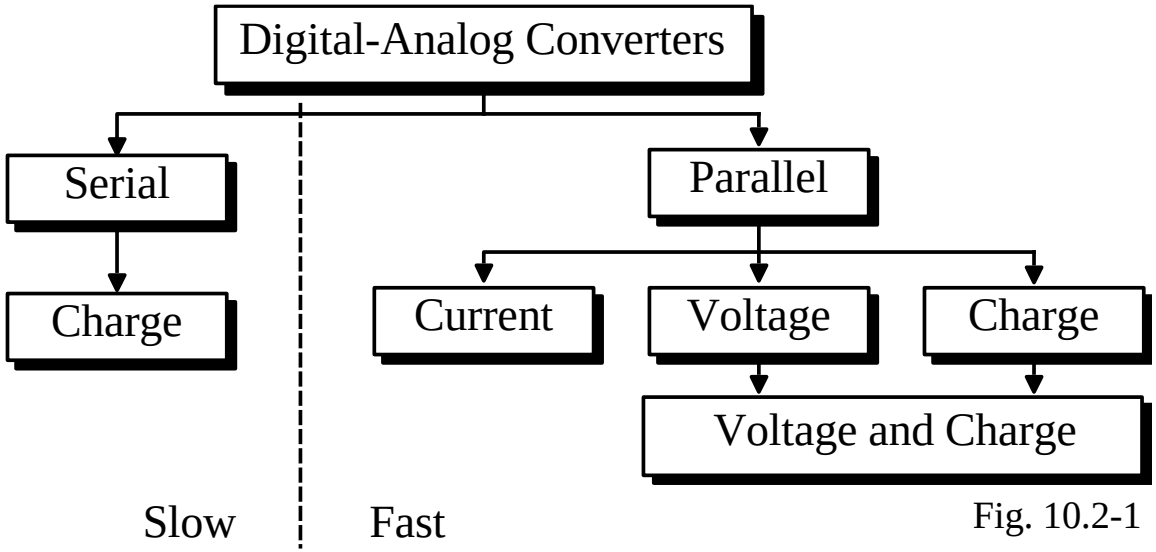



Fig. 10.2-1

# General Current Scaling DACs

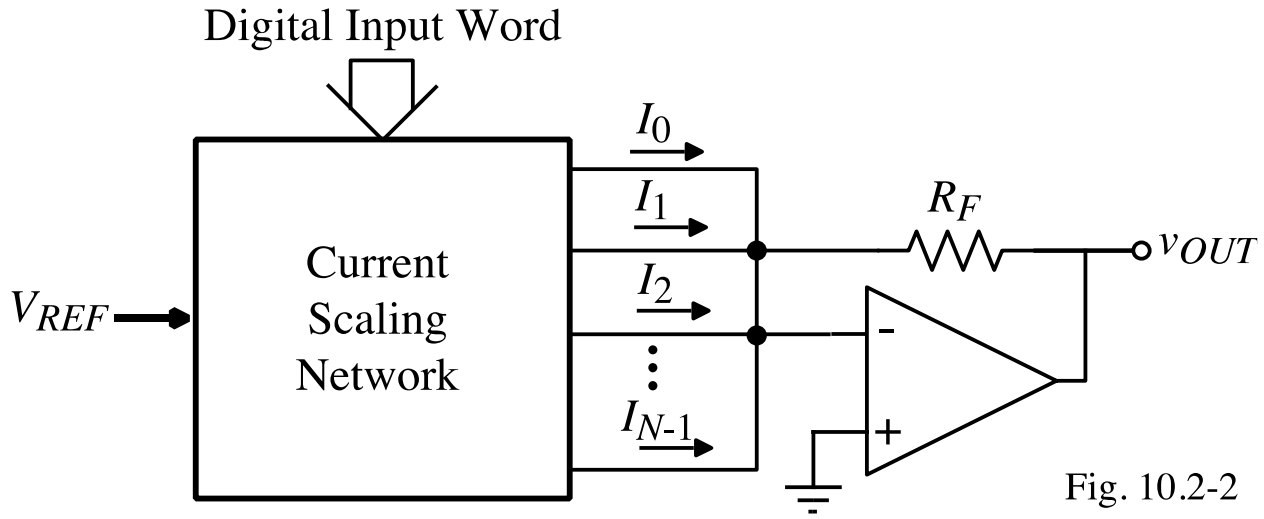



Fig. 10.2-2

The output voltage can be expressed as

$$V_{OUT} = -R_F(I_0 + I_1 + I_2 + \cdots + I_{N-1})$$

where the currents $I_0$, $I_1$, $I_2$, ... are binary weighted currents.

## Binary-Weighted Resistor DAC

Circuit:

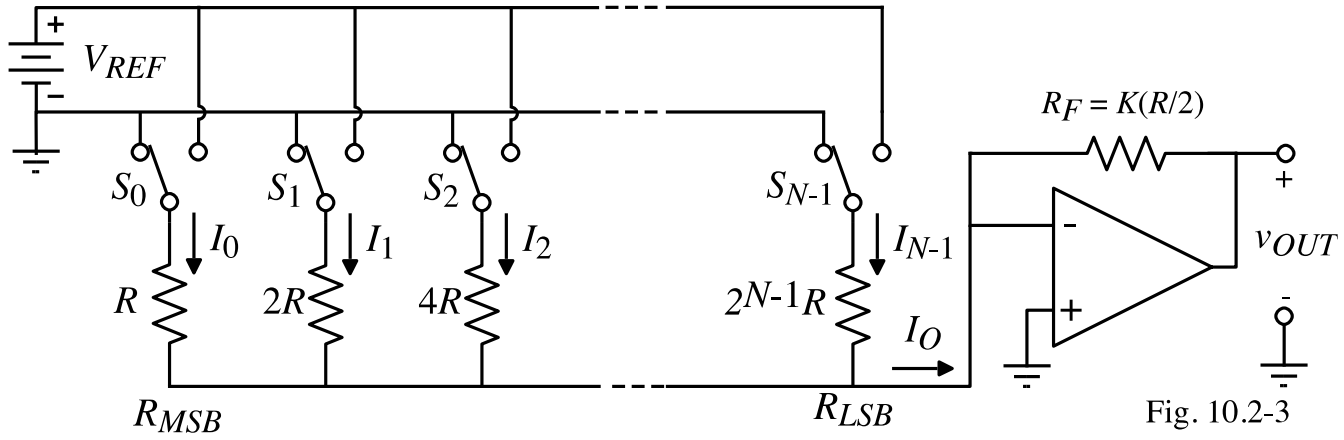



Fig. 10.2-3

Comments:

1.) $R_F$ can be used to scale the gain of the DAC. If $R_F = KR/2$, then

$$v_{OUT} = -R_F I_O = \frac{-KR}{2}\left(\frac{b_0}{R} + \frac{b_1}{2R} + \frac{b_2}{4R} + \cdots + \frac{b_{N-1}}{2^{N-1}R}\right)V_{REF}$$

$$\Rightarrow v_{OUT} = -K\left(\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \cdots + \frac{b_{N-1}}{2^N}\right)V_{REF}$$

where $b_i$ is 1 if switch $S_i$ is connected to $V_{REF}$ or 0 if switch $S_i$ is connected to ground.

2.) Component spread value $= \frac{R_{MSB}}{R_{LSB}} = \frac{R}{2^{N-1}R} = \frac{1}{2^{N-1}}$

3.) Attributes:

Insensitive to parasitics $\Rightarrow$ fast
Trimming required for large values of $N$

Large component spread value
Nonmonotonic

## R-2R Ladder Implementation of the Binary Weighted Resistor DAC

Use of the R-2R concept to avoid large element spreads:

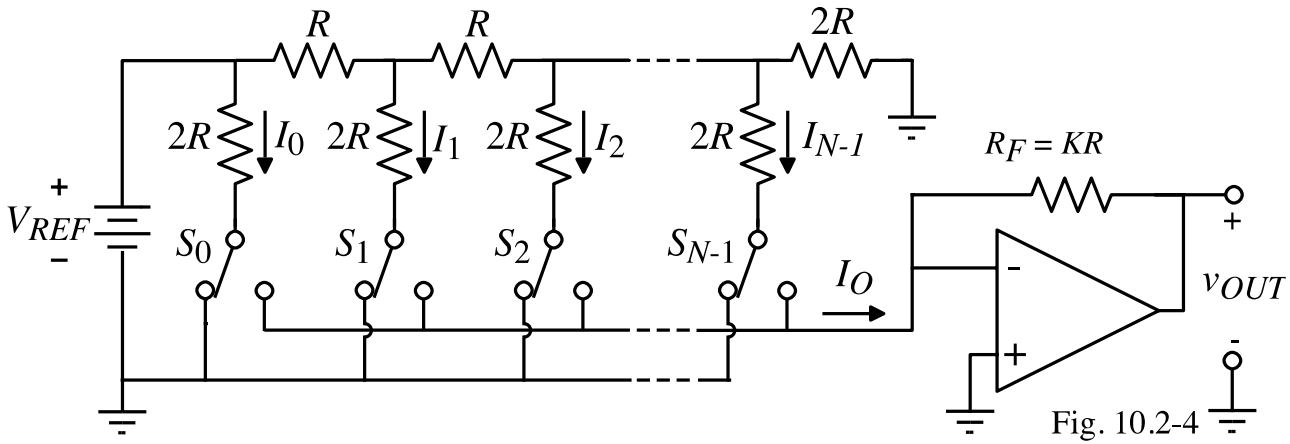



Fig. 10.2-4

How does the R-2R ladder work?

"The resistance seen to the right of any of the vertical 2*R* resistors is 2*R*."

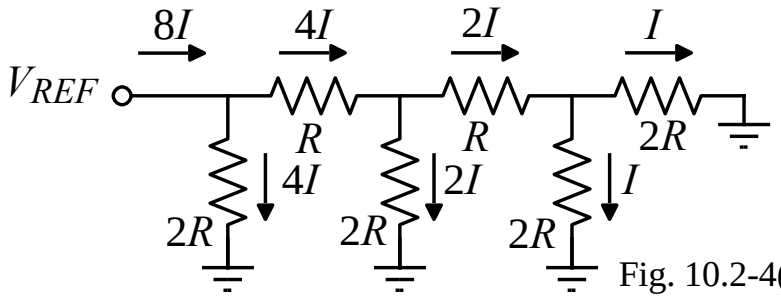



Fig. 10.2-4(2R-R)

Attributes:

- Not sensitive to parasitics
  (currents through the resistors never change as $S_i$ is varied)
- Small element spread. Resistors made from same unit (2*R* consist of two in series or *R* consists of two in parallel)
- Not monotonic

# Current Scaling Using Binary Weighted MOSFET Current Sinks

Circuit:

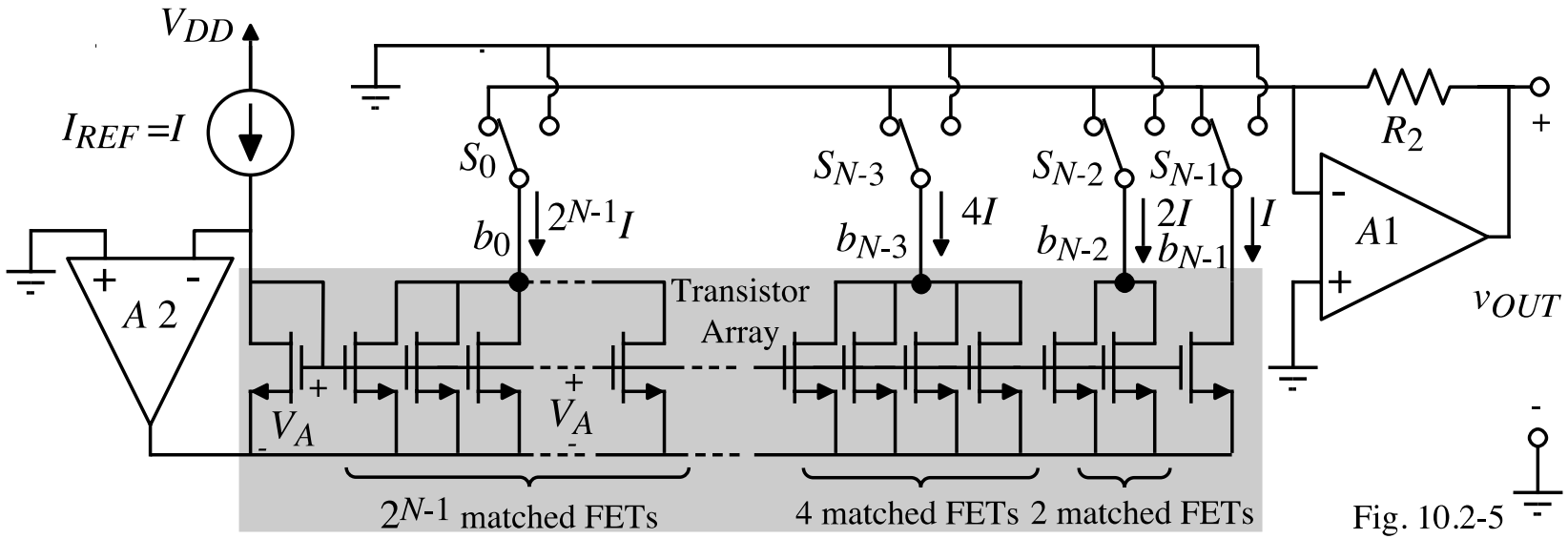



Fig. 10.2-5

Operation:

$$v_{OUT} = R_2(b_{N-1}\cdot I + b_{N-2}\cdot 2I + b_{N-3}\cdot 4I + \cdots + b_0\cdot 2^{N-1}\cdot I)$$

If $I = I_{REF} = \dfrac{V_{REF}}{2^N R_2}$, then $v_{OUT} = \left(\dfrac{b_0}{2} + \dfrac{b_1}{4} + \dfrac{b_2}{8} + \cdots + \dfrac{b_{N-3}}{2^{N-2}} + \dfrac{b_{N-2}}{2^{N-1}} + \dfrac{b_{N-1}}{2^N}\right)V_{REF}$

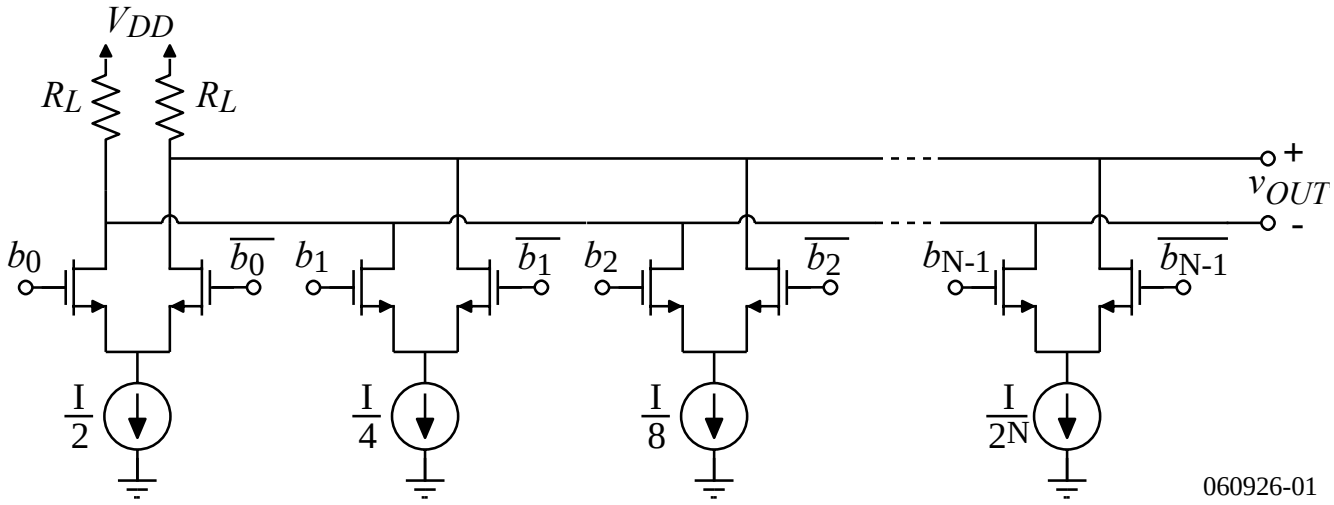
Attributes:

Fast (no floating nodes) and not monotonic

Accuracy of MSB greater than LSBs

## High-Speed Current DACs

Current scaling DAC using current switches:




$$v_{OUT} = IR_L\left[\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \cdots + + \frac{b_{N-1}}{2^N}\right]$$

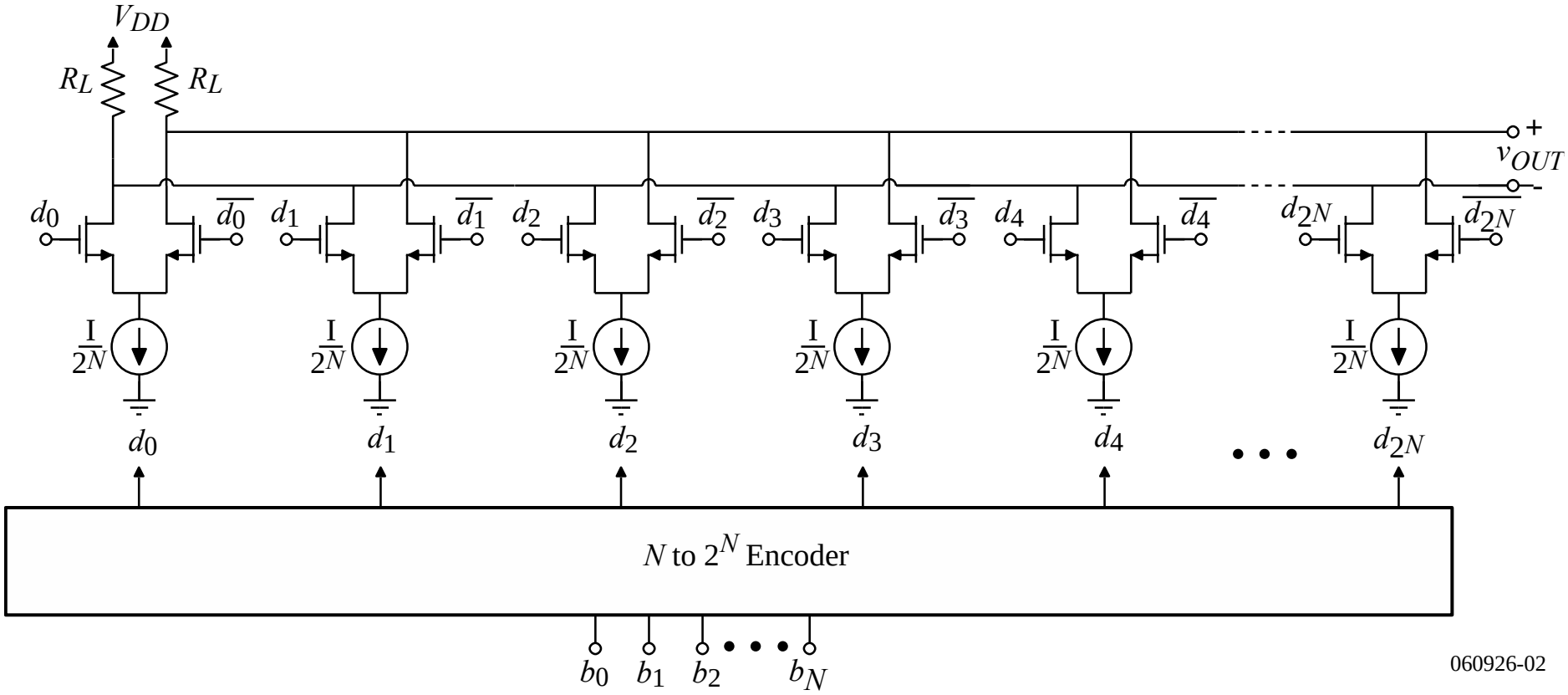
where

$$b_i = \begin{cases} +1 \text{ if the bit is 1} \\ \\ -1 \text{ if the bit is 0} \end{cases}$$

A single-ended DAC can be obtained by replacing the left $R_L$ by a short.

## High-Speed, High-Accuracy Current Scaling DACs

The accuracy is increased by using the same value of current for each switch as shown.




For a 4 bit DAC, there would be 16 current switches.

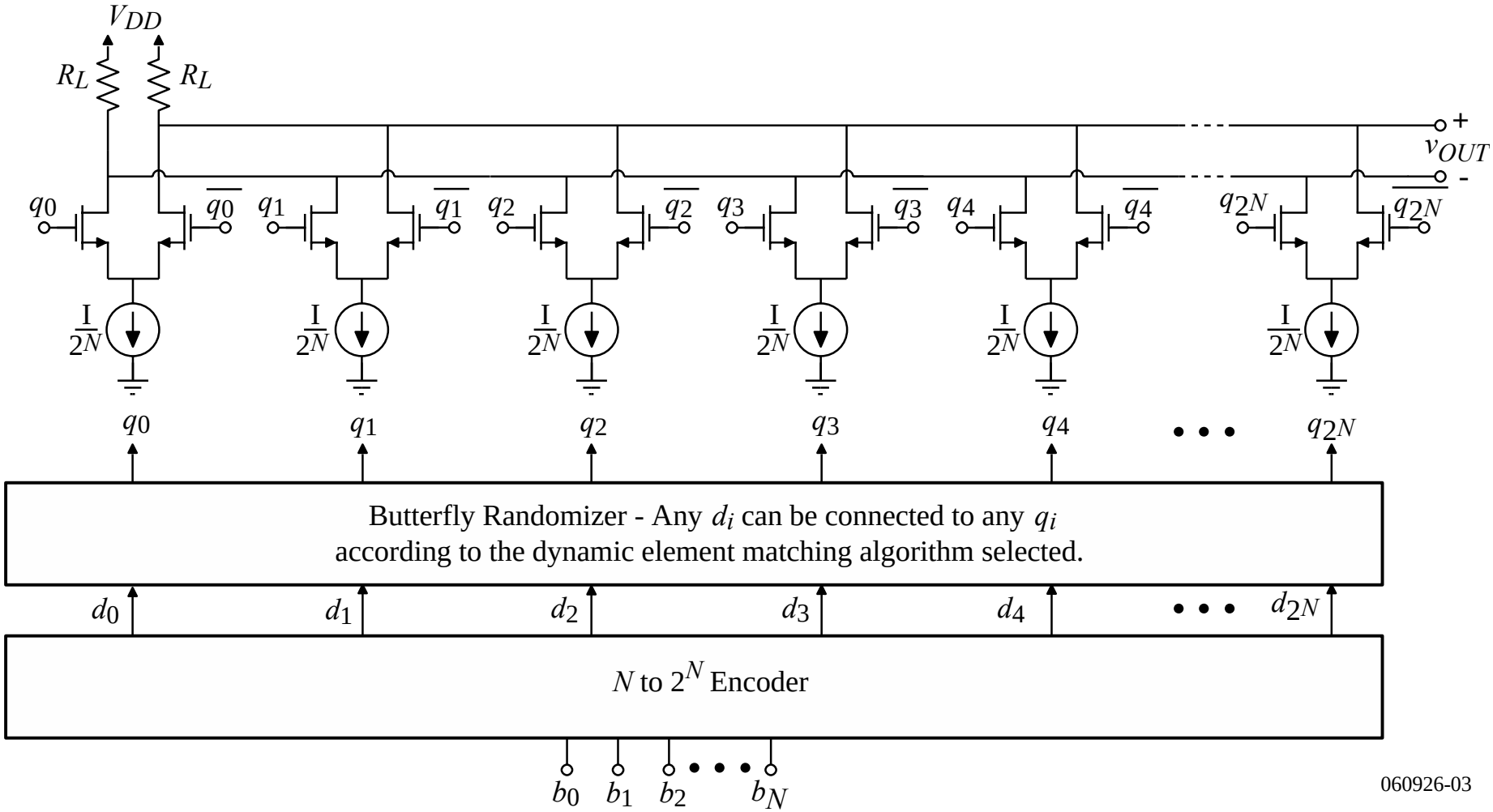
The MSB bit would switch 8 of the current switches to one side.

The next-MSB bit would switch 4 of the current switches to one side.

Etc.

# Increasing the Accuracy of the Current Switching DAC

The accuracy of the previous DAC can be increased by using dynamic element matching techniques. This is illustrated below where a butterfly switching element allows the switch control bits, $d_i$, to be "randomly" connected to any of the current switches.



# VOLTAGE SCALING DIGITAL-ANALOG CONVERTERS

## General Voltage Scaling Digital Analog Converter

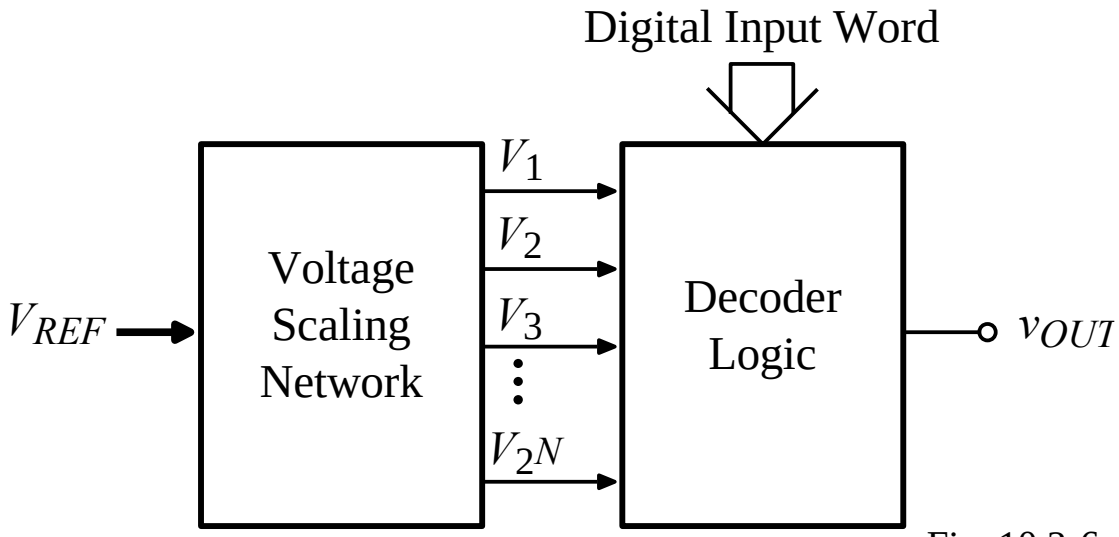



Fig. 10.2-6

Operation:

Creates all possible values of the analog output then uses a decoding network to determine which voltage to select based on the digital input word.

# 3-Bit Voltage Scaling Digital-Analog Converter

The voltage at any tap can be expressed as: $v_{OUT} = \frac{V_{REF}}{8}(n - 0.5) = \frac{V_{REF}}{16}(2n - 1)$

Attributes:

- Guaranteed monotonic
- Compatible with CMOS technology
- Large area if $N$ is large
- Sensitive to parasitics
- Requires a buffer
- Large current can flow through the resistor string.

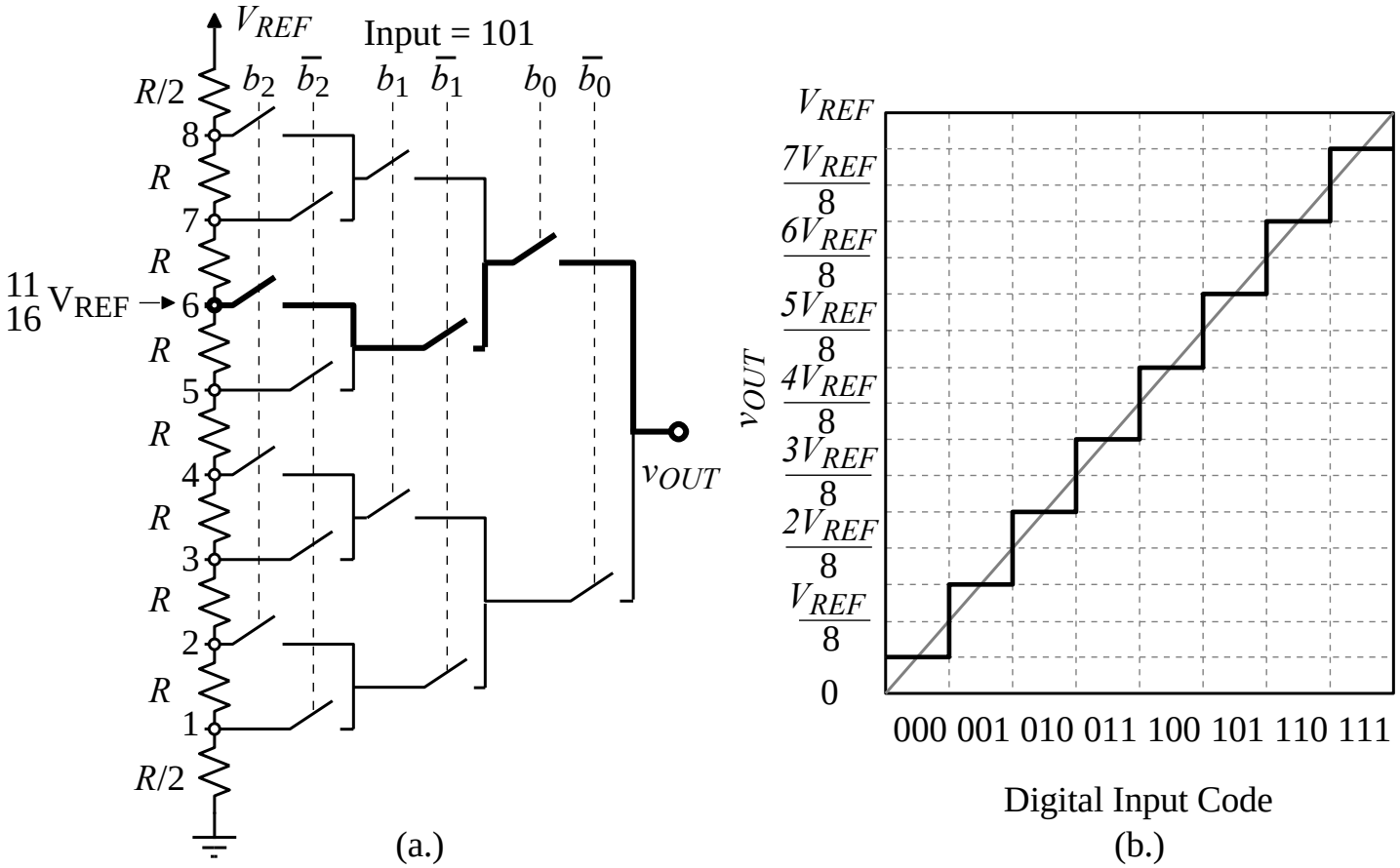



Figure 10.2-7 - (a.) Implementation of a 3-bit voltage scaling DAC. (b.) Input-output characteristics of Fig. 10.2-7(a.)

# Alternate Realization of the 3-Bit Voltage Scaling DAC

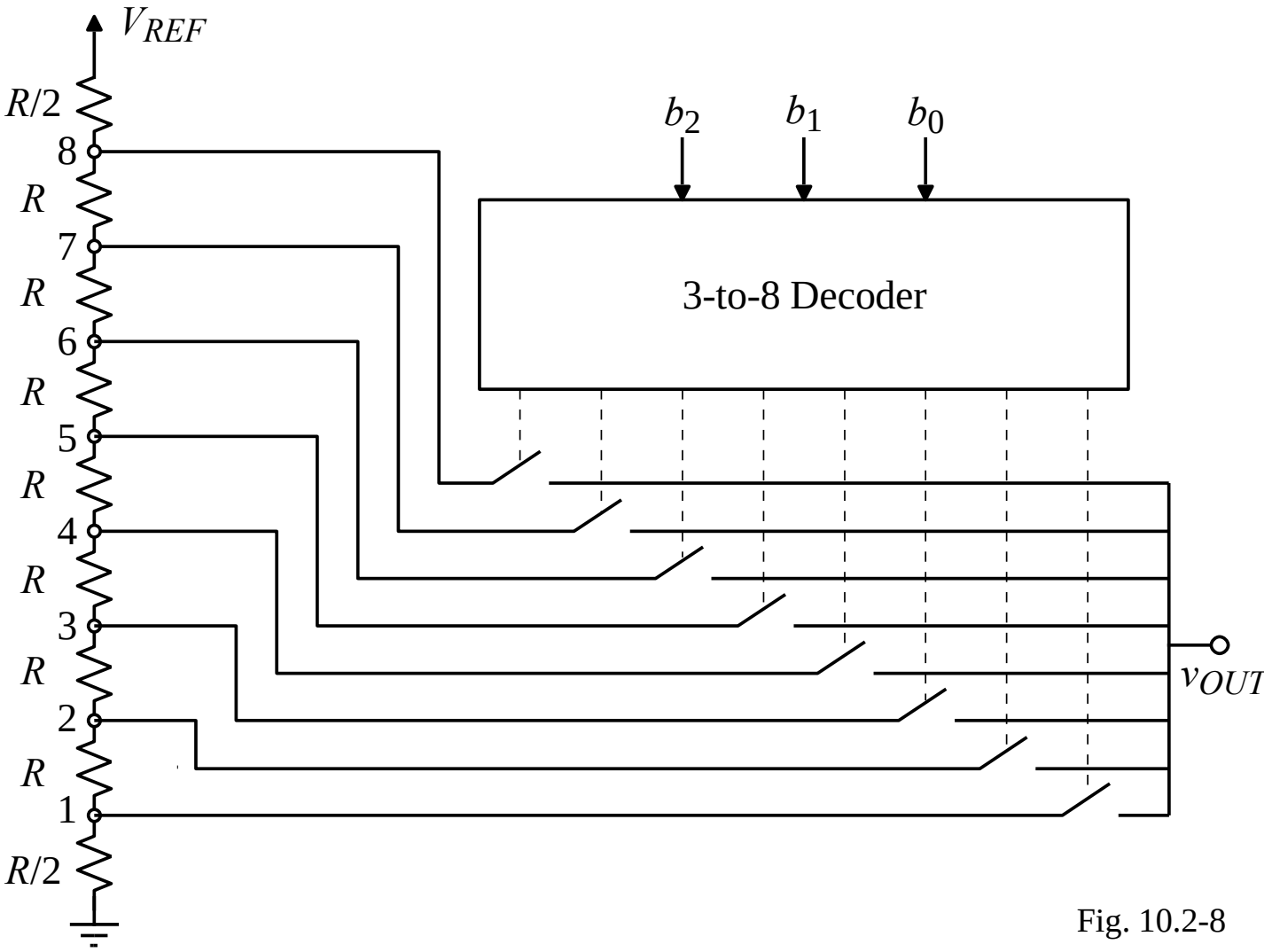



Fig. 10.2-8

## INL and DNL of the Voltage Scaling DAC

Find an expression for the INL and DNL of the voltage scaling DAC using a worst-case approach. For an $n$-bit DAC, assume there are $2^n$ resistors between $V_{REF}$ and ground and that the resistors are numbered from 1 to $2^n$ beginning with the resistor connected to $V_{REF}$ and ending with the resistor connected to ground.

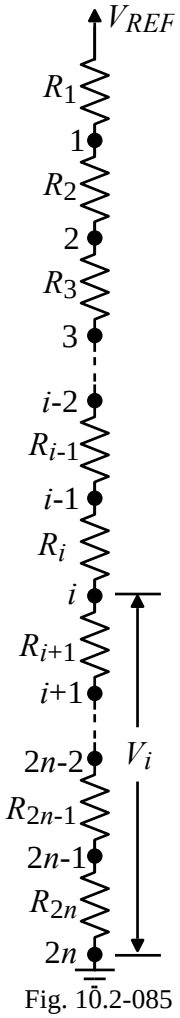


Fig. 10.2-085

Integral Nonlinearity

The voltage at the $i$-th resistor from the top is,

$$v_i = \frac{(2^n\text{-}i)R}{(2^n\text{-}i)R + iR} V_{REF}$$

where there are $i$ resistors above $v_i$ and $2^n$-i below.

For worst case, assume that $i = 2^{n-1}$ (midpoint). Define $R_{max} = R + \Delta R$ and $R_{min} = R - \Delta R$.

The worst case $INL$ is

$$INL = v_{2^{n-1}}(\text{actual}) - v_{2^{n-1}}(\text{ideal})$$

Therefore,

$$INL = \frac{2^{n-1}(R+\Delta R)V_{REF}}{2^{n-1}(R+\Delta R) + 2^{n-1}(R-\Delta R)} - \frac{V_{REF}}{2} = \frac{\Delta R}{2R} V_{REF}$$

$$\boxed{INL = \frac{2^n}{2^n}\left(\frac{\Delta R}{2R}\right)V_{REF} = 2^{n-1}\left(\frac{\Delta R}{R}\right)\left(\frac{V_{REF}}{2^n}\right) = 2^{n-1}\left(\frac{\Delta R}{R}\right) LSBs}$$

Differential Nonlinearity

The worst case $DNL$ is

$$DNL = v_{step}(\text{act}) - v_{step}(\text{ideal})$$

Substituting the actual and ideal steps gives,

$$= \frac{(R\pm\Delta R)V_{REF}}{2^n R} - \frac{R\,V_{REF}}{2^n R}$$

$$= \left(\frac{R\pm\Delta R}{R} - \frac{R}{R}\right)\frac{V_{REF}}{2^n}$$

$$= \frac{\pm\Delta R}{R}\,\frac{V_{REF}}{2^n}$$

Therefore,

$$\boxed{DNL = \frac{\pm\Delta R}{R} LSBs}$$

## Example 34-3 – Accuracy Requirements of a Voltage-Scaling DAC

If the resistor string of a voltage scaling digital-analog converter consists of $2n$ polysilicon resistors having a relative accuracy of ±1%, what is the largest number of bits that can be resolved and keep the worst case *INL* within ±0.5 LSB? For this number of bits, what is the worst case *DNL*?

*Solution*

From the previous page, we can write that

$$2^{n-1}\left(\frac{\Delta R}{R}\right) = 2^{n-1}\left(\frac{1}{100}\right) \leq \frac{1}{2}$$

This inequality can be simplified

$$2^n \leq 100$$

which has a solution of $n = 6$.

The value of the *DNL* for $n = 6$ is found from the previous page as

$$DNL = \frac{\pm 1}{100} LSBs = \pm 0.01 LSBs$$

(This is the reason the resistor string is monotonic.)

## SUMMARY

- DACs scale a voltage reference as an analog output according to a digital word input
- Quantization noise is an inherent ±0.5 *LSB* uncertainty in digitizing an analog value with a finite resolution converter
- The MSB requires the greatest accuracy with the LSB requiring the least accuracy
- *Integral Nonlinearity* (*INL*) is the maximum difference between the actual finite resolution characteristic and the ideal finite resolution characteristic measured vertically (% or *LSB*)
- *Differential Nonlinearity* (*DNL*) is a measure of the separation between adjacent levels measured at each vertical jump (% or *LSB*)
- The limits to DAC speed include the parasitic capacitors, the op amp gain-bandwidth, and the op amp slew rate
- Current scaling DACs scale the reference voltage into binary-weighted currents that are summed into to a resistor to obtain the analog output voltage.
- Current scaling DACs are generally fast but have large element spreads and are not monotonic
- The voltage scaling DAC creates all possible analog voltages and selects which one corresponds to the digital input. The voltage scaling DAC is a monotonic converter.