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# LECTURE 33 – HIGH SPEED COMPARATORS

## LECTURE ORGANIZATION

### Outline

- Speed limitations of comparators
- High speed comparators
- Summary

*CMOS Analog Circuit Design, 3<sup>rd</sup> Edition Reference*

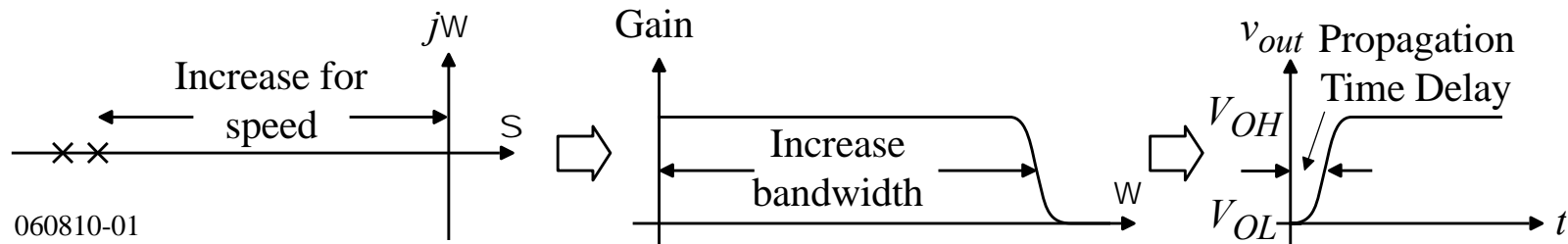
Pages 466-469 and 488-492

## SPEED LIMITATIONS OF COMPARATORS

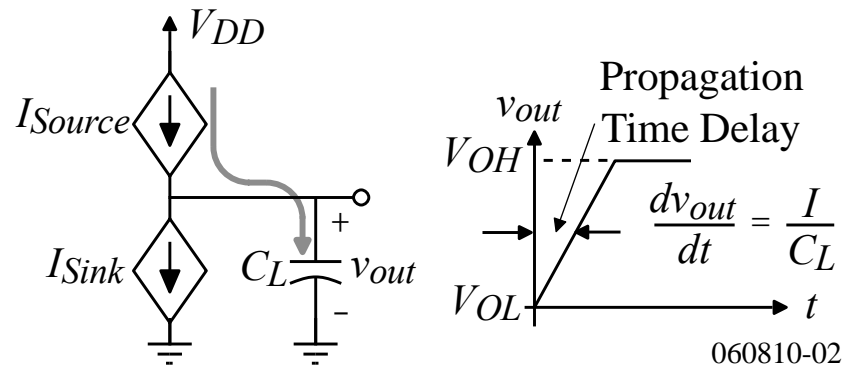
### Speed Limitations of Comparators

The speed of a comparator is limited by either:

- Linear response – response time is inversely proportional to the magnitude of poles

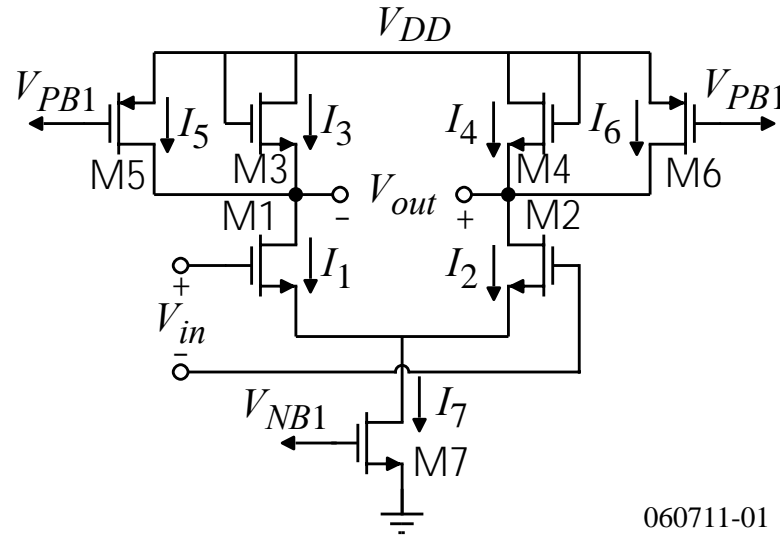


- Slew rate – delay is proportional to capacitance and inversely proportional to current sinking or sourcing capability



## Maximizing the Linear Response

Consider the amplifier of Example 27-3 given below:



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One stage of this amplifier had a gain of 10 and a dominant pole at 551MHz. The response of this amplifier to a step input is

$$V_{out}(t) = 10V_{in} (1 - e^{-p_1 t})$$

If the output signal swing is 1V and the step is 0.1V, the propagation time delay is,

$$V_{in}(\text{min}) = 1/10 = 0.1\text{V} \Rightarrow k = 1$$

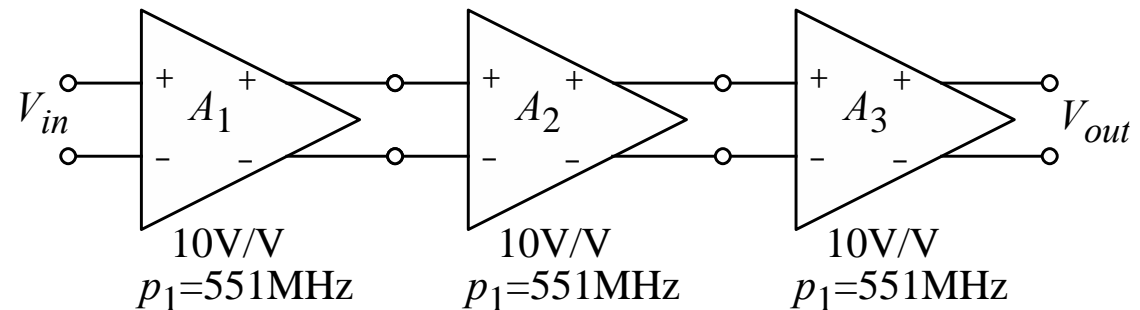
$$\therefore t_p = \frac{1}{p_1} \ln \left[ \frac{2k}{2k-1} \right] = \frac{1}{2\pi \cdot 551 \times 10^6} \ln \left[ \frac{2}{2-1} \right] = 0.20 \text{ ns}$$

## Trading Speed for Sensitivity (Gain)

In the previous example, the gain was too small for good sensitivity. To enhance the sensitivity, cascade three of the gain of 10 stages. The result is,

The frequency response of this amplifier is,

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{1000}{(1 + s/p_1)^3}$$



The step response of this amplifier is

$$v_{out}(t) = \frac{A_o}{2} V_{in} p_1^3 t^2 e^{-p_1 t} \approx \frac{A_o}{2} V_{in} p_1^3 t^2 [1 - p_1 t + p_1^2 t^2 - \dots] \approx \frac{A_o}{2} V_{in} p_1^3 t^2 \quad \text{if } p_1 t < 1$$

The propagation delay time is for  $k = 100$  is

$$t_p^2 = \frac{V_{OH} - V_{OL}}{A_o} \frac{1}{V_{in} p_1^3} = \frac{1}{k p_1^3} \quad \rightarrow \quad t_p = 0.491 \times 10^{-15} \text{ sec. !!!}$$

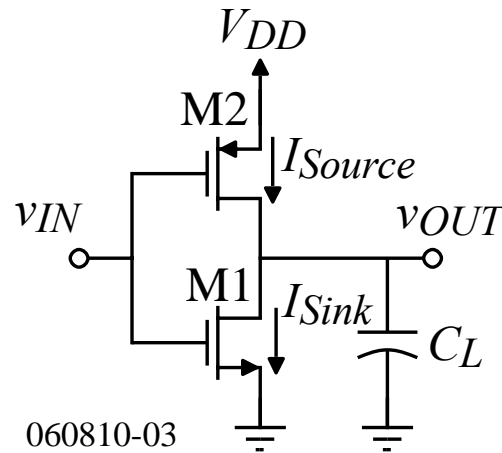
The speed of the amplifier will be limited by the slew capability.

Note: Slew rate  $\approx 1\text{V}/10^{-15} \text{ sec} = 10^{15} \text{ V/sec} \rightarrow i_{\text{Required for } 1\text{fF}} \approx C(dV/dt) = 1\text{A}!!!$

## Maximizing Speed for Slew Rate Limitation

The key is to make the sourcing/sinking current large and the capacitance small.

Best possible sinking/sourcing circuit in CMOS is:



Assuming a  $W/L$  ratio of 42 for M1 and 200 for M2, if the input can swing to  $V_{DD}$  ( $=2.5V$ ) and ground, the sourcing and sinking currents are:

$$I_{Sourcing} = \frac{K_p'W}{2L} (V_{DD} - |V_{TP}|)^2 = \frac{25 \cdot 200}{2} (2.5V - 0.5)^2 \mu A = 10.0 \text{ mA}$$

$$I_{Sinking} = \frac{K_n'W}{2L} (V_{DD} - V_{TN})^2 = \frac{120 \cdot 42}{2} (2.5V - 0.5)^2 \mu A = 10.1 \text{ mA}$$

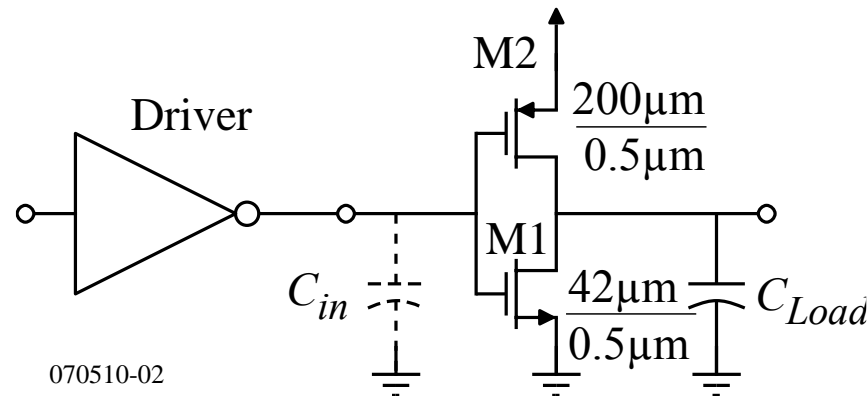
If larger currents are required, cascaded stages can be used to optimize the delay versus the current output.

## Driver Delay of a Push-Pull Inverter

If too much current is required, the device sizes become large and the driver delay increases. For the previous example, the input capacitance for the driver assuming  $C_{ox} \approx 6\text{fF}/\mu\text{m}^2$  and the channel lengths are  $0.5\mu\text{m}$ , is,

$$C_{in} = C_{gs1} + C_{gs2} = 2 \cdot (2/3) C_{ox}(W_1L_1 + W_2L_2)$$

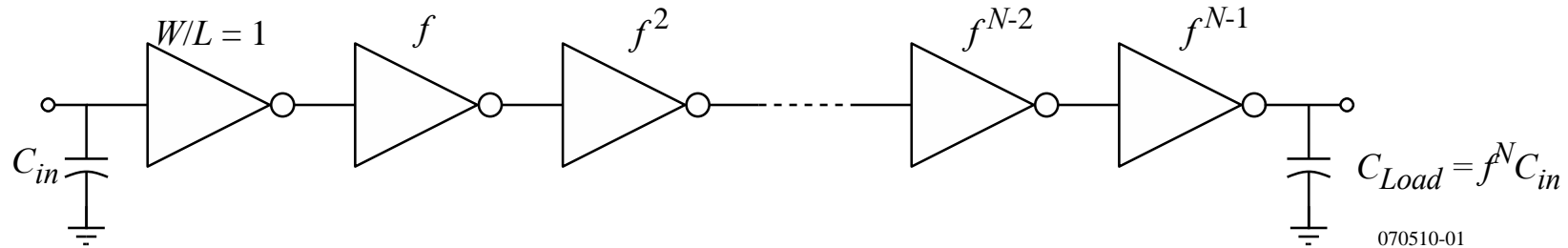
$$= 1.33 \cdot 6\text{fF}/\mu\text{m}^2(121\mu\text{m}^2) = 0.968 \text{ pF}$$



If the effective resistance of the driver is  $30\text{k}\Omega$ , then the delay is  $29 \text{ ns}$  which is much too large.

## Optimizing the Delay of a Chain of Push-Pull Inverters

For a series of  $N$  inverters as shown below, the  $W/L$  is increased by a factor of  $f$  for each succeeding stage.



From the above figure we see that  $C_{Load} = f^N C_{in} \rightarrow N = \frac{\ln(C_{Load}/C_{in})}{\ln f}$

The delay of a single, push-pull inverter can be expressed as,

$$t_{inv} = \tau_{inv} \left( \frac{C_j}{C_{j-1}} + \gamma_{inv} \right)$$

where

$$\tau_{inv} = R_{eff} C_{in} \quad (R_{eff} \text{ is the effective output resistance of the inverter})$$

$$\gamma_{inv} = \frac{C_{self}}{C_{in}} = \frac{C_{junction}}{C_{in}} \quad (C_{junction} \text{ is the bulk-drain capacitances})$$

## Optimizing the Delay of a Chain of Push-Pull Inverters – Continued

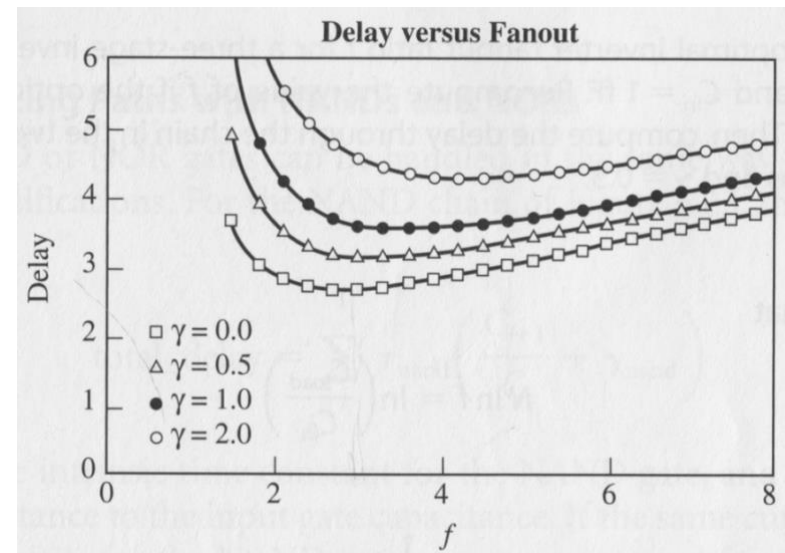
The total delay of the chain of inverters is

$$t_{total} = N \tau_{inv} \left( \frac{C_j}{C_{j-1}} + \gamma_{inv} \right)$$

Setting  $f = \frac{C_j}{C_{j-1}}$  gives

$$t_{total} = \frac{\ln(C_{Load}/C_{in})}{\ln f} \tau_{inv} (f + \gamma_{inv})$$

Plotting the total delay versus  $f$  for various values of  $\gamma_{inv}$  shows that the optimum value of  $f$  lies in the range of 2.5 to 4<sup>†</sup>.



<sup>†</sup> D.A. Hodges, H.G. Jackson, and R.A. Saleh, *Analysis and Design of Digital Integrated Circuits in Deep Submicron Technology*, 3<sup>rd</sup> ed., McGraw-Hill Book Co., 2004, Chapter 6.



### **Example 33-1 – Finding the Optimum Delay for a Chain of Inverters**

Assume that  $C_{Load}$  is 5pf,  $C_{in} = 50\text{fF}$ ,  $\tau_{inv} = 10\text{ps}$ , and  $\gamma_{inv} = 0.5$ . If  $f = 3.6$ , find the optimal number of stages and the total delay of this chain of inverters.

#### **Solution**

From above we get the optimal number of stages as,

$$N = \frac{\ln(C_{Load}/C_{in})}{\ln f} = \frac{\ln(100)}{\ln 3.6} = 3.59$$

If we choose  $N = 4$ , then  $f$  can be recomputed as

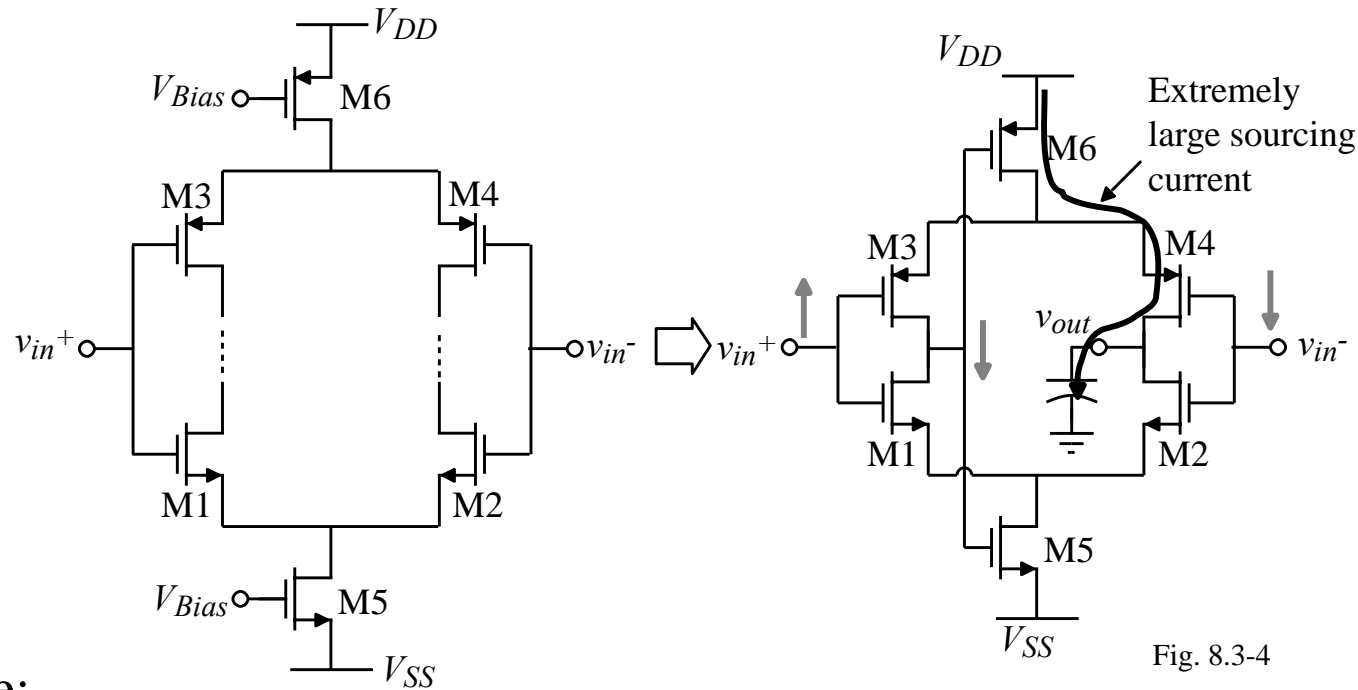
$$\ln f = \frac{1}{4} \ln(100) \Rightarrow f = 3.16$$

The total delay is,

$$t_{total} = N \tau_{inv} \left( \frac{C_j}{C_{j-1}} + \gamma_{inv} \right) = 4 \cdot 10\text{ps} (3.16 + 0.5) = 146\text{ps}$$

## Self-Biased Differential Amplifier<sup>†</sup>

Not as good as the push-pull inverter but interesting.



Advantage:

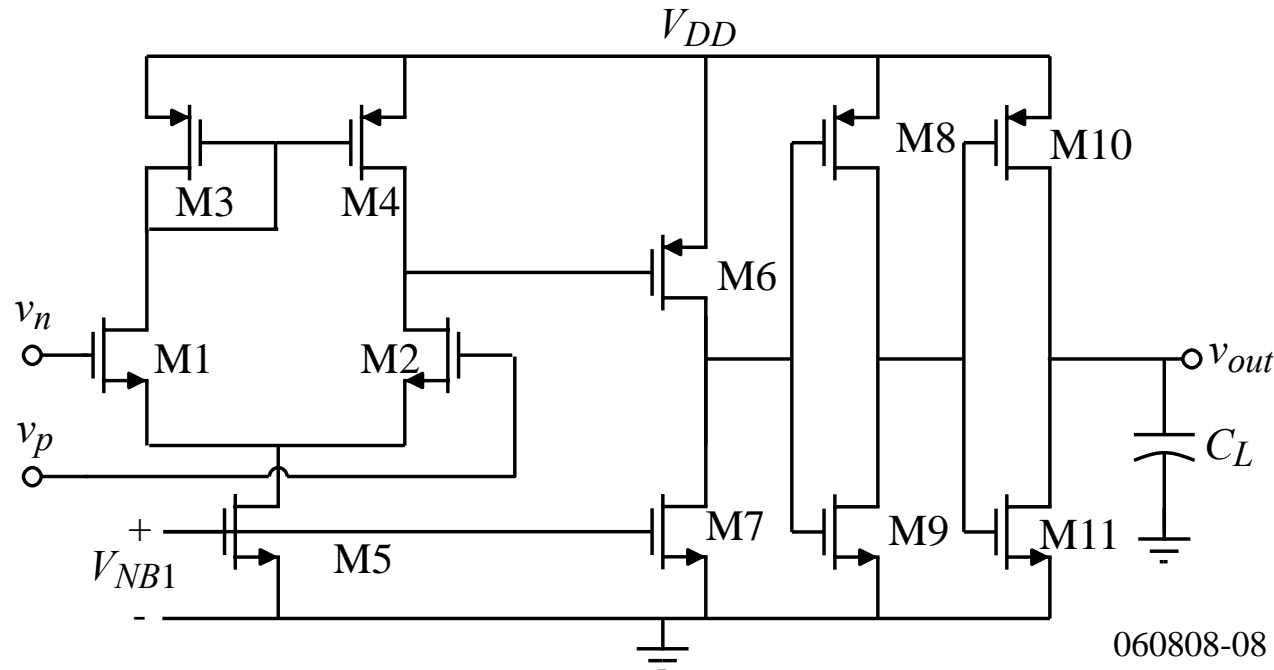
Large sink or source current with out a large quiescent current.

Disadvantage:

Poor common mode range ( $v_{in}^+$  slower than  $v_{in}^-$ )

<sup>†</sup> M. Bazes, "Two Novel Full Complementary Self-Biased CMOS Differential Amplifiers," *IEEE Journal of Solid-State Circuits*, Vol. 26, No. 2, Feb. 1991, pp. 165-168.

## Comparators that Can Drive Large Capacitive Loads



### Comments:

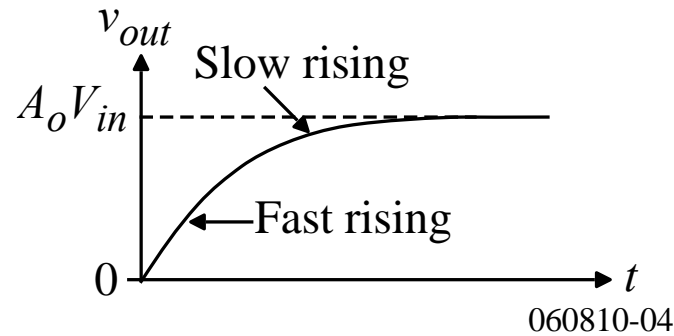
- Slew rate =  $3\text{V}/\mu\text{s}$  into  $50\text{pF}$
- Linear rise/fall time =  $100\text{ns}$  into  $50\text{pF}$
- Propagation delay time  $\approx 1\mu\text{s}$
- Loop gain  $\approx 32,000$  V/V
- The quiescent dc currents in the output stages are not well defined
- Use the principle of optimizing the delay in cascaded inverters

## HIGH SPEED COMPARATORS

### A Study in Exponentials

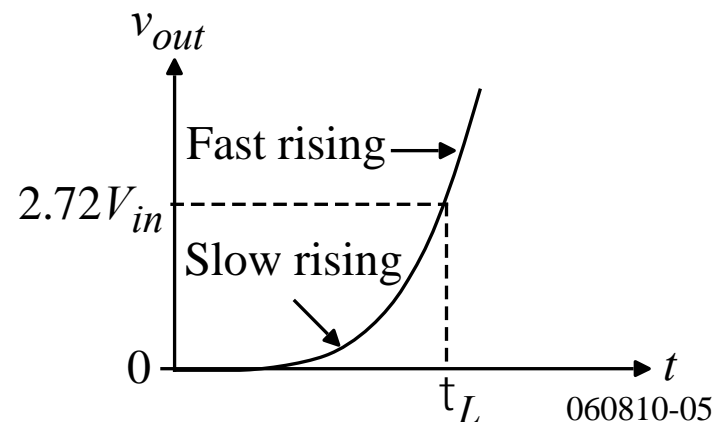
The step response of an amplifier with a gain of  $A_o$  and a dominant pole at  $\omega_A$  is,

$$v_{out}(t) = A_o[1 - \exp(-\omega_A t)] V_{in}$$



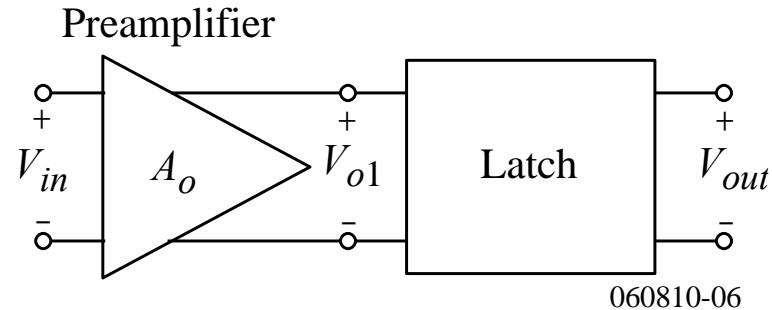
The latch response to a step input of  $V_{in}$  is,

$$v_{out}(t) = V_{in} \exp\left(\frac{t}{t_L}\right)$$

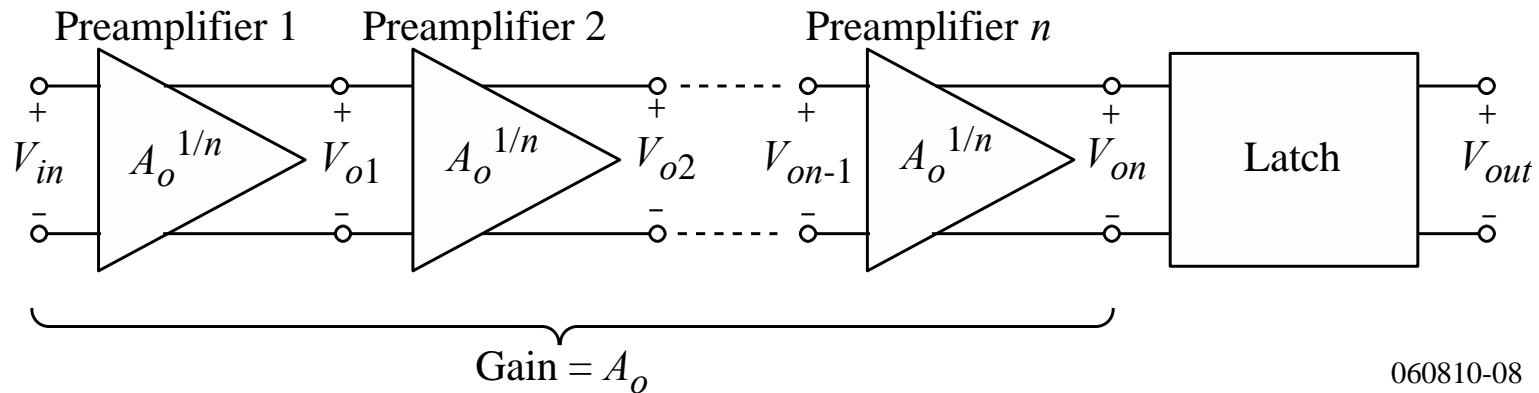


## A High-Speed Comparator Architecture

Cascade an amplifier with a latch to take advantage of the exponential characteristics of the previous slide.



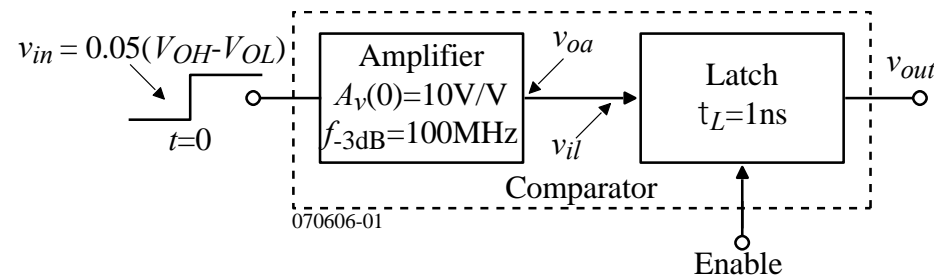
In order to keep the bandwidth of the amplifier large, the gain will be small. To achieve



Therefore, the question is how many stages of the amplifier and what is the gain of each stage for optimum results?

### Example 33-2 – Optimizing the Propagation Time Delay

A comparator consists of an amplifier cascaded with a latch as shown below. The amplifier has a voltage gain of  $10\text{V/V}$  and  $f_{-3\text{dB}} = 100\text{MHz}$  and the latch has a time constant of  $1\text{ns}$ . The maximum and minimum voltage swings of the amplifier and latch are  $V_{OH}$  and  $V_{OL}$ . When should the latch be enabled after the application of a step input to the amplifier of  $0.05(V_{OH}-V_{OL})$  to get minimum overall propagation time delay? What is the value of the minimum propagation time delay?



### Solution

The solution is based on the figure shown.

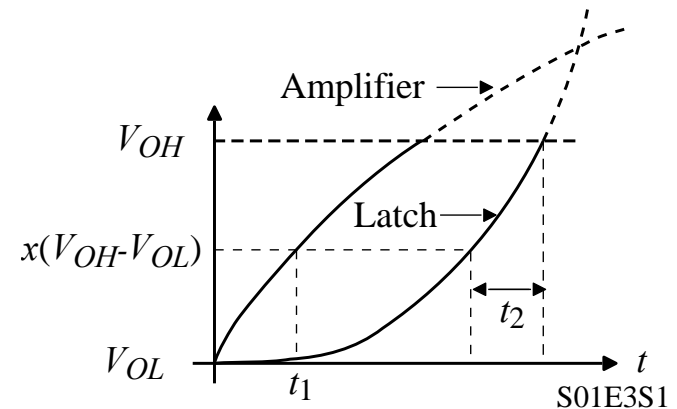
We note that,

$$v_{oa}(t) = 10[1 - e^{-\omega_{3\text{dB}}t}]0.05(V_{OH} - V_{OL}).$$

If we define the input voltage to the latch as,

$$v_{il} = x \cdot (V_{OH} - V_{OL})$$

then we can solve for  $t_1$  and  $t_2$  as follows:



**Example 33-2 - Continued**

$$x \cdot (V_{OH} - V_{OL}) = 10[1 - e^{-\omega_{3dB}t_1}]0.05(V_{OH} - V_{OL}) \rightarrow x = 0.5[1 - e^{-\omega_{3dB}t_1}]$$

This gives,

$$t_1 = \frac{1}{\omega_{3dB}} \ln \left( \frac{1}{1-2x} \right)$$

From the propagation time delay of the latch we get,

$$t_2 = \tau_L \ln \left( \frac{V_{OH} - V_{OL}}{2v_{il}} \right) = \tau_L \ln \left( \frac{1}{2x} \right)$$

$$\therefore t_p = t_1 + t_2 = \frac{1}{\omega_{3dB}} \ln \left( \frac{1}{1-2x} \right) + \tau_L \ln \left( \frac{1}{2x} \right) \rightarrow \frac{dt_p}{dx} = 0 \text{ gives}$$

$$2x = \frac{2\tau_L\omega_{3dB}}{2+2\tau_L\omega_{3dB}} = \frac{0.4\pi}{2+0.4\pi} = 0.3859 \quad (x = 0.1930)$$

$$t_1 = \frac{10\text{ns}}{2\pi} \ln \left( \frac{1}{1-0.3859} \right) = 1.592\text{ns} \cdot 0.4875 = 0.7762 \text{ ns}$$

$$\text{and } t_2 = 1\text{ns} \ln \left( \frac{1}{0.3859} \right) = 0.9522\text{ns}$$

$$\therefore t_p = t_1 + t_2 = 0.776 \text{ ns} + 0.952 \text{ ns} = \underline{\underline{1.728 \text{ ns}}}$$

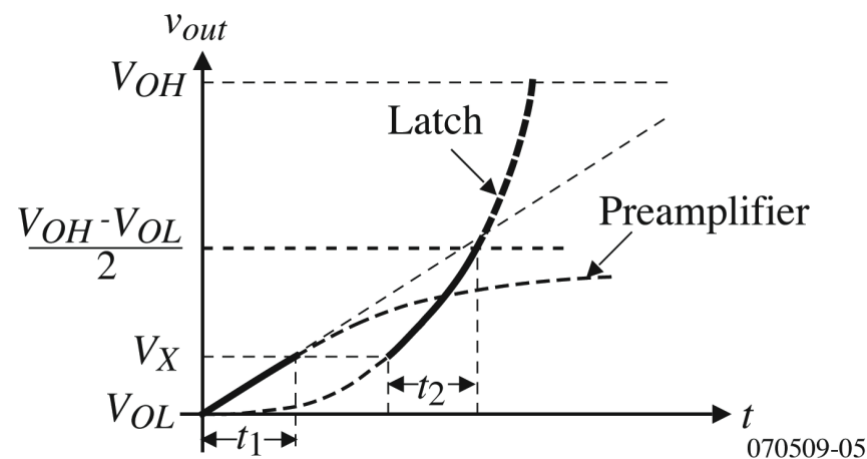
## Minimizing the Propagation Delay Time in Comparators

Facts:

- The input signal is equal to  $V_{in}(\text{min})$  for worst case
- Amplifiers have a step response with a negative argument in the exponential
- Latches have a step response with a positive argument in the exponential
- If the amplifiers rise too quickly, they will be slew limited

Approach:

- Use a cascade of low-gain, wide-bandwidth amplifiers to take a small input signal and amplify it without suffering slew limit
- Use a latch to take the amplified input and quickly reach  $0.5(V_{OH}-V_{OL})$



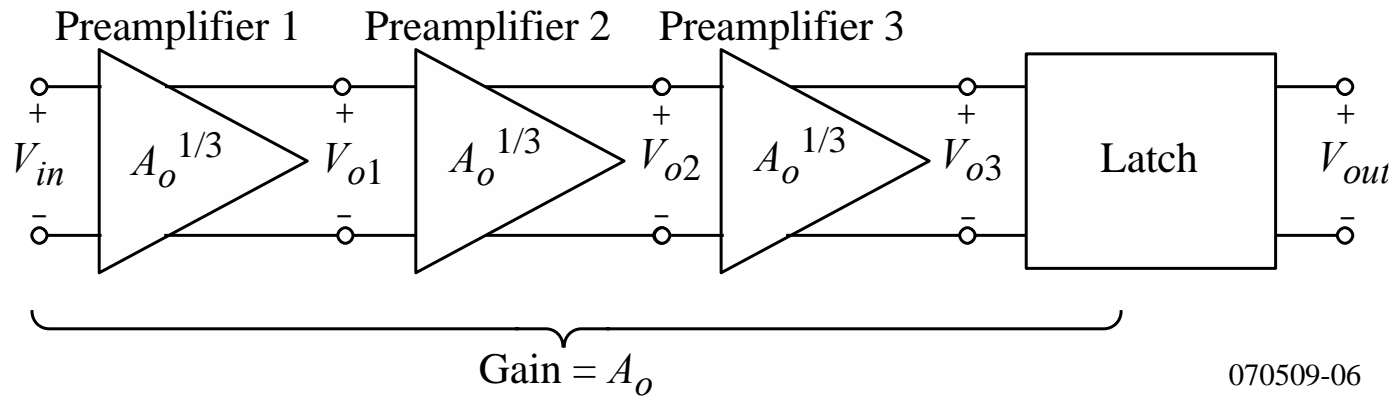


## Minimization of the Propagation Delay Time

Minimization of  $t_p$ :

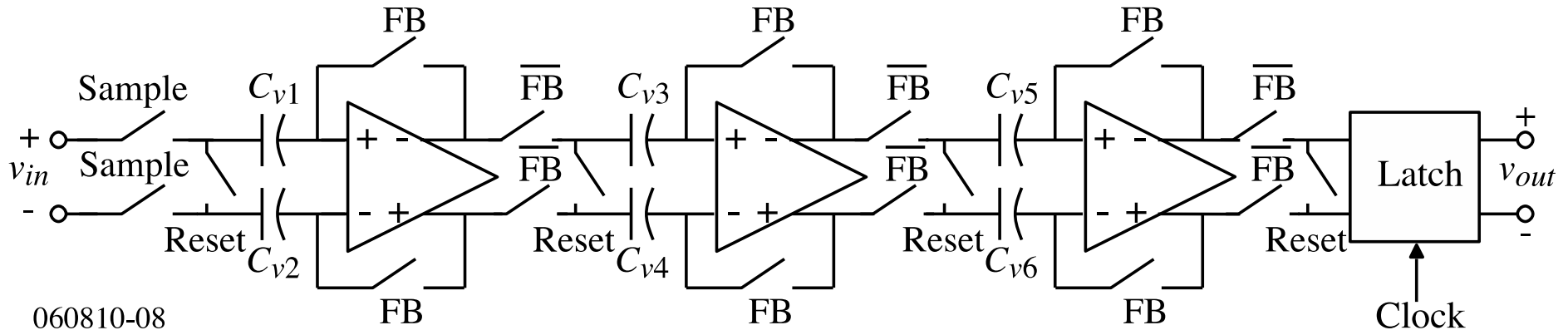
Q. If the preamplifier consists of  $n$  stages of gain  $A$  having a single-pole response, what is the value of  $n$  and  $A$  that gives minimum propagation delay time?

A.  $n = 6$  and  $A = 2.62$  but this is a very broad minimum and  $n$  is usually 3 and  $A \approx 6-7$  to save area.



## Fully Differential, Three-Stage Amplifier and Latch Comparator

Circuit:



Comments:

- Autozero and reset phase followed by comparison phase
- In the autozero phase, switches labeled “Reset” and “FB” are closed.
- In the sample phase, switches labeled “Sample” and “ $\overline{\text{FB}}$ ” are closed.
- Can run as high as 200Msps

## Preamplifier and Latch Circuits

Gain:

$$A_v = -\frac{g_{m1}}{g_{m3}} = -\frac{g_{m2}}{g_{m4}} = -\sqrt{\frac{K_N'(W_1/L_1)}{K_P'(W_3/L_3)}}$$

Dominant Pole:

$$|p_{dominant}| = \frac{g_{m3}}{C} = \frac{g_{m4}}{C}$$

where  $C$  is the capacitance seen from the output nodes to ground.

If  $(W_1/L_1)/(W_3/L_3) = 100$  and the bias current is  $100\mu\text{A}$ , then  $A = -3.85$  and the bandwidth is  $15.9\text{MHz}$  if  $C = 0.5\text{pF}$ .

Comments:

- If a buffer is used to reduce the output capacitance, one must take into account the loss of the buffer.
- The use of a preamplifier before the latch reduces the latch offset by the gain of the preamplifier so that the offset is due to the preamplifier only.

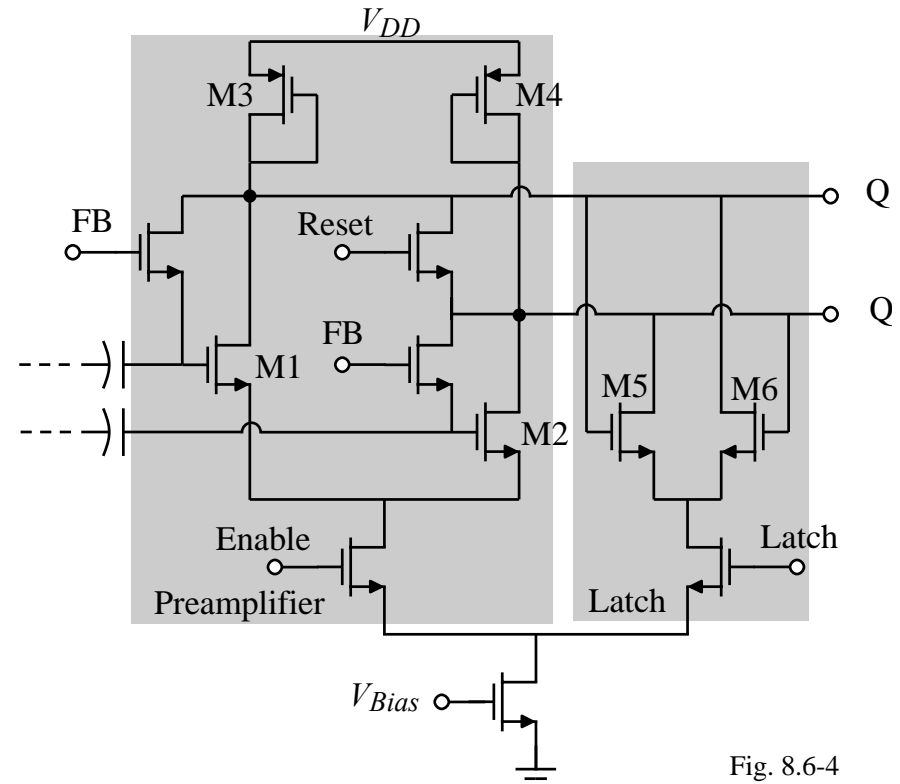


Fig. 8.6-4

## An Improved Preamplifier

Circuit:

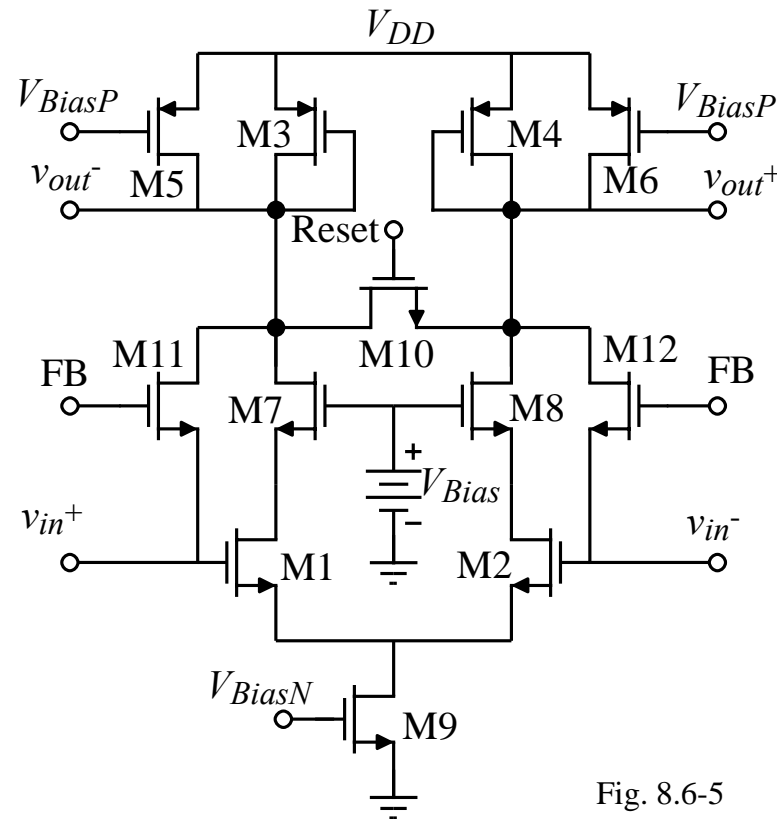


Fig. 8.6-5

Gain:

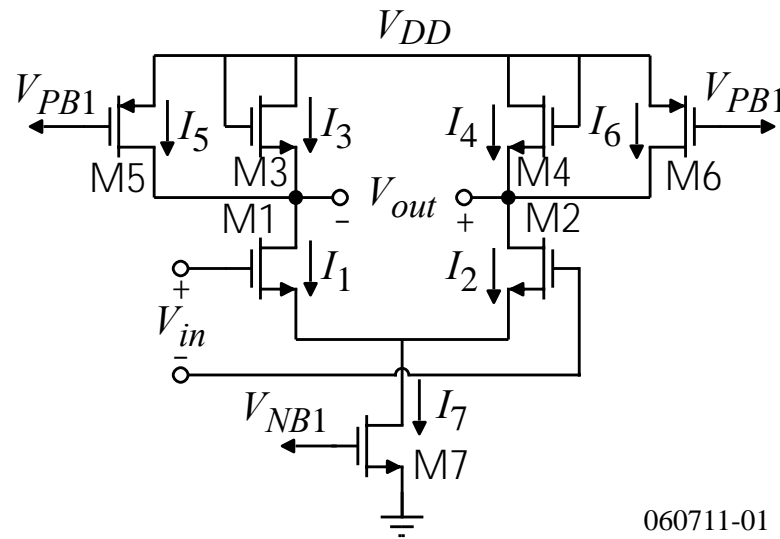
$$A_v = -\frac{g_{m1}}{g_{m3}} = -\sqrt{\frac{K_N'(W_1/L_1)I_1}{K_P'(W_3/L_3)I_3}} = -\sqrt{\frac{K_N'(W_1/L_1)}{K_P'(W_3/L_3)}} \sqrt{1 + \frac{I_5}{I_3}}$$

If  $I_5 = 24I_3$ , the gain is increased by a factor of 5

## Improved Frequency Response of the Amplifier

If the ratio of transconductance  $W/L$  is much larger than the load  $W/L$ , the frequency response will suffer. Using the technique of the previous slide, we can keep the ratio of the  $W/L$ s to a more reasonable value. The result is higher frequency response.

Amplifier of Example 27-3:



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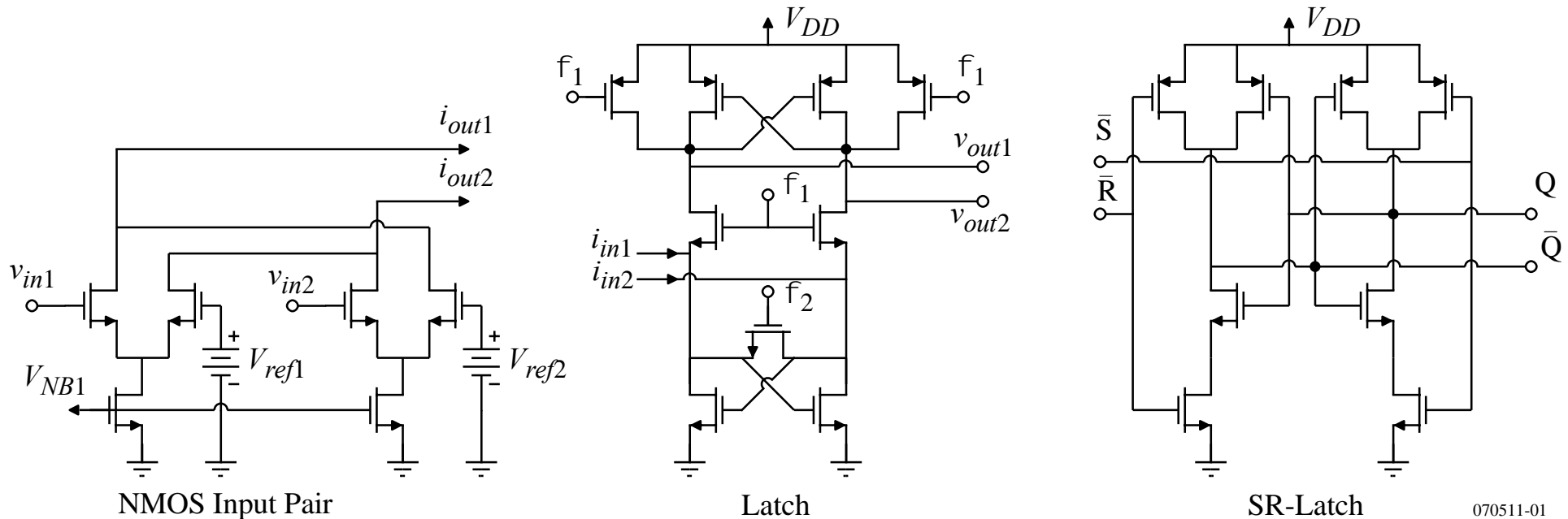
$$\text{Gain} = 20\text{dB}$$

$$f_{-3\text{dB}} = 551\text{MHz}$$

## High-Speed CMOS Comparator

The comparator used in a 12-bit, 200 Msp/s ADC is shown below<sup>†</sup>. The comparator is used in each of the 4-bit pipeline stages which requires 15 comparators.

The comparators consist of three stages including (a.) differential input pairs, (b.) a cross-coupled latch, and (c.) an SR latch to hold the comparator output until the next clock cycle.

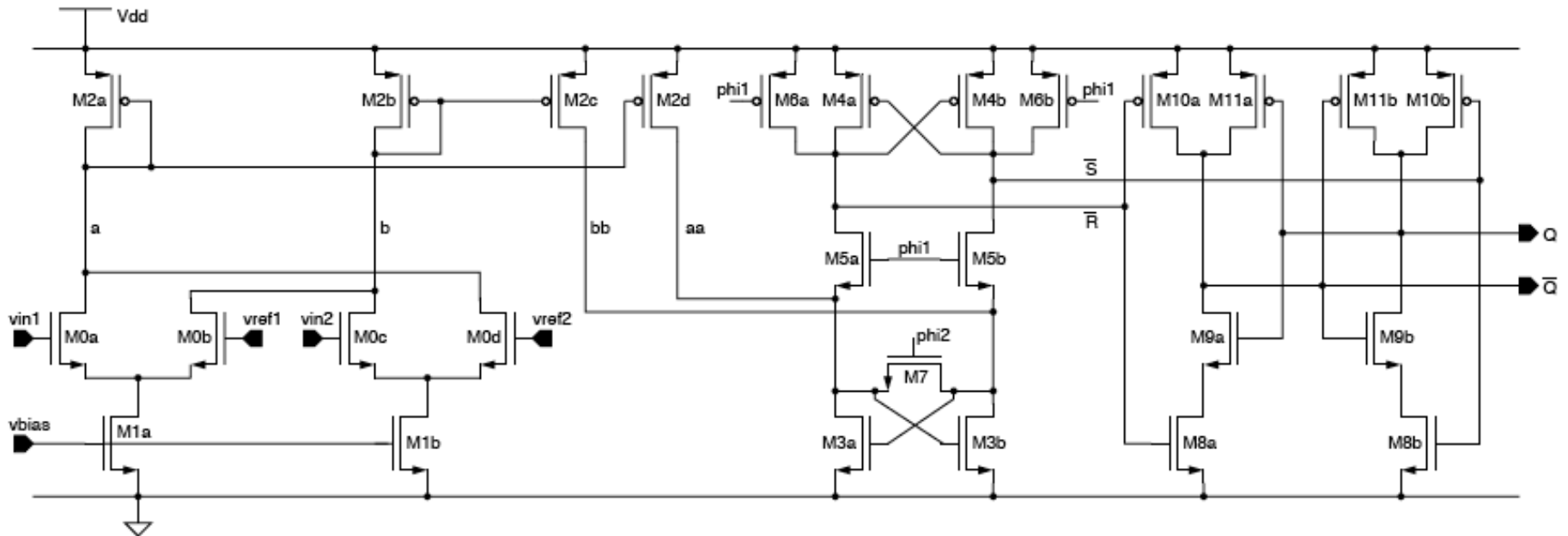


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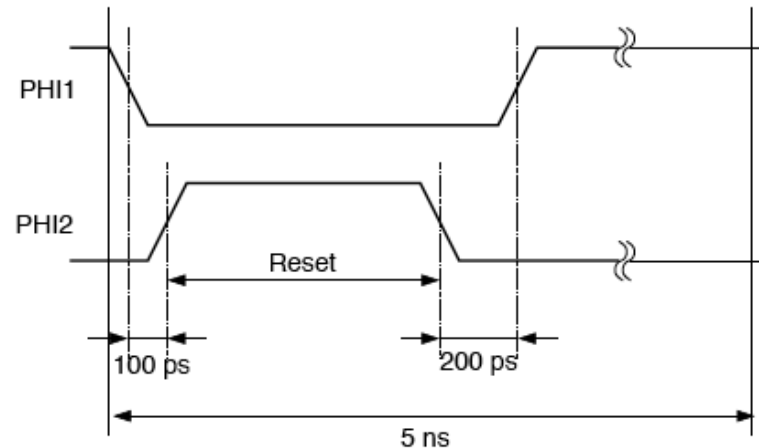
<sup>†</sup> T. Liechti, "Design of a High-Speed 12-bit Differential Pipelined A/D Converter," Diploma Project, Feb. 2004, Microelectronic Systems Laboratory, Swiss Federal Institute of Technology, Lausanne.

## High Speed CMOS Comparator – Continued

Schematic of the fully differential comparator:



Clock waveforms:



Mean comparator power dissipation is  $140\mu\text{W}$  under typical conditions

## SUMMARY

- Comparators are limited in speed either by bandwidth or slew rate
- Increasing the magnitude of the poles improves the bandwidth limitations
- Increasing the current sinking/sourcing ability improves the slew rate limitation
- Most high speed comparators use a combination of preamplifier followed by a latch
  - The preamplifier uses bandwidth to quickly build up the input
  - The latch uses positive feedback to take the signal to its final state