LECTURE 32 – IMPROVED OPEN-LOOP COMPARATORS AND LATCHES

LECTURE ORGANIZATION

Outline

- Autozeroing
- Hysteresis
- Simple Latches
- Summary

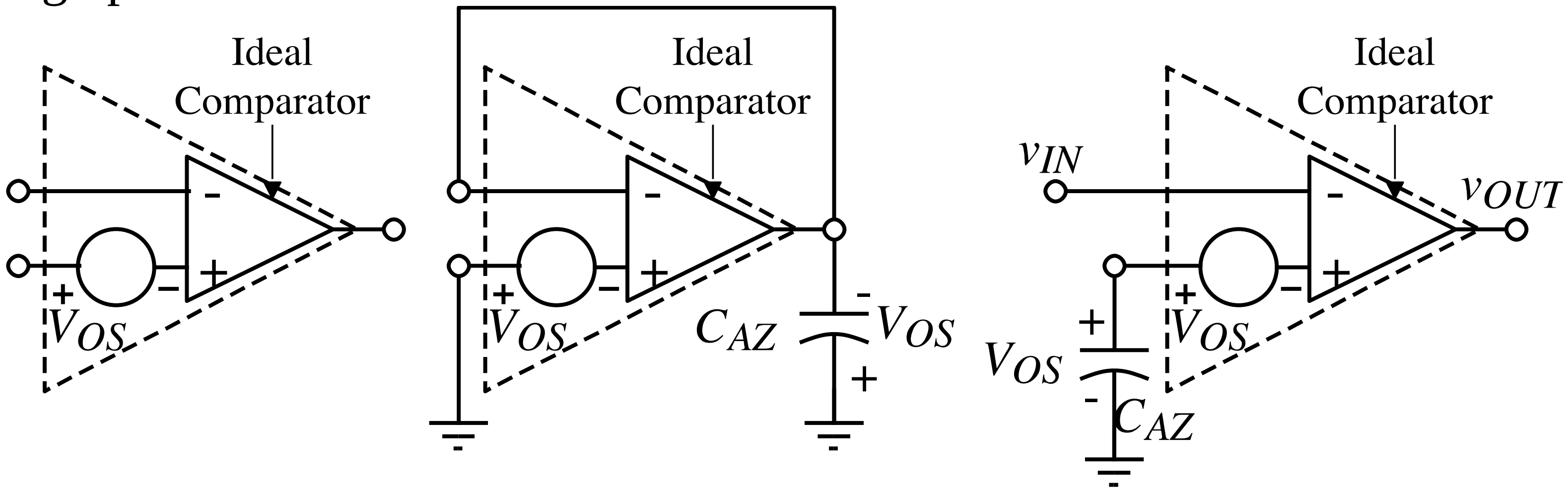
CMOS Analog Circuit Design, 3rd Edition Reference

Pages 469-488

AUTOZEROING

Principle of Autozeroing

Use the comparator as an op amp to sample the dc input offset voltage and cancel the offset during operation.



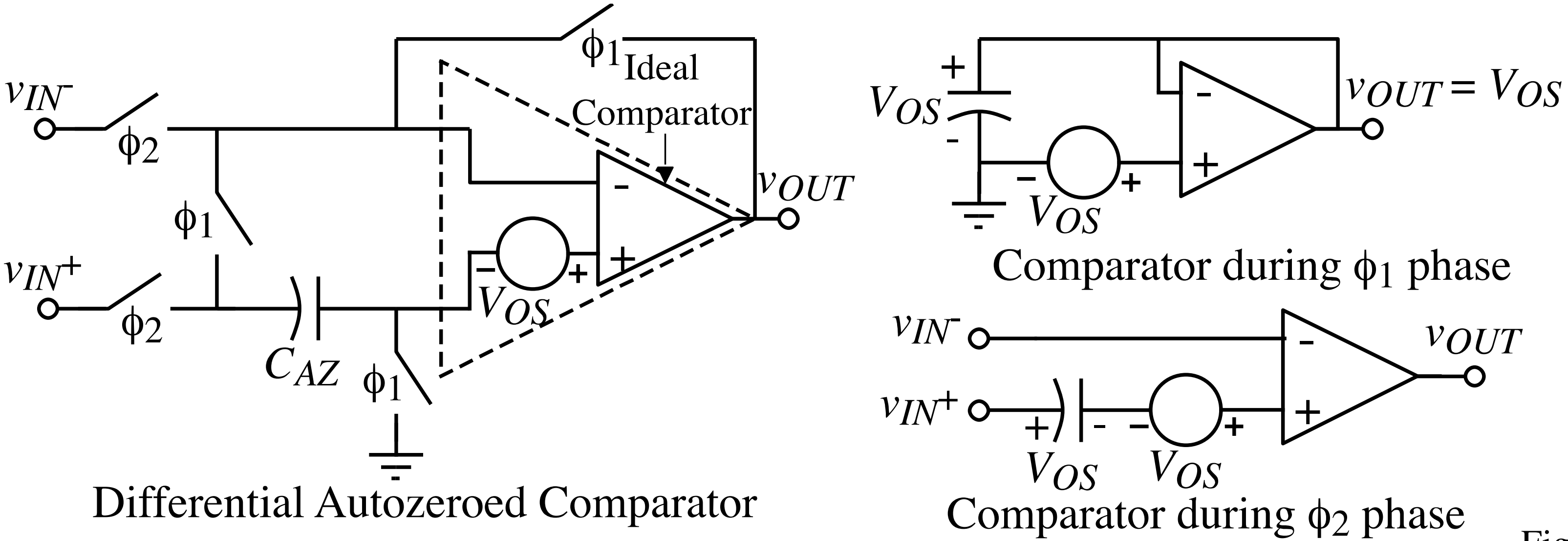
Model of Comparator. Autozero Cycle Comparison Cycle

Fig. 8.4-1

Comments:

- The comparator must be stable in the unity-gain mode (self-compensating comparators are ideal, the two-stage comparator would require compensation to be switched in during the autozero cycle.)
- Complete offset cancellation is limited by charge injection

Differential Implementation of Autozeroed Comparators



Differential Autozeroed Comparator

Comparator during ϕ_1 phase

Comparator during ϕ_2 phase

Fig. 8.4-2

Single-Ended Autozeroed Comparators

Noninverting:

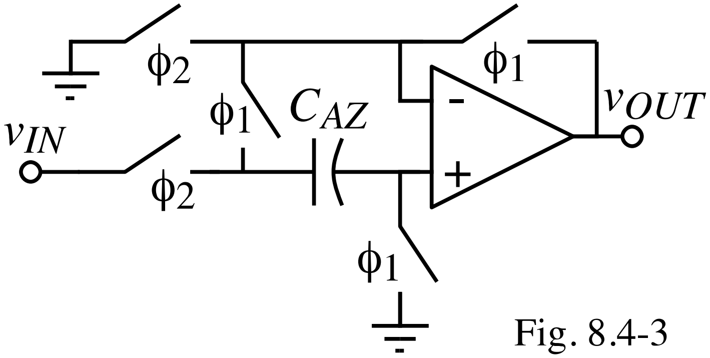


Fig. 8.4-3

Inverting:

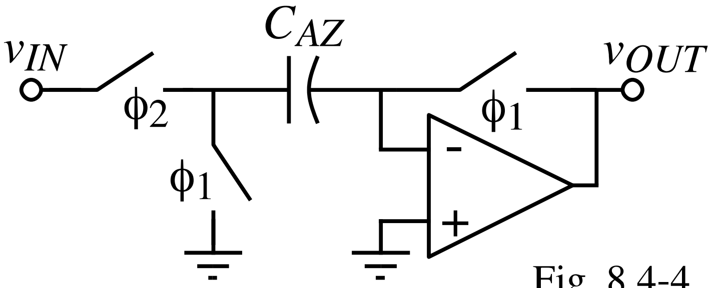


Fig. 8.4-4

Comment on autozeroing:

Need to be careful about noise that gets sampled onto the autozeroing capacitor and is present on the comparison phase of the process.

HYSTERESIS

Influence of Input Noise on the Comparator

Comparator without hysteresis:

Comparator with hysteresis:

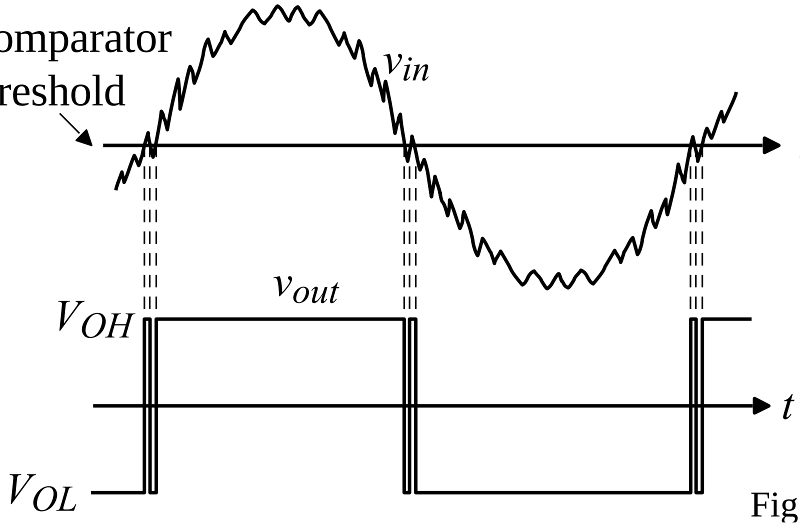


Fig. 8.4-6A

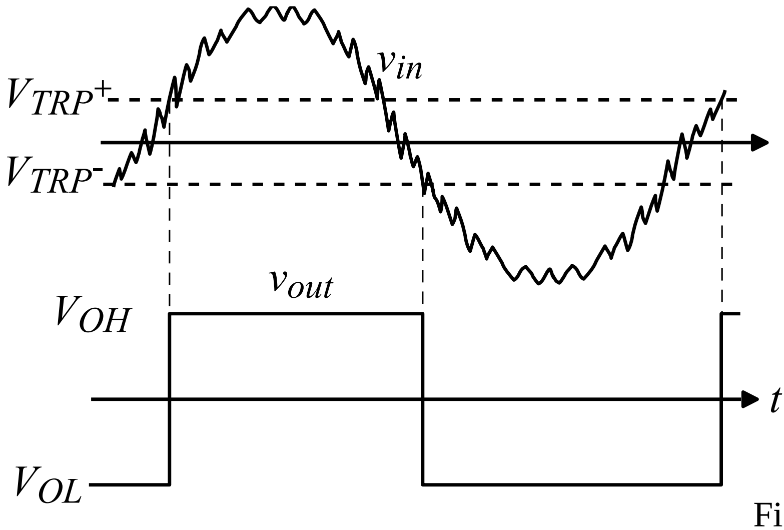
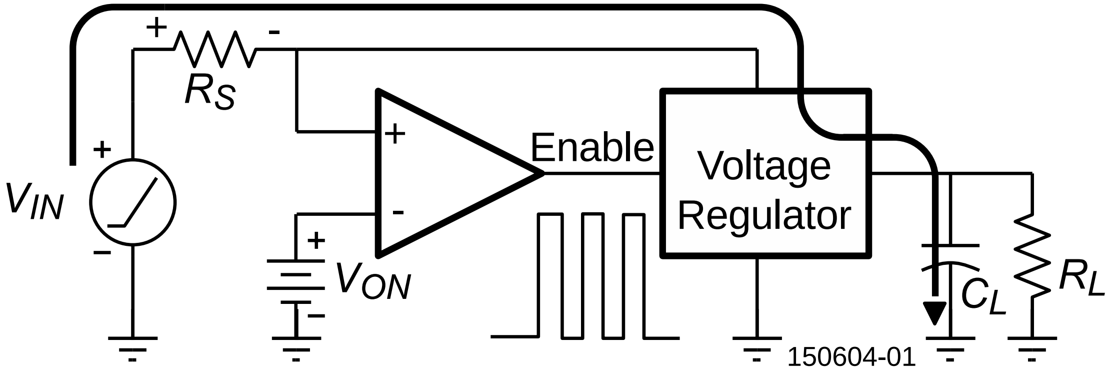


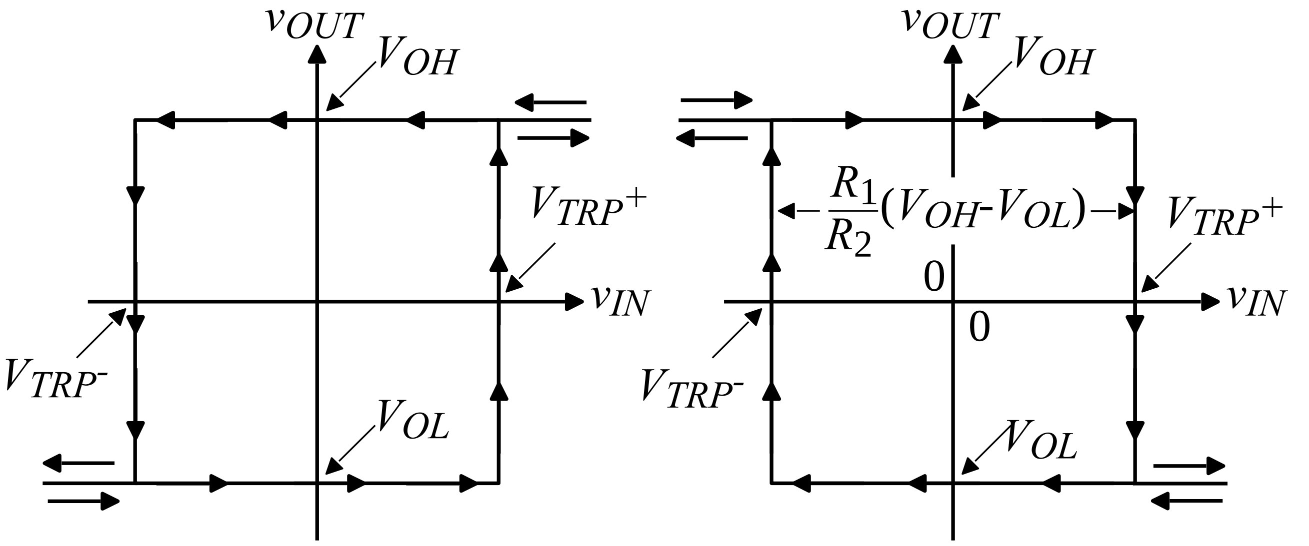
Fig. 8.4-6B

Voltage Regulator with input voltage having too large of source resistance, R_S:



Use of Hysteresis for Comparators in a Noisy Environment

Transfer curve of a comparator with hysteresis:



Counterclockwise Bistable Clockwise Bistable Fig. 8.4-5

Hysteresis is achieved by the use of positive feedback

- Externally
- Internally

Noninverting Comparator using External Positive Feedback

Circuit:

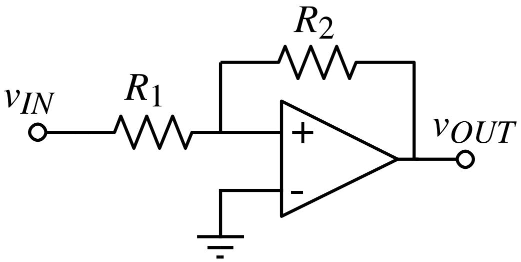
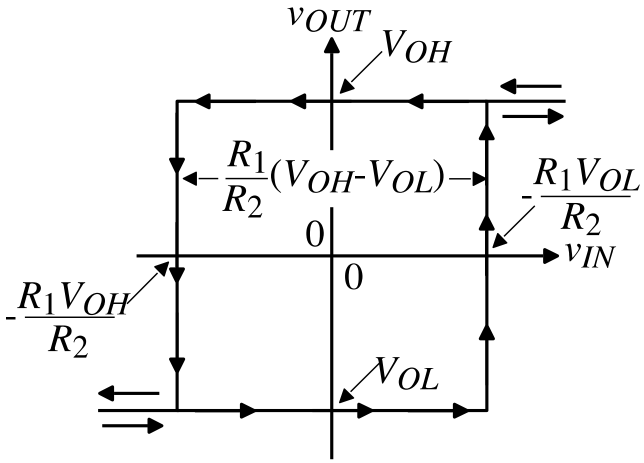


Fig. 8.4-7



Upper Trip Point:

Assume that $v_{OUT} = V_{OL}$, the upper trip point occurs when,

$$0 = \left(\frac{R_1}{R_1+R_2}\right)V_{OL} + \left(\frac{R_2}{R_1+R_2}\right)V_{TRP^+} \quad \rightarrow \quad V_{TRP^+} = -\frac{R_1}{R_2}V_{OL}$$

Lower Trip Point:

Assume that $v_{OUT} = V_{OH}$, the lower trip point occurs when,

$$0 = \left(\frac{R_1}{R_1+R_2}\right)V_{OH} + \left(\frac{R_2}{R_1+R_2}\right)V_{TRP^-} \quad \rightarrow \quad V_{TRP^-} = -\frac{R_1}{R_2}V_{OH}$$

Width of the bistable characteristic:

$$\Delta V_{in} = V_{TRP^+} - V_{TRP^-} = \left(\frac{R_1}{R_2}\right)\left(V_{OH} - V_{OL}\right)$$

Inverting Comparator using External Positive Feedback

Circuit:

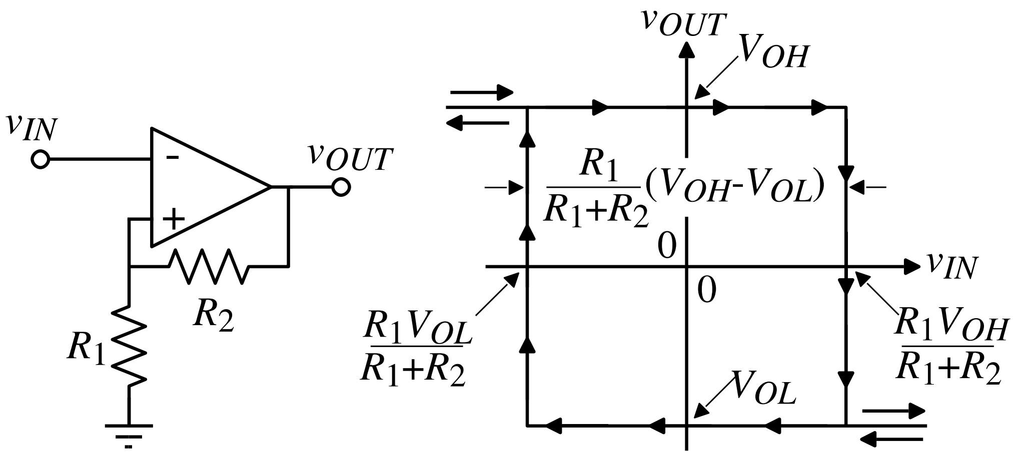


Fig. 8.4-8

Upper Trip Point:

$$v_{IN} = V_{TRP}^{+} = \left(\frac{R_1}{R_1+R_2}\right)V_{OH}$$

Lower Trip Point:

$$v_{IN} = V_{TRP}^{-} = \left(\frac{R_1}{R_1+R_2}\right)V_{OL}$$

Width of the bistable characteristic:

$$\Delta V_{in} = V_{TRP^+} - V_{TRP^-} = \left(\frac{R_1}{R_1+R_2}\right)\left(V_{OH} - V_{OL}\right)$$

Horizontal Shifting of the CCW Bistable Characteristic

Circuit:

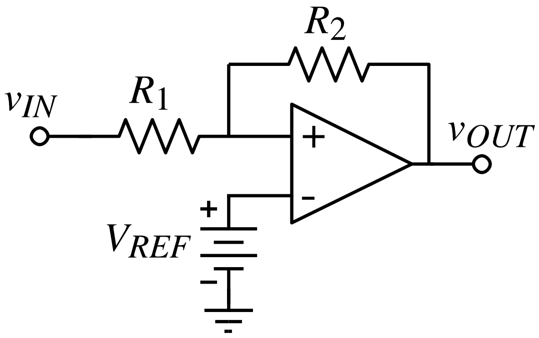
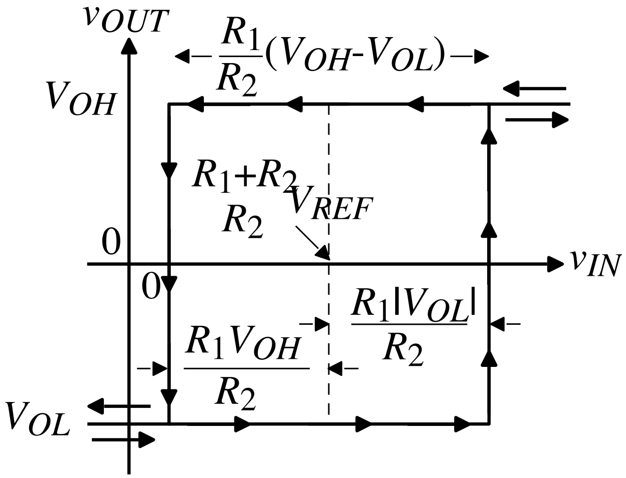


Fig. 8.4-9



Upper Trip Point:

$$V_{REF} = \left(\frac{R_1}{R_1+R_2}\right)V_{OL} + \left(\frac{R_2}{R_1+R_2}\right)V_{TRP^+} \quad \rightarrow \quad V_{TRP^+} = \left(\frac{R_1+R_2}{R_2}\right)V_{REF} - \frac{R_1}{R_2}V_{OL}$$

Lower Trip Point:

$$V_{REF} = \left(\frac{R_1}{R_1+R_2}\right)V_{OH} + \left(\frac{R_2}{R_1+R_2}\right)V_{TRP^-} \quad \rightarrow \quad V_{TRP^-} = \left(\frac{R_1+R_2}{R_2}\right)V_{REF} - \frac{R_1}{R_2}V_{OH}$$

Shifting Factor:

$$\pm\left(\frac{R_1+R_2}{R_2}\right)V_{REF}$$

Horizontal Shifting of the CW Bistable Characteristic

Circuit:

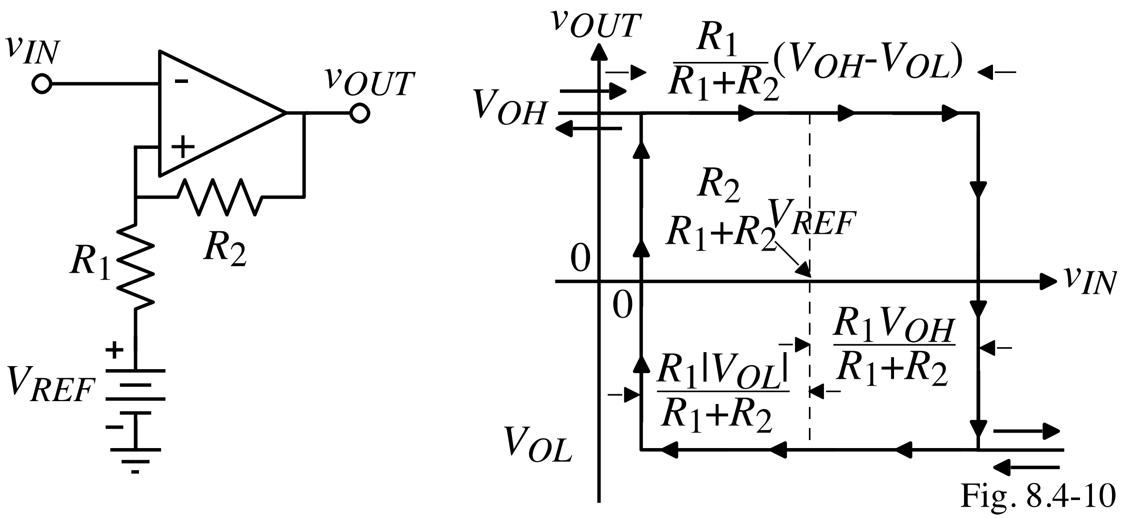


Fig. 8.4-10

Upper Trip Point:

$$v_{IN} = V_{TRP}^{+} = \left(\frac{R_1}{R_1+R_2}\right)V_{OH} + \left(\frac{R_2}{R_1+R_2}\right)V_{REF}$$

Lower Trip Point:

$$v_{IN} = V_{TRP}^{-} = \left(\frac{R_1}{R_1+R_2}\right)V_{OL} + \left(\frac{R_2}{R_1+R_2}\right)V_{REF}$$

Shifting Factor:

$$\pm\left(\frac{R_2}{R_1+R_2}\right)V_{REF}$$

Example 32-1 Design of an Inverting Comparator with Hysteresis

Use the inverting bistable to design a high-gain, open-loop comparator having an upper trip point of 1V and a lower trip point of 0V if V_{OH} = 2V and V_{OL} = -2V.

Solution

Putting the values of this example into the above relationships gives

$$1 = \left(\frac{R_1}{R_1+R_2}\right) 2 + \left(\frac{R_2}{R_1+R_2}\right) V_{REF}$$

and

$$0 = \left(\frac{R_1}{R_1+R_2}\right) (-2) + \left(\frac{R_2}{R_1+R_2}\right) V_{REF}$$

Solving these two equations gives $3R_1 = R_2$ and V_{REF} = (2/3)V.

Hysteresis using Internal Positive Feedback

Simple comparator with internal positive feedback:

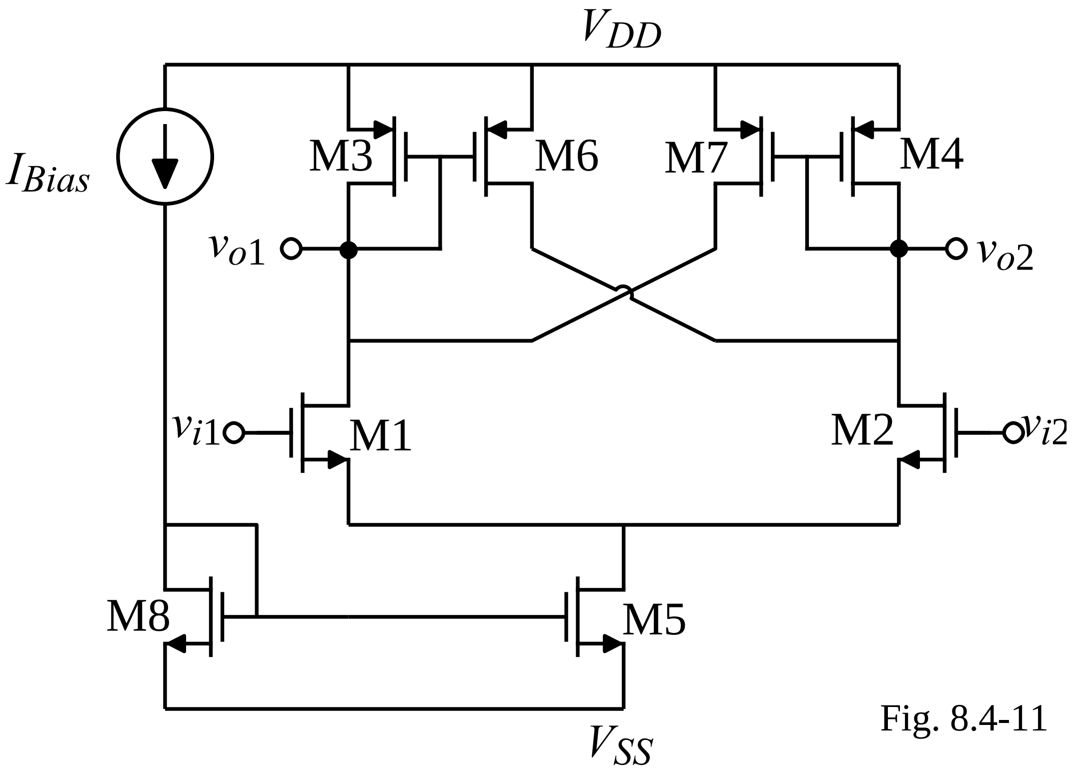


Fig. 8.4-11

Internal Positive Feedback - Upper Trip Point

Assume that the gate of M1 is on ground and the input to M2 is much smaller than zero. The resulting circuit is:

M1 on, M2 off → M3 on, M6 on (active), M4 and M7 off.

$\therefore \quad v_{o2}$ is high.

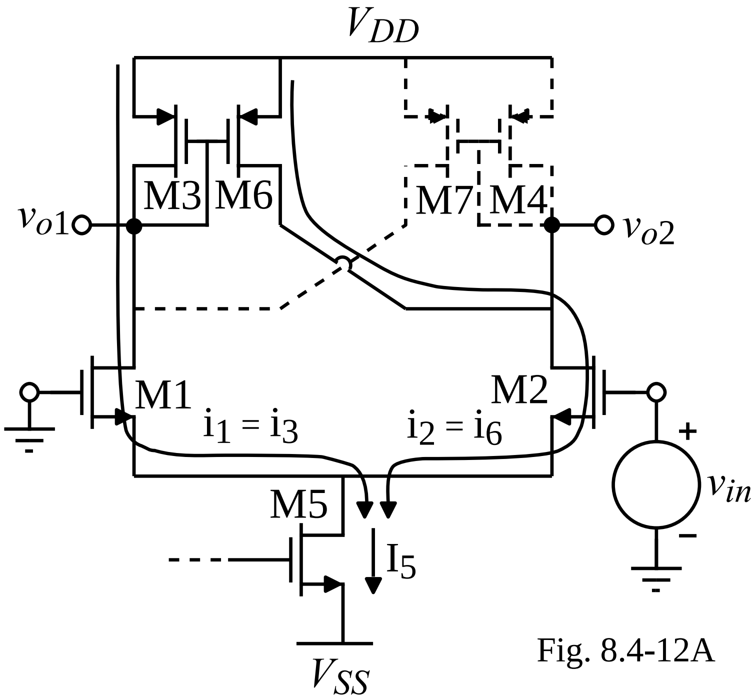


Fig. 8.4-12A

M6 wants to source the current $i_6 = \frac{W_6/L_6}{W_3/L_3} i_1$

As v_{in} begins to increase towards the trip point, the current flow through M2 increases. When $i_2 = i_6$, the upper trip point will occur.

$$\therefore \quad I_5 = i_1 + i_2 = i_3 + i_6 = i_3 + \left(\frac{W_6/L_6}{W_3/L_3}\right) i_3 = i_3 \left[1 + \frac{W_6/L_6}{W_3/L_3}\right] \rightarrow \; i_1 = i_3 = \frac{I_5}{1 + [(W_6/L_6)/(W_3/L_3)]}$$

Also, $i_2 = I_5 - i_1 = I_5 - i_3$

Knowing i_1 and i_2 allows the calculation of v_{GS1} and v_{GS2} which gives

$$V_{TRP}^{+} = v_{GS2} - v_{GS1} = \sqrt{\frac{2i_2}{\beta_2}} + V_{T2} - \sqrt{\frac{2i_1}{\beta_1}} - V_{T1}$$

Internal Positive Feedback - Lower Trip Point

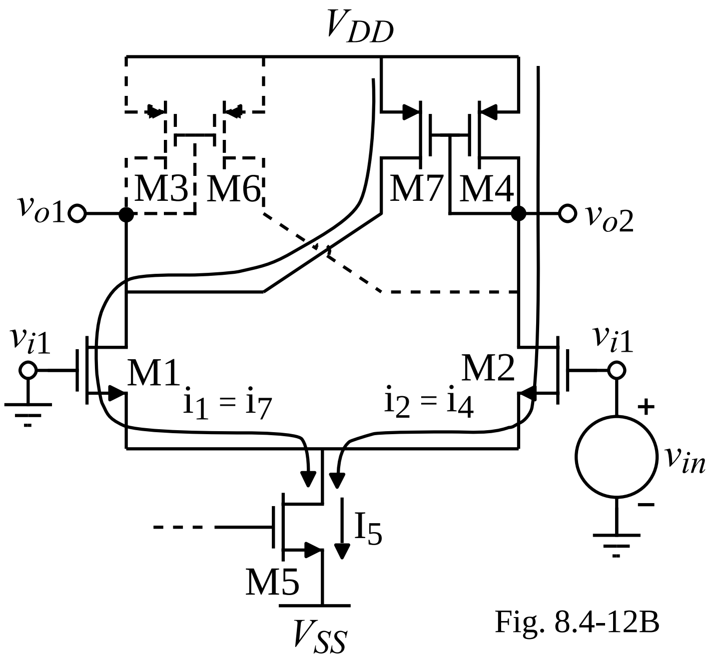


Fig. 8.4-12B

Assume that the gate of M1 is on ground and the input to M2 is much greater than zero. The resulting circuit is:

M2 on, M1 off → M4 and M7 on, M3 and M6 off.

$\therefore$ v_{o1} is high.

M7 wants to source the current $i_7 = \dfrac{W_7/L_7}{W_4/L_4}\, i_2$

As v_{in} begins to decrease towards the trip point, the current flow through M1 increases. When $i_1 = i_7$, the lower trip point will occur.

$$\therefore\ i_5 = i_1 + i_2 = i_7 + i_4 = \left(\frac{W_7/L_7}{W_4/L_4}\right) i_4 + i_4 = i_4\left[1 + \frac{W_7/L_7}{W_4/L_4}\right] \rightarrow i_2 = i_4 = \frac{i_5}{1 + [(W_7/L_7)/(W_4/L_4)]}$$

Also, $i_1 = i_5 - i_2 = i_5 - i_4$

Knowing i_1 and i_2 allows the calculation of v_{GS1} and v_{GS2} which gives

$$V_{TRP}^{-} = v_{GS2} - v_{GS1} = \sqrt{\frac{2i_2}{\beta_2}} + V_{T2} - \sqrt{\frac{2i_1}{\beta_1}} - V_{T1}$$

Example 32-2 - Calculation of Trip Voltages for a Comparator with Hysteresis

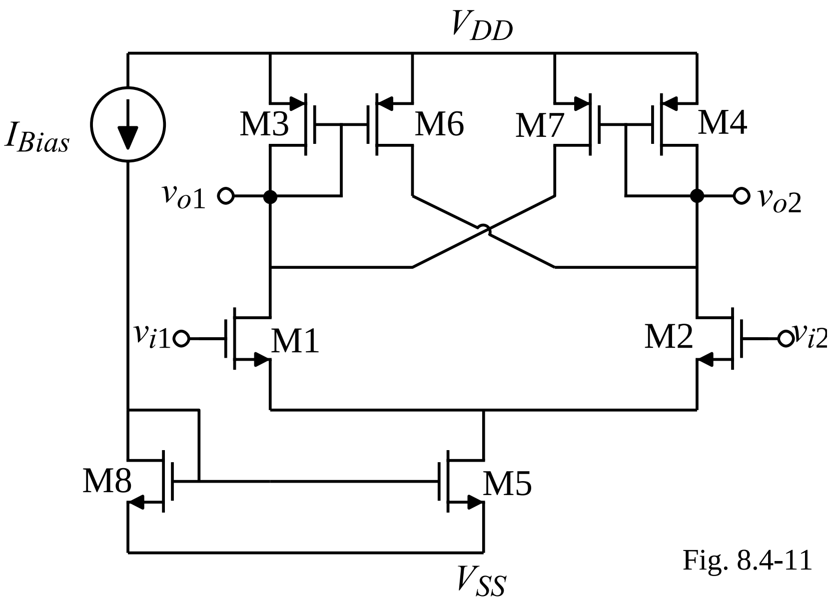


Fig. 8.4-11

Consider the circuit shown. If $K_N' = 110\mu A/V^2$, $K_P' = 50\mu A/V2$, and $V_{TN} = |V_{TP}| = 0.7V$, calculate the positive and negative threshold points if the device lengths are all 1 μm and the widths are given as: $W_1 = W_2 = W_6 = W_7 = 10\ \mu$m and $W_3 = W_4 = 2\ \mu$m. The gate of M1 is tied to ground and the input is the gate of M2. The current, $i_5 = 20\ \mu$A

Solution

To calculate the positive trip point, assume that the input has been negative and is heading positive.

$$i_6 = \frac{(W/L)_6}{(W/L)_3} i_3 = (5/1)(i_3) \quad \rightarrow \quad i_3 = \frac{i_5}{1 + [(W/L)_6/(W/L)_3]} = i_1 = \frac{20\ \mu A}{1+5} = 3.33\ \mu A$$

$$i_2 = i_5 - i_1 = 20 - 3.33 = 16.67\ \mu A \ \rightarrow \ v_{GS1} = \left(\frac{2i_1}{\beta_1}\right)^{1/2} + V_{T1} = \left(\frac{2\cdot 3.33}{(5)110}\right)^{1/2} + 0.7 = 0.81V$$

$$v_{GS2} = \left(\frac{2i_2}{\beta_2}\right)^{1/2} + V_{T2} = \left(\frac{2\cdot 16.67}{(5)110}\right)^{1/2} + 0.7 = 0.946V$$

$$\therefore \quad V_{TRP+} \cong v_{GS2} - v_{GS1} = 0.946 - 0.810 = 0.136V$$

Example 32-2 - Continued

Determining the negative trip point, similar analysis yields

$$i_4 = 3.33\ \mu\text{A}$$

$$i_1 = 16.67\ \mu\text{A}$$

$$v_{GS2} = 0.81\text{V}$$

$$v_{GS1} = 0.946\text{V}$$

$$V_{TRP-} \cong v_{GS2} - v_{GS1} = 0.81 - 0.946 = -0.136\text{V}$$

PSPICE simulation results of this circuit are shown below.

Remember the simple SAH model does not do a good job of modeling the knee or saturation voltage.

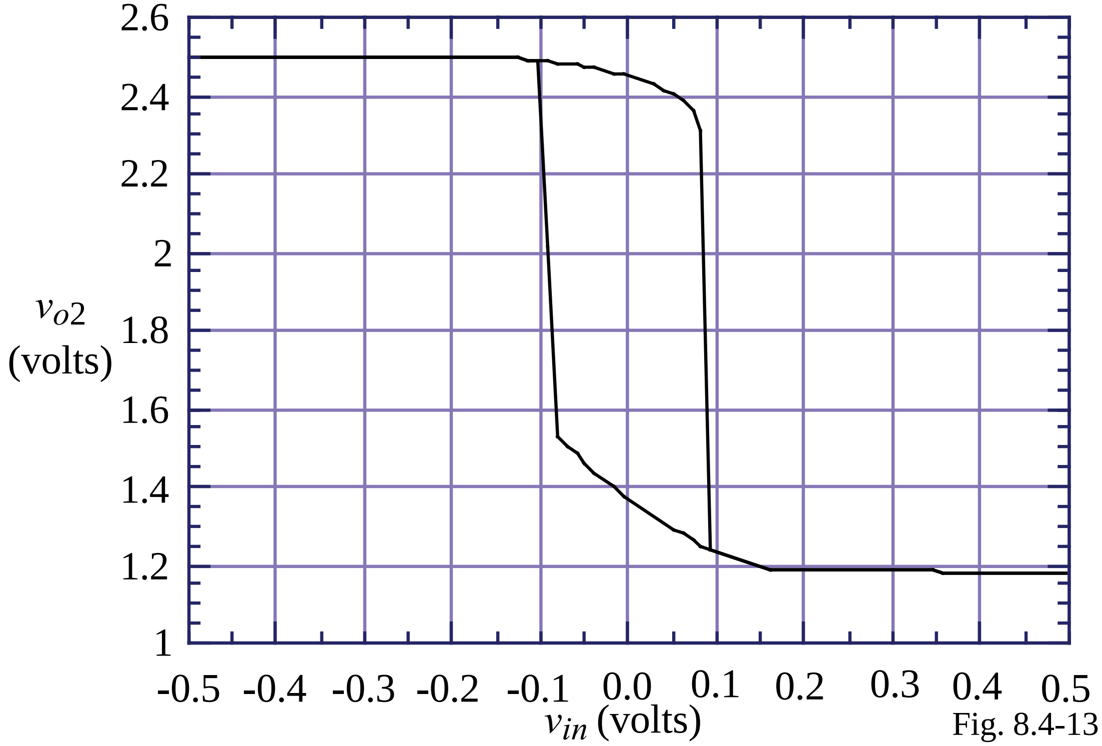


Fig. 8.4-13

Complete Comparator with Internal Hysteresis

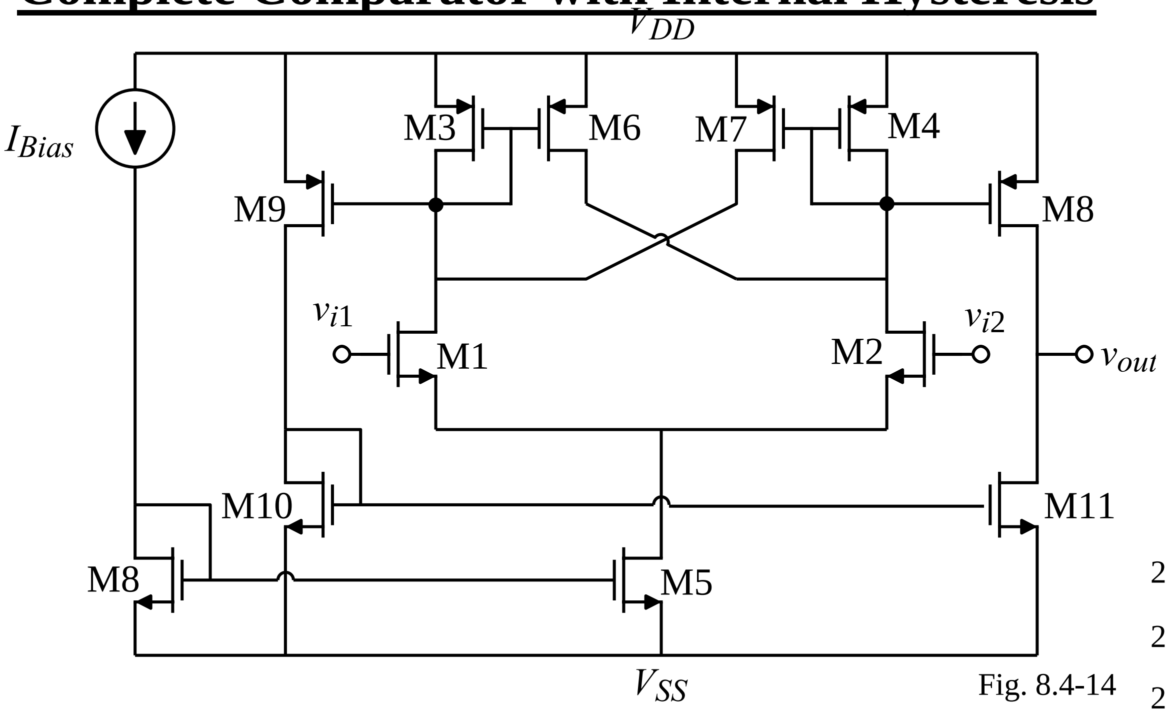
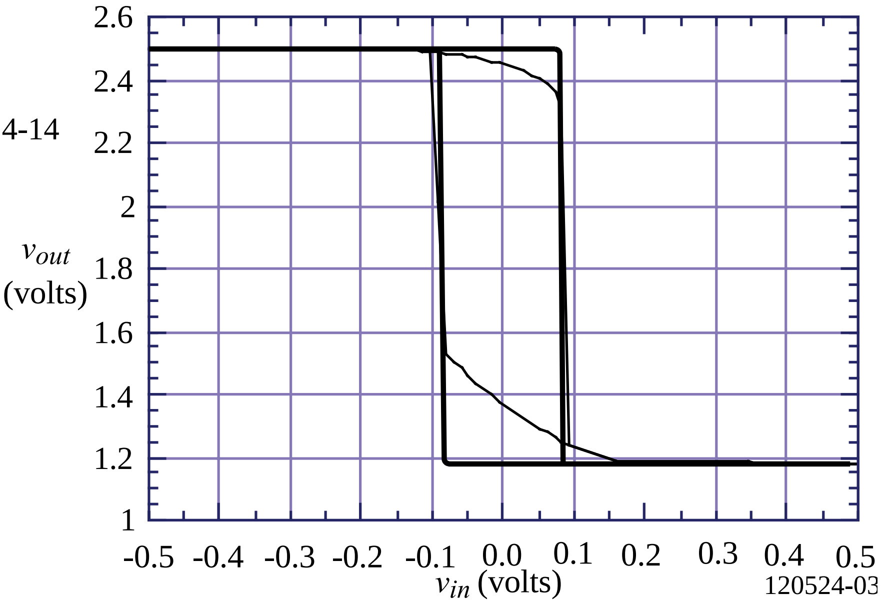


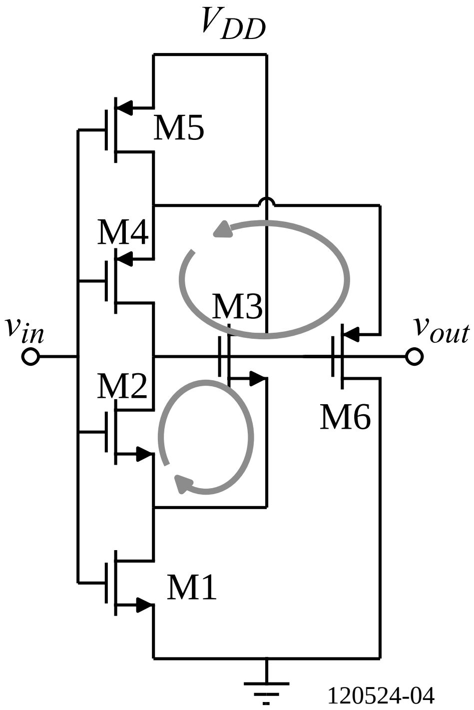
Fig. 8.4-14



Schmitt Trigger

The Schmitt trigger is a circuit that has better defined switching points.

Consider the following circuit:



How does this circuit work?

Assume the input voltage, v_{in}, is low and the output voltage, v_{out} , is high.

M3, M4 and M5 are on and M1, M2 and M6 are off.

When v_{in} is increased from zero, M2 starts to turn on causing M3 to start turning off. Positive feedback causes M2 to turn on further and eventually both M1 and M2 are on and the output is at zero.

The upper switching point, $V_{TRP}{}^{+}$ is found as follows:

When v_{in} is low, the voltage at the source of M2 (M3) is

$$v_{S2} = V_{DD}\text{-}V_{TN3}$$

$V_{TRP}{}^{+} = v_{in}$ when M2 turns on given as $V_{TRP}{}^{+} = V_{TN2} + v_{S2}$

$V_{TRP}{}^{+}$ occurs when the input voltage causes the currents in M3 and M1 to be equal.

Schmitt Trigger – Continued

Thus, $$i_{D1} = \beta_1(V_{TRP^+} - V_{TN1})^2 = \beta_3(V_{DD} - v_{S2} - V_{TN3})^2 = i_{D3}$$

which can be written as, assuming that $V_{TN2} = V_{TN3}$,

$$\beta_1(V_{TRP^+} - V_{TN1})^2 = \beta_3(V_{DD} - V_{TRP^+})^2 \Rightarrow \quad V_{TRP^+} = \frac{V_{TN1} + \sqrt{\beta_3/\beta_1}\, V_{DD}}{1 + \sqrt{\beta_3/\beta_1}}$$

The switching point, V_{TRP^-} is found in a similar manner and is:

$$\beta_5(V_{DD} - V_{TRP^-} - V_{TP5})^2 = \beta_6(V_{TRP^-})^2 \quad \Rightarrow \quad V_{TRP^-} = \frac{\sqrt{\beta_5/\beta_6}(V_{DD} - V_{TP5})}{1 + \sqrt{\beta_5/\beta_6}}$$

The bistable characteristic is,

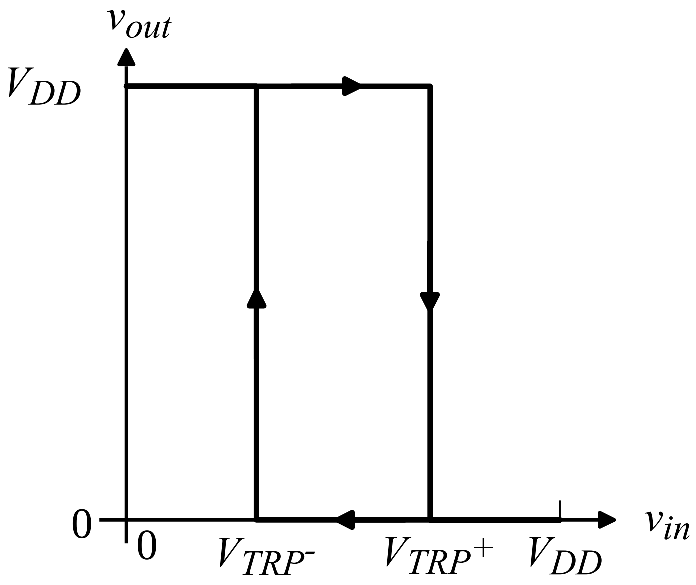


Fig. 8.4-16

SIMPLE LATCHES

Regenerative Comparators

Regenerative comparators use positive feedback to accomplish the comparison of two signals. Latches can have a faster switching speed than the previous comparators.

NMOS and PMOS latch:

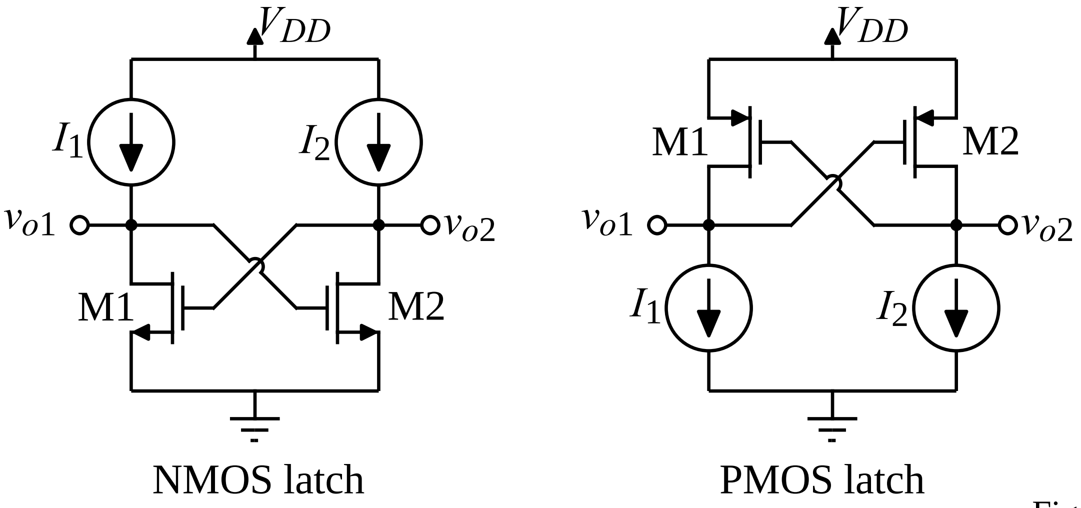


Fig. 8.5-3

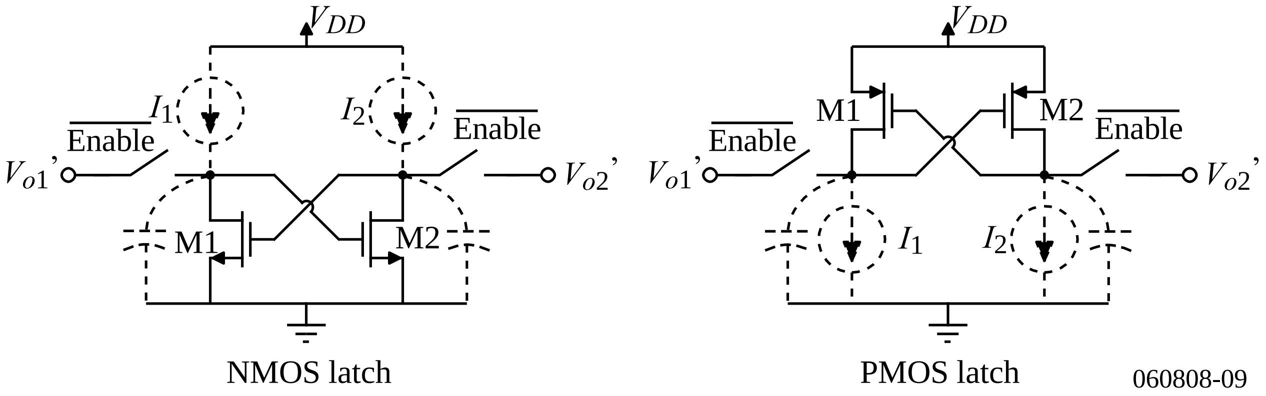
Operating Modes of the Latch

The latch has two modes of operation – enable or latch and $\overline{\text{Enable}}$ (enable_bar) or $\overline{\text{Latch}}$ (latch_bar).

1.) During the Enable_bar, the latch is turned off (currents are removed) and the unknown inputs are applied to it. The parasitic capacitance at the latch nodes hold the unknown voltage.

2.) During Enable, the latch is turned on, and the positive feedback acts on the applied inputs and causes one side of the latch to go high and the other side to go low.

Enable_bar:



The inputs are initially applied to the outputs of the latch.

V_{o1}' = initial input applied to v_{o1}

Step Response of a Latch (Enable)

Circuit:

R_i and C_i are the resistance and capacitance seen to ground from the *i*-th transistor.

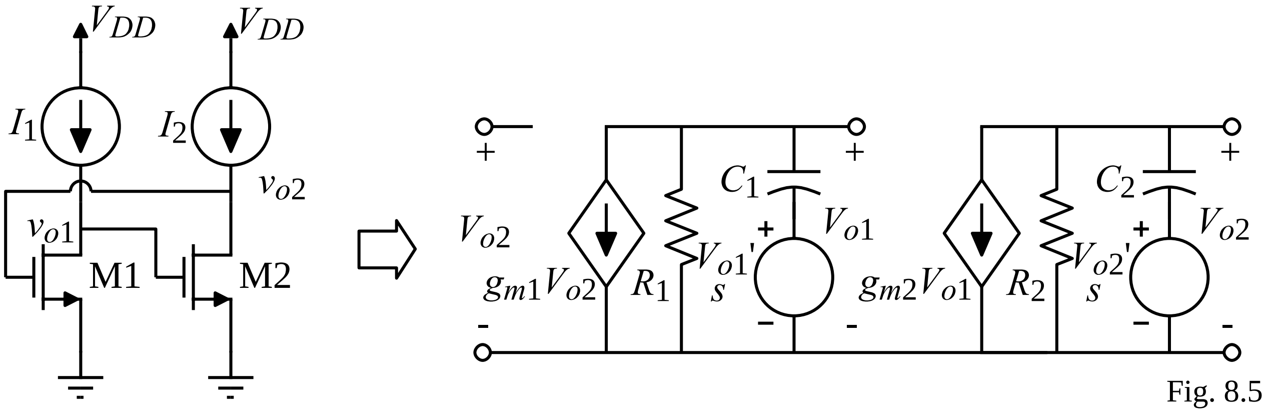


Fig. 8.5-4

Nodal equations:

$$g_{m1}V_{o2}+G_1V_{o1}+sC_1\left(V_{o1}-\frac{V_{o1}'}{s}\right) = g_{m1}V_{o2}+G_1V_{o1}+sC_1V_{o1}-C_1V_{o1}' = 0$$

$$g_{m2}V_{o1}+G_2V_{o2}+sC_2\left(V_{o2}-\frac{V_{o2}'}{s}\right) = g_{m2}V_{o1}+G_2V_{o2}+sC_2V_{o2}-C_2V_{o2}' = 0$$

Solving for V_{o1} and V_{o2} gives,

$$V_{o1} = \frac{R_1C_1}{sR_1C_1+1}V_{o1}' - \frac{g_{m1}R_1}{sR_1C_1+1}V_{o2} = \frac{\tau_1}{s\tau_1+1}V_{o1}' - \frac{g_{m1}R_1}{s\tau_1+1}V_{o2}$$

$$V_{o2} = \frac{R_2C_2}{sR_2C_2+1}V_{o2}' - \frac{g_{m2}R_2}{sR_2C_2+1}V_{o1} = \frac{\tau_2}{s\tau_2+1}V_{o2}' - \frac{g_{m2}R_2}{s\tau_2+1}V_{o1}$$

Defining the output, ΔV_o, and input, ΔV_i, as

$$\Delta V_o = V_{o2}-V_{o1} \quad \text{and} \quad \Delta V_i = V_{o2}'-V_{o1}'$$

Step Response of the Latch - Continued

Solving for ΔV_o gives, $$\Delta V_o = V_{o2}-V_{o1} = \frac{\tau}{s\tau+1}\Delta V_i + \frac{g_mR}{s\tau+1}\Delta V_o$$

or

$$\Delta V_o = \frac{\tau\,\Delta V_i}{s\tau+(1-g_mR)} = \frac{\dfrac{\tau\,\Delta V_i}{1-g_mR}}{\dfrac{s\tau}{1-g_mR}+1} = \frac{\tau'\,\Delta V_i}{s\tau'+1}$$

where

$$\tau' = \frac{\tau}{1-g_mR}$$

Taking the inverse Laplace transform gives

$$\Delta v_o(t) = \Delta V_i\, e^{-t/\tau'} = \Delta V_i\, e^{-t(1-g_mR)/\tau} \approx e^{g_mRt/\tau}\Delta V_i, \qquad \text{if } g_mR >>1.$$

Define the latch time constant as

$$\tau_L = |\tau'| \approx \frac{\tau}{g_mR} = \frac{C}{g_m} = \frac{0.67WLC_{ox}}{\sqrt{2K'(W/L)I}} = 0.67C_{ox}\sqrt{\frac{WL^3}{2K'I}}$$

if $C \approx C_{gs}$.

$\therefore$ $$\Delta V_{out}(t) = e^{t/\tau_L}\,\Delta V_i$$

Step Response of a Latch - Continued

Normalize the output voltage by (V_{OH}-V_{OL}) to get

$$\frac{\Delta V_{out}(t)}{V_{OH}-V_{OL}} = e^{t/\tau_L}\frac{\Delta V_i}{V_{OH}-V_{OL}}$$

which is plotted as,

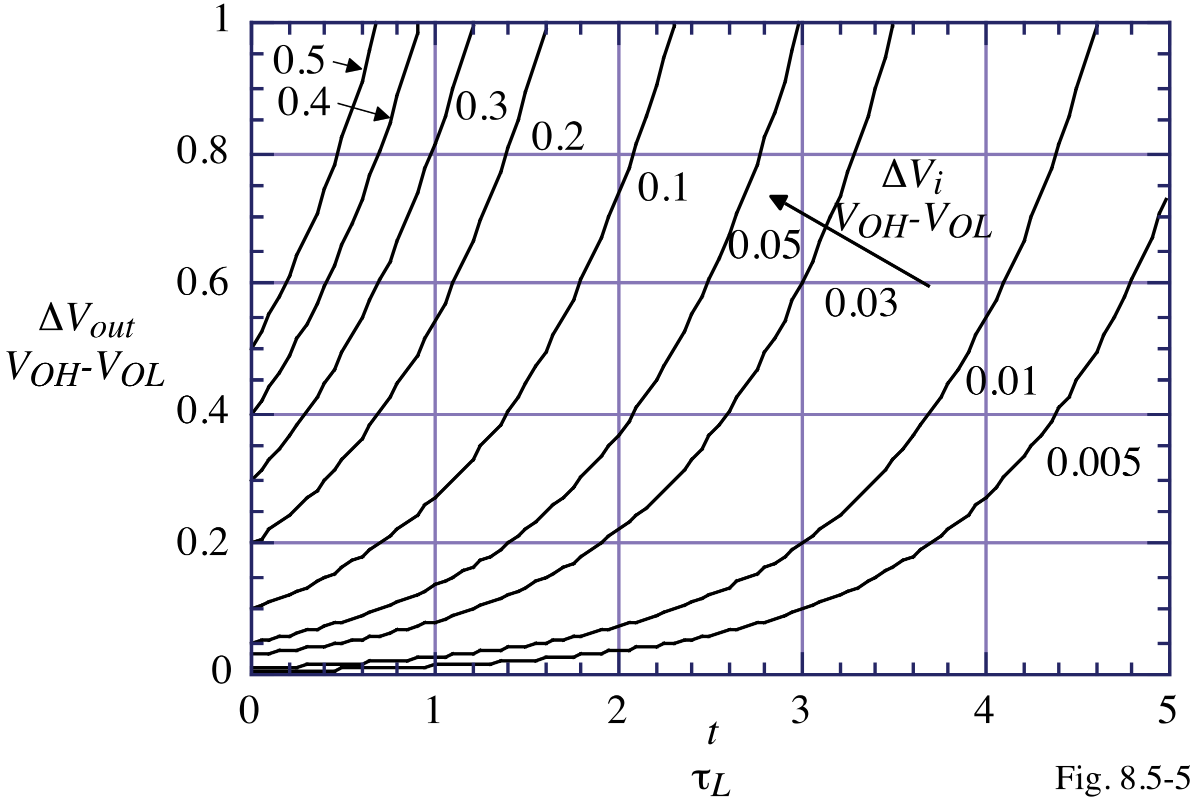


Fig. 8.5-5

The propagation delay time is $t_p = \tau_L\, ln\left(\frac{V_{OH}- V_{OL}}{2\Delta V_i}\right)$

Note that the larger the ΔV_i, the faster the response.

Example 32-3 - Time Domain Characteristics of a Latch.

Find the propagation time delay for the NMOS if the *W/L* of the latch transistors is 5μm/0.5μm and the latch dc current is 10μA when $\Delta V_i = 0.1(V_{OH}\text{-}V_{OL})$ and $\Delta V_i = 0.01(V_{OH}\text{-}V_{OL})$.

Solution

The transconductance of the latch transistors is

$$g_m = \sqrt{2\cdot120\cdot10\cdot10} = 155\mu\text{S}$$

The output conductance is 0.6μS which gives g_mR of 93V/V. Since g_mR is greater than 1, we can use the above results. Therefore the latch time constant is found as

$$\tau_L = 0.67C_{ox}\sqrt{\frac{WL^3}{2K'I}} = 0.67(60.6\text{x}10^{-4})\sqrt{\frac{(5\cdot0.5)\text{x}10^{-24}}{2\cdot120\text{x}10^{-6}\cdot10\text{x}10^{-6}}} = 0.131\text{ns}$$

Since the propagation time delay is the time when the output is $0.5(V_{OH}\text{-}V_{OL})$, then using the above results or Fig. 8.5-5 we find for $\Delta V_i = 0.01(V_{OH}\text{-}V_{OL})$ that $t_p = 3.91\tau_L = 0.512$ns and for $\Delta V_i = 0.1(V_{OH}\text{-}V_{OL})$ that $t_p = 1.61\tau_L = 0.211$ns.

Comparator using a Latch with a Built-In Reference[†]

How does it operate?

1.) Devices in shaded region operate in the triode region.

2.) When the latch/reset goes high, the upper cross-coupled inverter-latch regenerates. The drain currents of M5 and M6 are steered to obtain a final state determined by the mismatch between the R_1 and R_2 resistances.

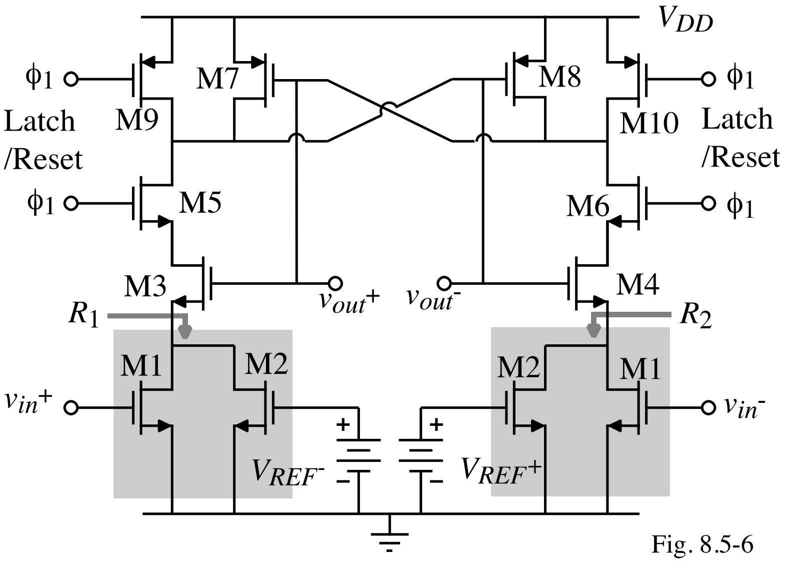


Fig. 8.5-6

$$\frac{1}{R_1} = K_N\left[\frac{W_1}{L}(v_{in}^+ - V_T) + \frac{W_2}{L}(V_{REF}^- - V_T)\right]$$

and

$$\frac{1}{R_2} = K_N\left[\frac{W_1}{L}(v_{in}^- - V_T) + \frac{W_2}{L}(V_{REF}^+ - V_T)\right]$$

3.) The input voltage which causes $R_1 = R_2$ is $v_{in}(\text{threshold}) = (W_2/W_1)V_{REF}$

$W_2/W_1 = 1/4$ generates a threshold of $\pm 0.25V_{REF}$.

Performance → 20Ms/s & 200μW

[†] T.B. Cho and P.R. Gray, “A 10b, 20Msamples/s, 35mW pipeline A/D Converter,” *IEEE J. Solid-State Circuits*, vol. 30, no. 3, pp. 166-172, March 1995.

Simple, Low Power Latched Comparator[†]

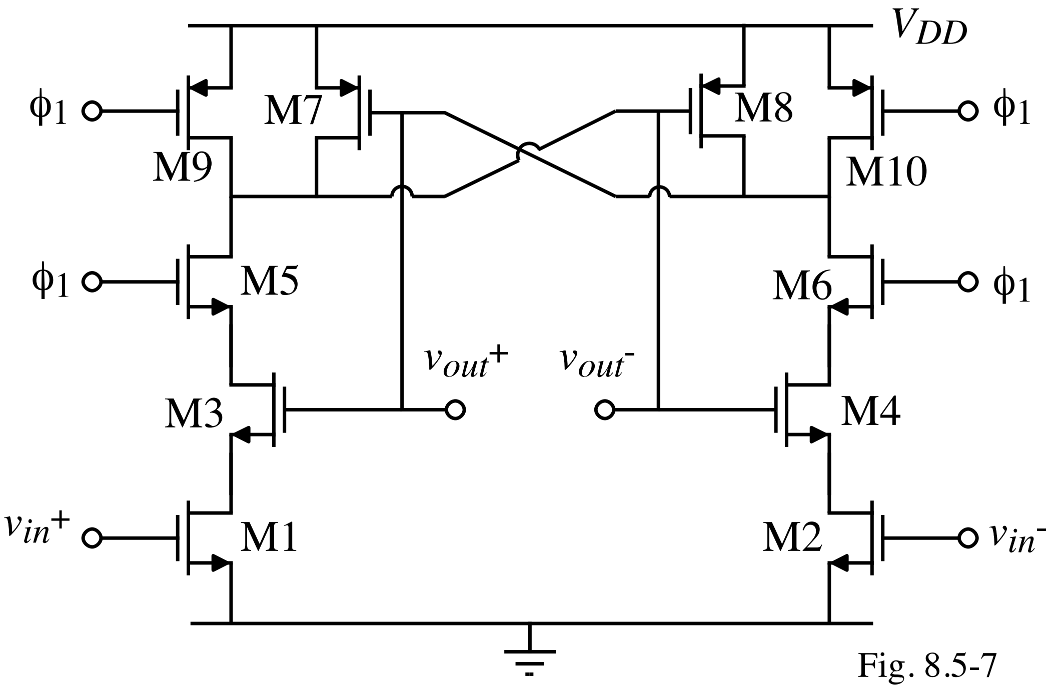


Fig. 8.5-7

Dissipated 50µW when clocked at 2MHz.

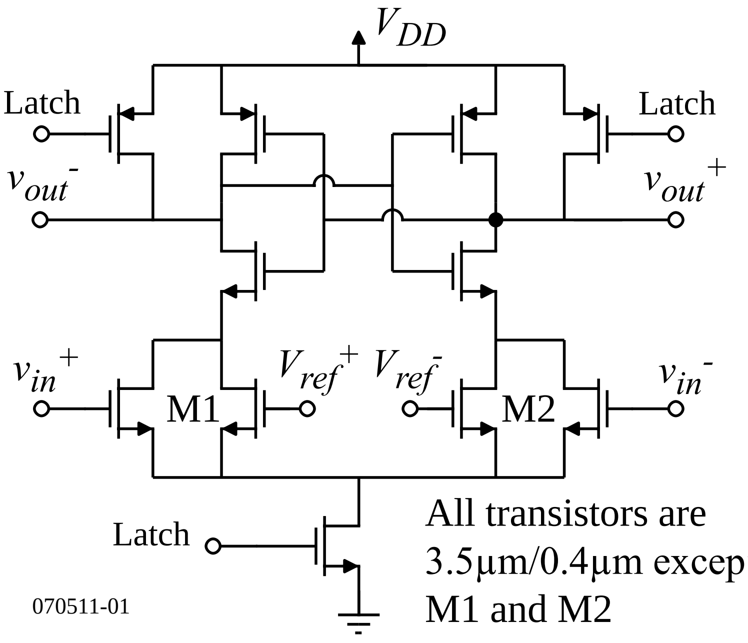
Self-referenced

[†] A. Coban, "1.5V, 1mW, 98-dB Delta-Sigma ADC", Ph.D. dissertation, School of ECE, Georgia Tech, Atlanta, GA 30332-0250.

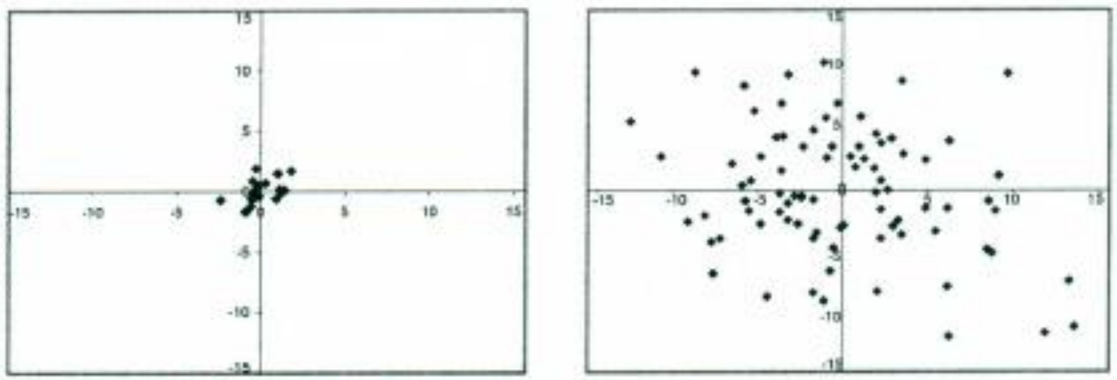
Tail-Referenced Latch

The previous two latches experience poor input offset voltage characteristics because the input devices are working in the linear region during the latch phase. The latch below keeps the input devices in the saturation region. The resulting larger gain of the input devices reduces the input offset voltage as shown.

The input offset voltage of the tail referenced latch is compared between two latches with the referenced latch for 100 samples. The *x*-axis is the deviation from the mean of the first latch and the *y*-axis is the deviation of the mean of the second latch.



All transistors are 3.5µm/0.4µm except M1 and M2



(A) Tail-Latch Referenced Comparator (B) Referenced Comparator

CMOS Latch

Circuit:

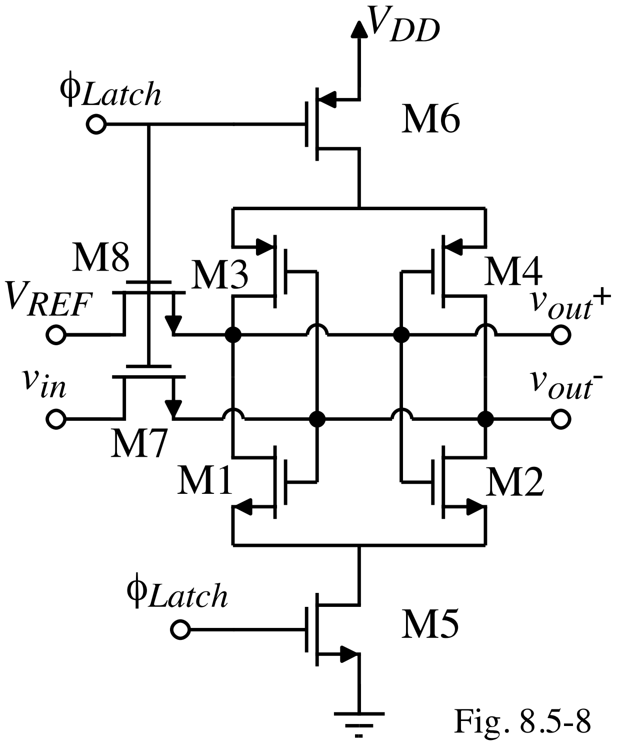


Fig. 8.5-8

Input offset voltage distribution:

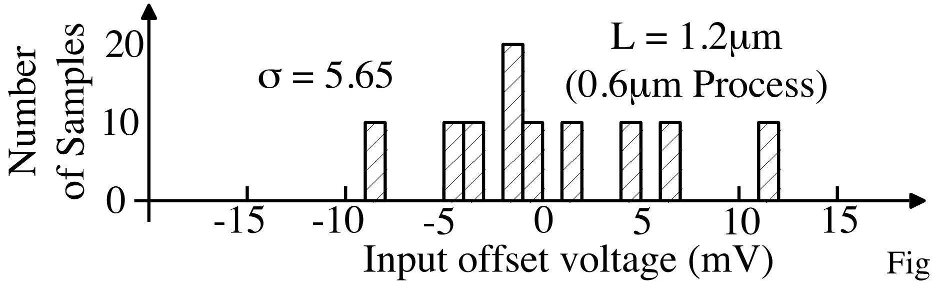
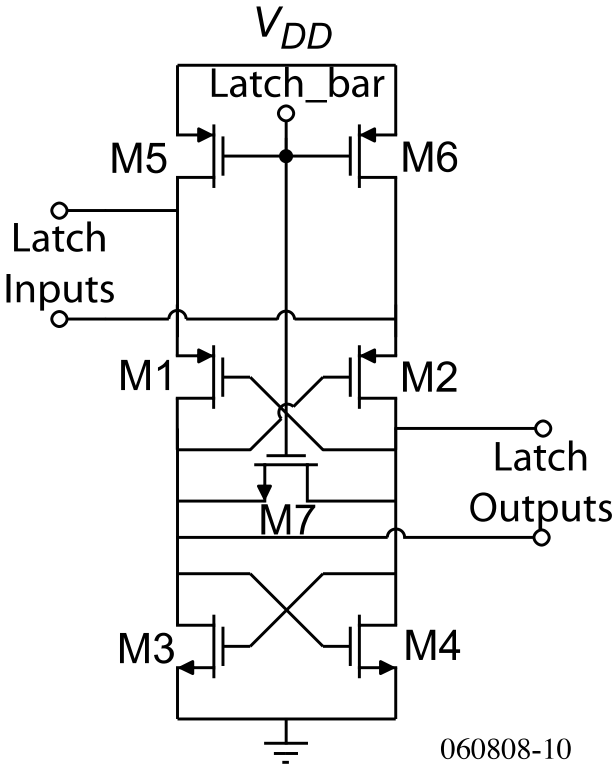


Fig. 8.5-9

CMOS Latch with Different Inputs and Outputs



When Latch_bar is high, M5 and M6 are off, M7 is on, and the latch is disabled and the outputs are shorted together.

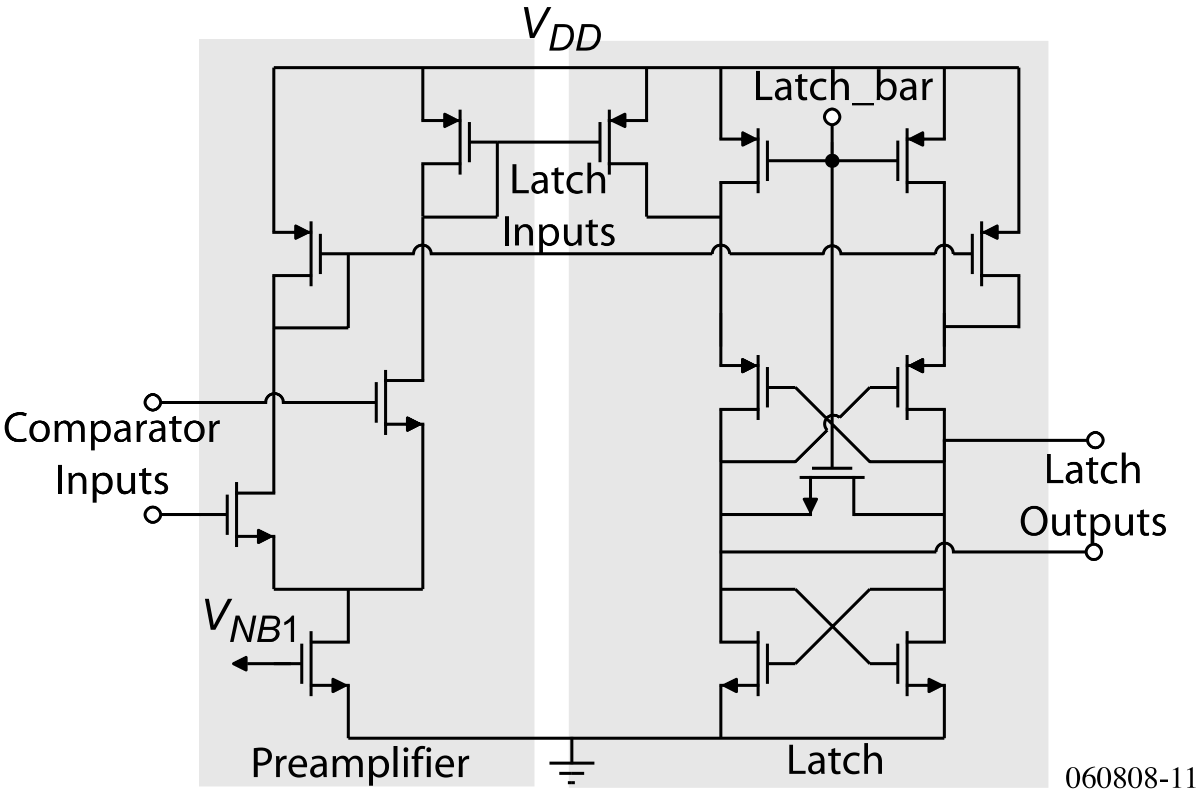
When Latch_bar is low, the input voltages stored at the sources of M1 and M2 will cause one of the latch outputs to be high and the other to be low.

The source of M1 and M2 that is higher will have a larger source-gate voltage resulting in a larger transconductance and more gain than the other transistor.

Metastability

Metastability is the condition where the latch cannot make a decision in the time allocated. Normally due to the fact that the input is small (within the input resolution range).

Metastability can be improved (reduced) by increasing the gain of the comparator by preceding it with an amplifier to keep the signal input to the latch as large as possible under all conditions. The preamplifier also reduced the input offset voltage.



SUMMARY

- The performance of open-loop comparators can be improved by the use of autozeroing and hysteresis
- Discrete-time comparators must work with clocks
- Regenerative comparators (latches) use positive feedback
- The propagation delay of the regenerative comparator is slow at the beginning and speeds up rapidly as time increases
- The highest speed comparators will use a combination of open-loop comparators and latches