LECTURE 31 – OPEN-LOOP COMPARATORS

LECTURE ORGANIZATION

Outline

- Characterization of comparators
- Dominant pole, open-loop comparators
- Two-pole, open-loop comparators
- Summary

***CMOS Analog Circuit Design*, 3rd Edition Reference**

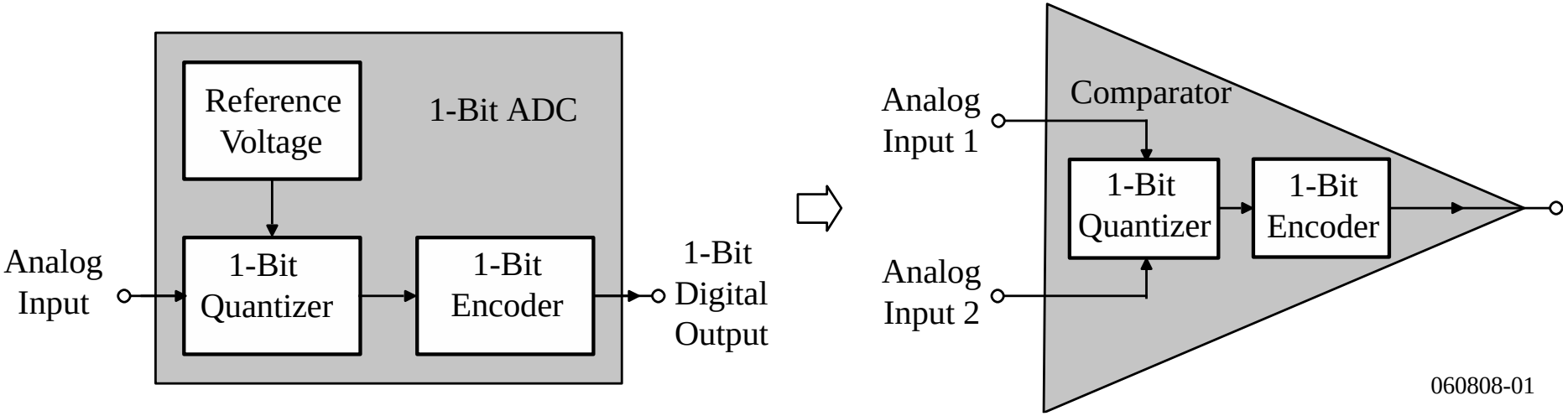
Pages 444-466

CHARACTERIZATION OF COMPARATORS

What is a Comparator?

The comparator is a circuit that compares one analog signal with another analog signal or a reference voltage and outputs a binary signal based on the comparison.

The comparator is basically a 1-bit analog-to-digital converter:



Comparator symbol:

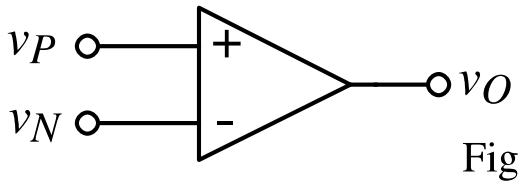


Fig. 8.1-1

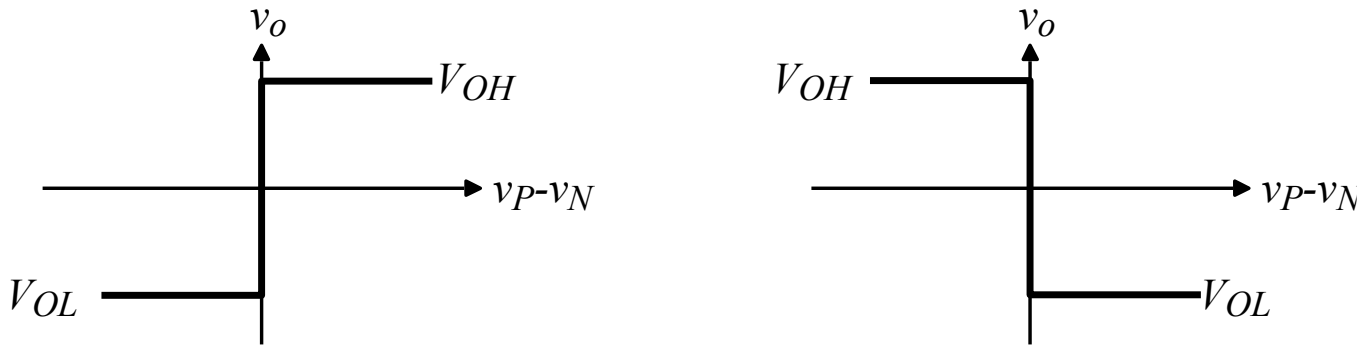
Noninverting and Inverting Comparators

The comparator output is binary with the two-level outputs defined as,

V_{OH} = the high output of the comparator

V_{OL} = the low level output of the comparator

Voltage transfer function of a Noninverting and Inverting Comparator:



Noninverting Comparator Inverting Comparator

Fig. 8.1-2A

Infinite Gain Comparator

Voltage transfer function curve:

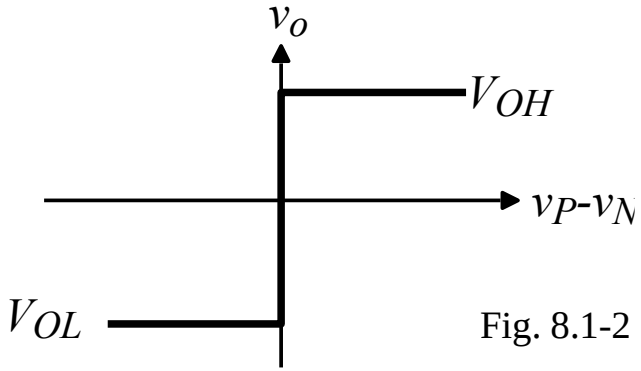
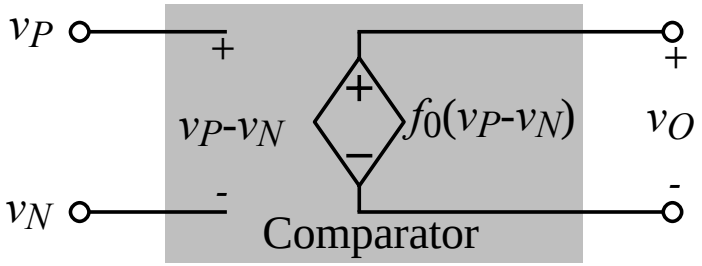


Fig. 8.1-2

Model:



$$f_0(v_P\text{-}v_N) = \begin{cases} V_{OH} \text{ for } (v_P\text{-}v_N) > 0 \\ V_{OL} \text{ for } (v_P\text{-}v_N) < 0 \end{cases}$$

Fig. 8.1-3

$$\text{Gain} = A_V = \lim_{\Delta V \to 0} \frac{V_{OH}\text{-}V_{OL}}{\Delta V} \quad \text{where } \Delta V \text{ is the input voltage change}$$

Finite Gain Comparator

Voltage transfer curve:

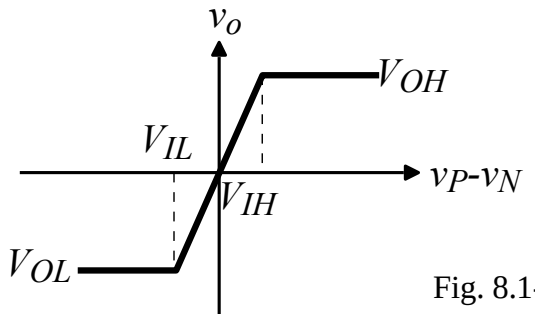


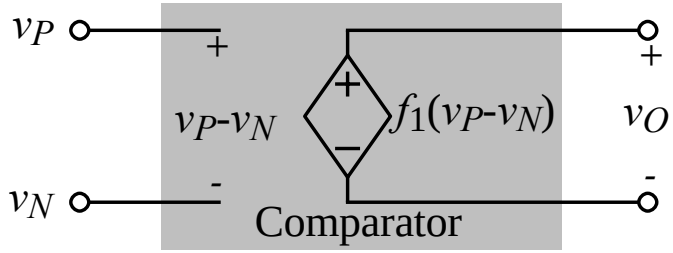
Fig. 8.1-4

where for a noninverting comparator,

V_{IH} = smallest input voltage at which the output voltage is V_{OH}

V_{IL} = largest input voltage at which the output voltage is V_{OL}

Model:



$$f_1(v_P\text{-}v_N) = \begin{cases} V_{OH} \text{ for } (v_P\text{-}v_N) > V_{IH} \\ A_v(v_P\text{-}v_N) \text{ for } V_{IL} < (v_P\text{-}v_N) < V_{IH} \\ V_{OL} \text{ for } (v_P\text{-}v_N) < V_{IL} \end{cases}$$

Fig. 8.1-5

The voltage gain is $A_v = \dfrac{V_{OH} - V_{OL}}{V_{IH} - V_{IL}}$

Input Offset Voltage of a Comparator

Voltage transfer curve:

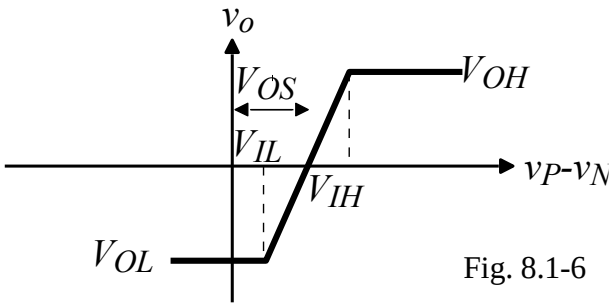


Fig. 8.1-6

V_{OS} = the input voltage necessary to make the output equal $\frac{V_{OH}+V_{OL}}{2}$ when $v_P = v_N$.

Model:

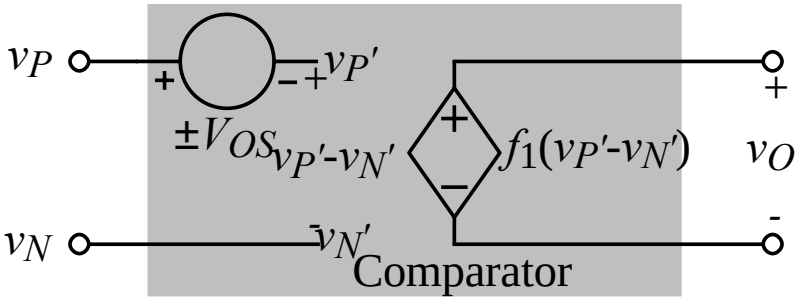


Fig. 8.1-7

Other aspects of the model:

ICMR = input common mode voltage range (all transistors remain in saturation)

R_{in} = input differential resistance

R_{icm} = common mode input resistance

Comparator Noise

Noise of a comparator is modeled as if the comparator were biased in the transition region.

Noise leads to an uncertainty in the transition region causing jitter or phase noise.

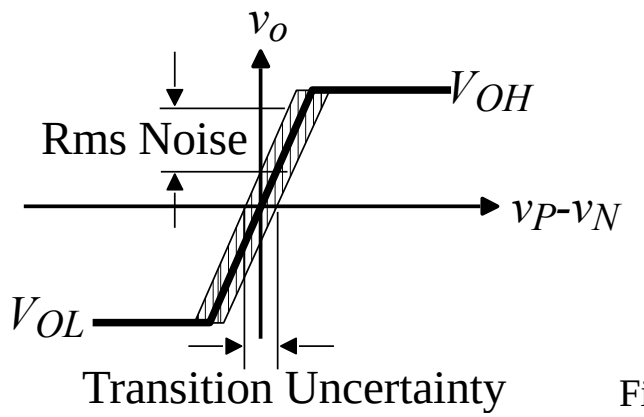


Fig. 8.1-8

Input Common Mode Range

Because the input is analog and normally differential, the input common mode range of the comparator is also important.

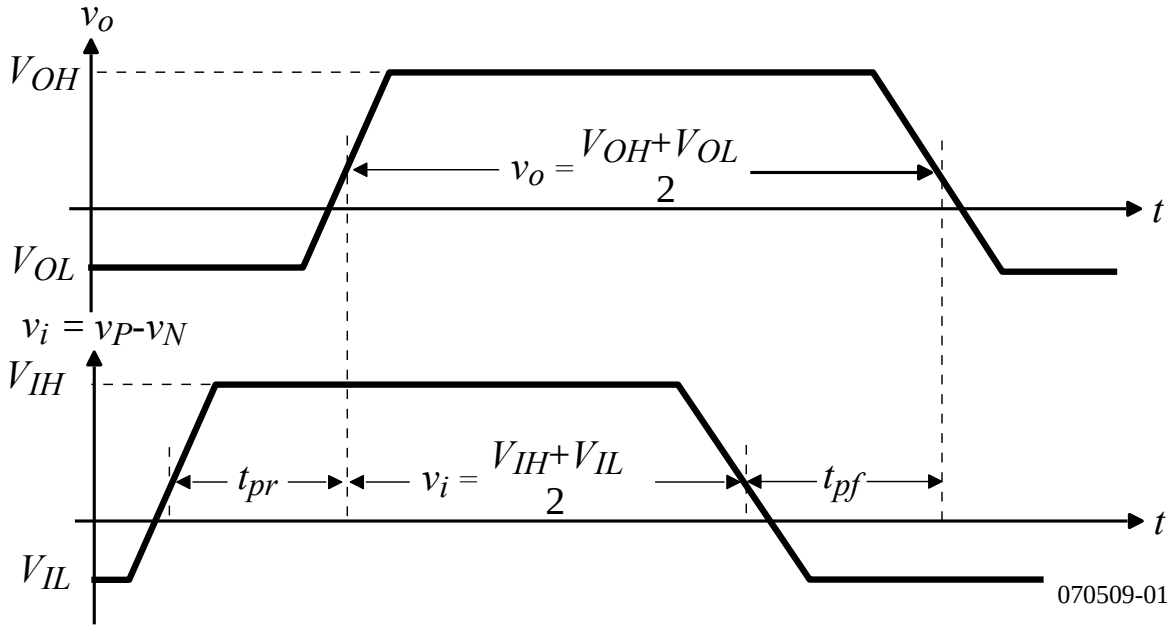
Input common mode range (*ICMR*):

> *ICMR* = the voltage range over which the input common-mode signal can vary without influence the differential performance

As we have seen before, the *ICMR* is defined by the common-mode voltage range over which all MOSFETs remain in the saturation region.

Propagation Delay Time

Rising propagation delay time:



Propagation delay time =

$$\frac{\text{Rising propagation delay time + Falling propagation delay time}}{2} = \frac{t_{pr} + t_{pf}}{2}$$

Linear Frequency Response – Dominant Single-Pole

Model:

$$A_v(s) = \frac{A_v(0)}{\frac{s}{\omega_c} + 1} = \frac{A_v(0)}{s\tau_c + 1}$$

where

$A_V(0)$ = dc voltage gain of the comparator

$\omega_C = \frac{1}{\tau_c}$ = -3dB frequency of the comparator or the magnitude of the pole

Step Response:

$$v_O(t) = A_V(0)\,[1 - e^{-t/\tau_C}]V_{in}$$

where

V_{in} = the magnitude of the step input.

Maximum slope of the step response:

$$\frac{dv_O(t)}{dt} = \frac{A_V(0)}{\tau_c} e^{-t/\tau_C} V_{in}$$

The maximum slope occurs at $t = 0$ giving,

$$\left.\frac{dv_O(t)}{dt}\right|_{t=0} = \frac{A_V(0)}{\tau_c} V_{in}$$

Propagation Time Delay

The rising propagation time delay for a single-pole comparator is:

$$\frac{V_{OH}-V_{OL}}{2} = A_v(0)\,[1 - e^{-t_p/\tau_c}]V_{in} \quad \rightarrow \quad t_p = \tau_c\, ln\left[\frac{1}{1 - \frac{V_{OH}-V_{OL}}{2A_v(0)V_{in}}}\right]$$

Define the minimum input voltage to the comparator as,

$$V_{in}(\text{min}) = \frac{V_{OH}-V_{OL}}{A_v(0)} \quad \rightarrow \quad t_p = \tau_c\, ln\left[\frac{1}{1 - \frac{V_{in}(\text{min})}{2V_{in}}}\right]$$

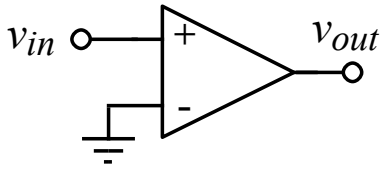
Define k as the ratio, V_{in}, to the minimum input voltage, $V_{in}(\text{min})$,

$$k = \frac{V_{in}}{V_{in}(\text{min})} \quad \rightarrow \quad t_p = \tau_c\, ln\left[\frac{2k}{2k-1}\right]$$

Thus, if $k = 1$, $t_p = 0.693\tau_c$.

Illustration:

Obviously, the more overdrive applied to the input, the smaller the propagation delay time.



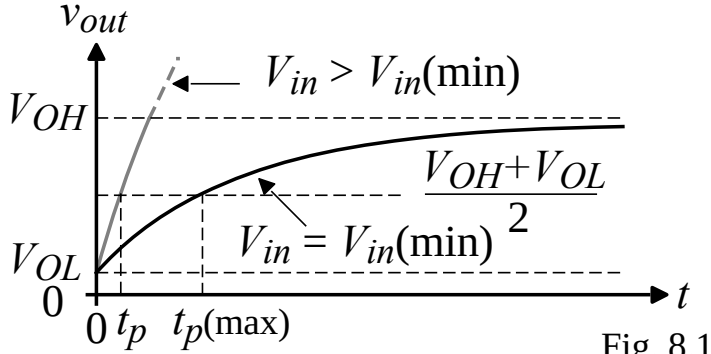


Fig. 8.1-10

Dynamic Characteristics - Slew Rate of a Comparator

If the rate of rise or fall of a comparator becomes large, the dynamics may be limited by the slew rate.

Slew rate comes from the relationship,

$$i = C\frac{dv}{dt}$$

where i is the current through a capacitor and v is the voltage across it.

If the current becomes limited, then the voltage rate becomes limited.

Therefore for a comparator that is slew rate limited we have,

$$t_p = \Delta T = \frac{\Delta V}{SR} = \frac{V_{OH} - V_{OL}}{2 \cdot SR}$$

where

SR = slew rate of the comparator.

If $SR <$ |maximum slope|, then the comparator is slewing.

Example 31-1 - Propagation Delay Time of a Comparator

Find the propagation delay time of an open loop comparator that has a dominant pole at 10^3 radians/sec, a dc gain of 10^4, a slew rate of 1V/μs, and a binary output voltage swing of 1V. Assume the applied input voltage is 10mV.

Solution

The input resolution for this comparator is $1V/10^4$ or 0.1mV. Therefore, the 10mV input is 100 times larger than v_{in}(min) giving a k of 100. Therefore, we get

$$t_p = \frac{1}{10^3} ln\left(\frac{2\cdot 100}{2\cdot 100-1}\right) = 10^{-3}\, ln\left(\frac{200}{199}\right) = 5.01\mu s$$

For slew rate considerations, we get

$$\text{Maximum slope} = \frac{10^4}{10^{-3}} \cdot 10mV = 10^5 \text{ V/sec.} = 0.1V/\mu s.$$

Therefore, the propagation delay time for this case is limited by the linear response and is 5.01μs.

DOMINANT POLE, OPEN-LOOP COMPARATORS

Dominant Pole Comparators

Any of the self-compensated op amps provide a straight-forward implementation of an open loop comparator without any modification.

The previous characterization gives the relationships for:

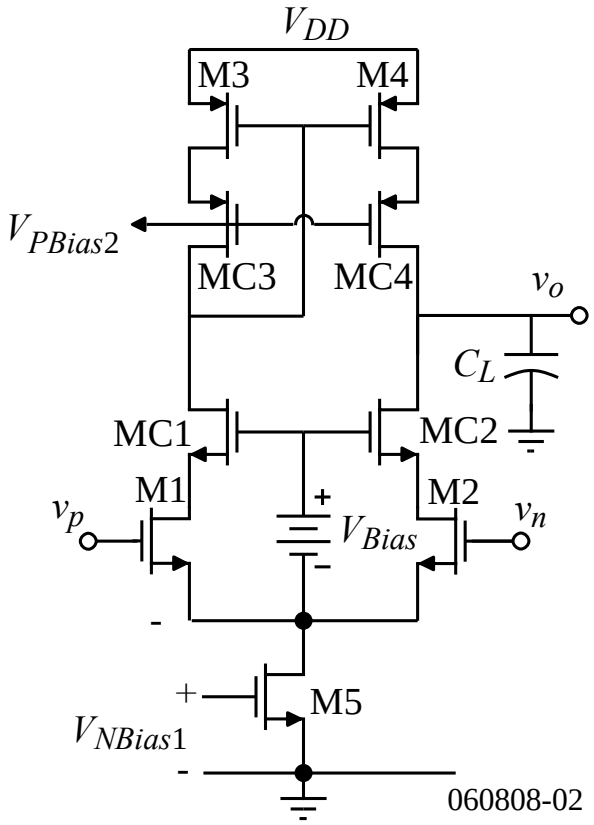
1.) The static characteristics

- Gain
- Input offset
- Noise

2.) The dynamic characteristics

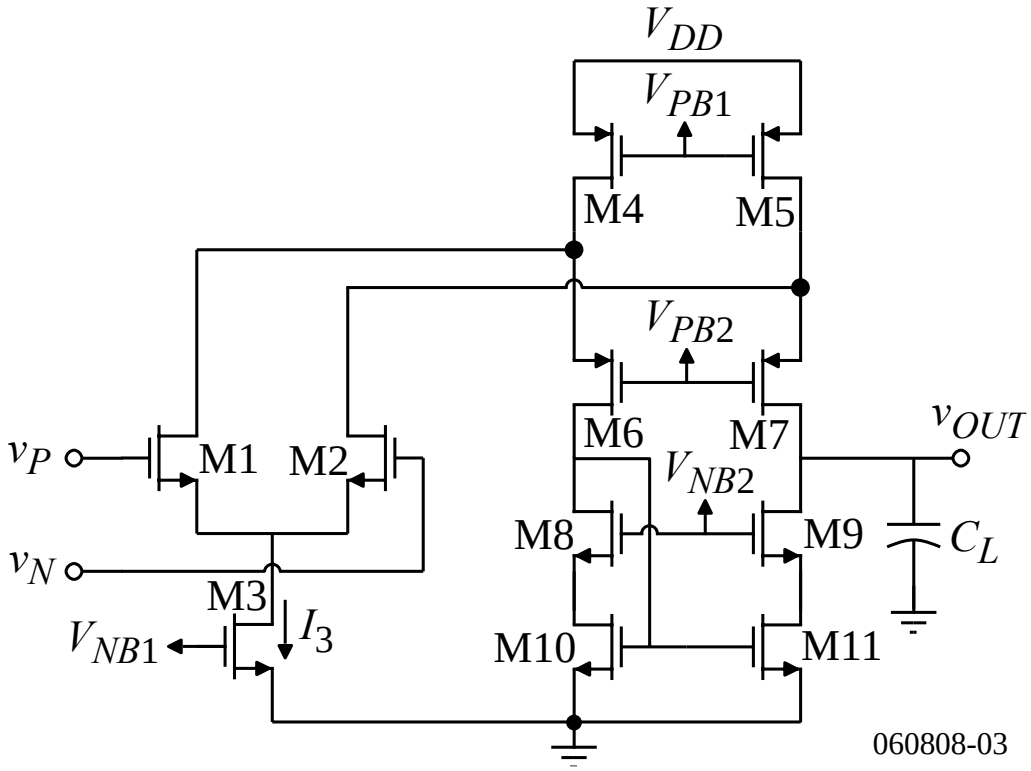
- Linear frequency response
- Slew rate response

Single-Stage Dominant Pole Comparator



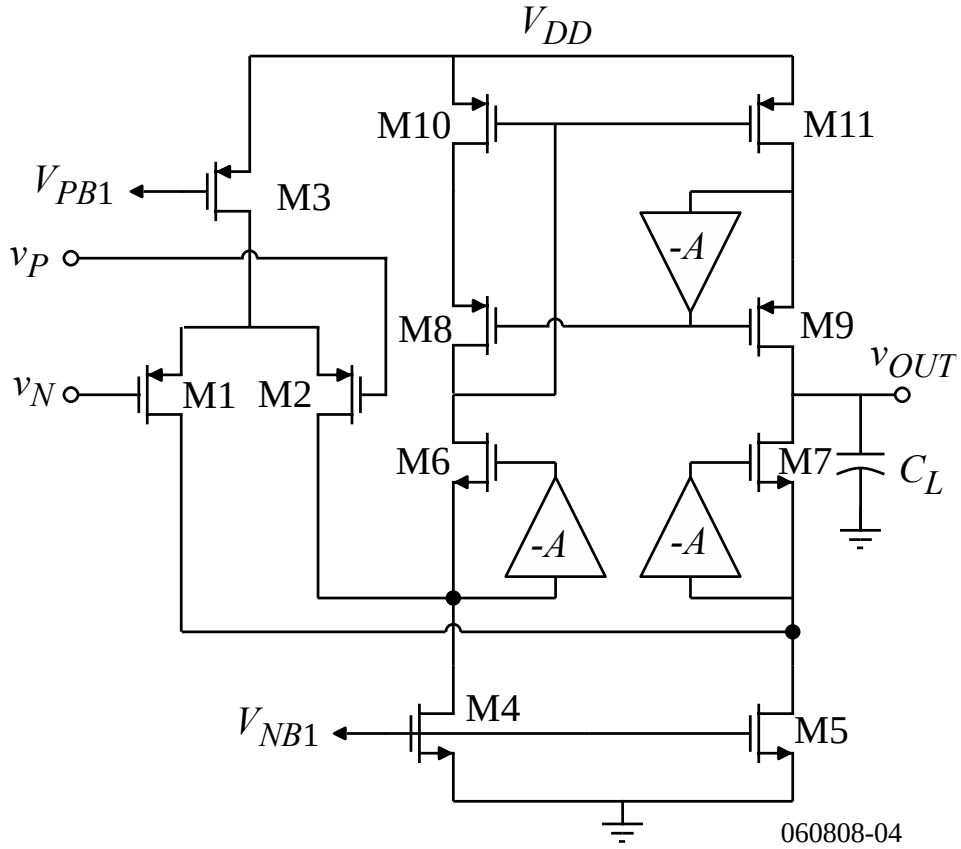
- Gain $\approx g_m^2 r_{ds}^2$
- Slew rate = I_5/C_L
- Dominant pole = $-1/(R_{out}C_L) = -1/(g_m r_{ds}^2 C_L)$

Folded-Cascode Comparator



- Gain $\approx g_m^2 r_{ds}^2$
- Slew rate = I_3/C_L
- Dominant pole = $-1/(R_{out}C_L) \approx -1/(g_m r_{ds}^2 C_L)$
- Slightly improved *ICMR*

Enhanced-Gain, Folded-Cascode Comparator

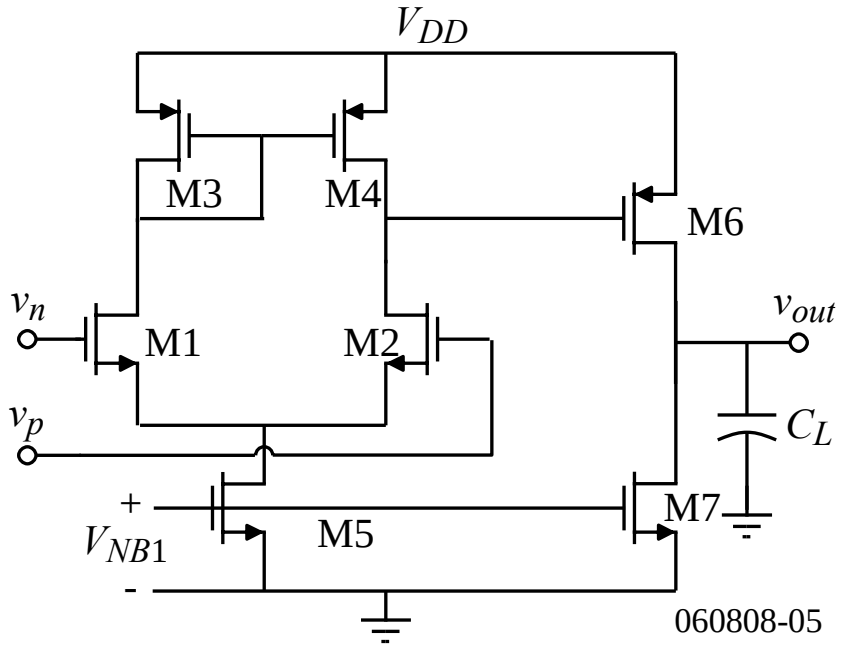


- Gain $\approx g_{m1}R_{out}$
- $R_{out} \approx [Ar_{ds7}g_{m7}(r_{ds1}\|r_{ds5})]\| (Ar_{ds9}g_{m9}r_{ds11})$
- Slew rate = I_3/C_L
- Dominant pole = $-1/(R_{out}C_L)$

TWO-POLE, OPEN-LOOP COMPARATORS

Two-Stage Comparator

The two-stage op amp without compensation is an excellent implementation of a high-gain, open-loop comparator.



- Much faster linear response – the two poles of the comparator are typically much larger than the dominant pole of the self-compensated type of comparator.
- Be careful not to close the loop because the amplifier is uncompensated.
- Slew rate: $SR^- = \frac{I_7}{C_{II}}$ and $SR^+ = \frac{I_6 - I_7}{C_{II}}$

Performance of the Two-Stage, Open-Loop Comparator

We know the performance should be similar to the uncompensated two-stage op amp. Emphasis on comparator performance:

- Maximum output voltage

$$V_{OH} = V_{DD} - (V_{DD}-V_{G6}(\text{min})-|V_{TP}|)\left[1 - \sqrt{1 - \frac{8I_7}{\beta_6(V_{DD}-V_{G6}(\text{min})-|V_{TP}|)^2}}\right]$$

- Minimum output voltage

$$V_{OL} = V_{SS}$$

- Small-signal voltage gain

$$A_V(0) = \left(\frac{g_{m1}}{g_{ds2}+g_{ds4}}\right)\left(\frac{g_{m6}}{g_{ds6}+g_{ds7}}\right)$$

- Poles

Input:

$$p_1 = \frac{-(g_{ds2}+g_{ds4})}{C_I}$$

Output:

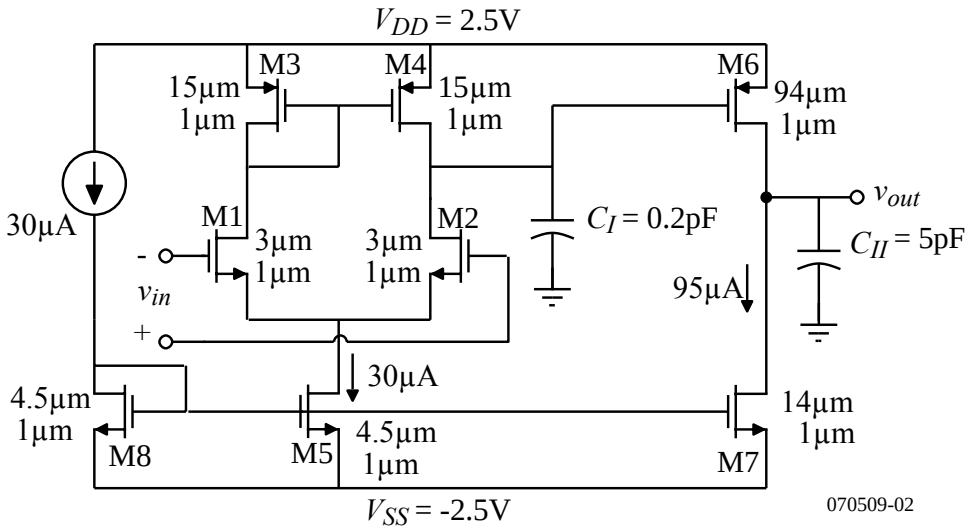
$$p_2 = \frac{-(g_{ds6}+g_{ds7})}{C_{II}}$$

- Frequency response

$$A_V(s) = \frac{A_V(0)}{\left(\frac{s}{p1} - 1\right)\left(\frac{s}{p2} - 1\right)}$$

Example 31-2 - Performance of a Two-Stage Comparator

Evaluate V_{OH}, V_{OL}, $A_v(0)$, $V_{in}(\text{min})$, p_1, p_2, for the two-stage comparator shown. The large signal model parameters are $K_N' = 110\mu A/V^2$, $K_P' = 50\mu A/V^2$, $V_{TN} = |V_{TP}| = 0.7V$, $\lambda_N = 0.04V^{-1}$ and $\lambda_P = 0.05V^{-1}$. Assume that the minimum value of $V_{G6} = 0V$ and that $C_I = 0.2pF$ and $C_{II} = 5pF$.



Solution

Using the above relations, we find that

$$V_{OH} = 2.5 - (2.5-0-0.7)\left[1 - \sqrt{1 - \frac{8\cdot 234x10^{-6}}{50x10^{-6}\cdot 38(2.5-0-0.7)^2}}\right] = 2.2V$$

V_{OL} is -2.5V. The gain can be found as $A_v(0) = 7696$. Therefore, the input resolution is

$$V_{in}(\text{min}) = (V_{OH}-V_{OL})/A_v(0) = 4.7V/7{,}696 = 0.611mV$$

Next, we find the poles of the comparator, p_1 and p_2.

$$p_1 = -(g_{ds2} + g_{ds4})/C_I = 15x10^{-6}(0.04+0.05)/0.2x10^{-12} = -6.75x10^6 \ (1.074MHz)$$

and

$$p_2 = -(g_{ds6} + g_{ds7})/C_{II}) = (95x10^{-6})(0.04+0.05)/5x10^{-12} = -1.71x10^6 \ (0.272MHz)$$

Linear Step Response of the Two-Stage Comparator

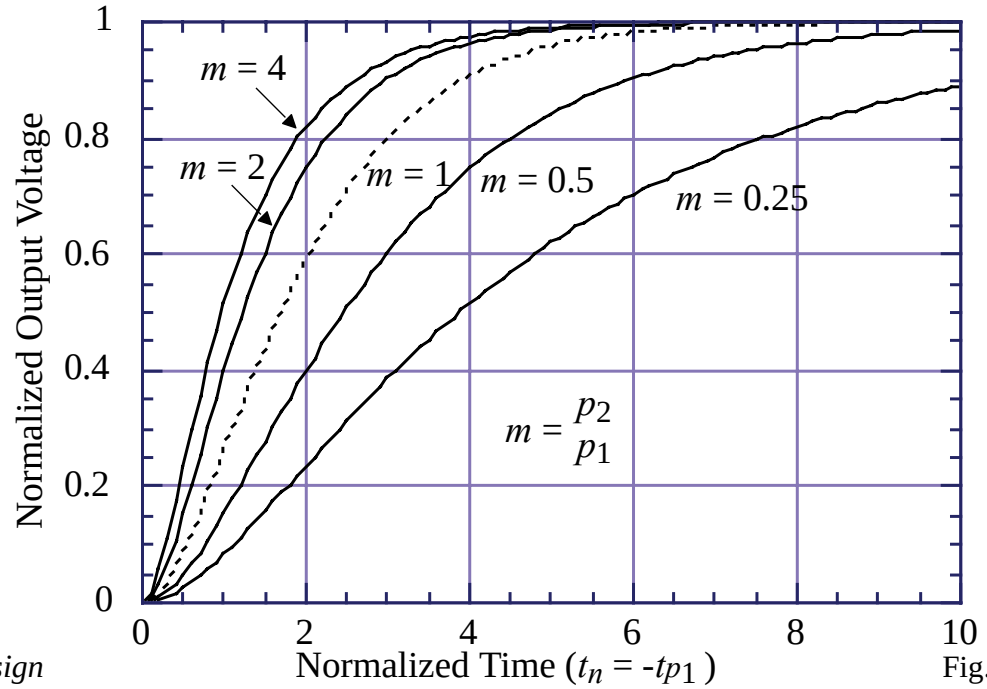
The step response of a circuit with two real poles ($p_1 \neq p_2$) is,

$$v_{out}(t) = A_v(0)V_{in}\left[1 + \frac{p_2 e^{tp_1}}{p_1 - p_2} - \frac{p_1 e^{tp_2}}{p_1 - p_2}\right]$$

Normalizing gives,

$$v_{out}'(t_n) = \frac{v_{out}(t)}{A_v(0)V_{in}} = 1 - \frac{m}{m-1}e^{-t_n} + \frac{1}{m-1}e^{-mt_n} \text{ where } m = \frac{p_2}{p_1} \neq 1 \text{ and } t_n = -tp_1$$

If $p_1 = p_2$ (m=1), then $v_{out}'(t_n) = 1 - e^{tp_1} + tp_1 e^{tp_1} = 1 - e^{-t_n} - t_n e^{-t_n}$



Linear Step Response of the Two-Stage Comparator - Continued

The above results are valid as long as the slope of the linear response does not exceed the slew rate.

- Slope at $t = 0$ is zero
- Maximum slope occurs at ($m \neq 1$)

$$t_n(\max) = \frac{ln(m)}{m\text{-}1}$$

and is

$$\frac{dv_{out}'(t_n(\max))}{dt_n} = \frac{m}{m\text{-}1}\left[\exp\left(\frac{\text{-}ln(m)}{m\text{-}1}\right) - \exp\left(\text{-}m\frac{ln(m)}{m\text{-}1}\right)\right]$$

- For the two-stage comparator using NMOS input transistors, the slew rate is

$$SR^- = \frac{I_7}{C_{II}}$$

$$SR^+ = \frac{I_6\text{-}I_7}{C_{II}} = \frac{0.5\beta_6(V_{DD}\text{-}V_{G6}(\min)\text{-}|V_{TP}|)^2 - I_7}{C_{II}}$$

Example 31-3 - Step Response of Ex. 31-2

Find the maximum slope of Ex. 31-2 and the time it occurs if the magnitude of the input step is v_{in}(min). If the dc bias current in M7 is 100µA, at what value of load capacitance, C_L would the transient response become slew limited? If the magnitude of the input step is $100v_{in}$(min), what is the new value of C_L at which slewing would occur?

Solution

The poles of the comparator were given in Ex. 31-2 as p_1 = -6.75x10^6 rads/sec. and p_2 = -1.71x10^6 rads/sec. This gives a value of m = 0.253. From the previous expressions, the maximum slope occurs at t_n(max) = 1.84 secs. Dividing by $|p_1|$ gives t(max) = 0.272µs. The slope of the transient response at this time is found as

$$\frac{dv_{out}'(t_n(\max))}{dt_n} = -0.338[\exp(-1.84) - \exp(-0.253\cdot 1.84)] = 0.159 \text{ V/sec}$$

Multiplying the above by $|p_1|$ gives $dv_{out}'(t(\max))/dt$ = 1.072V/µs. If the slew rate is less than 1.072V/µs, the transient response will experience slewing. Therefore, if $C_L \geq$ 100µA/1.072V/µs or 93.3pF, the comparator will slew.

If the input is $100v_{in}$(min), then we must unnormalize the output slope as follows.

$$\frac{dv_{out}'(t(\max))}{dt} = \frac{v_{in}}{v_{in}(\min)}\frac{dv_{out}'(t(\max))}{dt} = 100\cdot 1.072\text{V/µs} = 107.2\text{V/µs}$$

Therefore, the comparator will slew with a load capacitance greater than 0.933pF.

Propagation Delay Time (Non-Slew)

To find t_p, we want to set $0.5(V_{OH}\text{-}V_{OL})$ equal to $v_{out}(t_n)$. However, $v_{out}(t_n)$ given as

$$v_{out}(t_n) = A_v(0)V_{in}\left[1 - \frac{m}{m\text{-}1}e^{-t_n} + \frac{1}{m\text{-}1}e^{-mt_n}\right]$$

can't be easily solved so approximate the step response as a power series to get

$$v_{out}(t_n) \approx A_v(0)V_{in}\left[1 - \frac{m}{m\text{-}1}\left(1\text{-}t_n + \frac{t_n^2}{2} + \cdots\right) + \frac{1}{m\text{-}1}\left(1\text{-}mt_n + \frac{m^2t_n^2}{2} + \cdots\right)\right] \approx$$

$$\frac{mt_n^2A_v(0)V_{in}}{2}$$

Therefore, set $v_{out}(t_n) = 0.5(V_{OH}\text{-}V_{OL})$

$$\frac{V_{OH}\text{-}V_{OL}}{2} \approx \frac{mt_{pn}^2A_v(0)V_{in}}{2}$$

or

$$t_{pn} \approx \sqrt{\frac{V_{OH}\text{-}V_{OL}}{mA_v(0)V_{in}}} = \sqrt{\frac{V_{in}(\min)}{mV_{in}}} = \frac{1}{\sqrt{mk}}$$

This approximation is particularly good for large values of k.

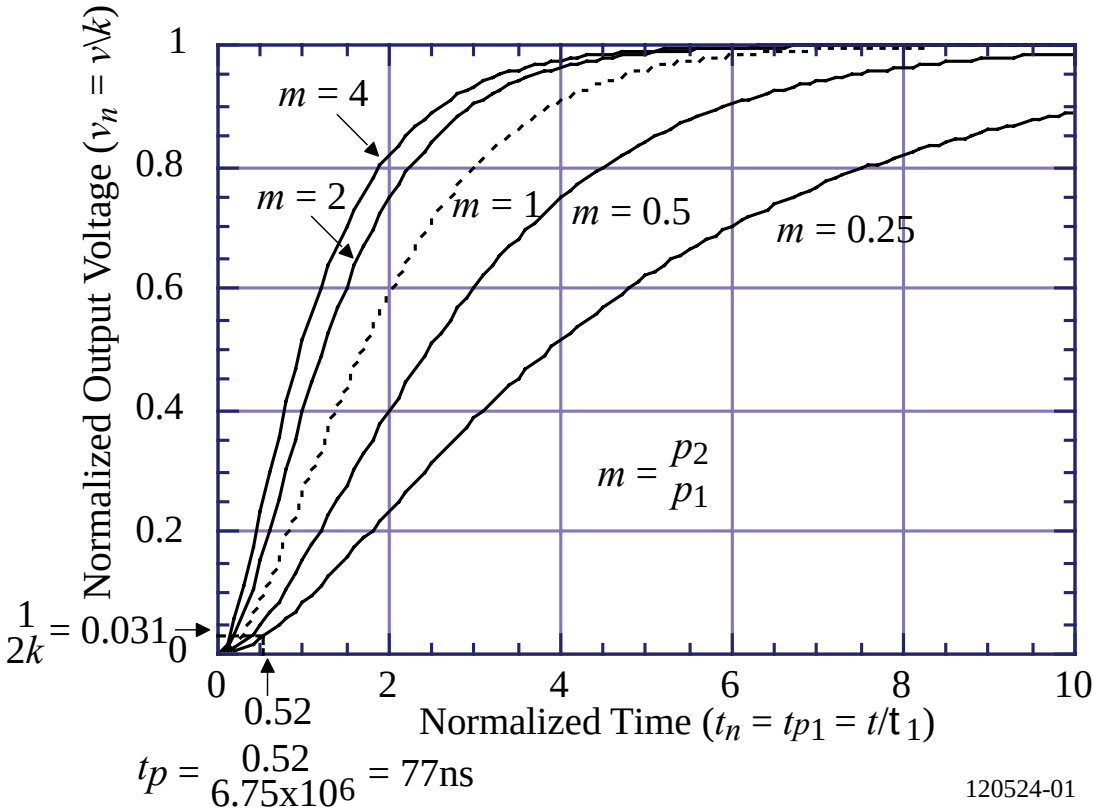
Example 31-4 - Propagation Delay Time of a Two-Pole Comparator (Non-Slew)

Find the propagation time delay of Ex. 31-2 if V_{in} = 10mV, 100mV and 1V.

Solution

From Ex. 31-2 we know that $V_{in}(\text{min})$ = 0.611mV and m = 0.253. For V_{in} = 10mV, k = 16.366 which gives $t_{pn} \approx 1/\sqrt{mk}$ = 0.491. The propagation time delay is equal to 0.491/6.75x10^6 or 72.9nS.

In the figure shown, t_{pn}, occurs when v_n is equal to $\dfrac{V_{OH}\text{-}V_{OL}}{2A_v(0)V_{in}} = \dfrac{1}{2k}$.



This corresponds well with the figure shown where the normalized propagation time delay is the time at which the amplitude is 1/2k or 0.031which corresponds to t_{pn} of approximately 0.52 compared with 0.491 of above.

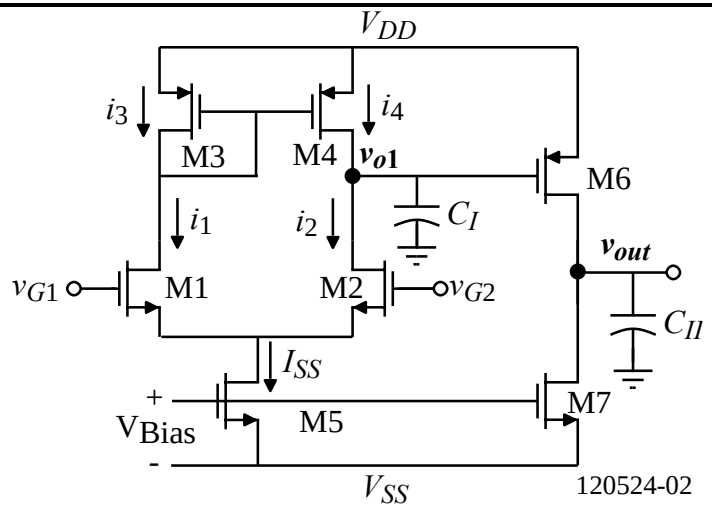
Similarly, for V_{in} = 100mV and 1V we get a propagation time delay of 23ns and 7.3ns, respectively.

Initial Operating States for the Two-Stage, Open-Loop Comparator

What are the initial operating states for the two-stage, open-loop comparator? The following table summarizes the results for the two-stage, open-loop comparator shown.

Conditions	Slew?	Initial State of v_{o1}	Initial State of v_{out}
$v_{G1}>V_{G2}$, $i_1<I_{SS}$ and $i_2>0$	No	$V_{DD}-V_{SD4}(\text{sat}) < v_{o1} < V_{DD}$	V_{SS}
$v_{G1}>>V_{G2}$, $i_1=I_{SS}$ and $i_2=0$	Yes	V_{DD}	V_{SS}
$v_{G1}<V_{G2}$, $i_1>0$ and $i_2<I_{SS}$	No	$v_{o1}=V_{G2}-V_{GS2,\text{act}}(I_{SS}/2)$, $\approx V_{SS}$ if M5 act.	V_{OH}, see below.
$v_{G1}<<V_{G2}$, $i_1>0$ and $i_2<I_{SS}$	No	V_{SS}	V_{OH}, see below.
$v_{G2}>V_{G1}$, $i_1>0$ and $i_2<I_{SS}$	No	$V_{S2}(I_{SS}/2)<v_{o1}<V_{S2}(I_{SS}/2)+V_{DS2}(\text{sat})$	V_{OH}, see below.
$v_{G2}>>V_{G1}$, $i_1>0$ and $i_2<I_{SS}$	No	$V_{G1}-V_{GS1}(I_{SS}/2)$, $\approx V_{SS}$ if M5 active	V_{OH}, see below.
$v_{G2}<V_{G1}$, $i_1<I_{SS}$ and $i_2>0$	No	$V_{DD}-V_{SD4}(\text{sat}) < v_{o1} < V_{DD}$	V_{SS}
$v_{G2}<<V_{G1}$, $i_1=I_{SS}$ and $i_2=0$	Yes	V_{DD}	V_{SS}

$$V_{OH} = V_{DD} - (V_{DD}-V_{G6}(\text{min})-|V_{TP}|) \times\left[1 - \sqrt{1 - \frac{8I_7}{\beta_6(V_{DD}-V_{G6}(\text{min})-|V_{TP}|)^2}}\right]$$



Trip Point of an Inverter

In order to determine the propagation delay time, it is necessary to know when the second stage of the two-stage comparator begins to "turn on".

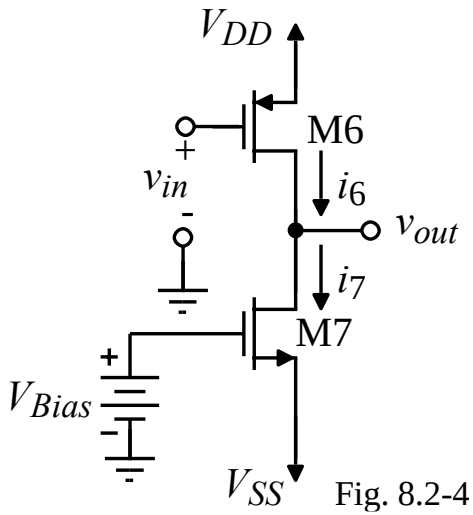


Fig. 8.2-4

Second stage:

Trip point:

Assume that M6 and M7 are saturated. (We know that the steepest slope occurs for this condition.)

Equate i_6 to i_7 and solve for v_{in} which becomes the trip point.

$$\therefore \qquad v_{in} = V_{TRP} = V_{DD} - |V_{TP}| - \sqrt{\frac{K_N(W_7/L_7)}{K_P(W_6/L_6)}}\,(V_{Bias} - V_{SS} - V_{TN})$$

Example:

If $W_7/L_7 = W_6/L_6$, $V_{DD} = 2.5\text{V}$, $V_{SS} = -2.5\text{V}$, and $V_{Bias} = 0\text{V}$ the trip point for the circuit above is

$$V_{TRP} = 2.5 - 0.7 - \sqrt{110/50}\,(0 + 2.5 - 0.7) = -0.870\text{V}$$

Propagation Delay Time of a Slewing, Two-Stage, Open-Loop Comparator

Previously we calculated the propagation delay time for a nonslewing comparator.

If the comparator slews, then the propagation delay time is found from

$$i_i = C_i \frac{dv_i}{dt_i} = C_i \frac{\Delta v_i}{\Delta t_i}$$

where

C_i is the capacitance to ground at the output of the i-th stage

The propagation delay time of the i-th stage is,

$$t_i = \Delta t_i = C_i \frac{\Delta V_i}{I_i}$$

The propagation delay time is found by summing the delays of each stage.

$$t_p = t_1 + t_2 + t_3 + \cdots$$

Example 31-5 - Propagation Time Delay of a Two-Stage, Open-Loop Comparator

For the two-stage comparator shown assume that C_I = 0.2pF and C_{II} = 5pF. Also, assume that v_{G1} = 0V and that v_{G2} has the waveform shown. If the input voltage is large enough to cause slew to dominate, find the propagation time delay of the rising and falling output of the comparator and give the propagation time delay of the comparator.

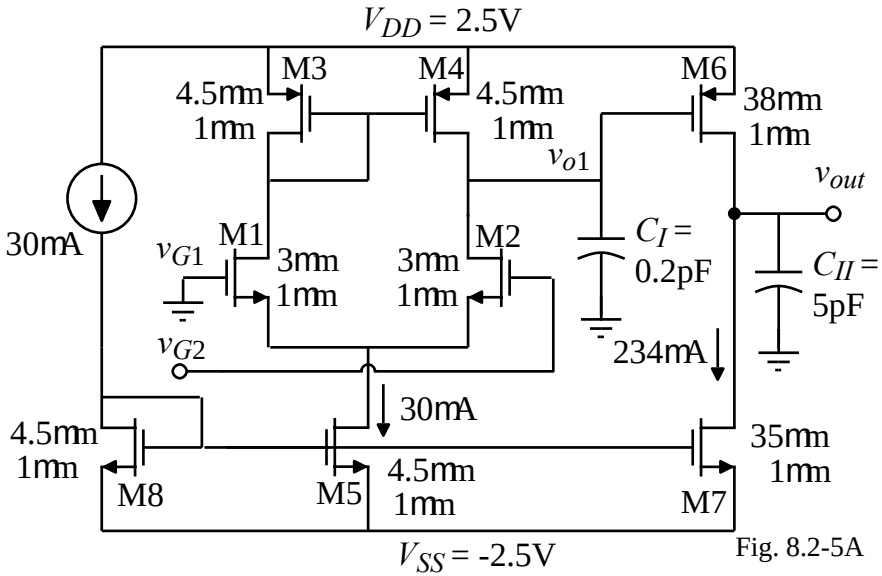


Fig. 8.2-5A

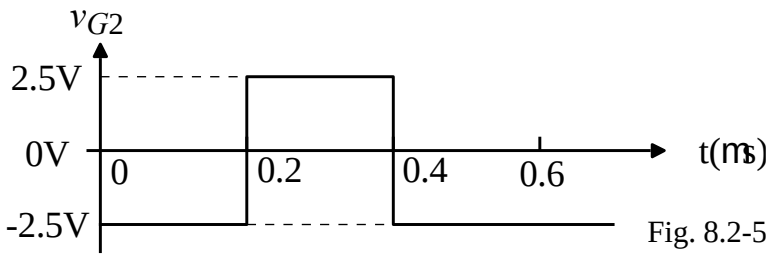


Fig. 8.2-5

Solution

1.) Total delay = sum of the first and second stage delays, t_1 and t_2

2.) First, consider the change of v_{G2} from -2.5V to 2.5V at 0.2µs.

The last row of table on Slide 31-26 gives v_{o1} = +2.5V and v_{out} = -2.5V

3.) t_{f1}, requires C_I, ΔV_{o1}, and I_5. C_I = 0.2pF, I_5 = 30µA and ΔV_1 can be calculated by finding the trip point of the output stage.

Example 31-5 - Continued

4.) The trip point of the output stage by setting the current of M6 when saturated equal to 234µA.

$$\frac{\beta_6}{2}(V_{SG6}-|V_{TP}|)^2 = 234\mu A \rightarrow V_{SG6} = 0.7 + \sqrt{\frac{234\cdot 2}{50\cdot 38}} = 1.196V$$

Therefore, the trip point of the second stage is $V_{TRP2} = 2.5 - 1.196 = 1.304V$

Therefore, $\Delta V_1 = 2.5V - 1.304V = V_{SG6} = 1.196V$. Thus the falling propagation time delay of the first stage is

$$t_{fo1} = 0.2pF\left(\frac{1.196V}{30\mu A}\right) = 8\ ns$$

5.) The rising propagation time delay of the second stage requires C_{II}, ΔV_{out}, and I_6. C_{II} is given as 5pF, $\Delta V_{out} = 2.5V$ (assuming the trip point of the circuit connected to the output of the comparator is 0V), and I_6 can be found as follows:

$$V_{G6}(guess) \approx 0.5[V_{G6}(I_6=234\mu A) + V_{G6}(min)]$$

$$V_{G6}(min) = V_{G1} - V_{GS1}(I_{SS}/2) + V_{DS2} \approx -V_{GS1}(I_{SS}/2) = -0.7 - \sqrt{\frac{2\cdot 15}{110\cdot 3}} = -1.00V$$

$$V_{G6}(guess) \approx 0.5(1.304V-1.00V) = 0.152V$$

Therefore $V_{SG6} = 2.348V$ and $I_6 = \frac{\beta_6}{2}(V_{SG6}-|V_{TP}|)^2 = \frac{38\cdot 50}{2}(2.348 - 0.7)^2 = 2{,}580\mu A$

Example 31-5 - Continued

6.) The rising propagation time delay for the output can expressed as

$$t_{rout} = 5\text{pF}\left(\frac{2.5\text{V}}{2580\mu\text{A-}234\mu\text{A}}\right) = 5.3\text{ ns}$$

Thus the total propagation time delay of the rising output of the comparator is approximately 13.3 ns and most of this delay is attributable to the first stage.

7.) Next consider the change of v_{G2} from 2.5V to -2.5V at 0.4µs. We shall assume that v_{G2} has been at 2.5V long enough for the conditions of the table on Slide 31-26 to be valid. Therefore, $v_{o1} \approx V_{SS}$ = -2.5V and $v_{out} \approx V_{DD}$. The propagation time delays for the first and second stages are calculated as

$$t_{ro1} = 0.2\text{pF}\left(\frac{1.304\text{V-}(-1.00\text{V})}{30\mu\text{A}}\right) = 15.4\text{ ns}$$

$$t_{fout} = 5\text{pF}\left(\frac{2.5\text{V}}{234\mu\text{A}}\right) = 53.42\text{ns}$$

8.) The total propagation time delay of the falling output is 68.82 ns. Taking the average of the rising and falling propagation time delays gives a propagation time delay for this two-stage, open-loop comparator of about 41.06ns.

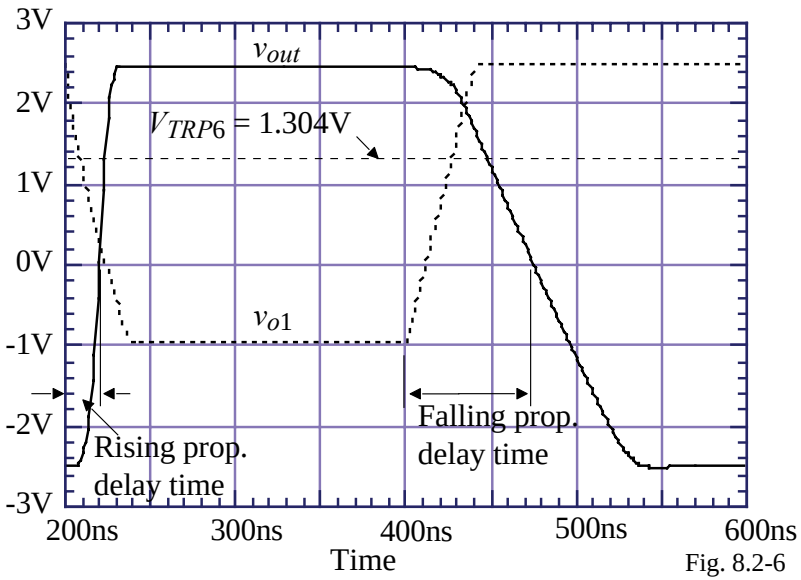


Fig. 8.2-6

SUMMARY

- The two-stage, open-loop comparator has two poles which should as large as possible
- The transient response of a two-stage, open-loop comparator will be limited by either the bandwidth or the slew rate
- It is important to know the initial states of a two-stage, open-loop comparator when finding the propagation delay time
- If the comparator is gainbandwidth limited then the poles should be as large as possible for minimum propagation delay time
- If the comparator is slew rate limited, then the current sinking and sourcing ability should be as large as possible