LECTURE 30 – LOW VOLTAGE OP AMPS

LECTURE ORGANIZATION

Outline

- Introduction
- Low voltage input stages
- Low voltage gain stages
- Low voltage bias circuits
- Low voltage op amps
- Summary

***CMOS Analog Circuit Design*, 3rd Edition Reference**

Pages 419-436

INTRODUCTION

Implications of Low-Voltage, Strong-Inversion Operation

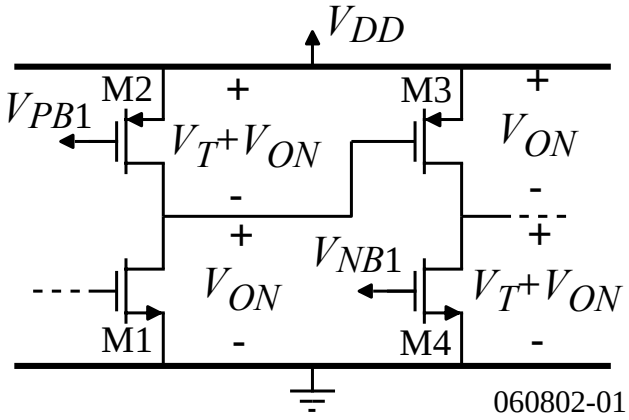
- Reduced power supply means decreased dynamic range
- Nonlinearity will increase because the transistor is working close to V_{DS}(sat)
- Large values of λ because the transistor is working close to V_{DS}(sat)
- Increased drain-bulk and source-bulk capacitances because they are less reverse biased.
- Large values of currents and *W/L* ratios to get high transconductance
- Small values of currents and large values of *W/L* will give small V_{DS}(sat)
- Severely reduced input common mode range
- Switches will require charge pumps

What are the Limits of Power Supply?

The limit comes when there is no signal range left when the dc drops are subtracted from V_{DD}.

Minimum power supply (no signal swing range):

$$V_{DD}(\text{min.}) = V_T + 2V_{ON}$$

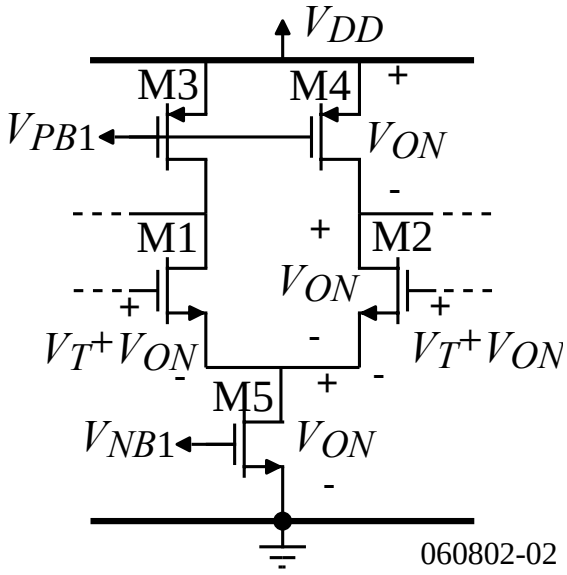


For differential amplifiers, the minimum power supply is:

$$V_{DD}(\text{min.}) = 3V_{ON}$$

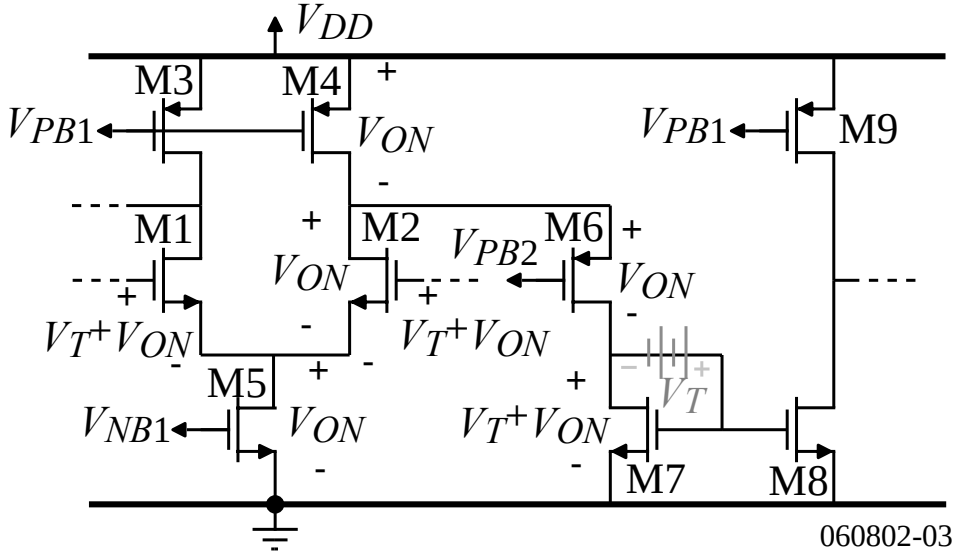
However, to have any input common mode range, the effective minimum power supply is,

$$V_{DD}(\text{min.}) = V_T + 2V_{ON}$$



Minimum Power Supply Limit – Continued

The previous consideration of the differential amplifier did not consider getting the signal out of the amplifier. This will add another V_{ON}.



Therefore,

$$V_{DD}(\text{min.}) = V_T + 3V_{ON}$$

This could be reduced to $3V_{ON}$ with the floating battery but its implementation probably requires more than $3V_{ON}$ of power supply.

Note the output signal swing is $V_T + V_{ON}$ while the input common range is V_{ON}.

LOW VOLTAGE INPUT STAGES

Input Common Mode Voltage Range

Minimum power supply (*ICMR* = 0):

$$V_{DD}(\text{min}) = V_{SD3}(\text{sat})-V_{T1}+V_{GS1}+V_{DS5}(\text{sat})$$
$$= V_{SD3}(\text{sat})+V_{DS1}(\text{sat})+V_{DS5}(\text{sat})$$

Input common-mode range:

$$V_{icm}(\text{upper}) = V_{DD} - V_{SD3}(\text{sat}) + V_{T1}$$
$$V_{icm}(\text{lower}) = V_{DS5}(\text{sat}) + V_{GS1}$$

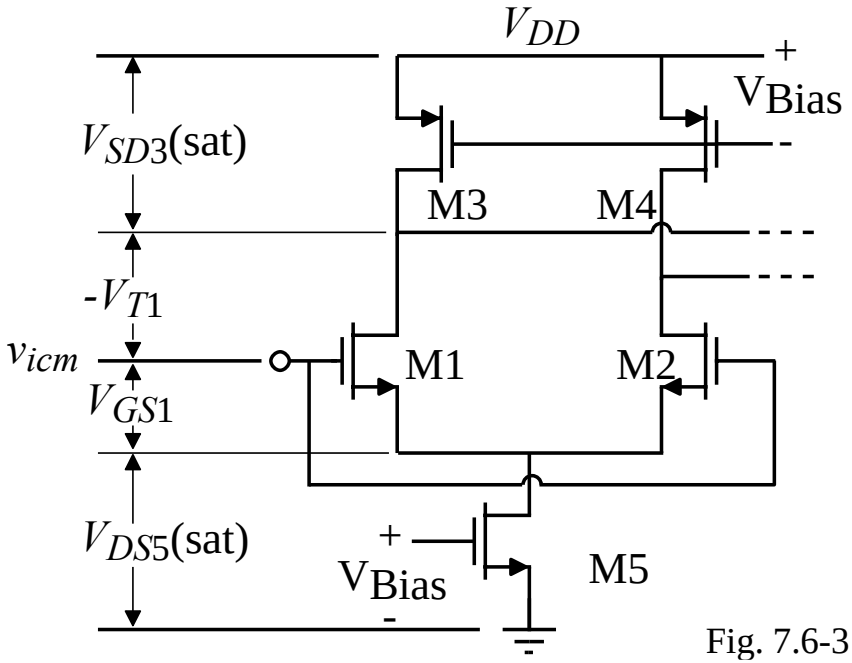


Fig. 7.6-3

If the threshold magnitudes are 0.7V, V_{DD} = 1.5V and the saturation voltages are 0.3V, then

$V_{icm}(\text{upper}) = 1.5 - 0.3 + 0.7 = 1.9\text{V}$

and

$V_{icm}(\text{lower}) = 0.3 + 1.0 = 1.3\text{V}$

giving an *ICMR* of 0.6V.

Increasing *ICMR* using Parallel Input Stages

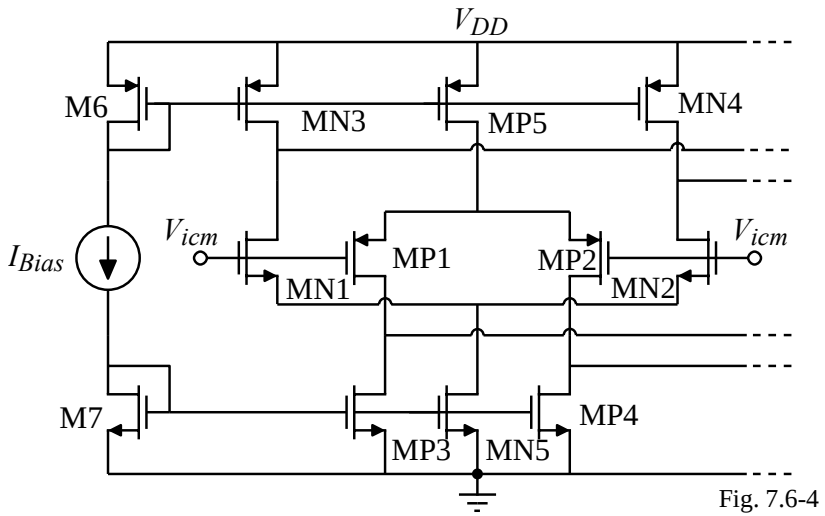


Fig. 7.6-4

Turn-on voltage for the n-channel input:

$V_{onn} = V_{DSN5}(\text{sat}) + V_{GSN1}$

Turn-on voltage for the p-channel input:

$V_{onp} = V_{DD} - V_{SDP5}(\text{sat}) - V_{SGP1}$

The sum of V_{onn} and V_{onp} equals the minimum power supply.

Regions of operation:

$V_{DD} > V_{icm} > V_{onp}$: (n-channel on and p-channel off) $g_m(\text{eq}) = g_{mN}$

$V_{onp} \geq V_{icm} \geq V_{onn}$: (n-channel on and p-channel on) $g_m(\text{eq}) = g_{mN} + g_{mP}$

$V_{onn} > V_{icm} > 0$: (n-channel off and p-channel on) $g_m(\text{eq}) = g_{mP}$

where $g_m(\text{eq})$ is the equivalent input transconductance of the above input stage, g_{mN} is the input transconductance for the n-channel input and g_{mP} is the input trans-conductance for the p-channel input.

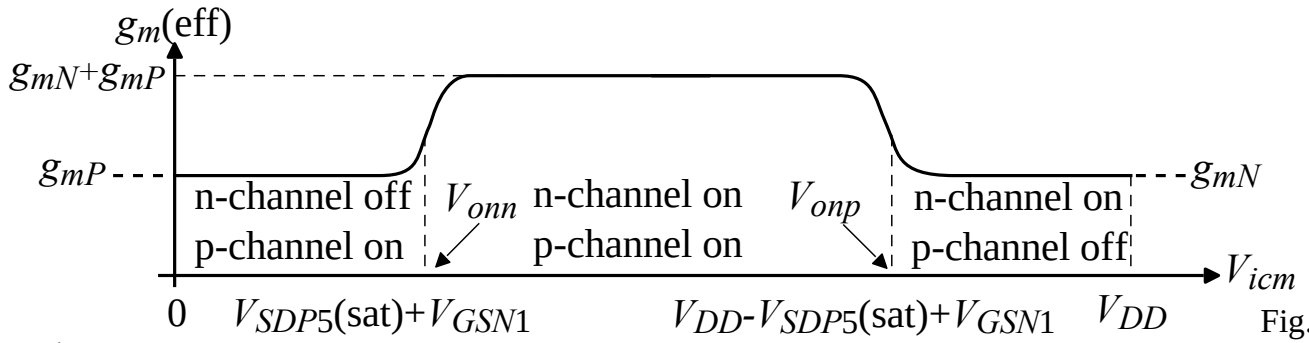


Fig. 7.6-5

Removing the Nonlinearity in Transconductances as a Function of *ICMR*

Increase the bias current in the differential amplifier that is on when the other differential amplifier is off.

Three regions of operation depending on the value of V_{icm}:

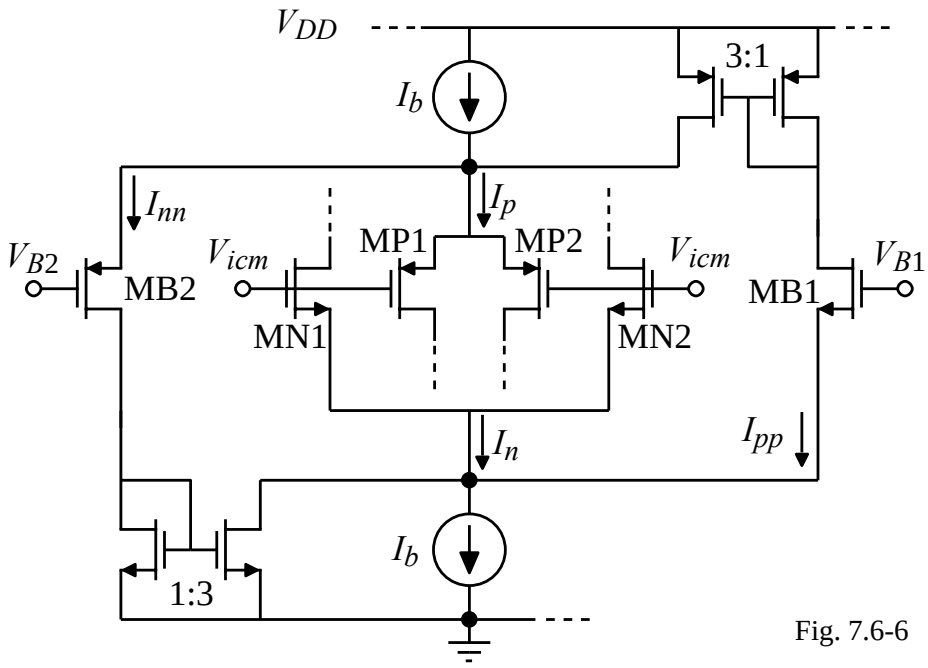


Fig. 7.6-6

1.) $V_{icm} < V_{onn}$: n-channel diff. amp. off and p-channel on with $I_p = 4I_b$:

$$g_m(\text{eff}) = \sqrt{\frac{K_P' W_P}{L_P}}\, 2\sqrt{I_b}$$

2.) $V_{onn} < V_{icm} < V_{onp}$: both on with $I_n = I_p = I_b$:

$$g_m(\text{eff}) = \sqrt{\frac{K_N' W_N}{L_N}}\sqrt{I_b} + \sqrt{\frac{K_P' W_P}{L_P}}\sqrt{I_b}$$

3.) $V_{icm} > V_{onp}$: p-channel diff. amp. off and n-channel on with $I_n = 4I_b$:

$$g_m(\text{eff}) = \sqrt{\frac{K_N' W_N}{L_N}}\, 2\sqrt{I_b}$$

How Does the Current Compensation Work?

Set $V_{B1} = V_{onn}$ and $V_{B2} = V_{onp}$.

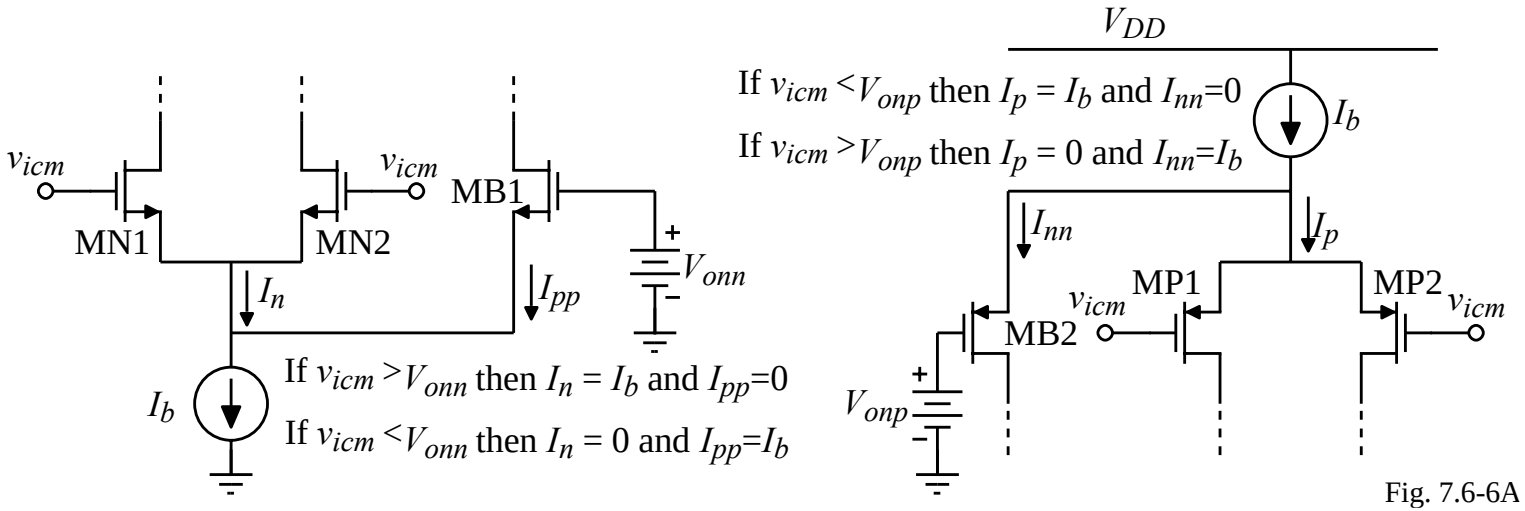


Fig. 7.6-6A

Result:

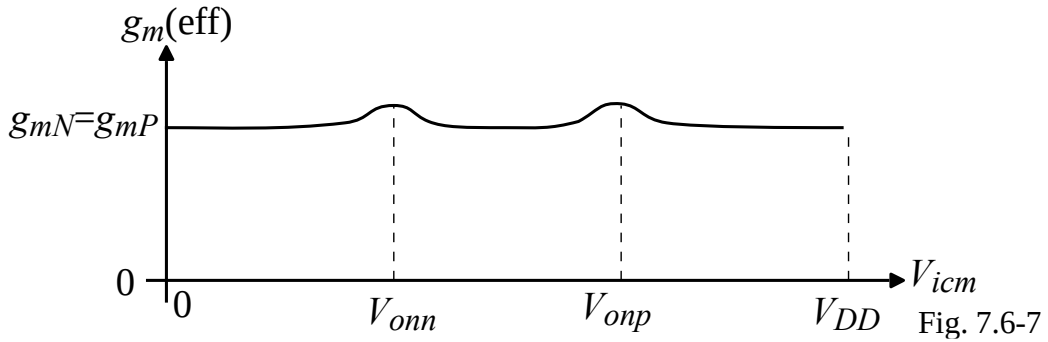


Fig. 7.6-7

The above techniques and many similar ones are good for power supply values down to about 1.5V. Below that, different techniques must be used or the technology must be modified (natural devices).

Natural Transistors

Natural or native NMOS transistors normally have a threshold voltage around 0.1V before the threshold is increased by increasing the *p* concentration in the channel.

If these transistors are characterized, then they provide a means of achieving low voltage operation.

Minimum power supply ($ICMR = 0$):

$$V_{DD}(\text{min}) = 3V_{ON}$$

Input common mode range:

$$V_{icm}(\text{upper}) = V_{DD} - V_{ON} + V_T(\text{natural})$$

$$V_{icm}(\text{lower}) = 2V_{ON} + V_T(\text{natural})$$

If $V_T(\text{natural}) \approx V_{ON} = 0.1\text{V}$, then

$$V_{icm}(\text{upper}) = V_{DD}$$

$$V_{icm}(\text{lower}) = 3V_{ON} = 0.3\text{V}$$

Therefore,

$$ICMR = V_{DD} - 3V_{ON} = V_{DD} - 0.3\text{V} \quad \Rightarrow \quad V_{DD}(\text{min}) \approx 1\text{V}$$

Matching tends to be better (less doping and magnitude is smaller).

Bulk-Driven MOSFET

A depletion device would permit large *ICMR* even with very small power supply voltages because V_{GS} is zero or negative.

When a MOSFET is driven from the bulk with the gate held constant, it acts like a depletion transistor.

Cross-section of an n-channel bulk-driven MOSFET:

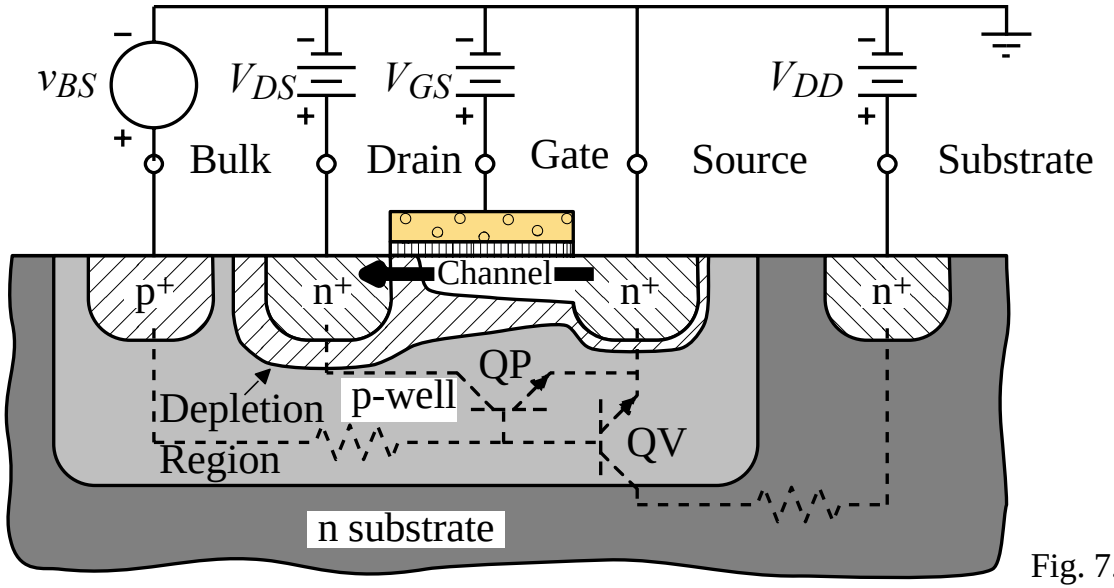


Fig. 7.6-8

Large signal equation:

$$i_D = \frac{K_N'W}{2L}\left[V_{GS} - V_{T0} - \gamma\sqrt{2|\phi_F| - v_{BS}} + \gamma\sqrt{2|\phi_F|}\right]^2$$

Small-signal transconductance:

$$g_{mbs} = \frac{\gamma\sqrt{(2K_N'W/L)I_D}}{2\sqrt{2|\phi_F| - V_{BS}}}$$

Bulk-Driven MOSFET - Continued

Transconductance characteristics:

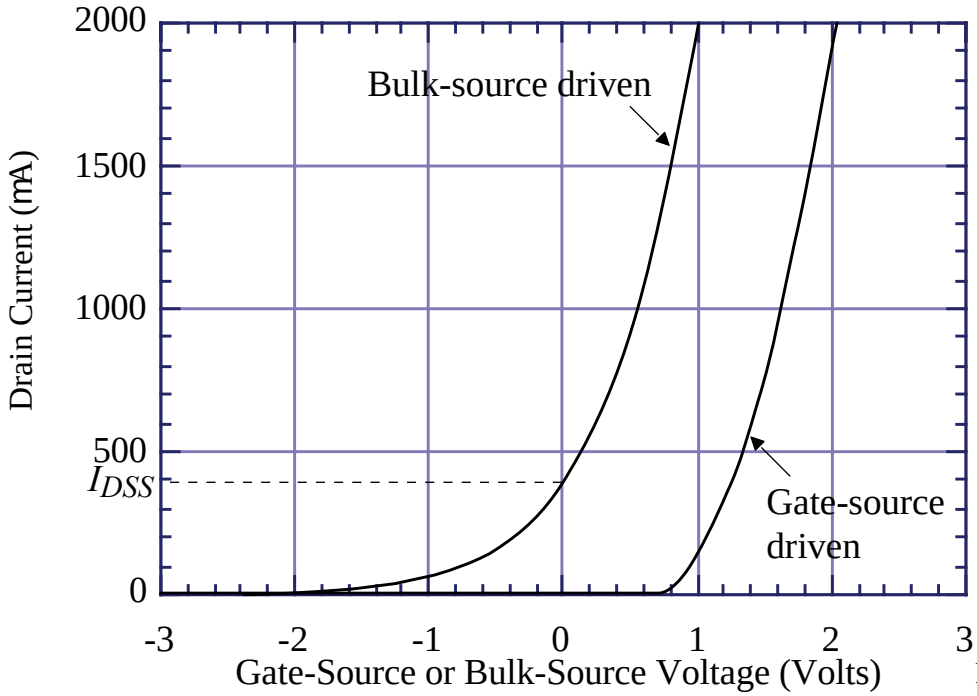


Fig. 7.6-9

Saturation: $V_{DS} > V_{BS} - V_P$ gives,

$$V_{BS} = V_P + V_{ON}$$

$$i_D = I_{DSS}\left(1 - \frac{V_{BS}}{V_P}\right)^2$$

Comments:

- g_m (bulk) > g_m(gate) if $V_{BS} > 0$ (forward biased)
- Noise of both configurations are the same (any differences comes from the gate versus bulk noise)
- Bulk-driven MOSFET tends to be more linear at lower currents than the gate-driven MOSFET
- Very useful for generation of I_{DSS} floating current sources.

Bulk-Driven, n-channel Differential Amplifier

What is the *ICMR*?

$$V_{icm}(\text{min}) = V_{SS} + V_{DS5}(\text{sat}) + V_{BS1} = V_{SS} + V_{DS5}(\text{sat}) - |V_{P1}| + V_{DS1}(\text{sat})$$

Note that V_{icm} can be less than V_{SS} if $|V_{P1}| > V_{DS5}(\text{sat}) + V_{DS1}(\text{sat})$

$V_{icm}(\text{max}) = ?$

As V_{icm} increases, the current through M1 and M2 is constant so the source increases. However, the gate voltage stays constant so that V_{GS1} decreases. Since the current must remain constant through M1 and M2 because of M5, the bulk-source voltage becomes less negative causing V_{TN1} to decrease and maintain the currents through M1 and M2 constant. If V_{icm} is increased sufficiently, the bulk-source voltage will become positive. However, current does not start to flow until V_{BS} is greater than 0.3 volts so the effective $V_{icm}(\text{max})$ is

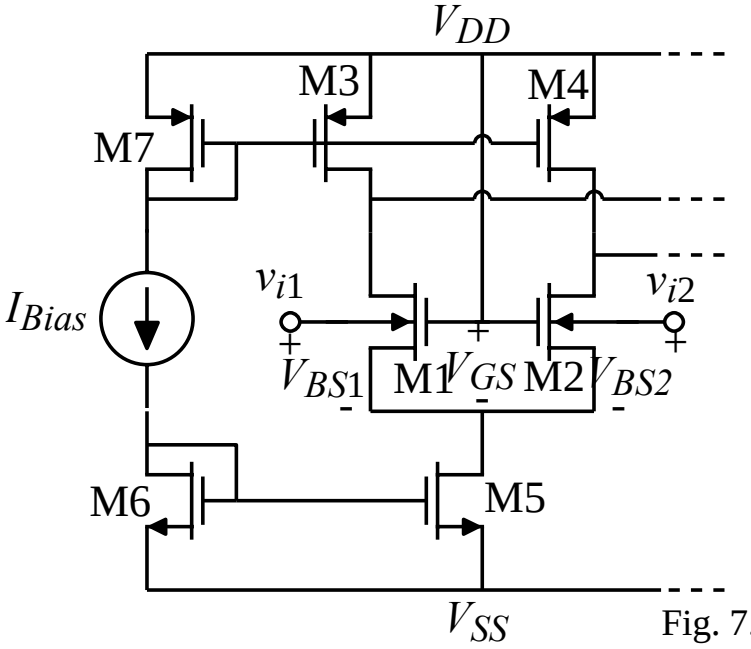


Fig. 7.6-10

$$V_{icm}(\text{max}) \approx V_{DD} - V_{SD3}(\text{sat}) - V_{DS1}(\text{sat}) + V_{BS1}.$$

Illustration of the *ICMR* of the Bulk-Driven, Differential Amplifier

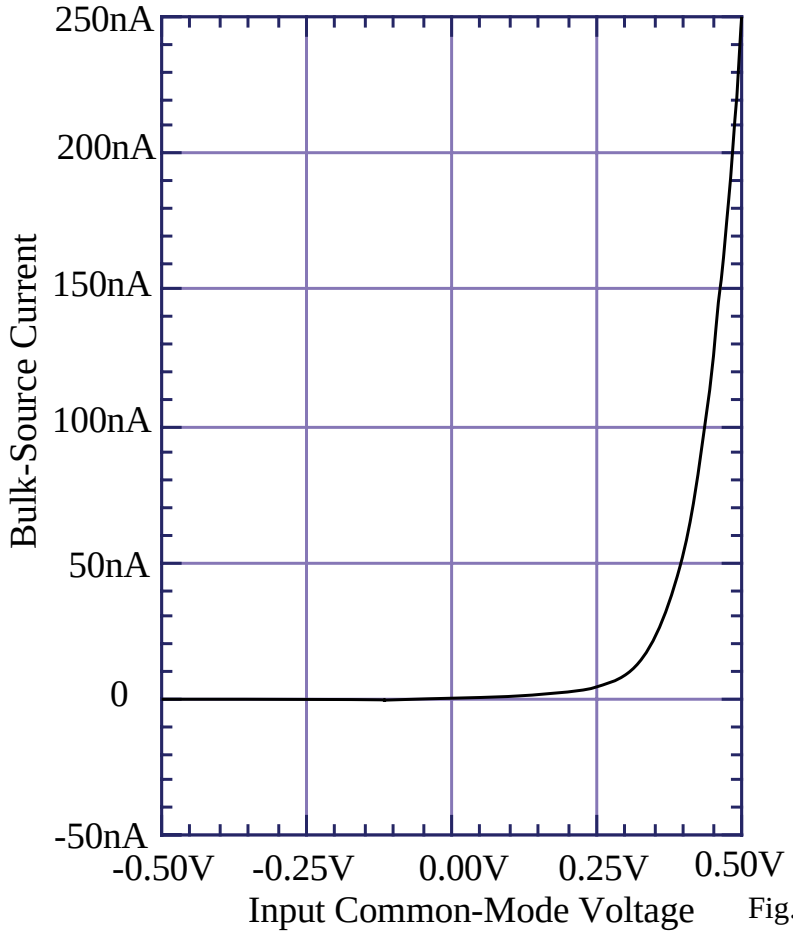


Fig. 7.6-10A

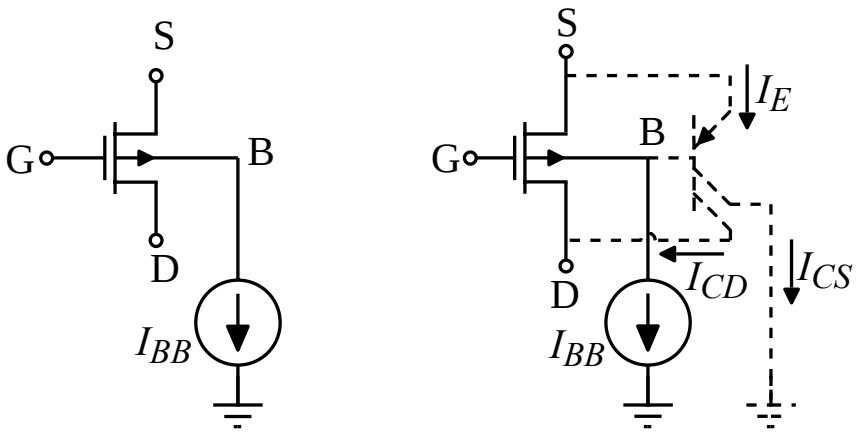
Comments:

- Effective *ICMR* is from V_{SS} to V_{DD} -0.3V
- The transconductance of the input stage can vary as much as 100% over the *ICMR* which makes it very difficult to compensate

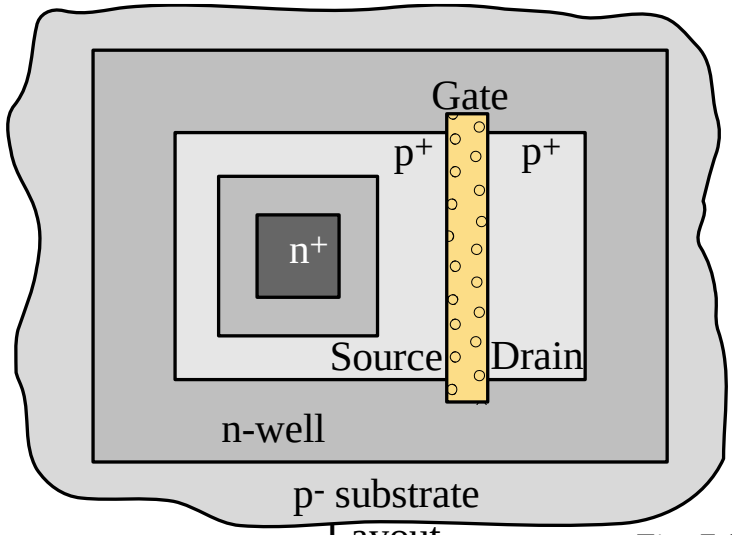
Reduction of V_T through Forward Biasing the Bulk-Source

The bulk can be used to reduce the threshold sufficiently to permit low voltage applications. The key is to control the amount of forward bias of the bulk-source.

Current-Driven Bulk Technique†:



Reduced Threshold MOSFET Parasitic BJT



Layout Fig. 7.6-19

Problem:

Want to limit the BJT current to some value called, I_{max}.

Therefore,

$$I_{BB} = \frac{I_{max}}{\beta_{CS} + \beta_{CD} + 1}$$

† T. Lehmann and M. Cassia, "1V Power Supply CMOS Cascode Amplifier," *IEEE J. of Solid-State Circuits*, Vol. 36, No. 7, 2001.

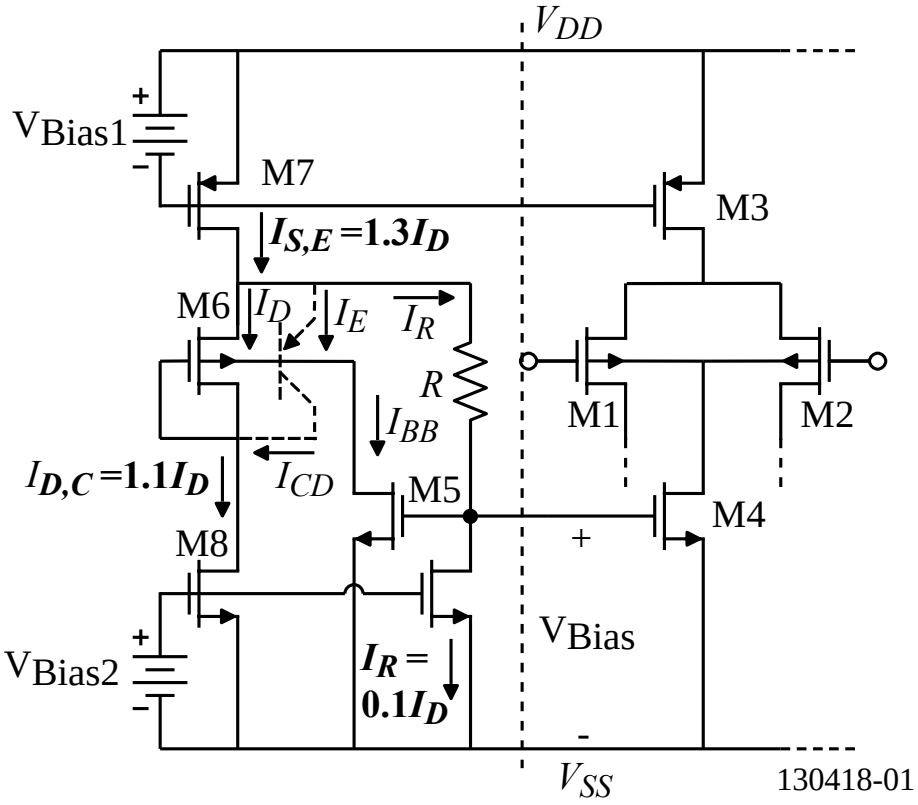
Current-Driven Bulk Technique

Bias circuit for keeping I_{max} defined independent of BJT betas.

Note:

$I_{D,C} = I_{CD} + I_D$

$I_{S,E} = I_D + I_E + I_R$



The circuit feedback causes a bulk bias current I_{BB} and hence a bias voltage V_{BIAS} such that

$$I_{S,E} = I_D + I_{BB}(1+\beta_{CS} + \beta_{CD}) + I_R$$

Use $V_{Bias}1$ and $V_{Bias}2$ to set $I_{D,C} \approx 1.1I_D$, $I_{S,E} \approx 1.3I_D$ and $I_R \approx 0.1I_D$ which sets I_{BB} at $0.1I_D$ assuming we can neglect I_{CS} with respect to I_{CD}. This is illustrated as follows,

$$I_{S,E} \approx I_D + I_{BB}(1+\beta_{CD}) + I_R = I_D + I_{BB} + I_{CD} + I_R = I_D + I_{BB} + 0.1I_D + 0.1I_D = 1.3I_D$$

For this circuit to work, the following conditions must be satisfied:

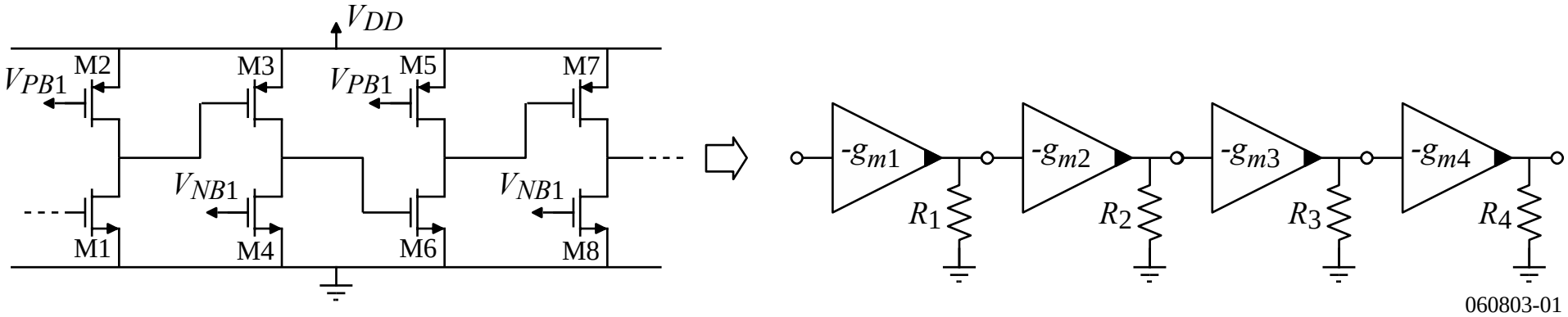
$$V_{BE} < V_{TN} + I_R R \quad \text{and} \quad |V_{TP}| + V_{DS}(\text{sat}) < V_{TN} + I_R R$$

If $|V_{TP}| > V_{TN}$, then the level shifter $I_R R$ can be eliminated.

LOW VOLTAGE GAIN STAGES

Cascade Stages

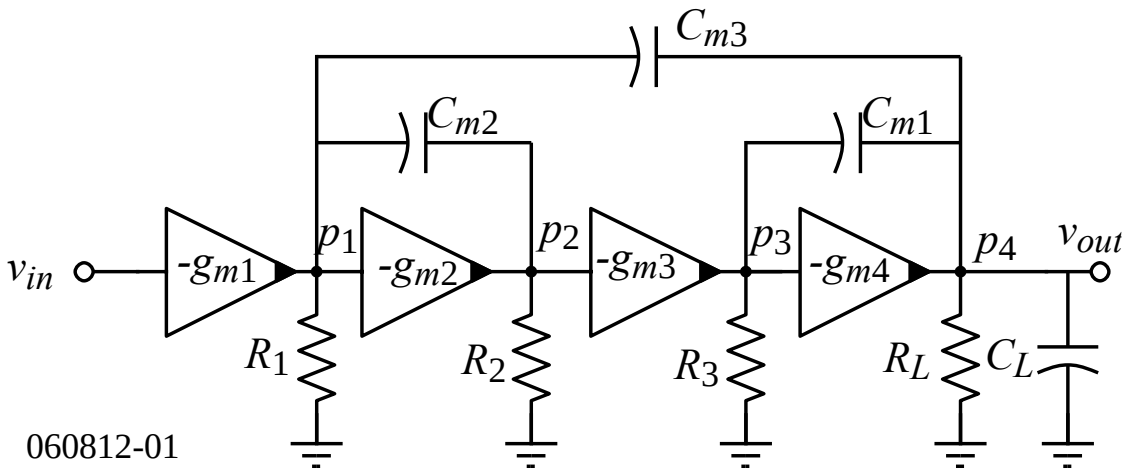
Simple cascade of inverters:



The problem with this approach is the number of poles that occur (one per stage) if the amplifier is to be used in a closed loop application. Instability or poor transient response will result.

Nested Miller Compensation

Principle: Use Miller compensation to split the poles within a feedback loop.



Compensating Results:

1) C_{m1} pushes p_4 to higher frequencies and p_3 down to lower frequencies

2) C_{m2} pushes p_2 to higher frequencies and p_1 down to lower frequencies

3) C_{m3} pushes p_3 to higher frequencies (feedback path) & pulls p_1 further to lower frequencies

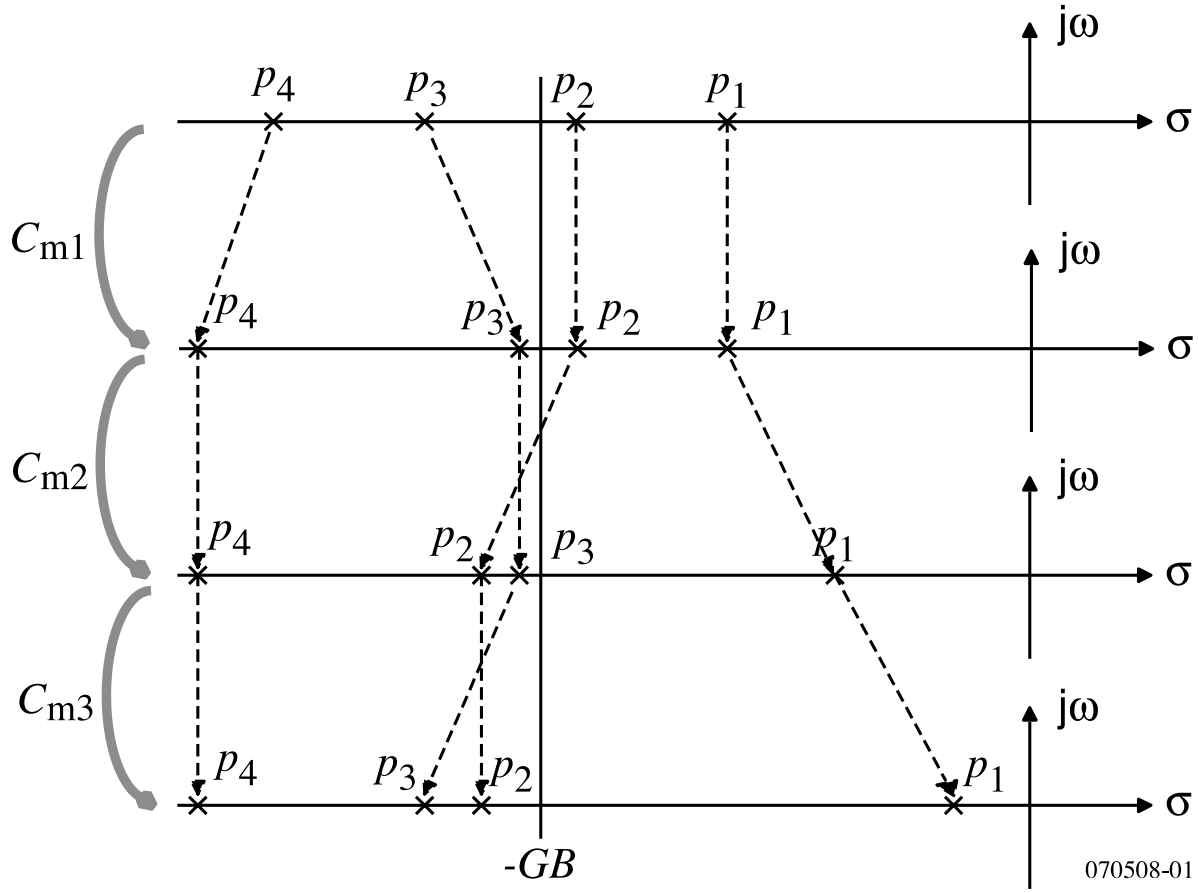
Equations:

$$GB \approx g_{m1}/C_{m3} \qquad p_2 \approx g_{m2}/C_{m3} \qquad p_3 \approx g_{m3}C_{m3}/(C_{m1}C_{m2}) \qquad p_4 \approx g_{m4}/C_L$$

The objective is to get all poles larger than GB:

$$GB < p_2, p_3, p_4$$

Illustration of the Nested Miller Compensation Technique

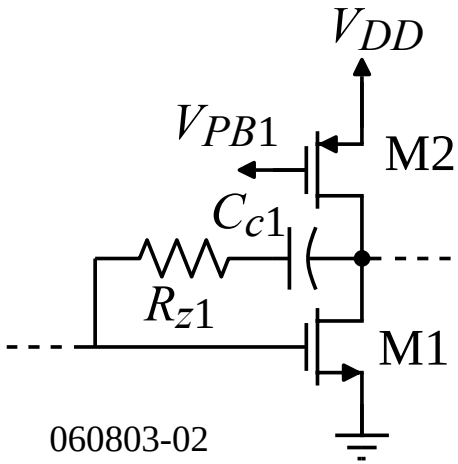


This approach is complicated by the feedforward paths which create RHP zeros.

Elimination of the RHP Zeros

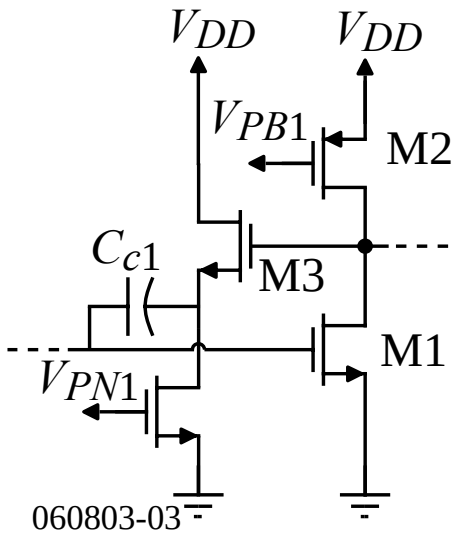
The following are least three ways in which the RHP zeros can be eliminated.

1.) Nulling resistor.



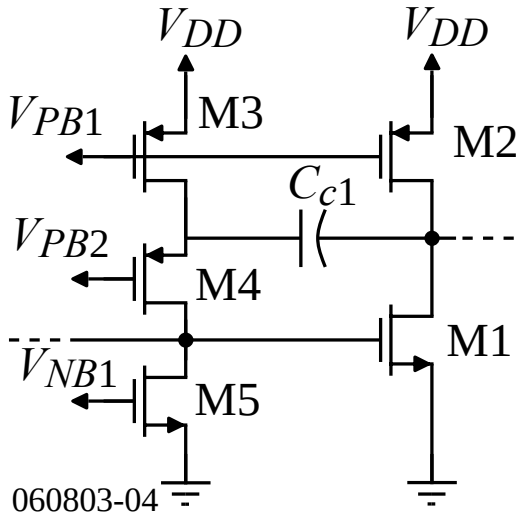
$$z_1 = \frac{1}{C_{c1}(1/g_{m1} - R_{z1})}$$

2.) Feedback only – buffer.



Increases the minimum power supply by V_{ON}.

3.) Feedback only – gain.

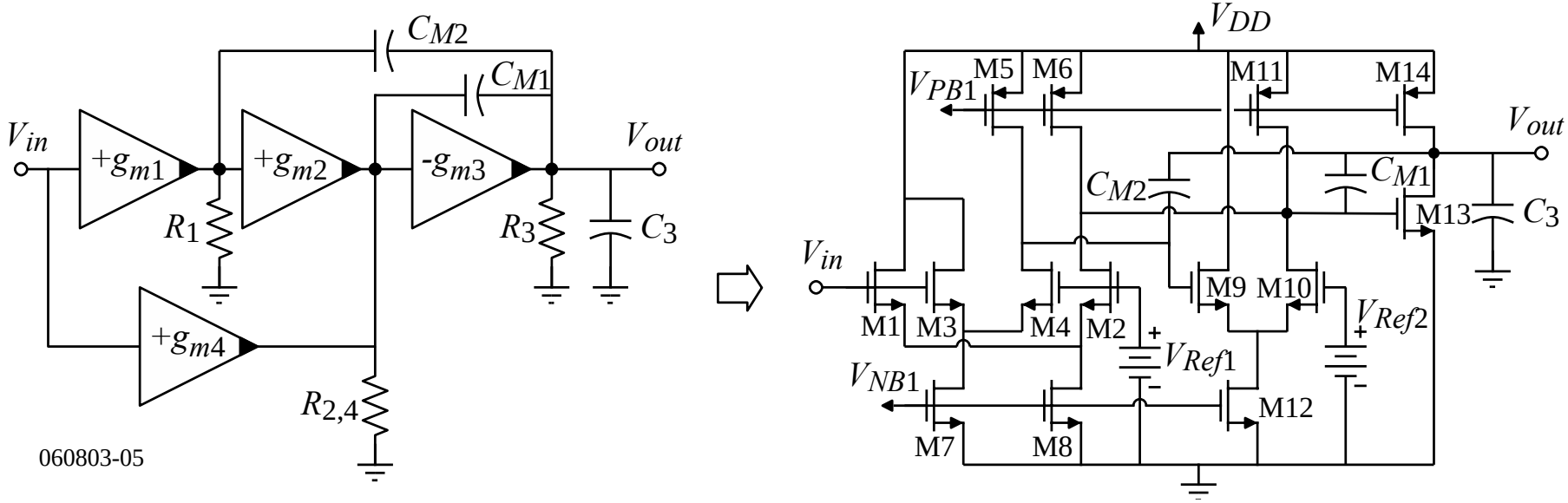


Increases the pole and increases the minimum power supply by V_{ON}.

Use of LHP Zeros to Compensate Cascaded Amplifiers

Principle: Feedforward around a noninverting stage creates a LHP zero or inverting feedforward around an inverting stage also creates a LHP zero.

Example of Multipath, Nested Miller Compensation†:



Unfortunately, the analysis becomes quite complex - for the details refer to the reference below.

† R. Hogervorst and J. H. Huijsing, *Design of Low-Voltage, Low-Power Operational Amplifier Cells*, Kluwer Academic Publishers, 1996, pp. 127-131.

LOW VOLTAGE BIAS CIRCUITS

A Low-Voltage Current Mirror with Wide Input and Output Swings

The current mirror below requires a power supply of V_T+3V_{ON} and has a V_{in}(min) = V_{ON} and a V_{out}(min) = $2V_{ON}$ (less for the regulated cascode output mirror).

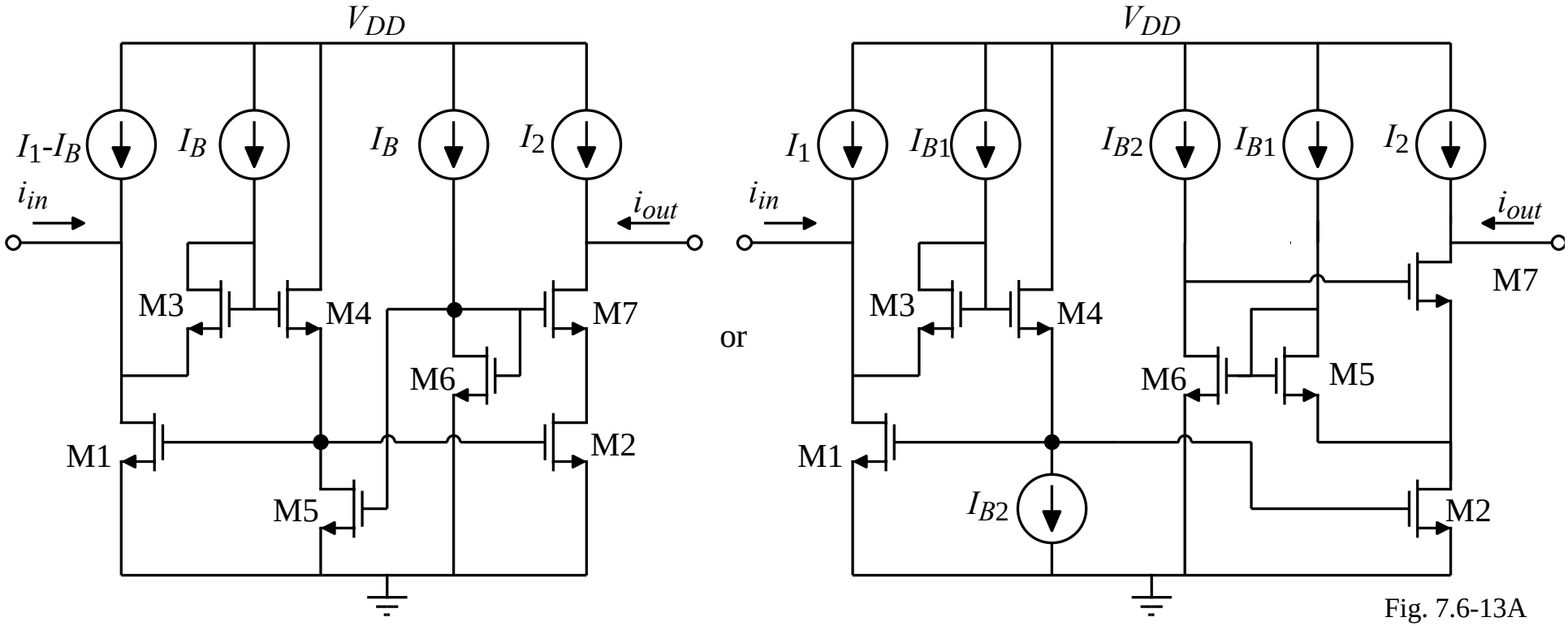
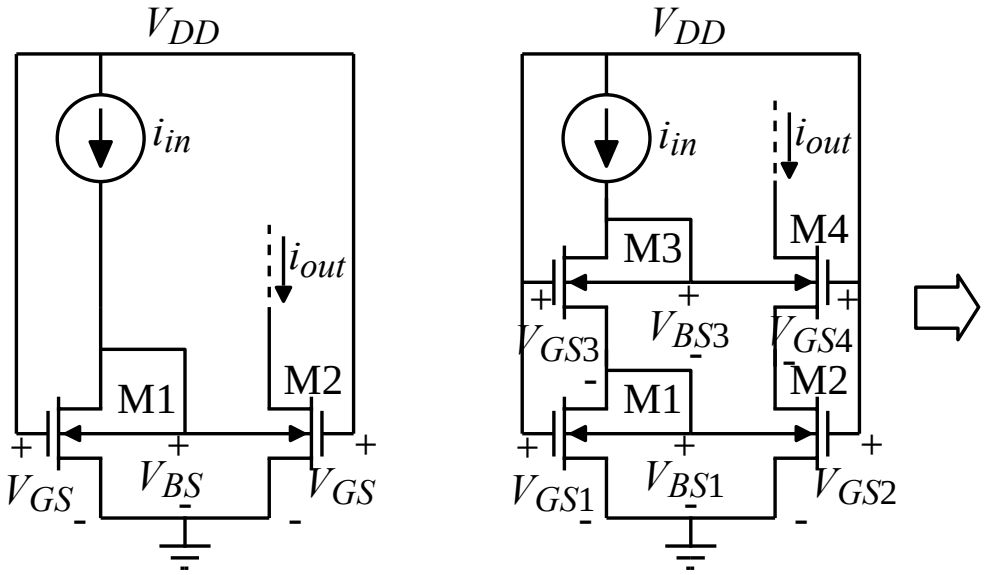


Fig. 7.6-13A

Low-Voltage Current Mirrors using the Bulk-Driven MOSFET

The biggest problem with current mirrors is the large minimum input voltage required for previously examined current mirrors.

If the bulk-driven MOSFET is biased with a current that exceeds I_{DSS} then it is enhancement and can be used as a current mirror.



Simple bulk-driven current mirror

Cascodebulk-driven current mirror.

Fig.7.6-11

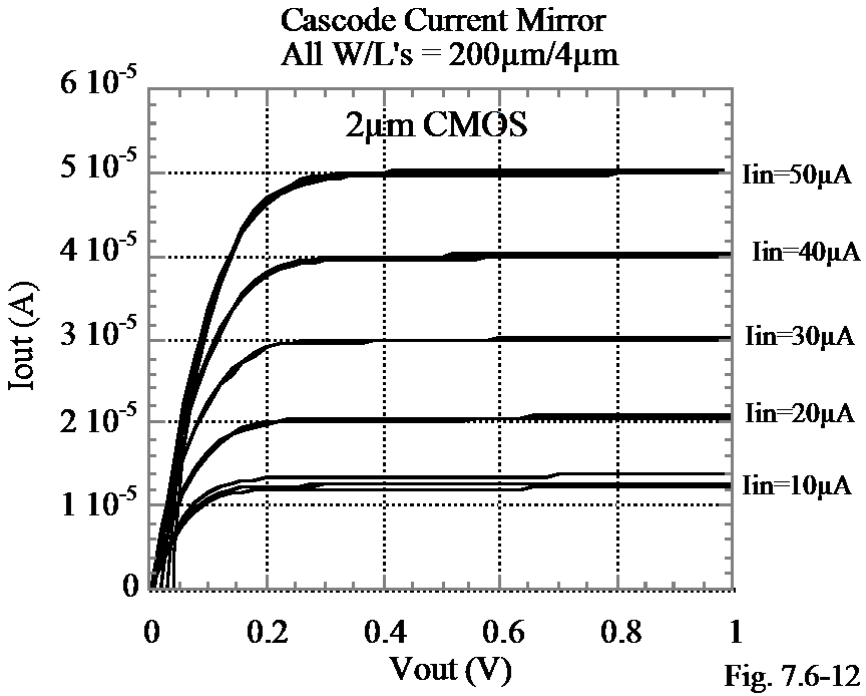
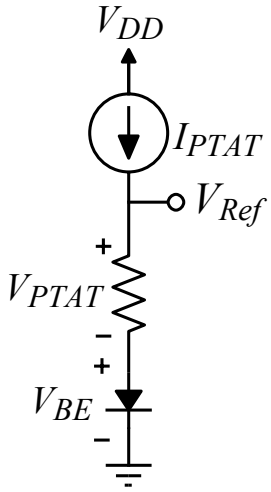


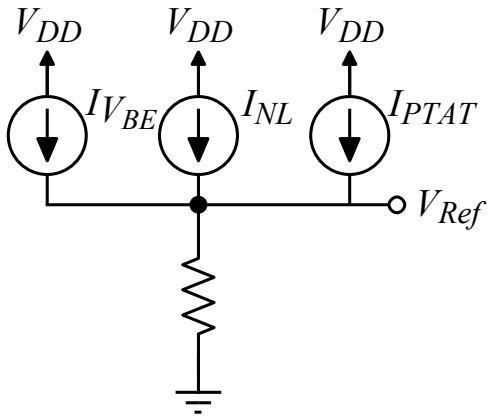
Fig. 7.6-12

The cascode current mirror gives a minimum input voltage of less than 0.5V for currents less than 100µA

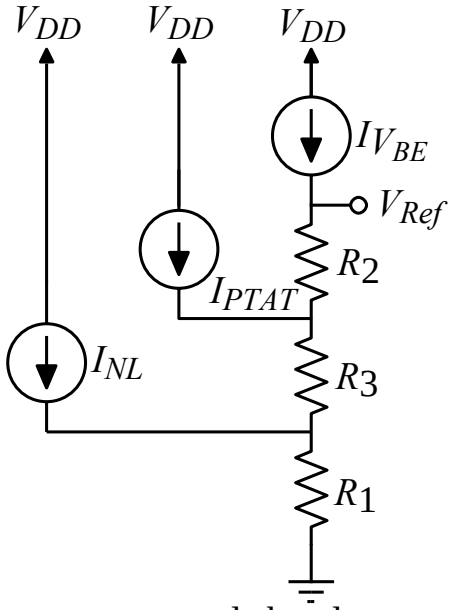
Bandgap Topologies Compatible with Low Voltage Power Supply



Voltage-mode bandgap topology.



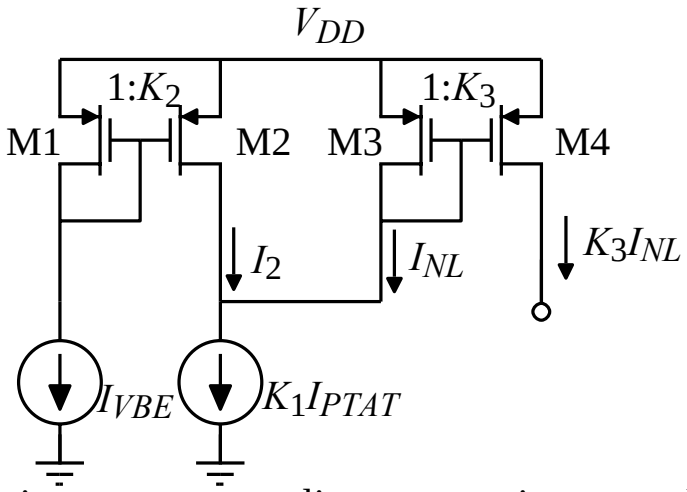
Current-mode bandgap topology.



Voltage-current mode bandgap topology.

Fig. 7.6-14

Technique for Canceling the Bandgap Curvature



Circuit to generate nonlinear correction term, I_{NL}.

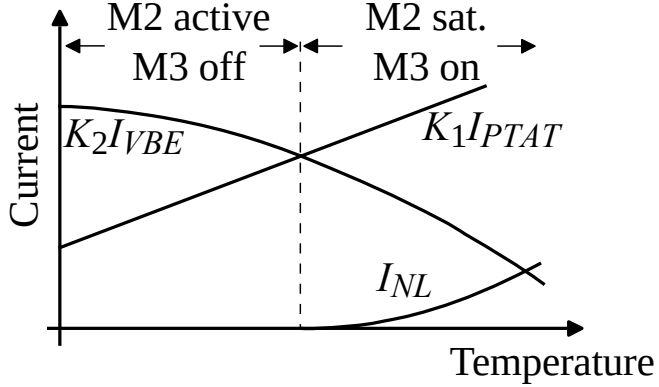


Illustration of the various currents.

Fig. 7.6-16

$$I_{NL} = \begin{cases} 0 & , \quad K_2I_{VBE} > K_1I_{PTAT} \\ K_1I_{PTAT} - K_2I_{VBE} & , \quad K_2I_{VBE} < K_1I_{PTAT} \end{cases}$$

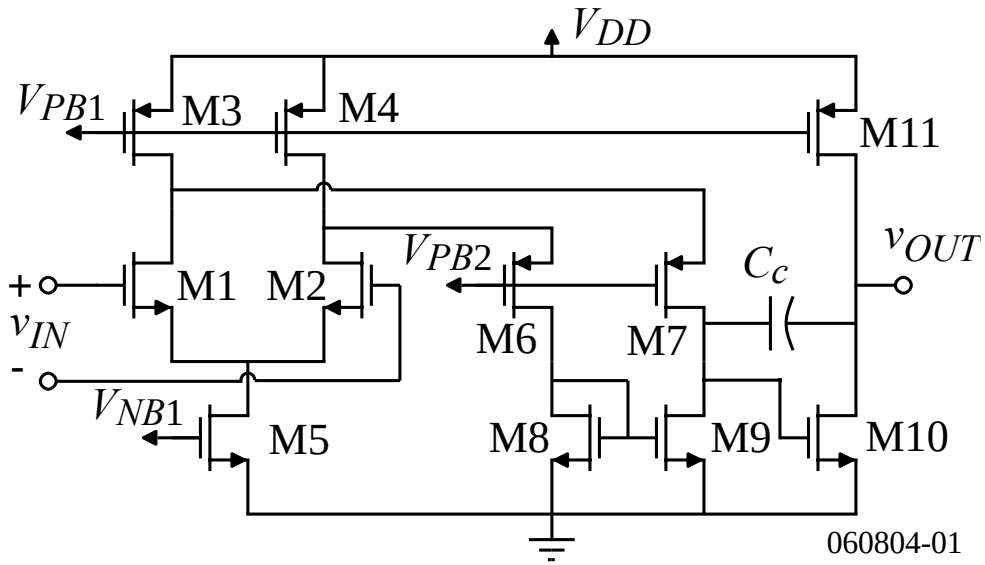
The combination of the above concept with the previous slide yielded a curvature-corrected bandgap reference of 0.596V with a TC of 20ppm/C° from -15C° to 90C° using a 1.1V power supply.† In addition, the line regulation was 408 ppm/V for $1.2 \le V_{DD} \le 10$V and 2000 ppm/V for $1.1 \le V_{DD} \le 10$V. The quiescent current was 14µA.

† G.A. Rincon-Mora and P.E. Allen, "A 1.1-V Current-Mode and Piecewise-Linear Curvature-Corrected Bandgap Reference," *J. of Solid-State Circuits*, vol. 33, no. 10, October 1998, pp. 1551-1554.

LOW VOLTAGE OP AMPS

A Low Voltage Op Amp using Normal Technology

V_{DD}(min) = $3V_{ON} + V_T$ ($ICMR = V_{ON}$):



Performance:

Gain ≈ $g_m^2 r_{ds}^2$

Miller compensated

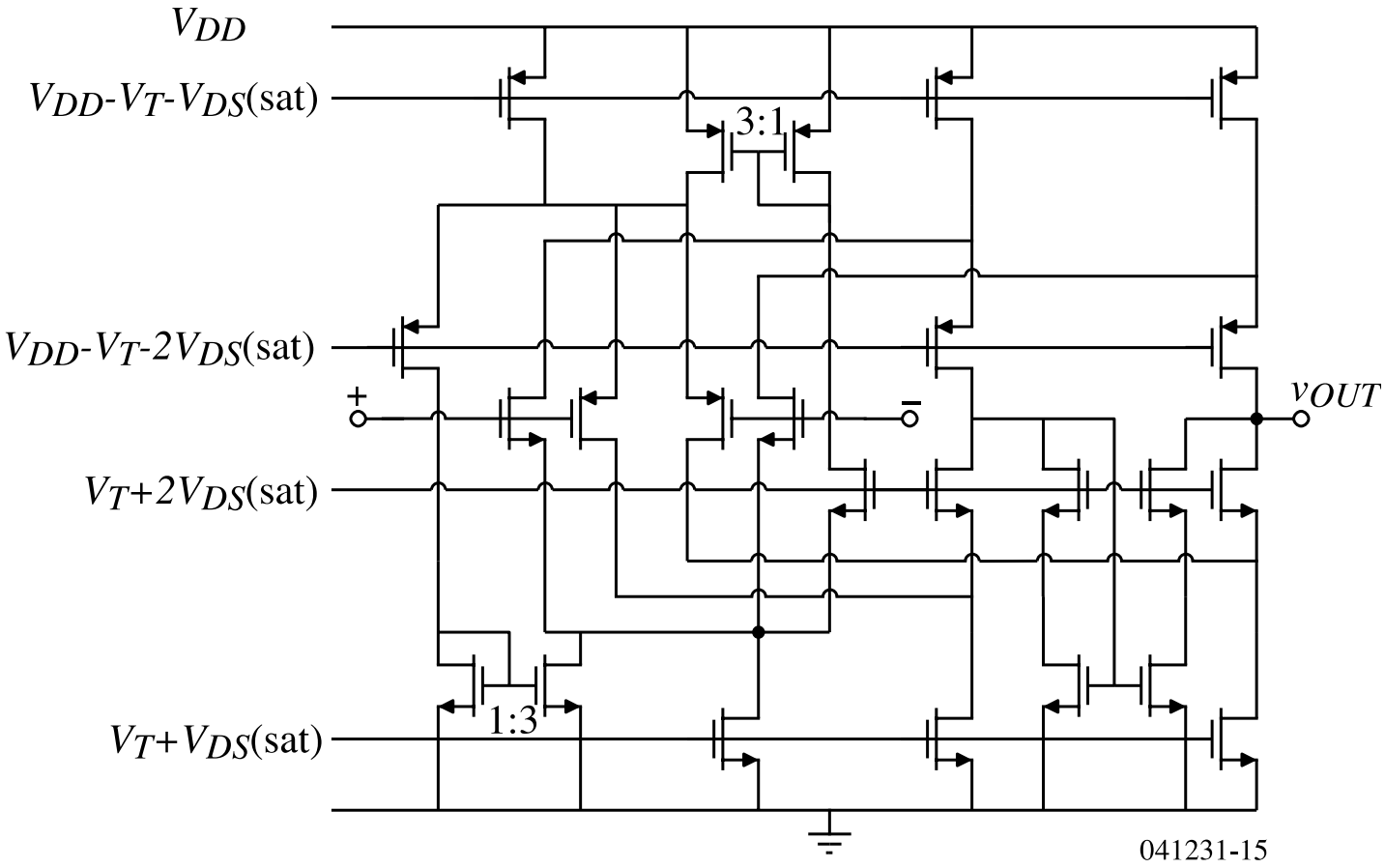
Output swing is V_{DD} -2V_{ON}

Max. CM input = V_{DD}

Min. CM input = 2V_{ON} + V_T

A Low-Voltage, Wide *ICMR* Op Amp

$V_{DD}(\text{min}) = 4V_{ON} + 2V_T$ ($ICMR = V_{DD}$):

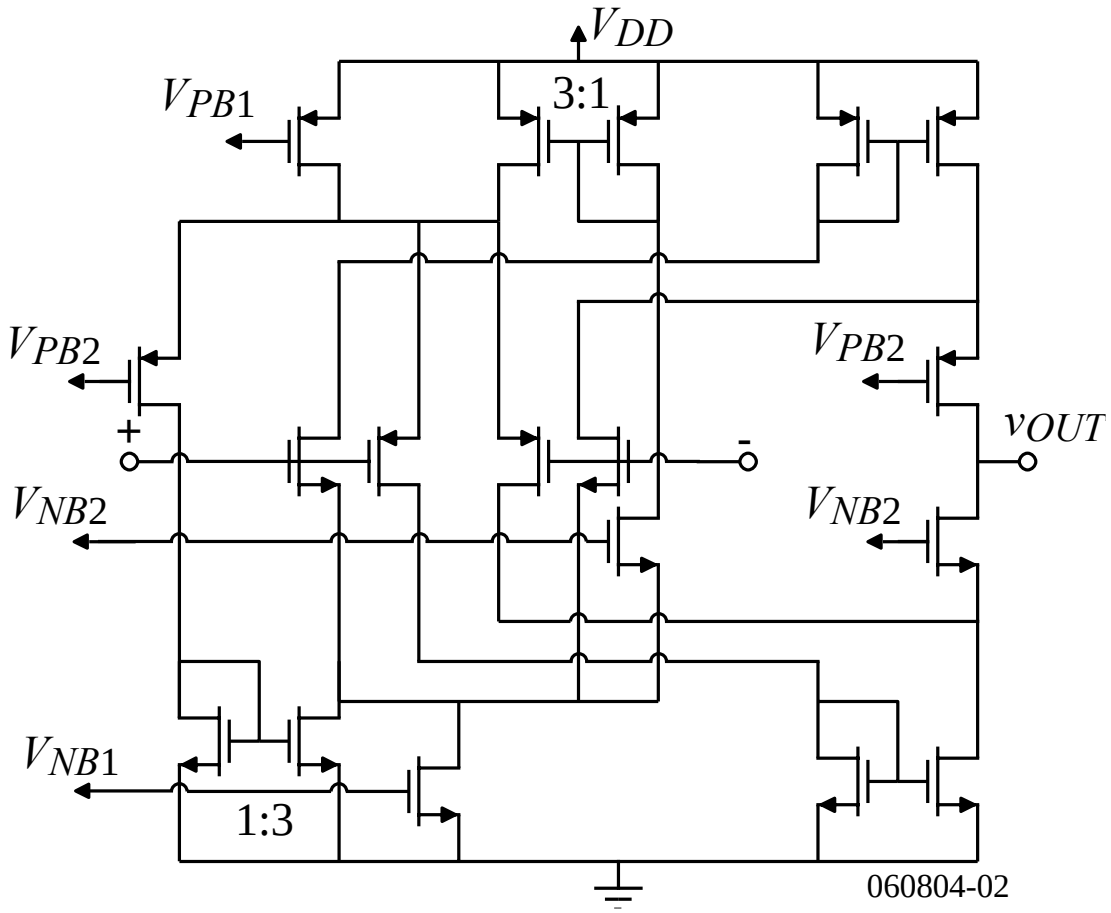


Performance:

Gain ≈ $g_m^2 r_{ds}^2$, self compensated, and output swing is V_{DD} -4V_{ON}

An Alternate Low-Voltage, Wide *ICMR* Op Amp

$V_{DD}(\text{min}) = 4V_{ON} + 2V_T$ ($ICMR = V_{DD}$):



A 1-Volt, Two-Stage Op Amp

Uses a bulk-driven differential input amplifier.

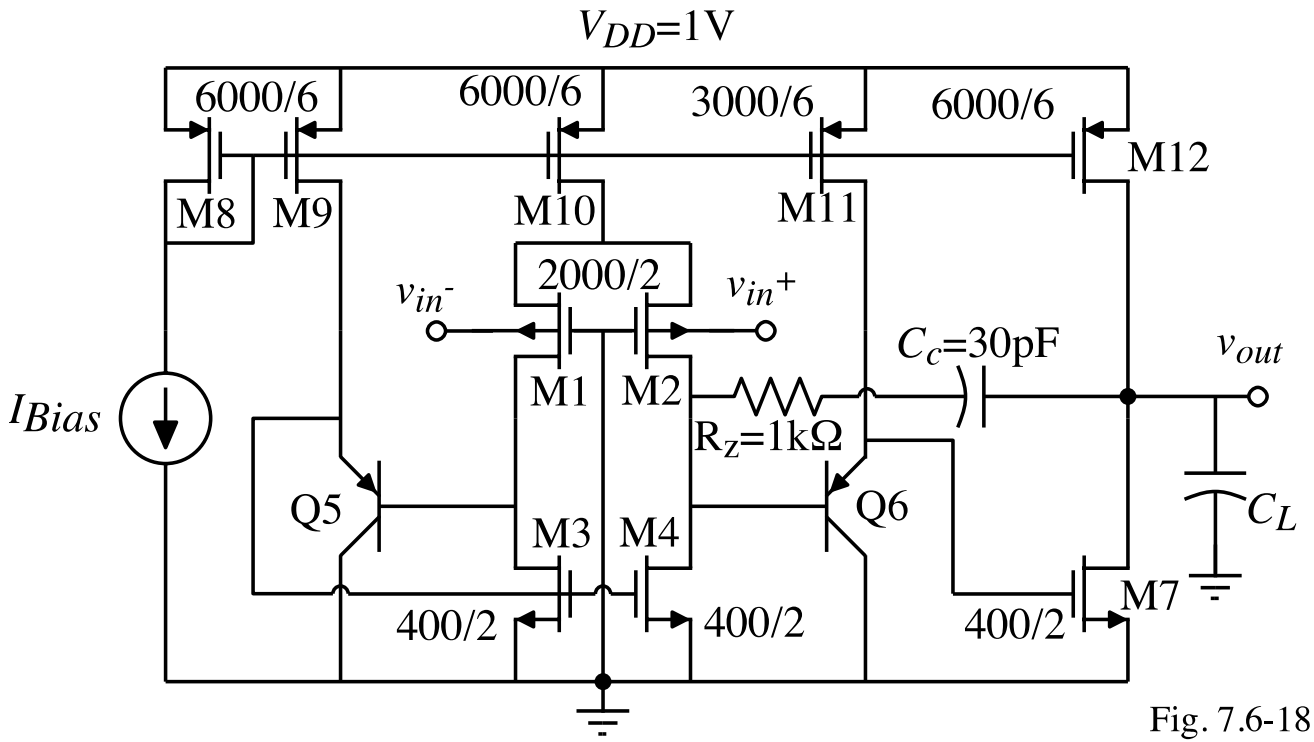


Fig. 7.6-18

Performance of the 1-Volt, Two-Stage Op Amp

Specification (V_{DD}=0.5V, V_{SS}=-0.5V)	Measured Performance (C_L = 22pF)
DC open-loop gain	49dB (V_{icm} mid range)
Power supply current	300µA
Unity-gainbandwidth (*GB*)	1.3MHz (V_{icm} mid range)
Phase margin	57° (V_{icm} mid range)
Input offset voltage	±3mV
Input common mode voltage range	-0.475V to 0.450V
Output swing	-0.475V to 0.491V
Positive slew rate	+0.7V/µsec
Negative slew rate	-1.6V/µsec
THD, closed loop gain of -1V/V	-60dB (0.75Vp-p, 1kHz sinewave) -59dB (0.75Vp-p, 10kHz sinewave)
THD, closed loop gain of +1V/V	-59dB (0.75Vp-p, 1kHz sinewave) -57dB (0.75Vp-p, 10kHz sinewave)
Spectral noise voltage density	367nV/$\sqrt{\text{Hz}}$ @ 1kHz 181nV/$\sqrt{\text{Hz}}$ @ 10kHz, 81nV/$\sqrt{\text{Hz}}$ @ 100kHz 444nV/$\sqrt{\text{Hz}}$ @ 1MHz
Positive Power Supply Rejection	61dB at 10kHz, 55dB at 100kHz, 22dB at 1MHz
Negative Power Supply Rejection	45dB at 10kHz, 27dB at 100kHz, 5dB at 1MHz

A 1-Volt, Folded-Cascode OTA using the Current-Driven Bulk Technique

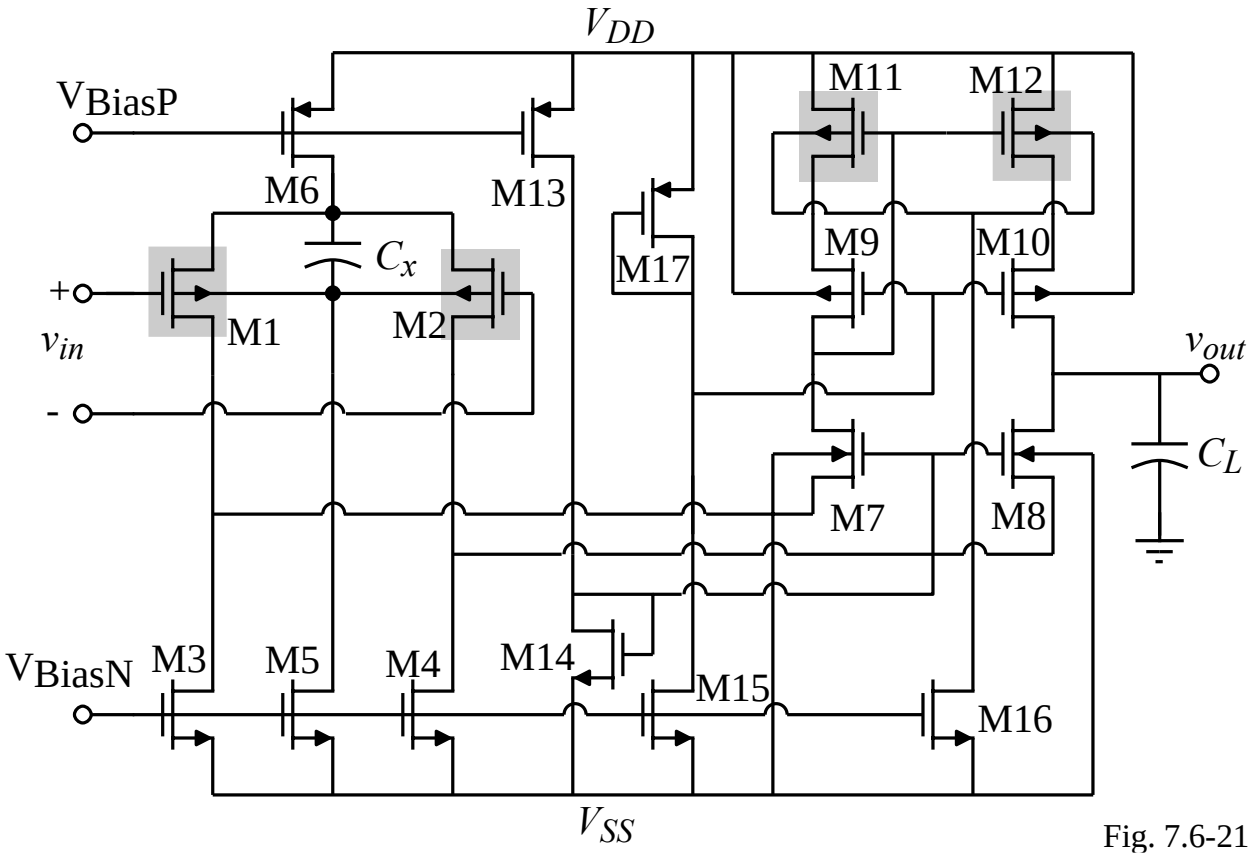


Fig. 7.6-21

Transistors with forward-biased bulks are in a shaded box.

For large common mode input changes, C_x, is necessary to avoid slewing in the input stage.

To get more voltage headroom at the output, the transistors of the cascode mirror have their bulks current driven.

A 1-Volt, Folded-Cascode OTA using the Current-Driven Bulk Technique - Continued

Experimental results:

0.5µm CMOS, 40µA total bias current (C_x = 10pF)

Supply Voltage	1.0V	0.8V	0.7V
Common-mode input range	0.0V-0.65V	0.0V-0.4V	0.0V-0.3V
High gain output range	0.35V-0.75V	0.25V-0.5V	0.2V-0.4V
Output saturation limits	0.1V-0.9V	0.15V-0.65V	0.1V-0.6V
DC gain	62dB-69dB	46dB-53dB	33dB-36dB
Gain-Bandwidth	2.0MHz	0.8MHz	1.3MHz
Slew-Rate (C_L=20pF)	0.5V/µs	0.4V/µs	0.1V/µs
Phase margin (C_L=20pF)	57°	54°	48°

The nominal value of bulk current is 10nA gives a 10% increase in differential pair quiescent current assuming a BJT β of 100.

SUMMARY

- Integrated circuit power supplies are rapidly decreasing (today 2-3Volts)
- Classical analog circuit design techniques begin to deteriorate at 1.5-2 Volts
- Approaches for lower voltage circuits:
  - Use natural NMOS transistors ($V_T \approx 0.1$V)
  - Drive the bulk terminal
  - Forward bias the bulk
  - Use depeletion devices
- The dynamic range will be compressed if the noise is not also reduced
- Fortunately, the threshold reduction continues to allow the techniques of this section to be used in today's technology