# LECTURE 29 – LOW POWER AND LOW NOISE OP AMPS

## LECTURE ORGANIZATION

**Outline**

- Review of subthreshold operation
- Low power op amps
- Review of MOSFET noise modeling and analysis
- Low noise op amps
- Summary

***CMOS Analog Circuit Design*, 3rd Edition Reference**

Pages 398-419

# REVIEW OF SUBTHRESHOLD OPERATION

## Subthreshold Operation

Most micropower op amps use transistors in the subthreshold region.

Subthreshold characteristics:

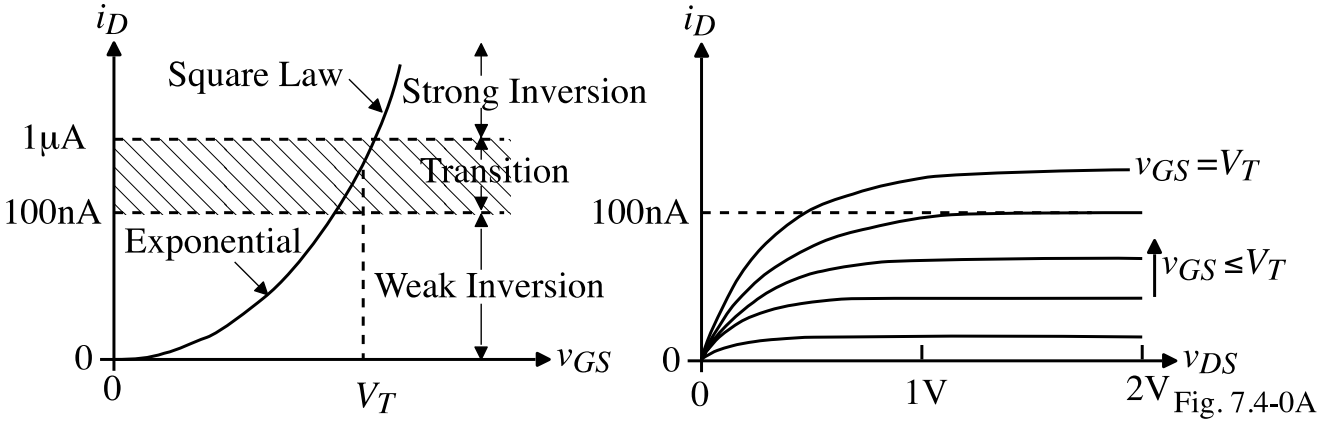


Fig. 7.4-0A

The model that has been developed for the large signal sub-threshold operation is:

$$i_D = I_t \frac{W}{L} \exp\left(\frac{v_{GS}-V_T}{nV_t}\right)\left(1 + \frac{v_{DS}}{V_A}\right) \quad \text{where } v_{DS} > 0 \text{ and } V_{DS}(\text{sat}) = V_{ON} = V_{GS} - V_T = 2nV_t$$

Small-signal model:

$$g_m = \left.\frac{di_D}{dv_{GS}}\right|_Q = I_t \frac{W}{L}\frac{I_t}{nV_t} \exp\left(\frac{v_{GS}-V_T}{nV_t}\right)\left(1 + \frac{v_{DS}}{V_A}\right) = \frac{I_D}{nV_t} = \frac{qI_D}{nkT} = \frac{I_D}{V_t}\frac{C_{ox}}{C_{ox}+C_{js}}$$

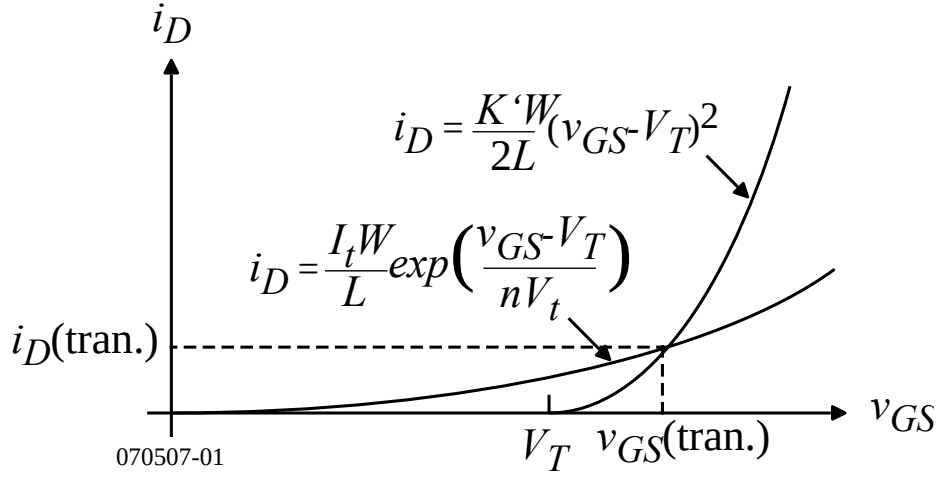
$$g_{ds} = \left.\frac{di_D}{dv_{DS}}\right|_Q \approx \frac{I_D}{V_A}$$

## Boundary Between Subthreshold and Strong Inversion

It is useful to develop a means of estimating when a MOSFET is making the transition between subthreshold and strong inversion to know when to use the proper model.

The relationship developed is based on the following concept:

We will solve for the value of $v_{GS}$ (actually $v_{GS}$ -$V_T$) and find the drain current where these two values are equal [$v_{GS}$(tran.) -$V_T$)].




The large signal expressions for each region are:

Subthreshold-

$$i_D \approx I_t \frac{W}{L} \exp\left(\frac{v_{GS}-V_T}{nV_t}\right) \Rightarrow v_{GS}-V_T = nV_t \ln\left(\frac{i_D}{I_t(W/L)}\right) \approx nV_t\left(1 - \frac{I_t(W/L)}{i_D}\right)$$

if $(I_tW/L)/i_D < 0.5$.

Strong inversion-

$$i_D = \frac{K'W}{2L}(v_{GS}-V_T)^2 \quad \Rightarrow \quad v_{GS}-V_T = \sqrt{\frac{2i_D}{K'(W/L)}}$$

## Boundary Between Subthreshold and Strong Inversion - Continued

Equating the two large signal expressions gives,

$$nV_t\left(1 - \frac{I_t(W/L)}{i_D}\right) = \sqrt{\frac{2i_D}{K'(W/L)}} \Rightarrow n^2V_t^2\left(1 - \frac{I_t(W/L)}{i_D}\right)^2 = \frac{2i_D}{K'(W/L)}$$

Expanding gives,

$$n^2V_t^2\left(\frac{I_t^2(W/L)^2}{i_D^2} - \frac{2\,I_t(W/L)}{i_D} + 1\right) \approx n^2V_t^2 = \frac{2i_D}{K'(W/L)} \qquad \text{if} \quad (I_tW/L)/i_D < 0.5$$

Therefore we get,

$$i_D(\text{tran.}) = \frac{K'W}{2L}\,n^2V_t^2$$

For example, if $K'$ = 120μA/V$^2$, $W/L$ = 100, and $n$ = 2, then at room temperature the value of drain current at the transition between subthreshold and strong inversion is

$$i_D(\text{tran.}) = \frac{120\mu\text{A/V}^2 100}{2}\,4\cdot(0.026)^2 = 16.22\mu\text{A}$$

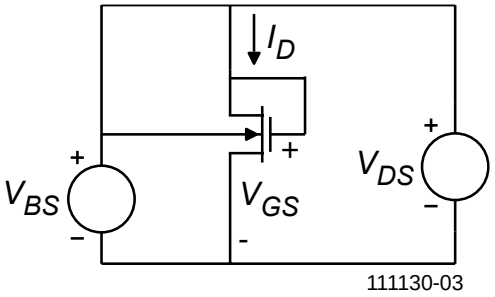
One will find for UDSM technology, that weak inversion or subthreshold operation can occur at large currents for large values of $W/L$.

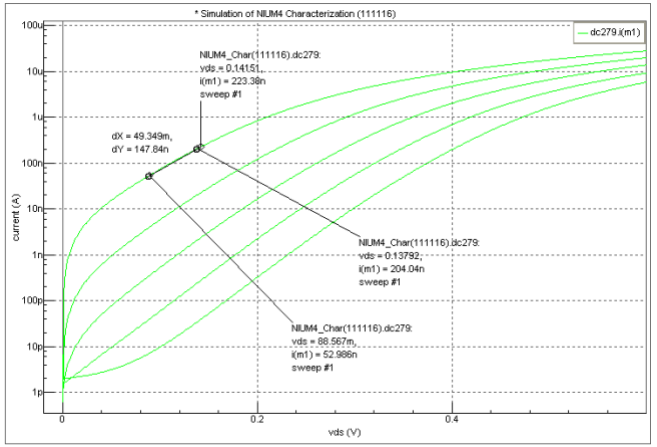
# Extraction of Weak Inversion Model Parameters

Model:

$$i_D = I_t \left(\frac{W}{L}\right) \exp\left(\frac{v_{GS} - V_T}{nV_t}\right)(1+\lambda\, v_{DS}) \quad \text{and} \quad v_{GS} = V_T - nV_t\, ln\left(\frac{i_D}{I_t\,(W/L)}\right)$$

Extraction circuit and results for low threshold NMOS:




1.) Extraction of $I_t$ (W/L=2.5).

Set $V_{GS} = V_T$ to get $I_D = I_t\left(\frac{W}{L}\right)$ which gives $I_t = I_D\left(\frac{L}{W}\right)$ = 204nA (0.4) = 81.6 nA

2.) Extraction of $n$:

Take the log of the current relationship to get,

$$\ln(i_D) = \ln\left(I_t \frac{W}{L}\right) + \frac{v_{GS} - V_T}{nV_t} \rightarrow \frac{d(\ln i_D)}{dv_{GS}} = \frac{1}{nV_t} \rightarrow n = \frac{1}{V_t}\left(\frac{V_{GS2} - V_{GS1}}{\ln(I_{D2}) - \ln(I_{D1})}\right)$$

$$n = \frac{1}{0.0259}\left(\frac{0.14151 - 0.088567}{\ln(223.38\text{nA}) - \ln(52.966\text{nA})}\right) = 1.418$$

# LOW POWER OP AMPS

## Two-Stage, Miller Op Amp Operating in Weak Inversion

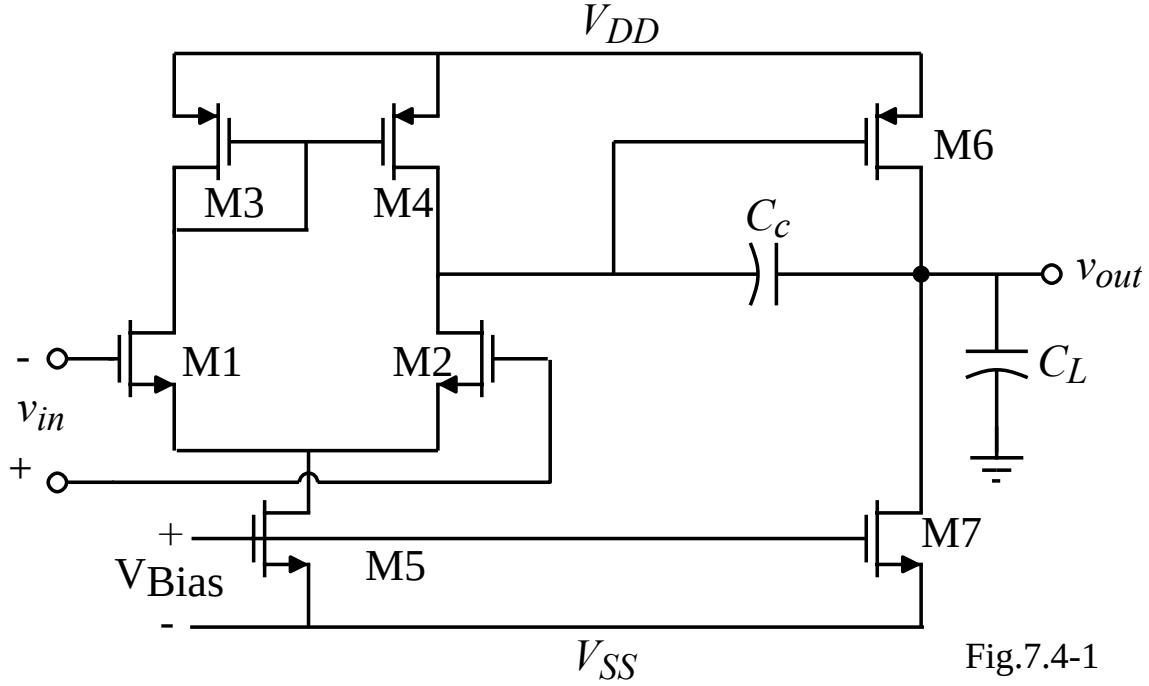



Fig.7.4-1

Low frequency response:

$$A_{vo} = g_{m2}g_{m6}\left(\frac{r_{o2}r_{o4}}{r_{o2}+r_{o4}}\right)\left(\frac{r_{o6}r_{o7}}{r_{o6}+r_{o7}}\right) = \frac{1}{n_2 n_6 (kT/q)^2(\lambda_2+\lambda_4)(\lambda_6+\lambda_7)} \quad \left(\text{No longer} \propto \frac{1}{\sqrt{I_D}}\right)$$

*GB* and *SR*:

$$GB = \frac{I_{D1}}{(n_1 kT/q)C} \qquad \text{and} \qquad SR = \frac{I_{D5}}{C} = 2\frac{I_{D1}}{C} = 2GB\left(n_1\frac{kT}{q}\right) = 2GBn_1V_t$$

## Example 29-1 Gain and GB Calculations for Subthreshold Op Amp.

Calculate the gain, *GB*, and *SR* of the op amp shown above. The currents are $I_{D5}$ = 200 nA and $I_{D7}$ = 500 nA. The device lengths are 1 $\mu$m. Values for n are 1.5 and 2.5 for p-channel and n-channel transistors respectively. The compensation capacitor is 5 pF. The channel length modulation parameters are $\lambda_N = 0.06\text{V}^{-1}$ and $\lambda_P = 0.08\text{V}^{-1}$. Assume that the temperature is 27 °C. If $V_{DD}$ = 1.5V and $V_{SS}$ = -1.5V, what is the power dissipation of this op amp?

*Solution*

The low-frequency small-signal gain is,

$$A_v = \frac{1}{(1.5)(2.5)(0.026)^2(0.06+0.08)(0.06+0.08)} = 20{,}126 \text{ V/V}$$

The gain bandwidth is

$$GB = \frac{100\text{x}10^{-9}}{2.5(0.026)(5\text{x}10^{-12})} = 307{,}690 \text{ rps} \cong 49.0 \text{ kHz}$$

The slew rate is

$$SR = (2)(307690)(2.5)(0.026) = 0.04 \text{ V}/\mu\text{s}$$

The power dissipation is,

$$P_{diss} = 3(0.7\mu\text{A}) = 2.1\mu\text{W}$$

## Push-Pull Output Op Amp in Weak Inversion

First stage gain is,

$$A_{vo} = \frac{g_{m2}}{g_{m4}} = \frac{I_{D2}n_4V_t}{I_{D4}n_2V_t} = \frac{I_{D2}n_4}{I_{D4}n_2} \cong 1$$

Total gain is,

$$A_{vo} = \frac{g_{m1}(S_6/S_4)}{(g_{ds6} + g_{ds7})} = \frac{(S_6/S_4)}{(\lambda_6 + \lambda_7)n_1V_t}$$

At room temperature ($V_t$ = 0.0259V) and for typical device lengths, gains of 60dB can be obtained.

The *GB* is,

$$GB = \frac{g_{m1}}{C}\left(\frac{S6}{S4}\right) = \frac{g_{m1}b}{C}$$

where *b* is the current ratio between M4:M6 and M3:M8.

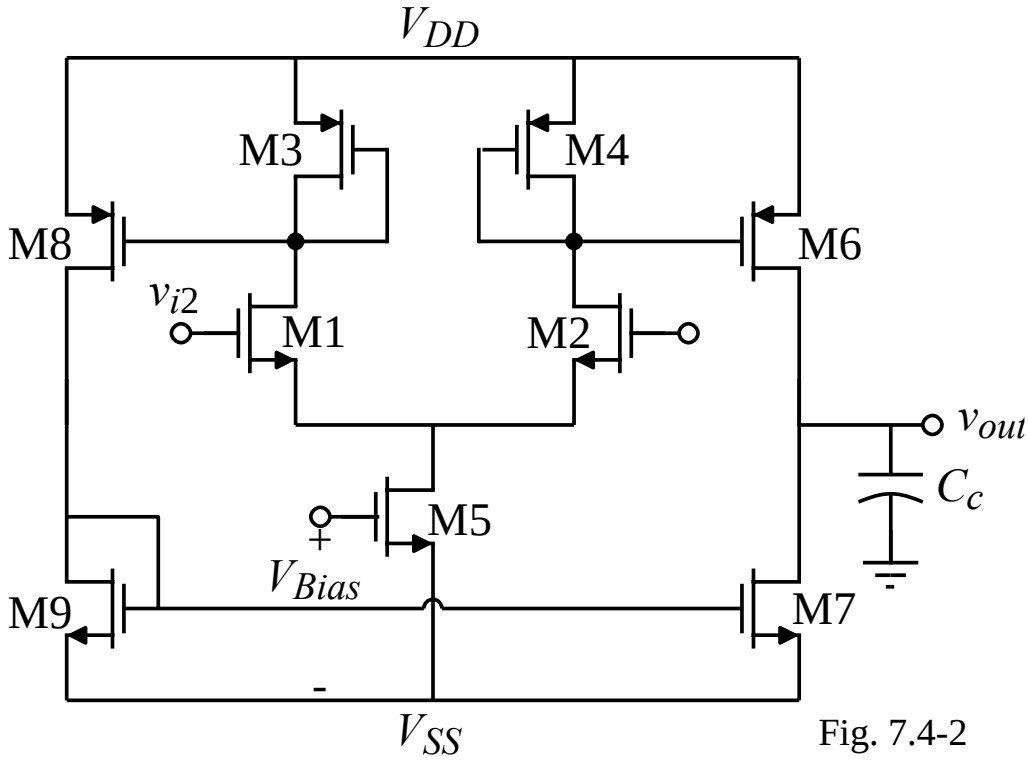



Fig. 7.4-2

## Increasing the Gain of the Previous Op Amp

1.) Can reduce the currents in M3 and M4 and introduce gain in the current mirrors.

2.) Use a cascode output stage (can't use self-biased cascode, currents are too low).

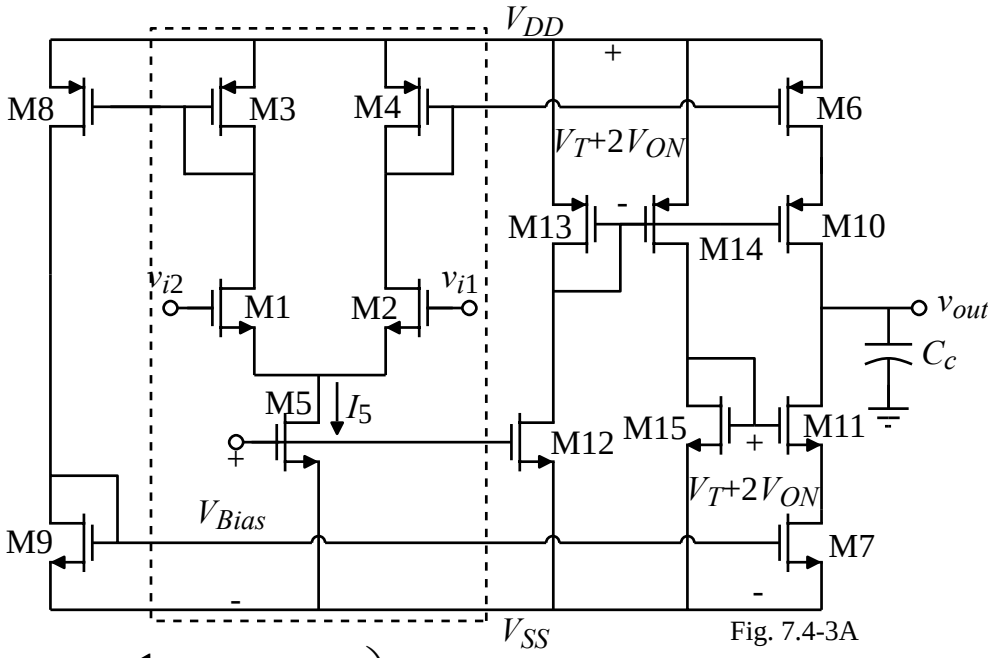


Fig. 7.4-3A

$$A_v = \left(\frac{g_{m1}+g_{m2}}{2}\right)R_{out}$$

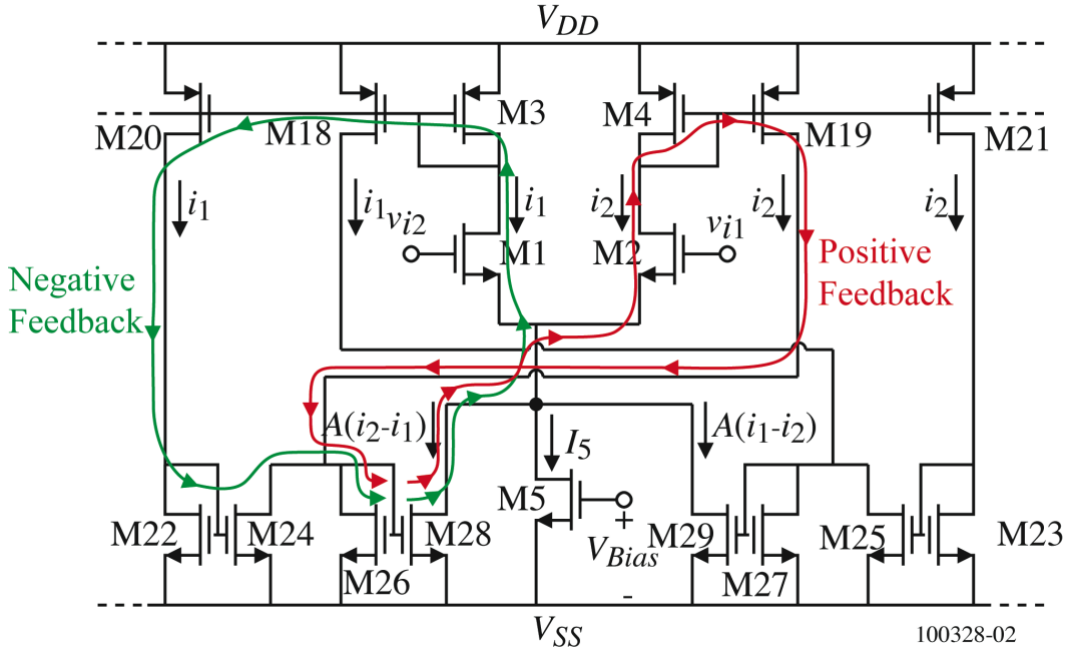
$$= \frac{\frac{I_5}{2n_nV_t}}{\frac{I_7^2\lambda_n^2}{\frac{I_7}{n_nV_t}} + \frac{I_7^2\lambda_p^2}{\frac{I_7}{n_pV_t}}} = \left(\frac{I_5}{2I_7}\right)\left(\frac{1}{n_nV_t^2(n_n\lambda_n^2+n_p\lambda_p^2)}\right)$$

Can easily achieve gains greater than 80dB with power dissipation of less than 1μW.

## Increasing the Output Current for Weak Inversion Operation

A significant disadvantage of the weak inversion is that very small currents are available to drive output capacitance so the slew rate becomes very small.

Dynamically biased differential amplifier input stage:




Note that the sinking current for M1 and M2 is

$$I_{sink} = I_5 + A(i_2\text{-}i_1) + A(i_1\text{-}i_2)$$ where $(i_2\text{-}i_1)$ and $(i_1\text{-}i_2)$ are only positive or zero.

If $v_{i1}>v_{i2}$, then $i_2>i_1$ and the sinking current is increased by $A(i_2\text{-}i_1)$.

If $v_{i2}>v_{i1}$, then $i_1>i_2$ and the sinking current is increased by $A(i_1\text{-}i_2)$.

## Dynamically Biased Differential Amplifier - Continued

How much output current is available from this circuit if there is no current gain from the input to output stage?

Assume transistors M18 through M21 are equal to M3 and M4 and that transistors M22 through M27 are all equal.

Let $\frac{W_{28}}{L_{28}} = A\left(\frac{W_{26}}{L_{26}}\right)$ and $\frac{W_{29}}{L_{29}} = A\left(\frac{W_{27}}{L_{27}}\right)$

The output current available can be found by assuming that $v_{in} = v_{i1}\text{-}v_{i2} > 0$.

$\therefore \quad i_1 + i_2 = I_5 + A(i_2\text{-}i_1)$

The ratio of $i_2$ to $i_1$ can be expressed as

$$\frac{i_2}{i_1} = \exp\left(\frac{v_{in}}{nV_t}\right)$$

If the output current is $i_{OUT} = b(i_2\text{-}i_1)$ then combining the above two equations gives,

$$i_{OUT} = \frac{bI_5\left[\exp\left(\frac{v_{in}}{nV_t}\right) - 1\right]}{(1+A) - (A\text{-}1)\exp\left(\frac{v_{in}}{nV_t}\right)} \quad \Rightarrow \quad i_{OUT} = \infty \text{ when } A = 2.16 \text{ and } \frac{v_{in}}{nV_t} = 1$$

where $b$ corresponds to any current gain through current mirrors (M6-M4 and M8-M3).

# Overdrive of the Dynamically Biased Differential Amplifier

The enhanced output current is accomplished by the use of positive feedback (M28-M2-M19-M28).

The loop gain is,

$$LG = \left(\frac{g_{m28}}{g_{m4}}\right)\left(\frac{g_{m19}}{g_{m26}}\right) = A\frac{g_{m19}}{g_{m4}} = A$$

Note that as the output current increases, the transistors leave the weak inversion region and the above analysis is no longer valid.

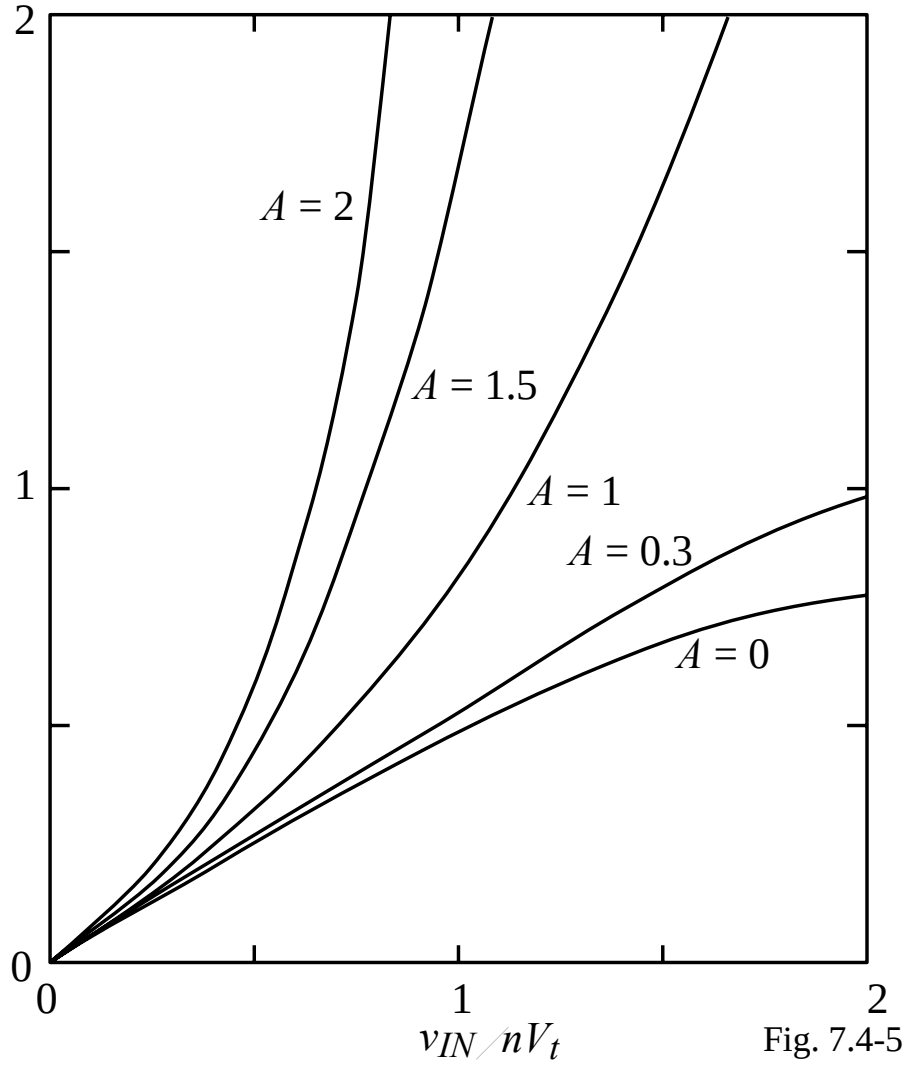
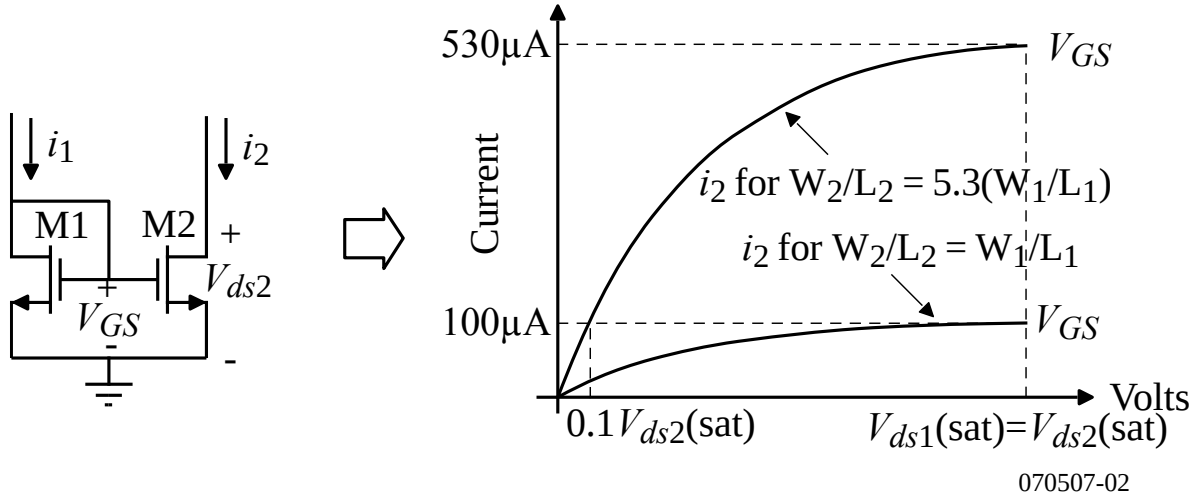



Fig. 7.4-5

## Increasing the Output Current for Strong Inversion Operation

An interesting technique is to bias the output transistor of a current mirror in the active region and then during large overdrive cause the output transistor to become saturated causing a significant current gain.

Illustration:



## Example 29-2 Current Mirror with M2 operating in the Active Region

Assume that M2 has a voltage across the drain-source of $0.1V_{ds}$(sat). Design the $W_2/L_2$ ratio so that $I_1 = I_2 = 100\mu A$ if $W_1/L_1 = 10$. Find the value of $I_2$ if M2 is saturated.

*Solution*

Using the value of $K_N' = 120\mu A/V^2$, we find that the saturation voltage of M2 is

$$V_{ds1}(\text{sat}) = \sqrt{\frac{2I_1}{K_N'(W_2/L_2)}} = \sqrt{\frac{200}{120\cdot 10}} = 0.408V$$

Now using the active equation of M2, we set $I_2 = 100\mu A$ and solve for $W_2/L_2$.

$$100\mu A = K_N'(W_2/L_2)[V_{ds1}(\text{sat})\cdot V_{ds2} - 0.5V_{ds2}^2]$$

$$= 120\mu A/V^2\,(W_2/L_2)[0.408\cdot 0.0408 - 0.5\cdot 0.0408^2]V^2 = 1.898\text{x}10^6(W_2/L_2)$$

Thus,

$$100 = 1.898(W_2/L_2) \quad \rightarrow \quad \frac{W_2}{L_2} = 52.7 \approx 53$$

Now if M2 should become saturated, the value of the output current of the mirror with $100\mu A$ input would be $530\mu A$ or a boosting of 5.3 times $I_1$.

# Implementation of the Current Mirror Boosting Concept

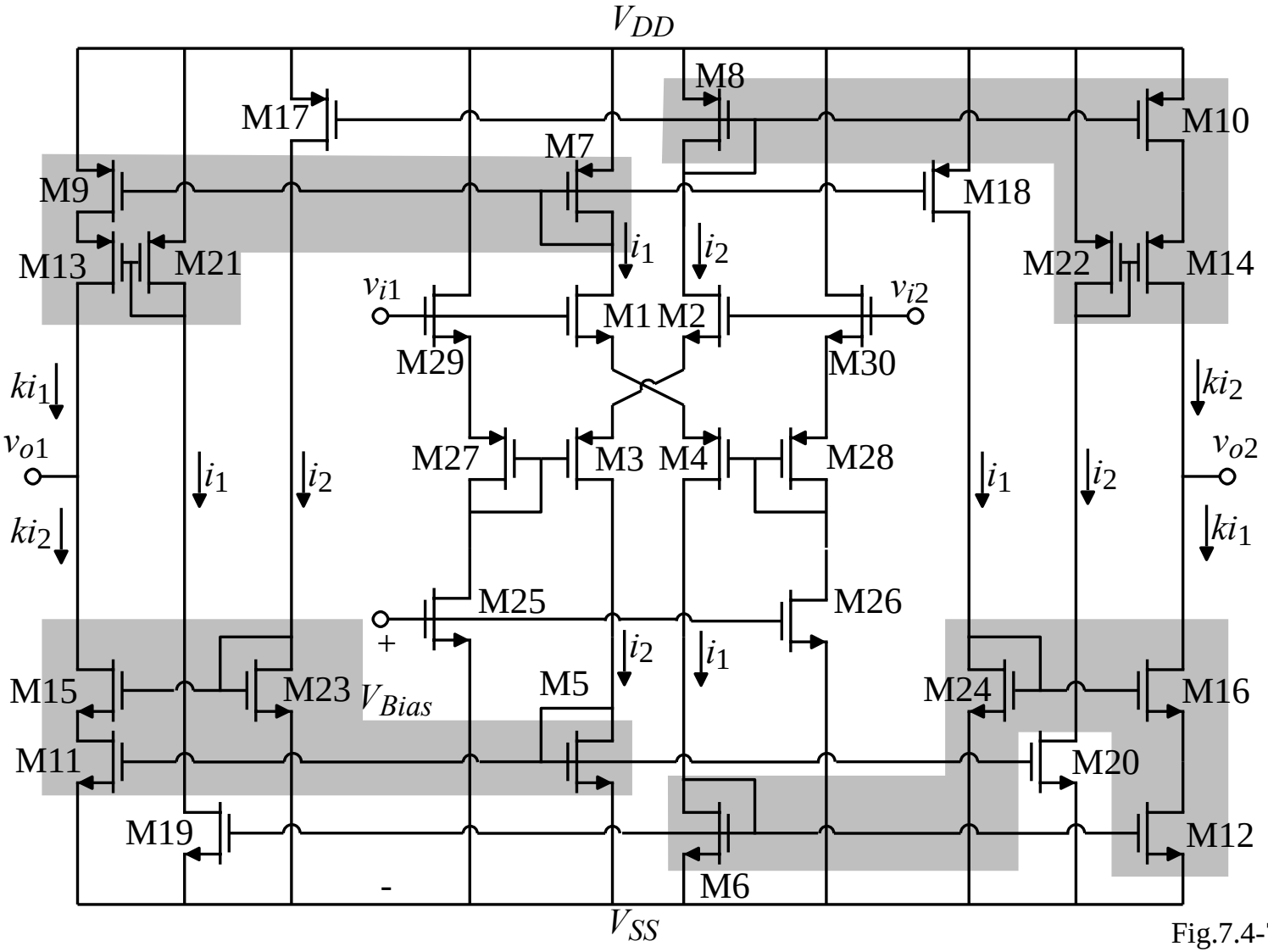



Fig.7.4-7

$k$ = overdrive factor of the current mirror

## A Better Way to Achieve the Current Mirror Boosting

It was found that when the current mirror boosting idea illustrated on the previous slide was used that when the current increased through the cascode device (M16) that $V_{GS16}$ increased limiting the increase of $V_{DS12}$. This can be overcome by the following circuit.

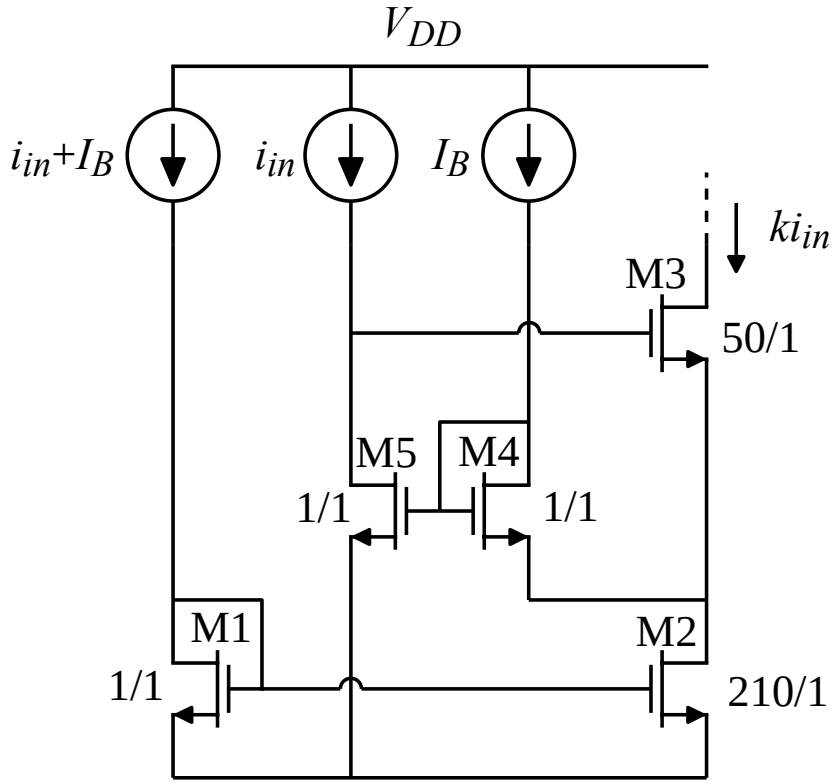



Fig. 7.4-7A

# REVIEW OF MOSFET NOISE MODELING AND ANALYSIS

## Transistor Noise Sources (Low-Frequency)

Drain current model:

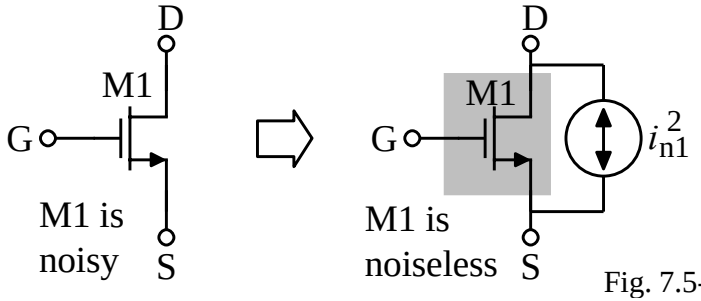



Fig. 7.5-0A

$$i_n^2 = \left[\frac{8kTg_m}{3} + \frac{(KF)I_D}{fC_{ox}L^2}\right] \quad \text{or} \quad i_n^2 = \left[\frac{8kTg_m(1+\eta)}{3} + \frac{(KF)I_D}{fC_{ox}L^2}\right] \text{ if } v_{BS} \neq 0$$

Recall that $\eta = \dfrac{g_{mbs}}{g_m}$

Gate voltage model assuming common source operation:

$$e_n^2 = \frac{\overline{i}_N^2}{g_m{}^2} = \left[\frac{8kT}{3g_m} + \frac{KF}{2fC_{ox}WLK'}\right] \quad \text{or}$$

$$e_n^2 = \left[\frac{8kT}{3g_m(1+\eta)} + \frac{KF}{2fC_{ox}WLK'}\right] \text{ if } v_{BS} \neq 0$$

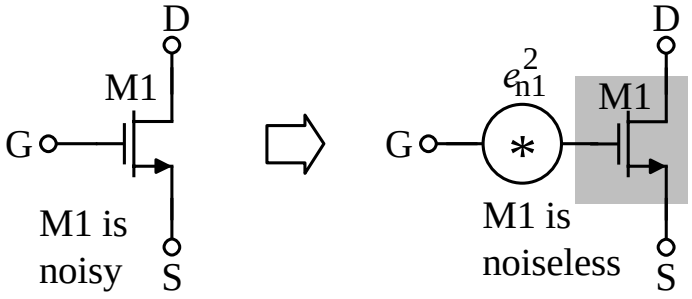



Fig. 7.5-0C

## Minimization of Noise in Op Amps

1.) Maximize the signal gain as close to the input as possible. (As a consequence, only the input stage will contribute to the noise of the op amp.)

2.) To minimize the 1/f noise:

a.) Use PMOS input transistors with appropriately selected dc currents and $W$ and $L$ values.

b.) Use lateral BJTs to eliminate the $1/f$ noise.

c.) Use chopper stabilization to reduce the low-frequency noise.

## Noise Analysis

1.) Insert a noise generator for each transistor that contributes to the noise. (Generally ignore the current source transistor of source-coupled pairs.)

2.) Find the output noise voltage across an open-circuit or output noise current into a short circuit.

3.) Reflect the total output noise back to the input resulting in the equivalent input noise voltage.

# LOW NOISE OP AMPS

## A Low-Noise, Two-Stage, Miller Op Amp

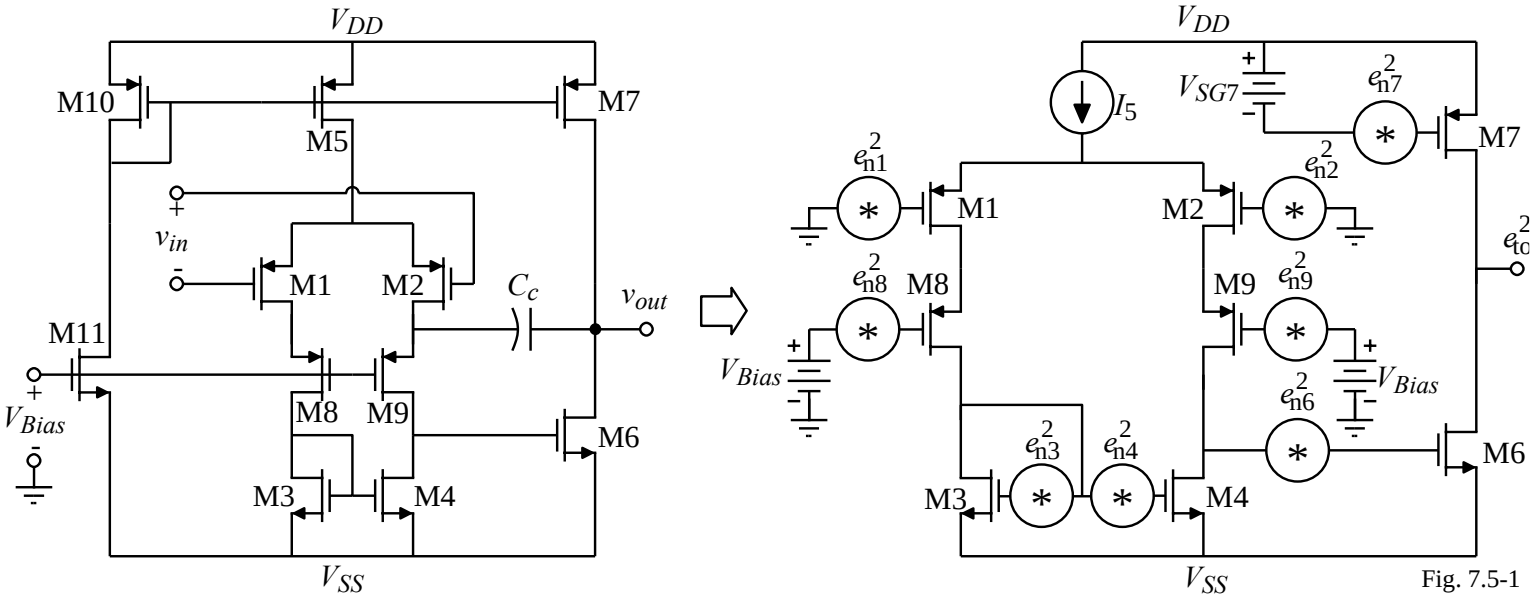



Fig. 7.5-1

The total output-noise voltage spectral density, $e_{to}^2$, is as follows where $g_{m8}(\text{eff}) \approx 1/r_{ds1}$,

$$e_{to}^2 = g_{m6}^2 R_{II}^2 \left[ e_{n6}^2 + e_{n7}^2 + R_I^2 \left( g_{m1}^2 e_{n1}^2 + g_{m2}^2 e_{n2}^2 + g_{m3}^2 e_{n3}^2 + g_{m4}^2 e_{n4}^2 + (e_{n8}^2 / r_{ds1}^2) + (e_{n9}^2 / r_{ds2}^2) \right) \right]$$

Divide by $(g_{m1} R_I g_{m6} R_{II})^2$ to get the eq. input-noise voltage spectral density, $e_{eq}^2$, as

$$e_{eq}^2 = \frac{e_{to}^2}{(g_{m1} g_{m6} R_I R_{II})^2} = \frac{2e_{n6}^2}{g_{m1}^2 R_I^2} + 2e_{n1}^2 \left[ 1 + \left( \frac{g_{m3}}{g_{m1}} \right)^2 \left( \frac{e_{n3}^2}{e_{n1}^2} \right) + \frac{e_{n8}^2}{g_{m1}^2 r_{ds1}^2 e_{n1}^2} \right] \approx 2e_{n1}^2 \left[ 1 + \left( \frac{g_{m3}}{g_{m1}} \right)^2 \left( \frac{e_{n3}^2}{e_{n1}^2} \right) \right]$$

where $e_{n6}^2 = e_{n7}^2$, $e_{n3}^2 = e_{n4}^2$, $e_{n1}^2 = e_{n2}^2$ and $e_{n8}^2 = e_{n9}^2$ and $g_{m1} R_I$ is large.

## 1/*f* Noise of a Two-Stage, Miller Op Amp

Consider the 1/*f* noise:

Therefore the noise generators are replaced by,

$$e_{ni}^2 = \frac{B}{fW_iL_i} \quad (\text{V}^2/\text{Hz}) \qquad \text{and} \qquad i_{ni}^2 = \frac{2BK'I_i}{fL_i^2} \quad (\text{A}^2/\text{Hz})$$

Therefore, the approximate equivalent input-noise voltage spectral density is,

$$e_{eq}^2 = 2e_{n1}^2\left[1 + \left(\frac{K_N'B_N}{K_P'B_P}\right)\left(\frac{L_1}{L_3}\right)^2\right] \quad (\text{V}^2/\text{Hz})$$

Comments;

- Because we have selected PMOS input transistors, $e_{n1}^2$ has been minimized if we choose $W_1L_1$ ($W_2L_2$) large.
- Make $L_1 << L_3$ to remove the influence of the second term in the brackets.

## Thermal Noise of a Two-Stage, Miller Op Amp

Let us focus next on the thermal noise:

The noise generators are replaced by,

$$e_{ni}^2 \approx \frac{8kT}{3g_m} \quad (\text{V}^2/\text{Hz}) \qquad \text{and} \qquad i_{ni}^2 \approx \frac{8kTg_m}{3} \quad (\text{A}^2/\text{Hz})$$

where the influence of the bulk has been ignored.

The approximate equivalent input-noise voltage spectral density is,

$$e_{eq}^2 = 2e_{n1}^2\left[1+\left(\frac{g_{m3}}{g_{m1}}\right)^2\left(\frac{e_{n3}^2}{e_{n1}^2}\right)\right] = 2e_{n1}^2\left[1+\sqrt{\frac{K_N W_3 L_1}{K_P W_1 L_3}}\right] (\text{V}^2/\text{Hz})$$

Comments:

- The choices that reduce the $1/f$ noise also reduce the thermal noise.

Noise Corner:

Equating the equivalent input-noise voltage spectral density for the $1/f$ noise and the thermal noise gives the noise corner, $f_c$, as

$$f_c = \frac{3g_m B}{8kTWL}$$

## Example 29-3 Design of A Two-Stage, Miller Op Amp for Low 1/*f* Noise

Use the model parameters of $K_N' = 120\mu A/V^2$, $K_P' = 25\mu A/V^2$, and $C_{ox} = 6fF/\mu m^2$ along with the value of $KF = 4x10^{-28}$ F·A for NMOS and $0.5x10^{-28}$ F·A for PMOS and design the previous op amp with $I_{D5} = 100\mu A$ to minimize the 1/f noise. Calculate the corresponding thermal noise and solve for the noise corner frequency. From this information, estimate the rms noise in a frequency range of 1Hz to 100kHz. What is the dynamic range of this op amp if the maximum signal is a 1V peak-to-peak sinusoid?

*Solution*

1.) The 1/f noise constants, $B_N$ and $B_P$ are calculated as follows.

$$B_N = \frac{KF}{2C_{ox}K_N'} = \frac{4x10^{-28}F\cdot A}{2\cdot 60x10^{-4}F/m^2\cdot 120x10^{-6}A/V^2} = 1.33x10^{-22}\,(V\cdot m)^2$$

and

$$B_P = \frac{KF}{2C_{ox}K_P'} = \frac{0.5x10^{-28}F\cdot A}{2\cdot 60x10^{-4}F/m^2\cdot 25x10^{-6}A/V^2} = 1.67x10^{-22}\,(V\cdot m)^2$$

2.) Now select the geometry of the various transistors that influence the noise performance.

To keep $e_{n1}^2$ small, let $W_1 = 100\mu m$ and $L_1 = 1\mu m$. Select $W_3 = 10\mu m$ and $L_3 = 20\mu m$ and let $W_8$ and $L_8$ be the same as $W_1$ and $L_1$ since they little influence on the noise.

## Example 29-3 - Continued

Of course, M1 is matched with M2, M3 with M4, and M8 with M9.

$$\therefore \quad e_{n1}^2 = \frac{B_P}{fW_1L_1} = \frac{1.67\text{x}10^{-22}}{f\cdot 100\mu\text{m}\cdot 1\mu\text{m}} = \frac{1.67\text{x}10^{-12}}{f} \ (\text{V}^2/\text{Hz})$$

$$e_{eq}^2 = 2\text{x}\frac{1.67\text{x}10^{-12}}{f}\left[1 + \left(\frac{120\cdot 1.33}{25\cdot 1.67}\right)^2\left(\frac{1}{20}\right)^2\right] = \frac{3.33\text{x}10^{-12}}{f}\,1.0365 = \frac{3.452\text{x}10^{-12}}{f}\,(\text{V}^2/\text{Hz})$$

Note at 100Hz, the voltage noise in a 1Hz band is $\approx 3.45\text{x}10^{-14}\text{V}^2$(rms) or 0.186μV(rms).

3.) The thermal noise at room temperature is

$$e_{n1}^2 = \frac{8kT}{3g_m} = \frac{8\cdot 1.38\text{x}10^{-23}\cdot 300}{3\cdot 500\text{x}10^{-6}} = 2.208\text{x}10^{-17}\ (\text{V}^2/\text{Hz})$$

which gives

$$e_{eq}^2 = 2\cdot 2.208\text{x}10^{-17}\left[1 + \sqrt{\frac{120\cdot 10\cdot 1}{25\cdot 100\cdot 20}}\right] = 4.416\text{x}10^{-17}\cdot 1.155 = 5.093\text{x}10^{-17}\ (\text{V}^2/\text{Hz})$$

## Example 29-3 - Continued

4.) The noise corner frequency is found by equating the two expressions for $e_{eq}^2$ to get

$$f_c = \frac{3.452\text{x}10^{-12}}{5.093\text{x}10^{-17}} = 67.8\text{kHz}$$

This noise corner is indicative of the fact that the thermal noise is much less than the 1/f noise.

5.) To estimate the rms noise in the bandwidth from 1Hz to 100,000Hz, we will ignore the thermal noise and consider only the 1/f noise. Performing the integration gives

$$V_{eq}(\text{rms})^2 = \int_1^{10^5} \frac{3.452\text{x}10^{-12}}{f} df = 3.452\text{x}10^{-12}[ln(100{,}000) - ln(1)]$$

$$= 0.408\text{x}10^{-10}\ \text{Vrms}^2 = 6.39\ \mu\text{Vrms}$$

The maximum signal in rms is 0.353V. Dividing this by 6.39μV gives 55,279 or 94.85dB which is equivalent to more than 15 bits of resolution.

6.) Note that the design of the remainder of the op amp will have little influence on the noise and is not included in this example.

# Low-Noise Op Amp using Lateral BJT's at the Input

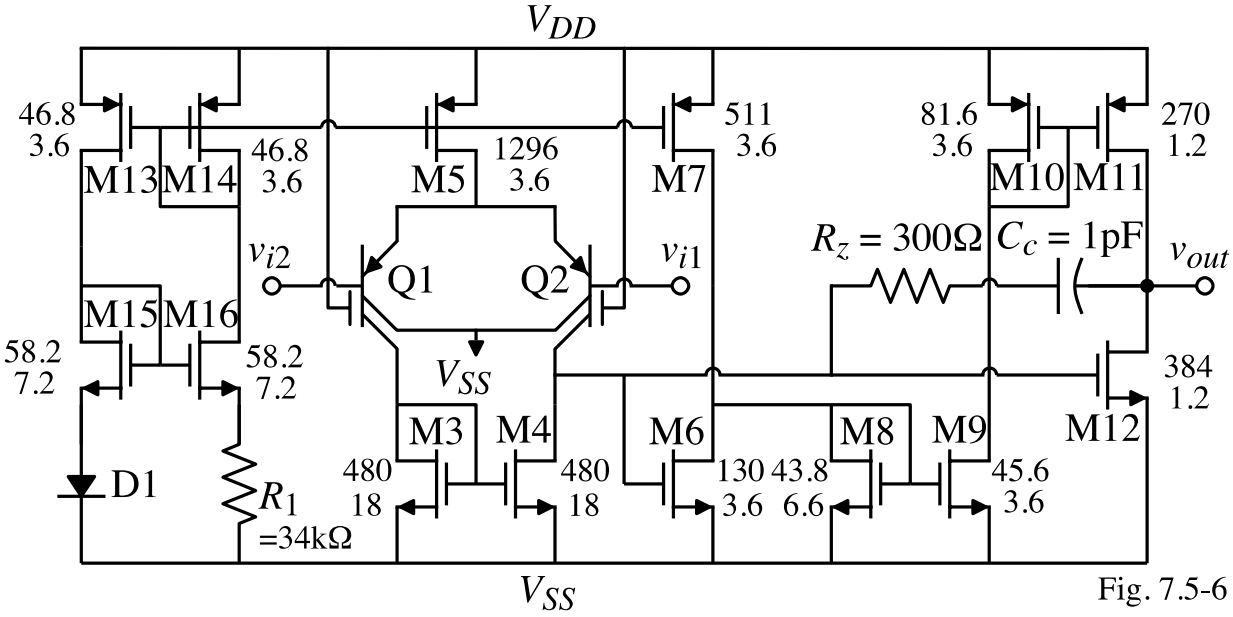



Fig. 7.5-6

Experimental noise performance:

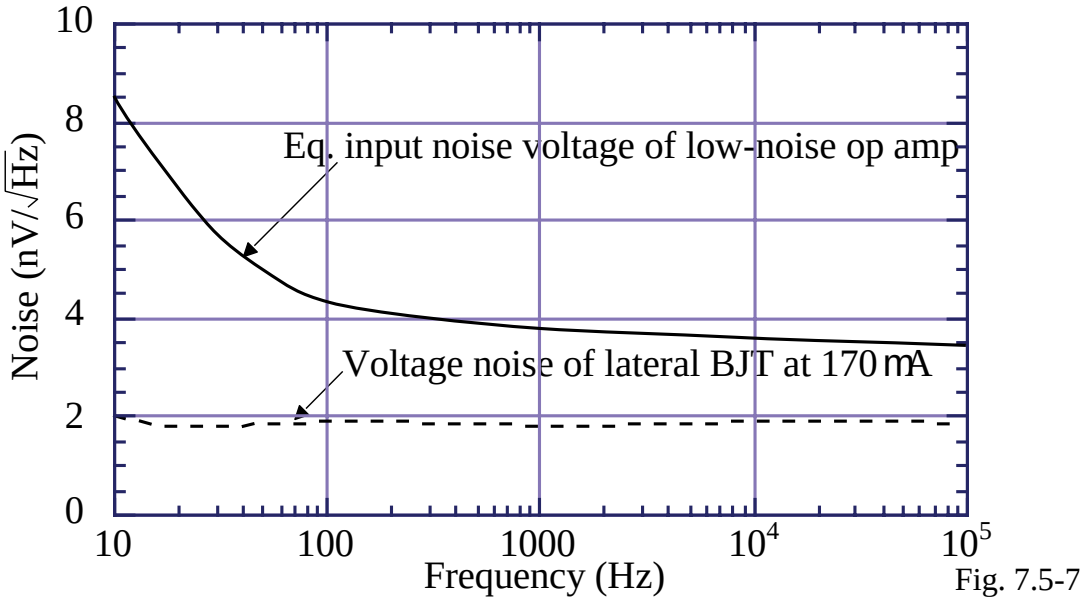



Fig. 7.5-7

## Summary of Experimental Performance for the Low-Noise Op Amp

| Experimental Performance | Value |
|---|---|
| Circuit area (1.2μm) | 0.211 mm$^2$ |
| Supply Voltages | ±2.5 V |
| Quiescent Current | 2.1 mA |
| -3dB frequency (at a gain of 20.8 dB) | 11.1 MHz |
| $e_n$ at 1Hz | 23.8 nV/$\sqrt{\text{Hz}}$ |
| $e_n$ (midband) | 3.2 nV/$\sqrt{\text{Hz}}$ |
| $f_c(e_n)$ | 55 Hz |
| $i_n$ at 1Hz | 5.2 pA/$\sqrt{\text{Hz}}$ |
| $i_n$ (midband) | 0.73 pA/$\sqrt{\text{Hz}}$ |
| $f_c(i_n)$ | 50 Hz |
| Input bias current | 1.68 μA |
| Input offset current | 14.0 nA |
| Input offset voltage | 1.0 mV |
| CMRR(DC) | 99.6 dB |
| PSRR$^+$(DC) | 67.6 dB |
| PSRR$^-$(DC) | 73.9 dB |
| Positive slew rate (60 pF, 10 kΩ load) | 39.0 V/μS |
| Negative slew rate (60 pF, 10 kΩ load) | 42.5 V/μS |

## Chopper-Stabilized Op Amps - Doubly Correlated Sampling (DCS)

Illustration of the use of chopper stabilization to remove the undesired signal, $v_u$, form the desired signal, $v_{in}$.

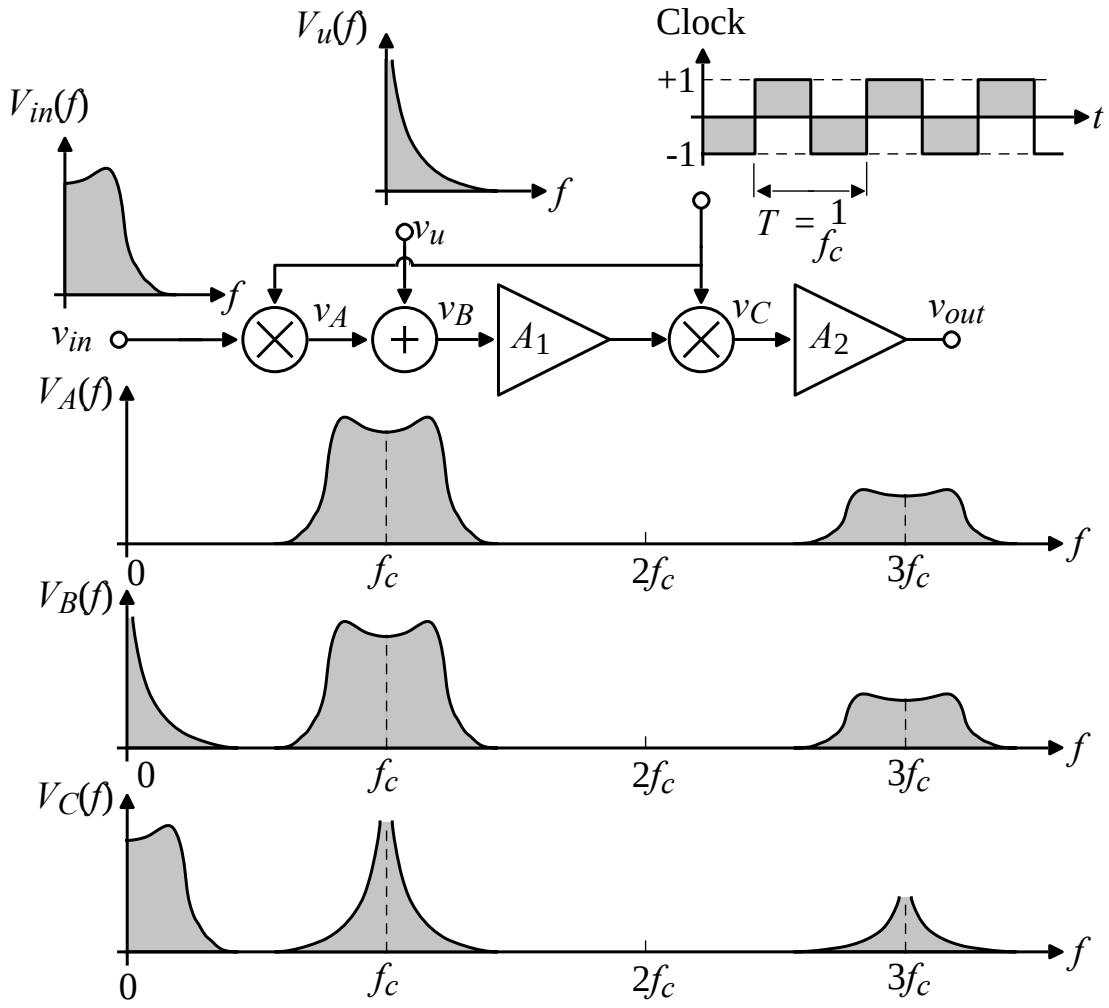
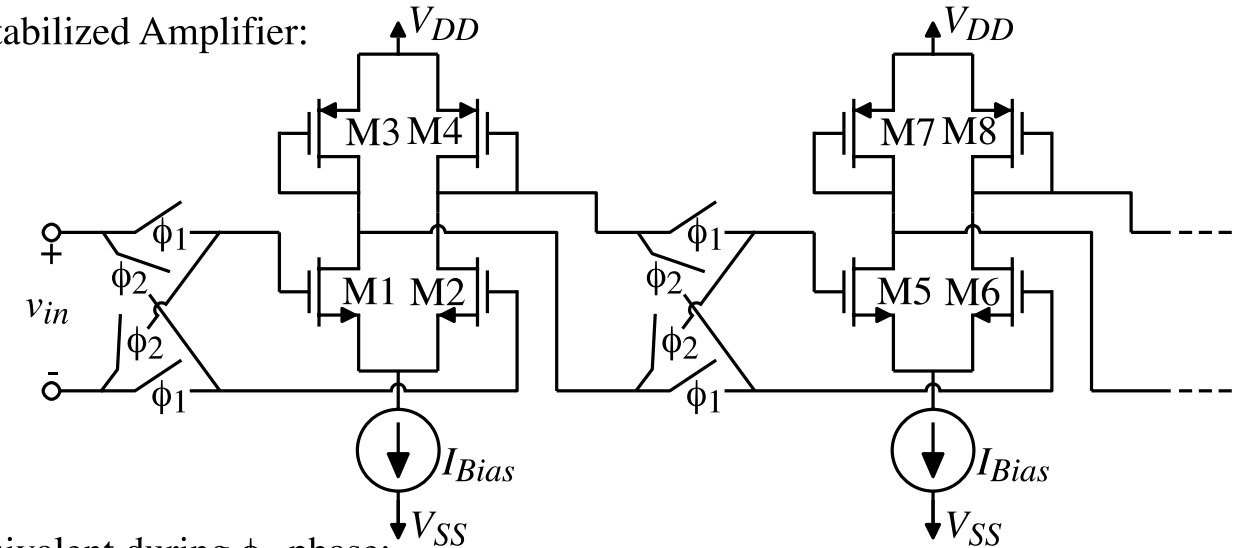


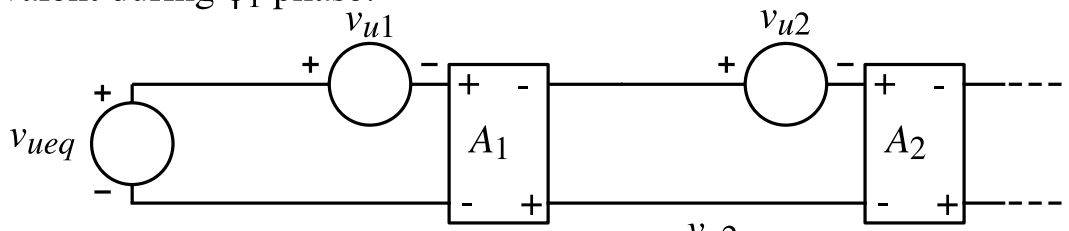

Fig. 7.5-8

# Chopper-Stabilized Amplifier

Chopper-stabilized Amplifier:

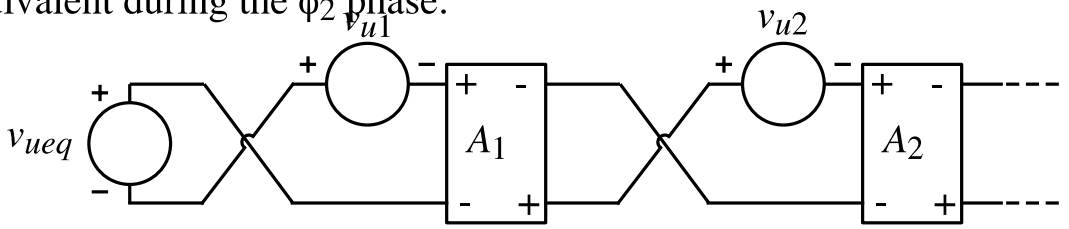



Circuit equivalent during $\phi_1$ phase:




$$v_{ueq} = v_{u1} + \frac{v_{u2}}{A_1}$$

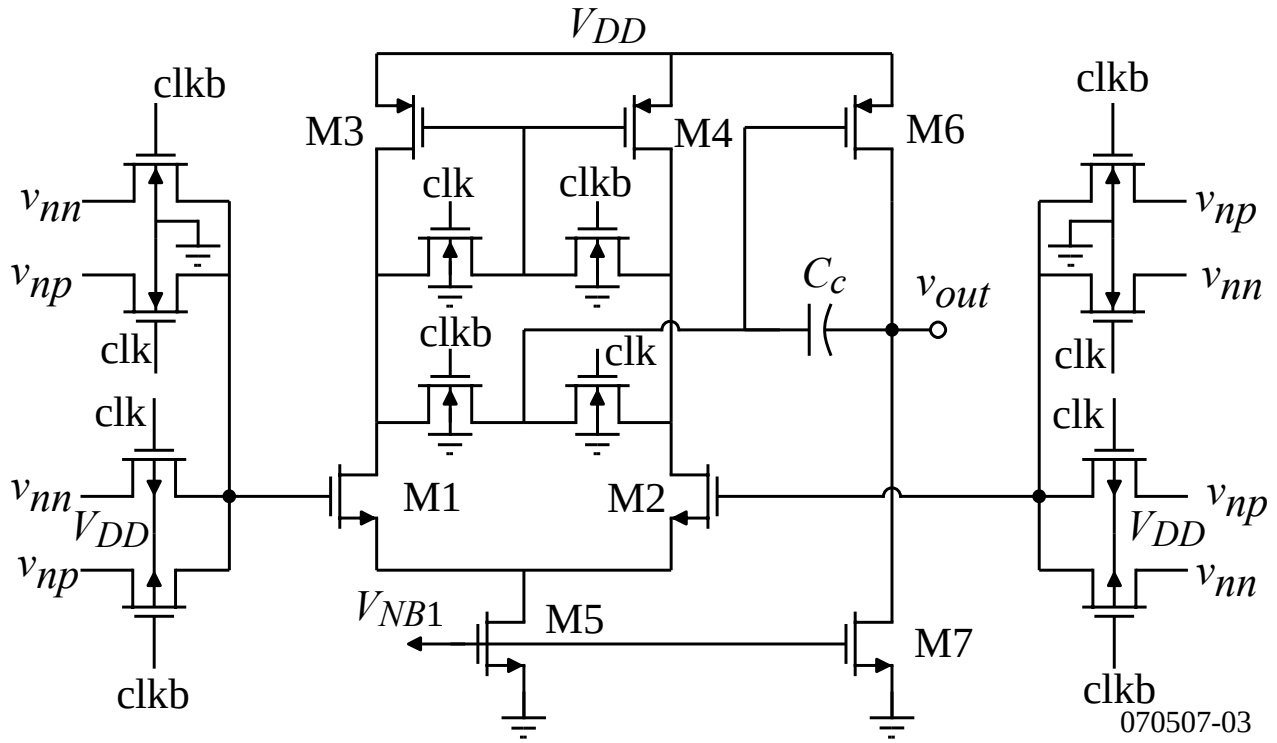
Circuit equivalent during the $\phi_2$ phase:




$$v_{ueq} = -v_{u1} + \frac{v_{u2}}{A_1}, \quad v_{ueq}(\text{aver}) = \frac{v_{u2}}{A_1}$$

Fig. 7.5-10

# Example of a Two-Stage, Chopper-Stablized Op Amp



# Experimental Noise Response of the Chopper-Stabilized Amplifier

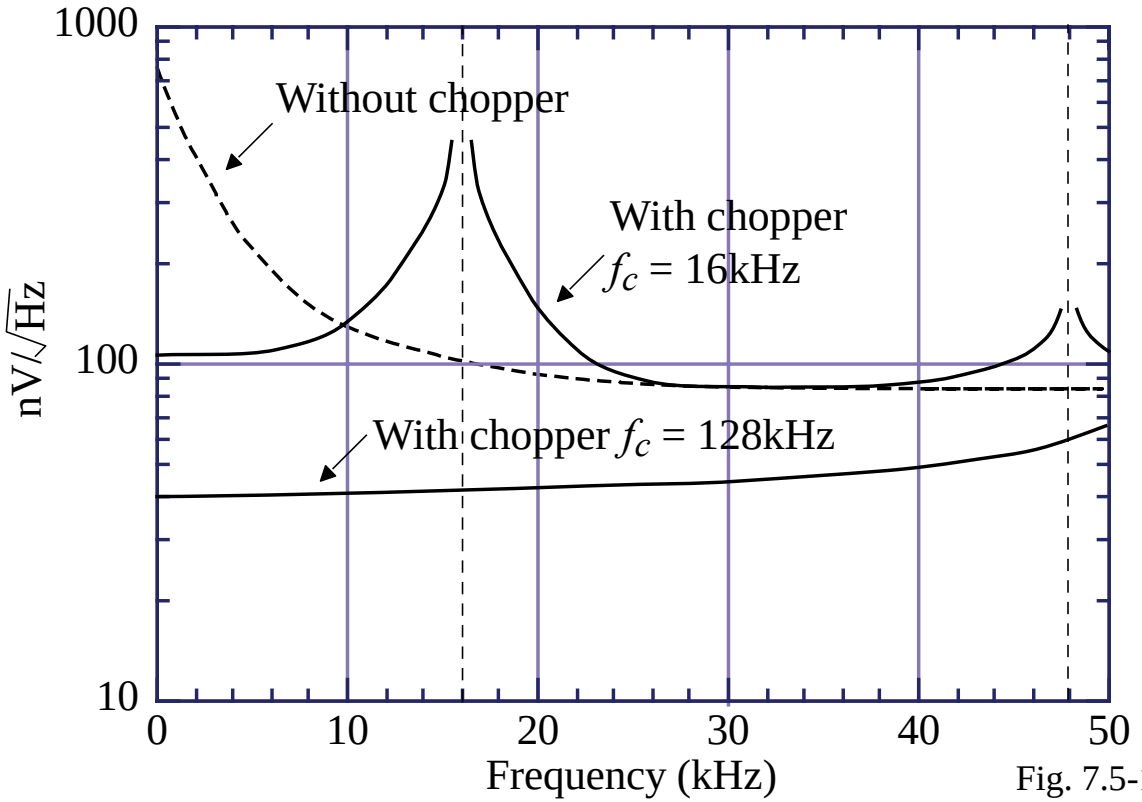



Fig. 7.5-11

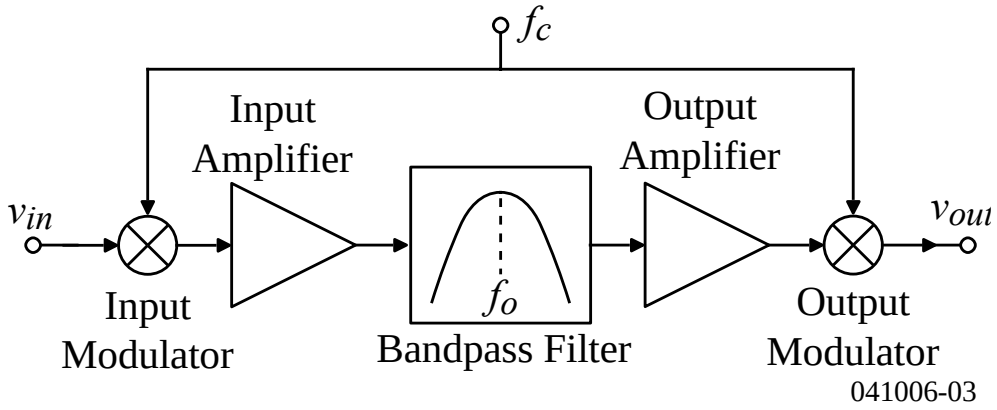
Comments:

- The switches in the chopper-stabilized op amp introduce a thermal noise equal to *kT/C* where *k* is Boltzmann's constant, *T* is absolute temperature and *C* are capacitors charged by the switches (parasitics in the case of the chopper-stabilized amplifier).
- Requires two-phase, non-overlapping clocks.
- Trade-off between the lowering of 1/*f* noise and the introduction of the *kT/C* noise.

## Improved Chopper Operation

In some cases, there are spurious signals in the neighborhood of the chopping frequencies and its harmonics. These spurious signals such as common-mode interference can mix to the baseband since the chopper amplifier is a time variant system and therefore inherently nonlinear.

A bandpass filter centered at the clock frequency can be used to eliminate the aliasing of the spurious signals and achieve a reduction in effective offset.




Let $\varepsilon = \dfrac{f_c - f_o}{f_o}$ and $\sigma_\varepsilon$ be a given bound of $\varepsilon$. It can be shown† that the achievable effective offset reduction, *EOR*, and the optimum $Q$ for the bandpass filter, $Q_{opt}$, is

$$EOR = \frac{8Q}{\pi(1 + 8Q_2\varepsilon)}, \ \varepsilon << 1 \qquad \text{and} \qquad Q_{opt} = 1/\sqrt{8\sigma_\varepsilon}$$

Improvements of 14dB reduction in effective offset are possible for $\varepsilon = 0.8\%$.

† C. Menolfi and Q. Huang, "A Fully Integrated, Untrimmed CMOS Instrumentation Amplifier with Submicrovolt Offset," *IEEE J. of Solid-State Circuits*, vol. 34, no.8, March 1999, pp. 415-420.

# SUMMARY

- Operation of transistors for low power op amps is generally in weak inversion
- Boosting techniques are needed to get output sourcing and sinking currents that are larger than that available during quiescent operation
- Be careful about using circuits at weak inversion, i.e. the self-biased cascode will cause the resistor to be too large
- Primary sources of noise for CMOS circuits is thermal and 1/f
- Noise analysis:

  1.) Insert a noise generator for each transistor that contributes to the noise. (Generally ignore the current source transistor of source-coupled pairs.)

  2.) Find the output noise voltage across an open-circuit or output noise current into a short circuit.

  3.) Reflect the total output noise back to the input resulting in the equivalent input noise voltage.
- Noise is reduced in op amps by making the input stage gain as large as possible and reducing the noise of this stage as much as possible.
- The input stage noise can be reduced by using lateral BJTs (particularily the 1/f noise)
- Doubly correlated sampling can transfer the noise at low frequencies to the clock frequency (this technique is used to achieve low input offset voltage op amps).