LECTURE 28 – DIFFERENTIAL-IN, DIFFERENTIAL-OUT OP AMPS

LECTURE ORGANIZATION

Outline

- Introduction
- Examples of differential output op amps
- Common mode output voltage stabilization
- Summary

***CMOS Analog Circuit Design*, 3rd Edition Reference**

Pages 386-397

INTRODUCTION

Why Differential Output Op Amps?

- Cancellation of common mode signals including clock feedthrough
- Increased signal swing

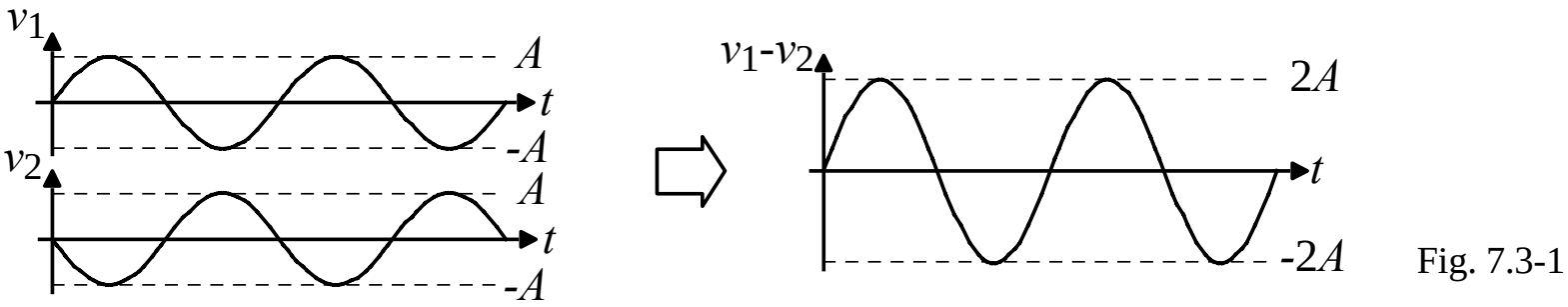


Fig. 7.3-1

- Cancellation of even-order harmonics

Symbol:

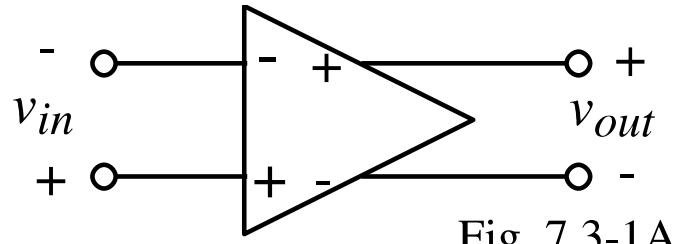
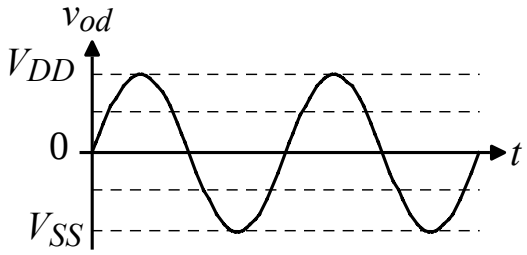


Fig. 7.3-1A

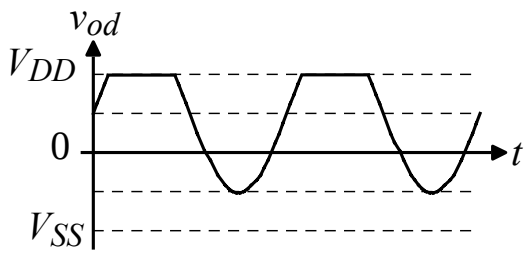
Common Mode Output Voltage Stabilization

If the common mode gain not small, it may cause the common mode output voltage to be poorly defined.

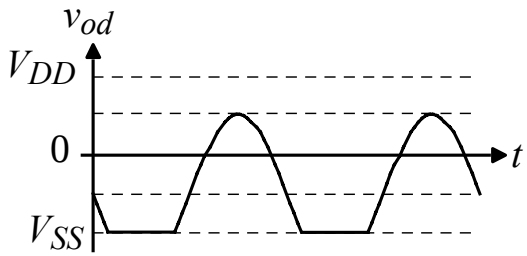
Illustration:



CM output voltage properly defined,
$V_{cm} = 0$



CM output voltage too large,
$V_{cm} = 0.5V_{DD}$



CM output voltage too small,
$V_{cm} = 0.5V_{SS}$

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Remember that:

$$v_{OUT} = A_{vd}(v_{ID}) \pm A_{cm}(v_{CM})$$

EXAMPLES OF DIFFERENTIAL OUTPUT OP AMPS (OTA'S)

Two-Stage, Miller, Differential-In, Differential-Out Op Amp

Note that the upper ICMR is

$$V_{DD} - V_{SGP} + V_{TN}$$

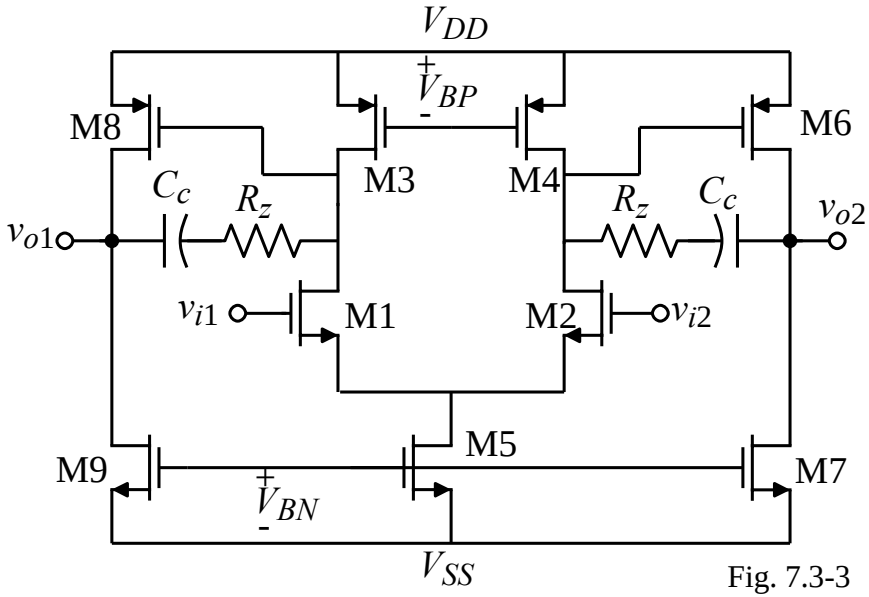


Fig. 7.3-3

$$(OCMR) = V_{DD} + |V_{SS}| - V_{SDP}(\text{sat}) - V_{DSN}(\text{sat})$$

The maximum peak-to-peak output voltage $\leq 2 \cdot OCMR$

Conversion between differential outputs and single-ended outputs:

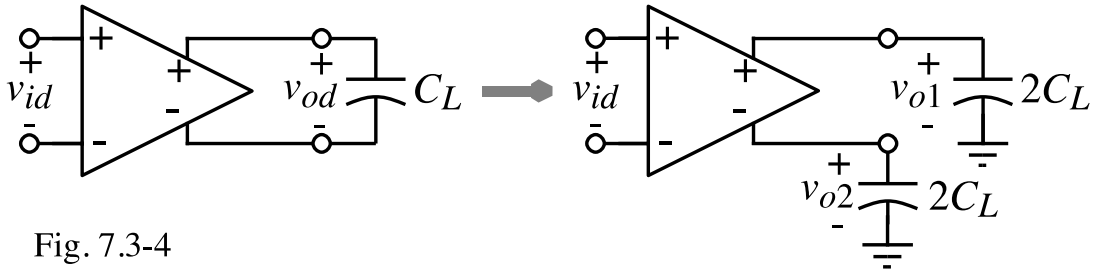


Fig. 7.3-4

Two-Stage, Miller, Differential-In, Differential-Out Op Amp with Push-Pull Output

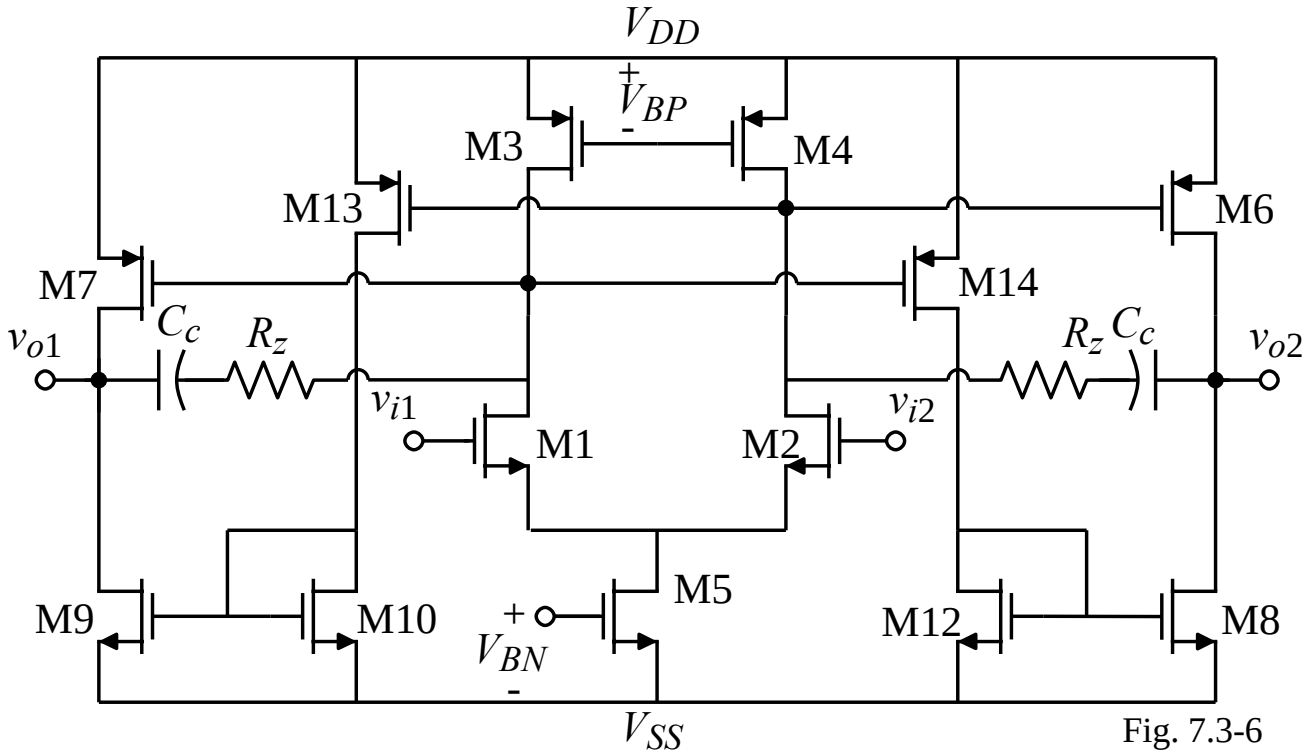
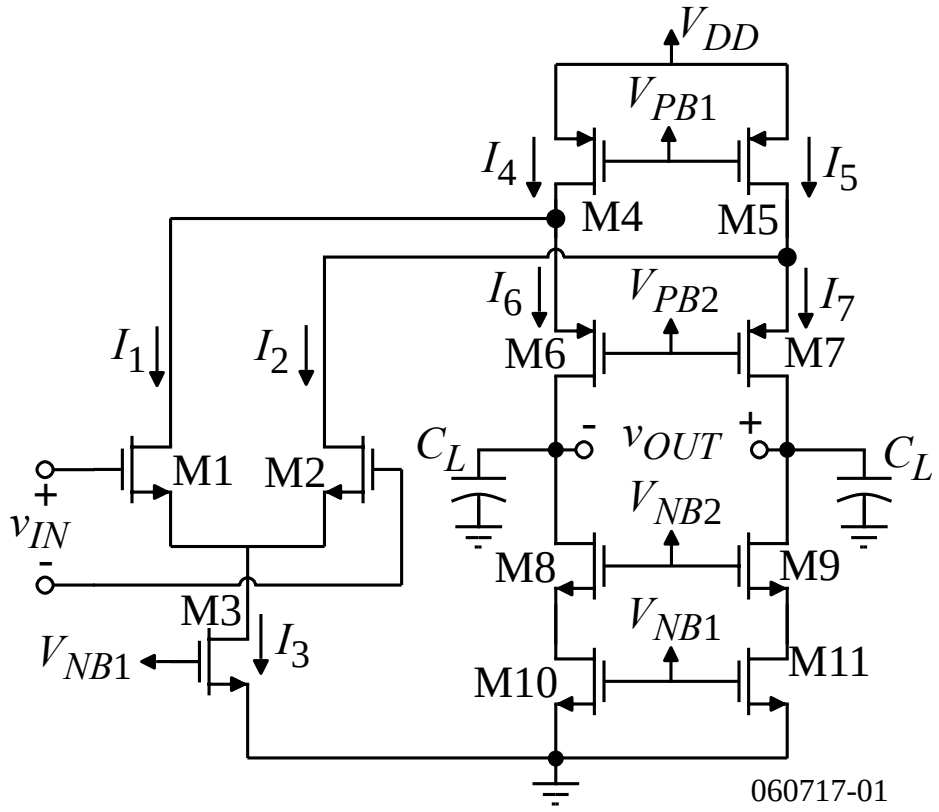


Fig. 7.3-6

Comments:

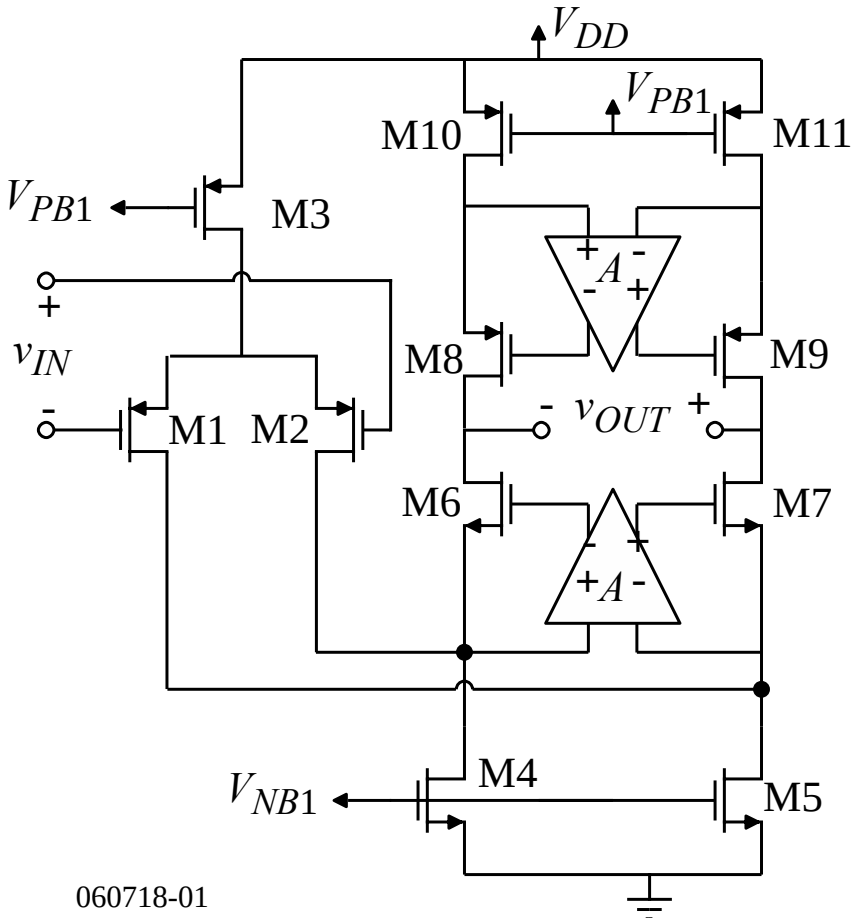
- Able to actively source and sink output current
- Output quiescent current poorly defined

Folded-Cascode, Differential Output Op Amp



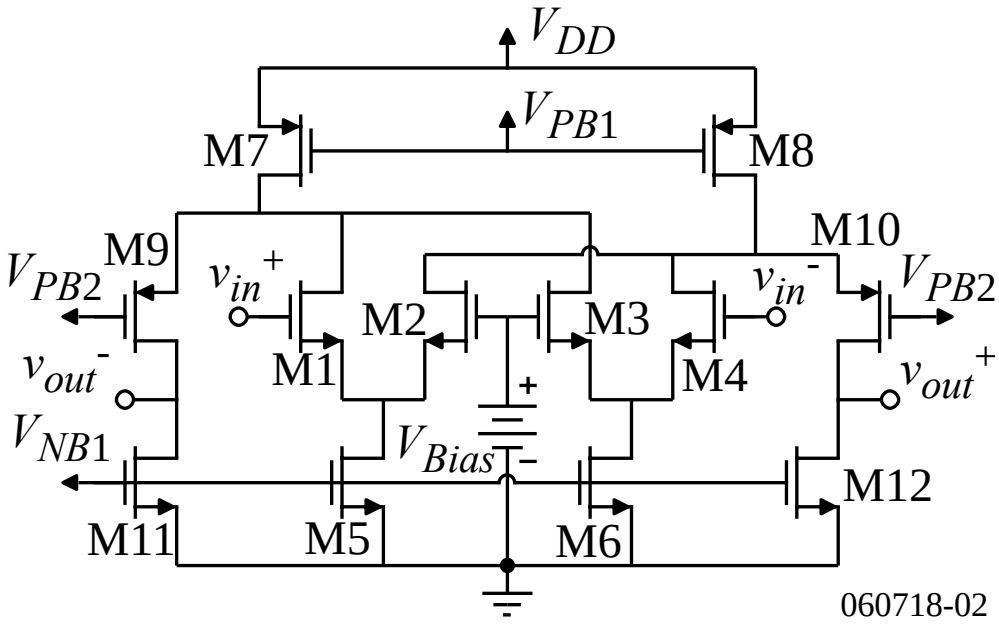
- No longer has the low-frequency asymmetry in signal path gains.
- Class A

Enhanced-Gain, Folded-Cascode, Differential Output Op Amp



What about the *A* amplifier?

Below is the upper *A* amplifier:



Note that V_{Bias} controls the dc voltage at the input of the *A* amplifier through the negative feedback loop.

- Balanced inputs
- Class A

Push-Pull Cascode Op Amp with Differential-Outputs

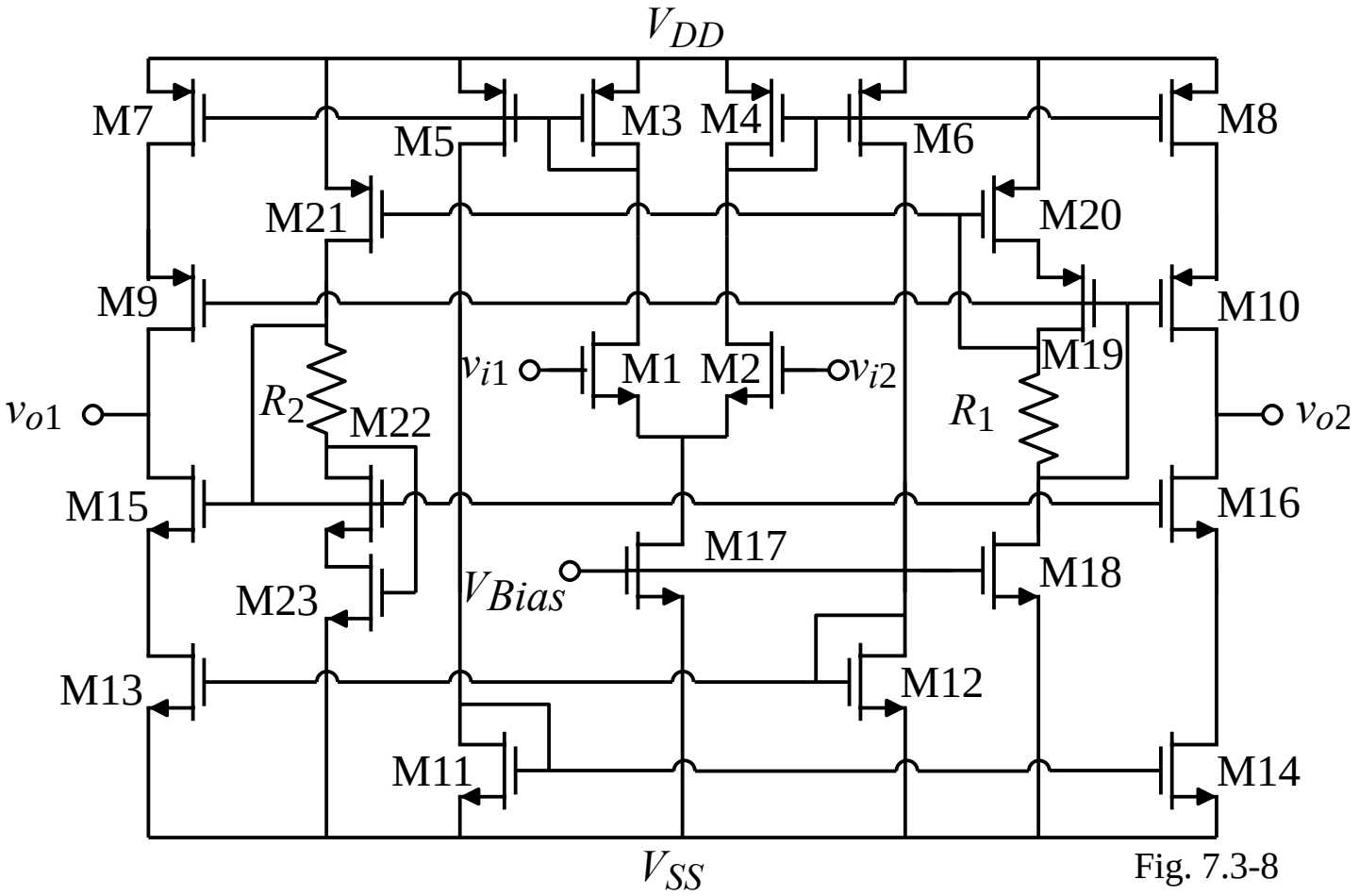
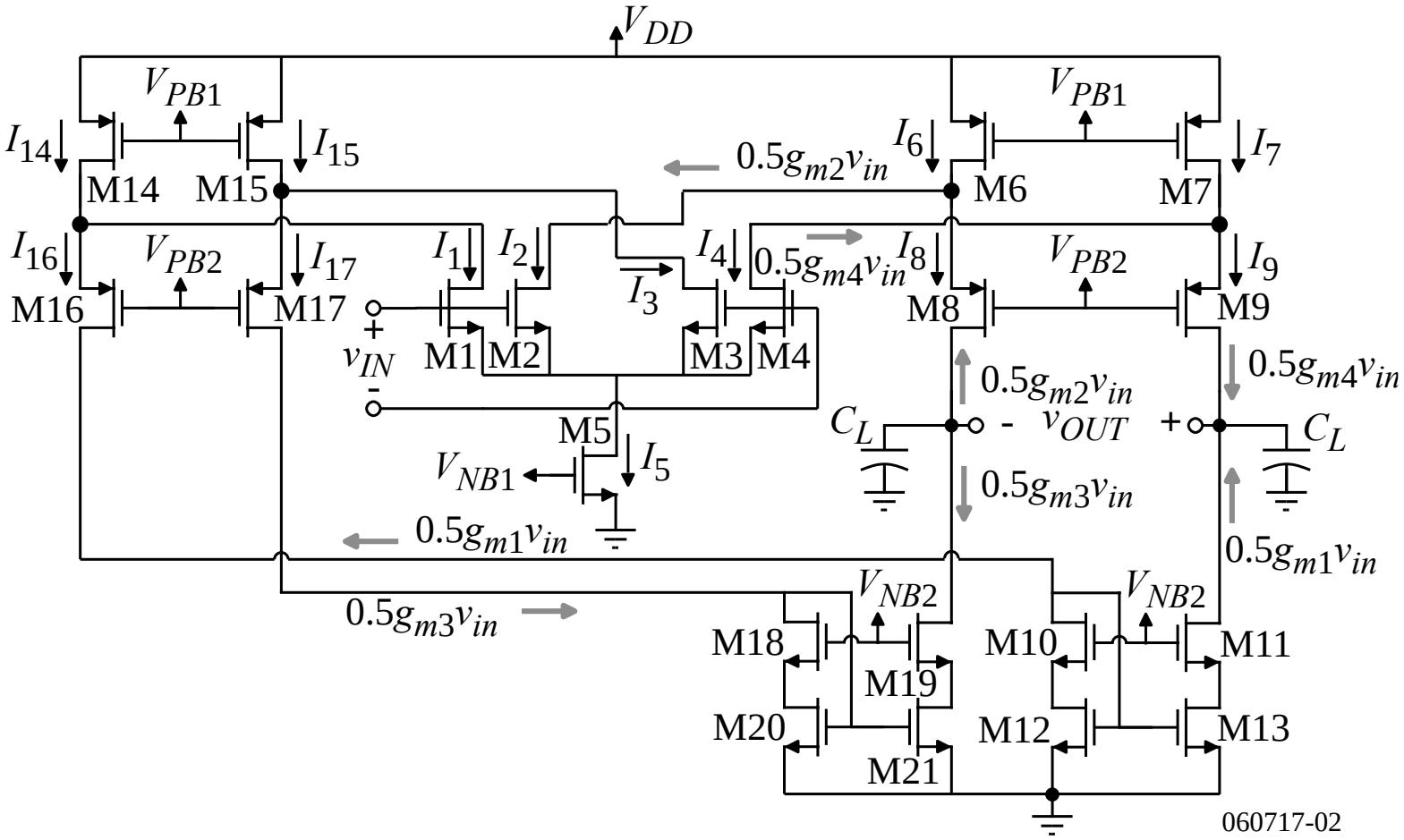


Fig. 7.3-8

- Output quiescent currents are well defined
- Self-biased circuits can be replaced with V_{NB2} and V_{PB2}

Folded-Cascode, Push-Pull, Differential Output Op Amp

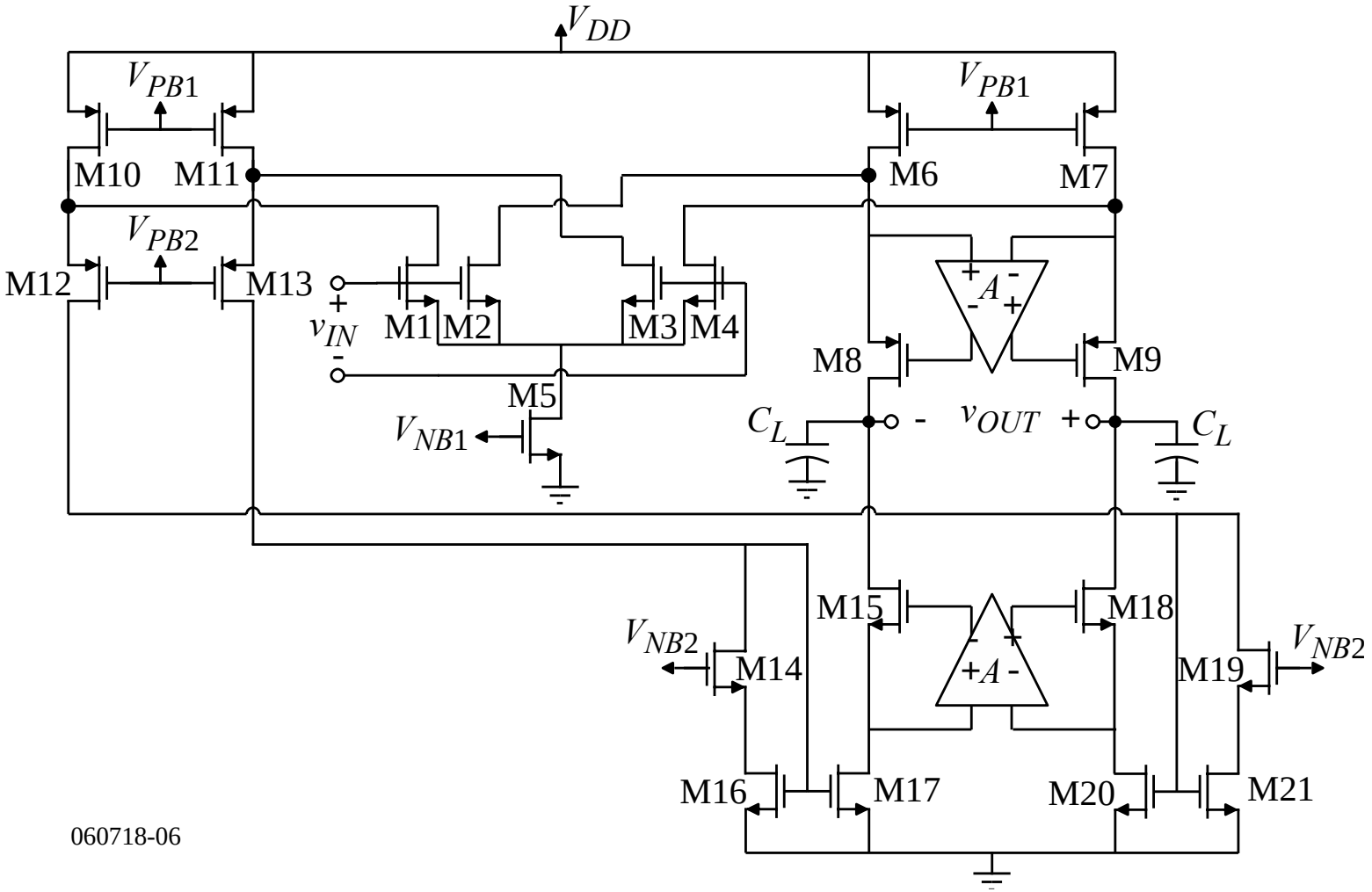


$$I_6 = I_7 = I_{14} = I_{15} > 0.5I_5$$

$$I_5 = I_1 + I_2 + I_3 + I_4$$

$$A_v = g_m R_{out}(\text{diff})$$

Enhanced-Gain, Folded-Cascode with Push-Pull Outputs



- Gain approaches $g_m{}^3 r_{ds}{}^3$

Cross-Coupled Differential Amplifier Stage

The cross-coupled input stage allows the push-pull output quiescent current to be well defined.

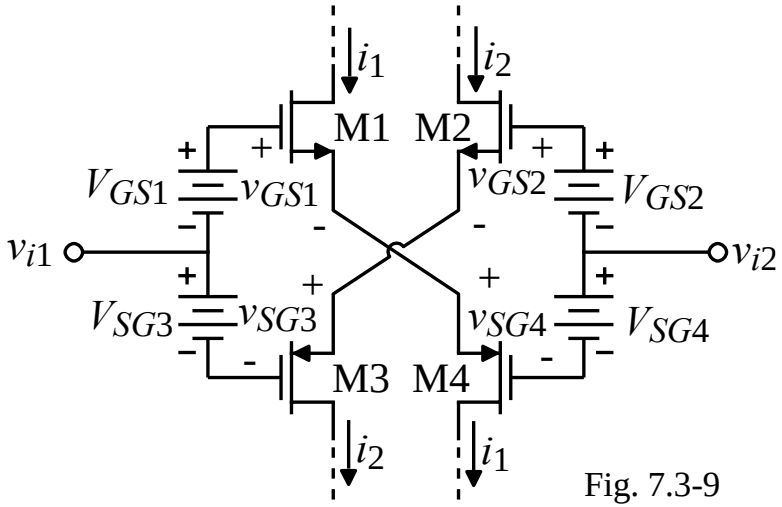


Fig. 7.3-9

Operation:

Voltage loop $v_{i1} - v_{i2} = -V_{GS1} + v_{GS1} + v_{SG4} - V_{SG4} = V_{SG3} - v_{SG3} - v_{GS2} + V_{GS2}$

Using the notation for ac, dc, and total variables gives,

$$v_{i2} - v_{i1} = v_{id} = (v_{sg1} + v_{gs4}) = -(v_{sg3} + v_{gs2})$$

If $g_{m1} = g_{m2} = g_{m3} = g_{m4}$, then half of the differential input is applied across each transistor with the correct polarity.

$$\therefore \qquad i_1 = \frac{g_{m1}v_{id}}{2} = \frac{g_{m4}v_{id}}{2} \qquad \text{and} \qquad i_2 = -\frac{g_{m2}v_{id}}{2} = -\frac{g_{m3}v_{id}}{2}$$

Class AB, Differential Output Op Amp using a Cross-Coupled Differential Input Stage

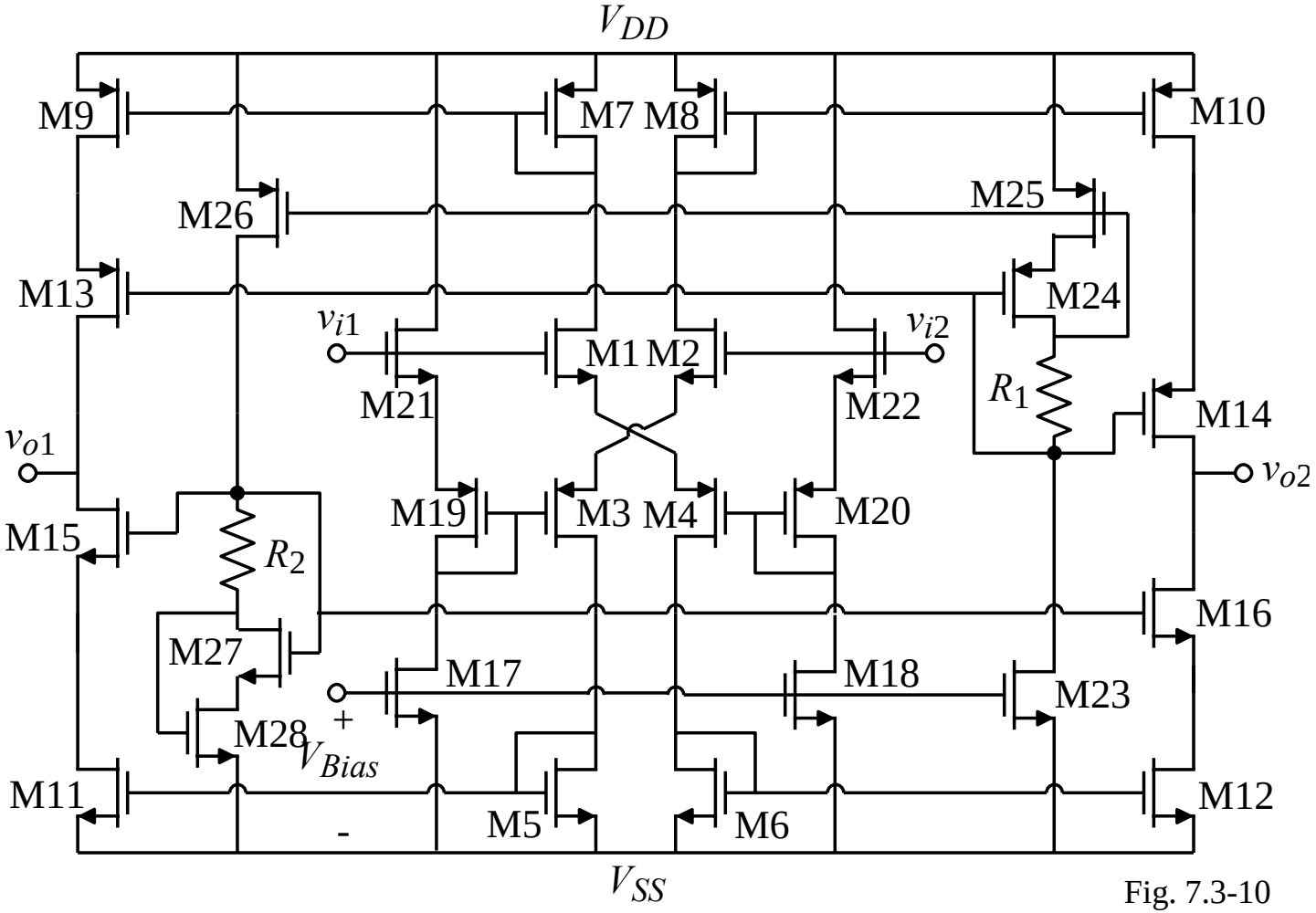


Fig. 7.3-10

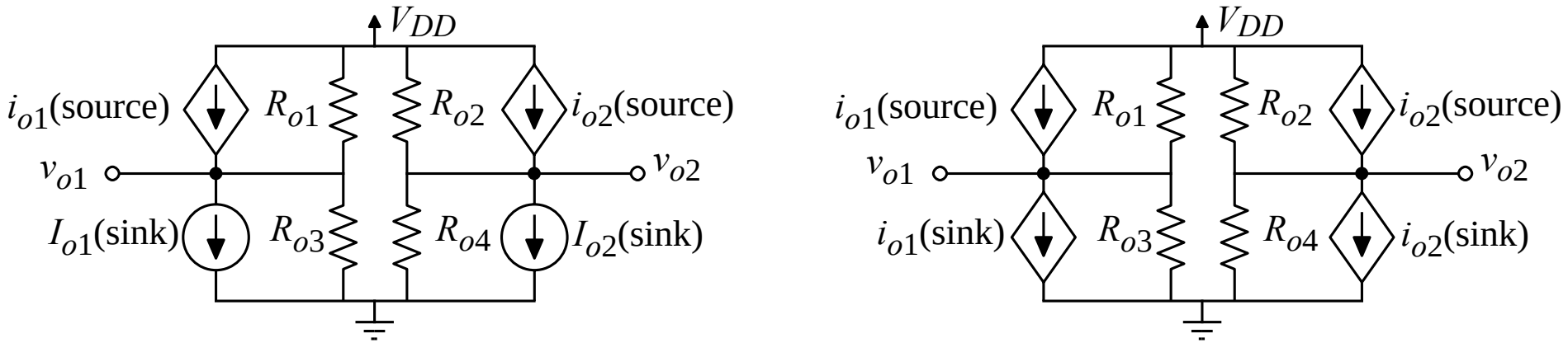
Quiescent output currents are defined by the current in the input cross-coupled differential amplifier.

COMMON MODE OUTPUT VOLTAGE STABILIZATION

Common Mode Feedback Circuits

Because the common mode gain is undefined, any common mode signal at the input can cause the output common mode voltage to be improperly defined. The common mode output voltage is stabilized by sensing the common mode output voltage and using negative feedback to adjust the common mode voltage to the desired value.

Model for the Output of Differential Output Op Amps:

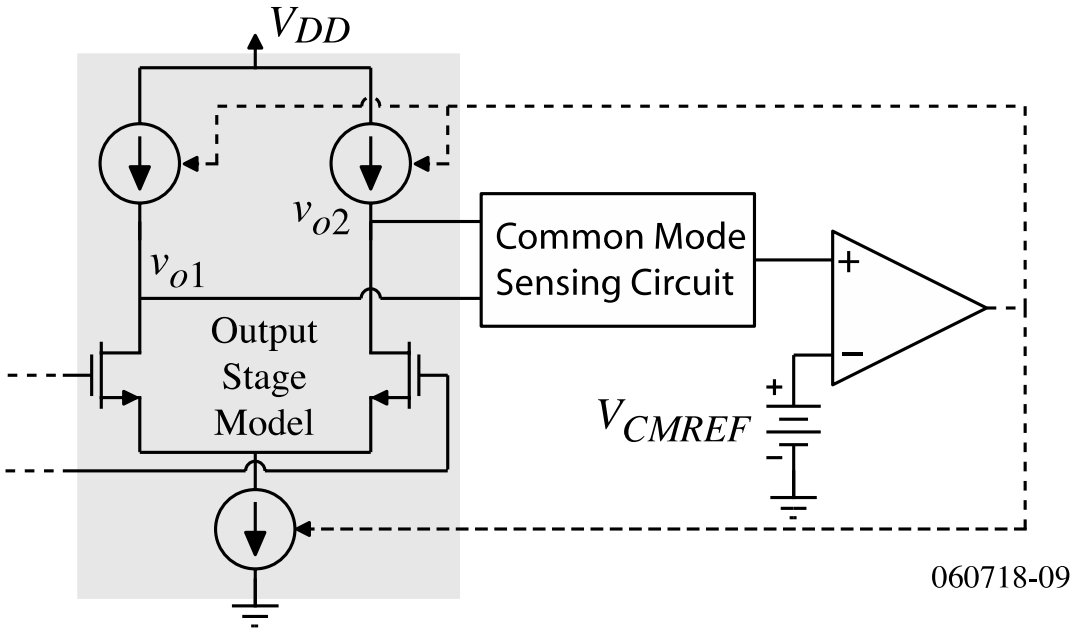


R_{oi} represents the self-resistance of the output sink/sources.

1.) If the common mode output voltage increases the sourcing current is too large.

2.) If the common mode output voltage decreases the sinking current is too large.

Conceptual View of Common-Mode Feedback



Function of the common-mode feedback circuit:

1.) If the common-mode output voltage increases, decrease the upper currents sources or increase the lower current sink until the common-mode voltage is equal to V_{CMREF}.

2.) If the common-mode output voltage decreases, increase the upper currents sources or decrease the lower current sink until the common-mode voltage is equal to V_{CMREF}.

Two-Stage, Miller, Differential-In, Differential-Out Op Amp with Common-Mode Feedback

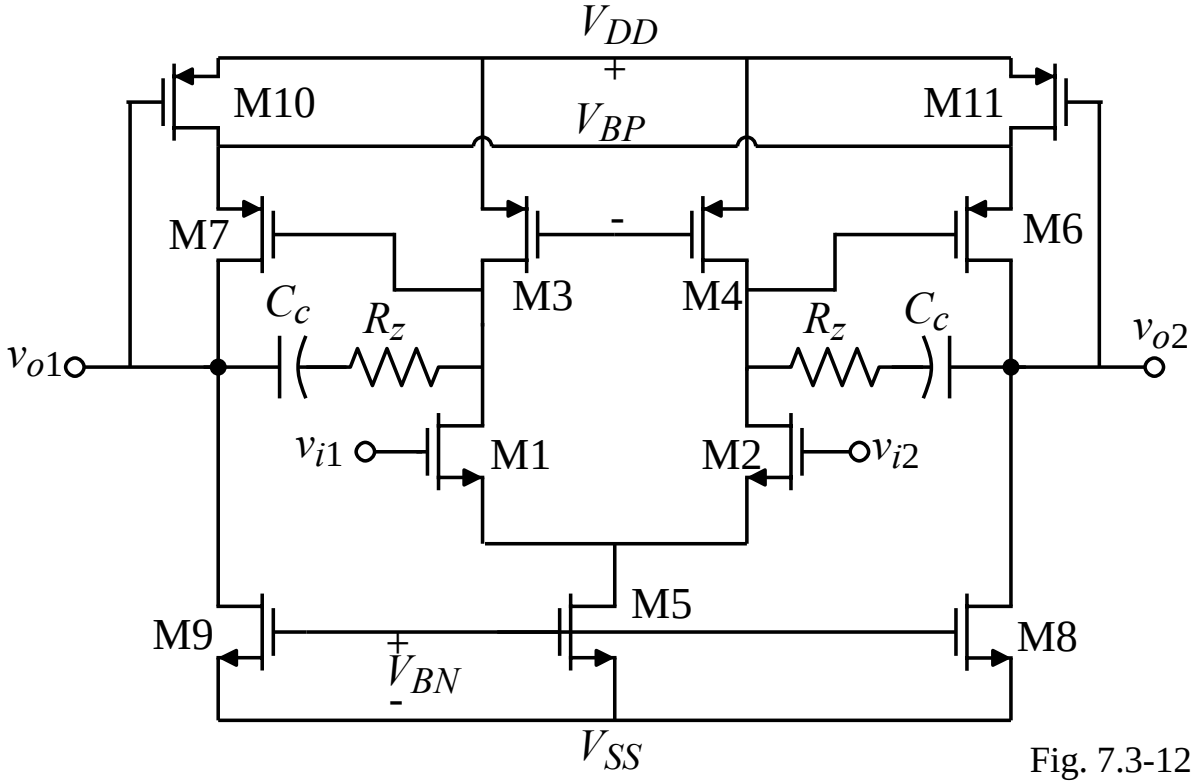


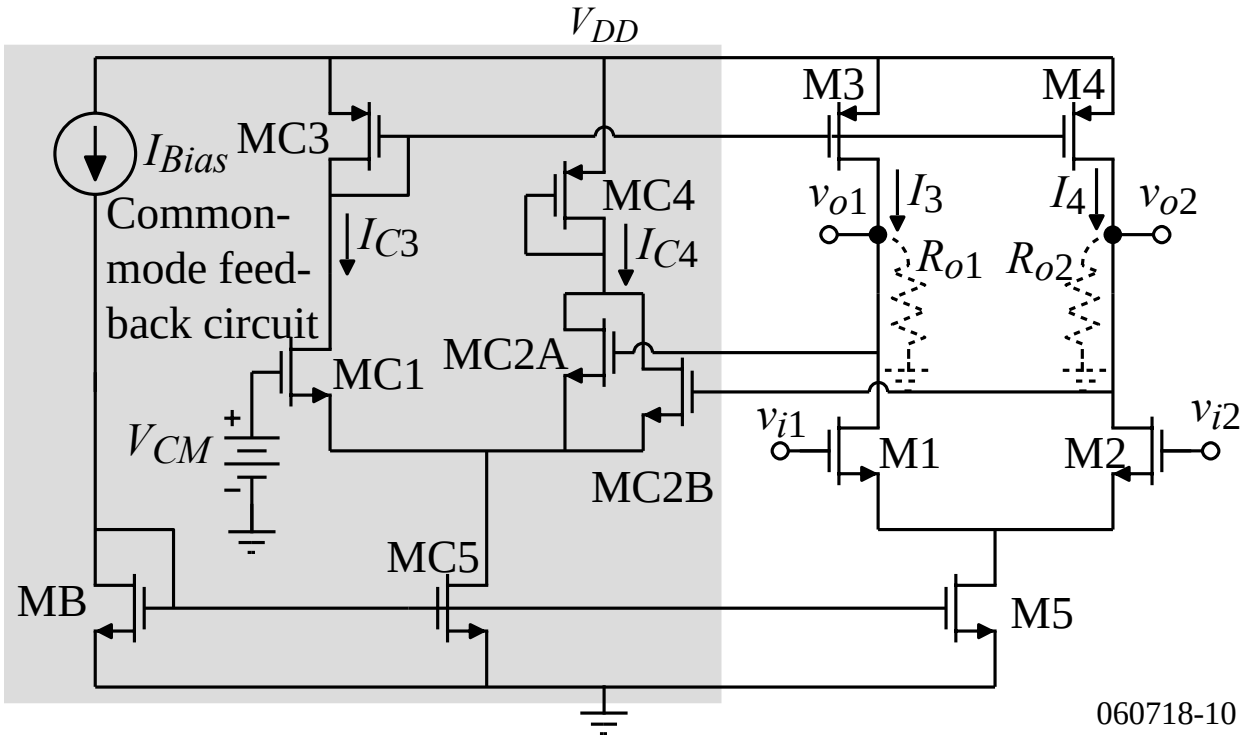
Fig. 7.3-12

Comments:

- Simple
- Unreferenced – value of common mode output voltage determined by the circuit characteristics

Common Mode Feedback Circuits

Implementation of common mode feedback circuit:



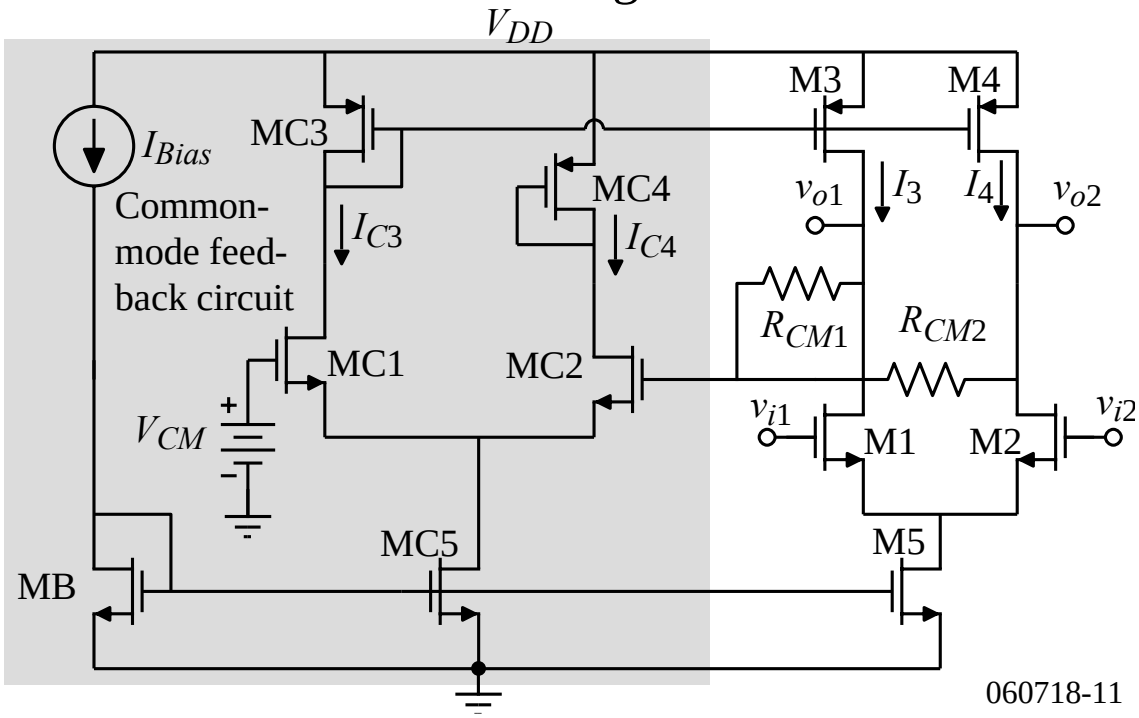
This scheme can be applied to any differential output amplifier.

CM Loop Gain = $-g_{mC1}R_{o1}$ which can be large if the output of the differential output amplifier is cascaded or a gain-enhanced cascode.

The common-mode loop gain may need to be compensated for proper dynamic performance.

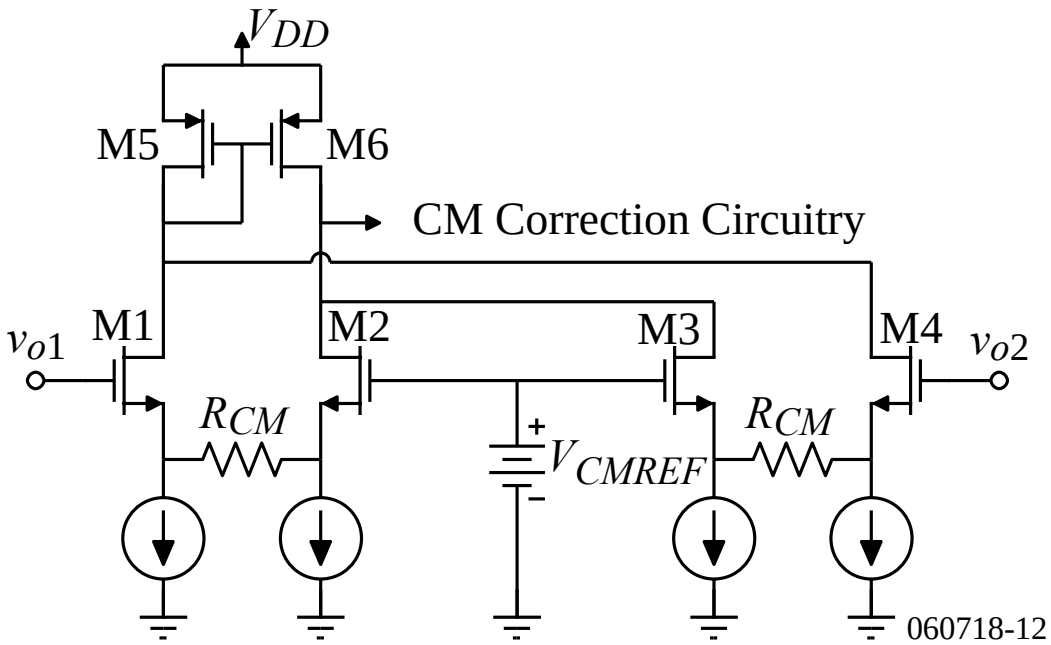
Common Mode Feedback Circuits – Continued

The previous circuit suffers when the input common mode voltage is low because the transistors MC2A and MC2B have a poor negative input common mode voltage. The following circuit alleviates this disadvantage:



An Improved Common-Mode Feedback Circuit

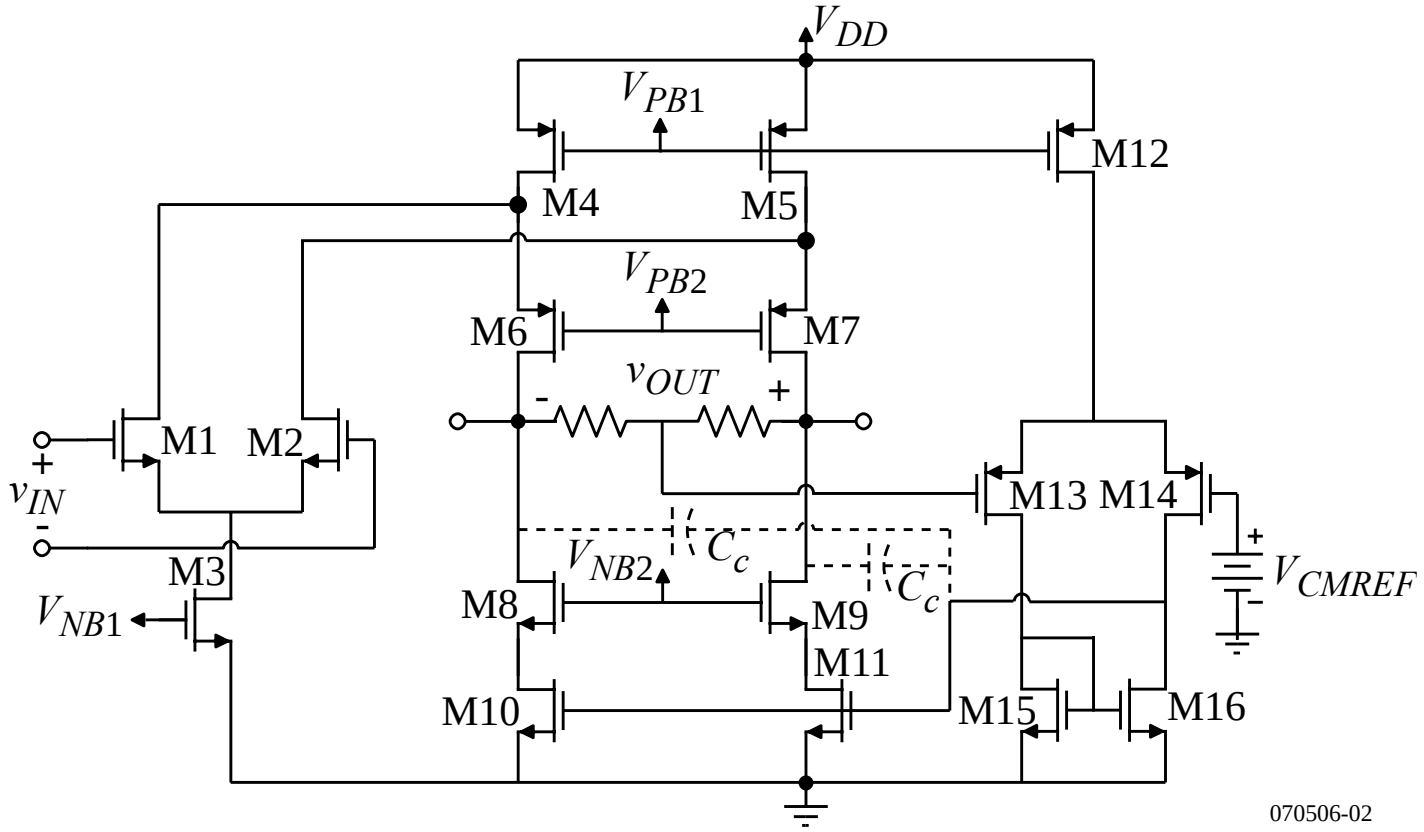
The resistance loading of the previous circuit can be avoided in the following CM feedback implementation:



This circuit is capable of sustaining a large differential voltage without loading the output of the differential output op amp.

Frequency Response of the CM Feedback Circuit

Consider the following CM feedback circuit implementation:

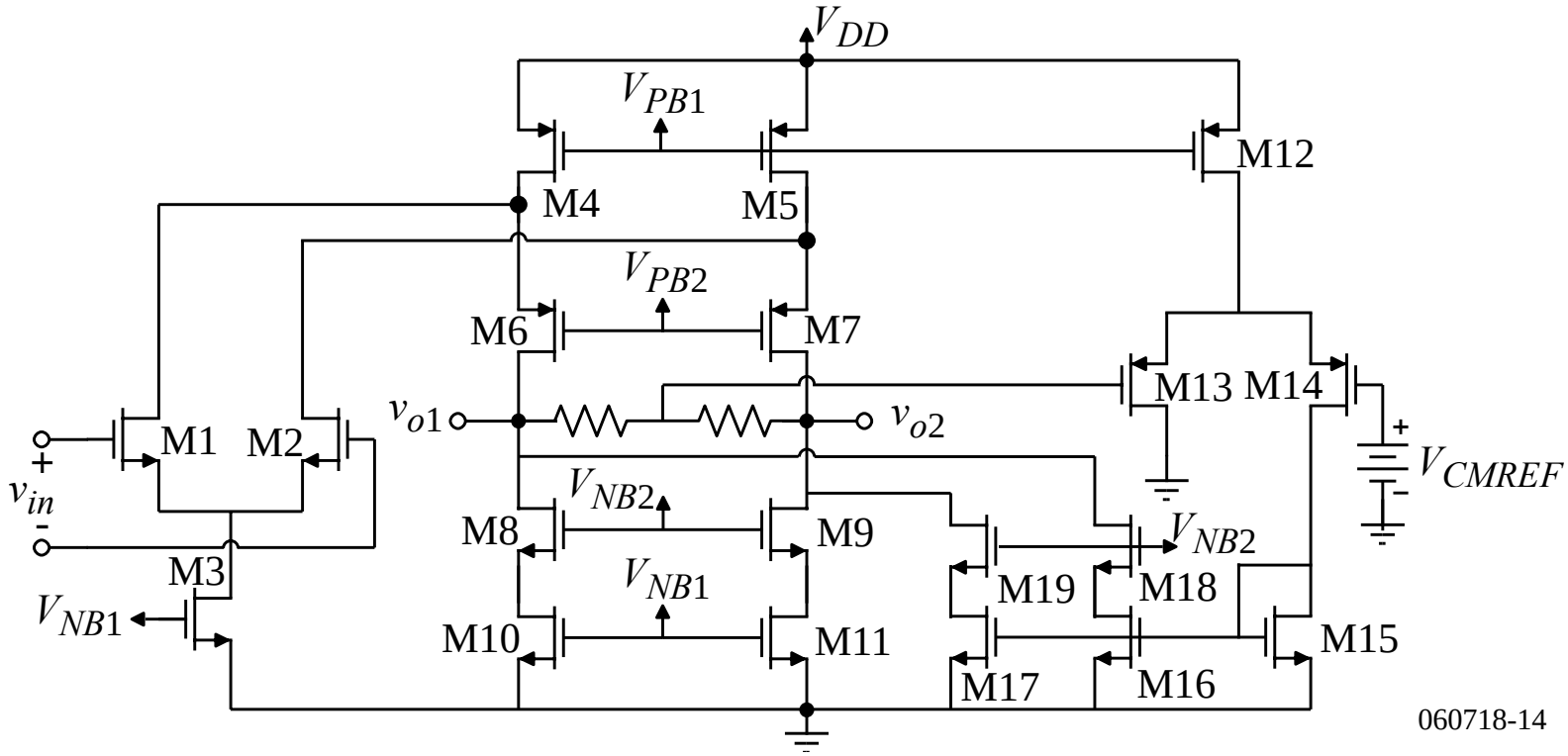


The CM feedback path has two poles – one at the gates of M10 and M11 and the dominant output pole of the differential output op amp.

Can compensate with Miller capacitors as shown.

Improved CM Feedback Frequency Response

The circuit on the previous page can be modified to eliminate the pole at the gates of M10 and M11 as follows:



- The need for compensation of the common mode loop no longer exists since there is only one dominant pole
- The dominant pole of the differential amplifier becomes the dominant pole of the common mode feedback

Implications of the Common Mode Feedback Correction Bandwidth

We have seen from the previous slides that the bandwidth of the common mode feedback correction circuit can be equal, less, or larger than the bandwidth of the differential gain of the op amp.

Common mode feedback BW < Differential mode BW:

- Common mode feedback correction circuit responds slower than the differential output voltage changes
- It is possible that the CM feedback correction circuit will not correct for the highest frequency CM disturbances and the differential output signal may be saturated or clipped

Common mode feedback BW ≈ Differential mode BW:

- The CM feedback correction circuit should be able to correct for all CM disturbances
- The compensation of the differential mode can be used for the CM feedback correction circuit

Common mode feedback BW > Differential mode BW:

- The CM feedback correction circuit will be able to correct for all CM disturbances
- Difficult to keep stable because of higher BW and can amplify noise

A Common Mode Feedback Correction Scheme for Discrete Time Applications

Correction Scheme:

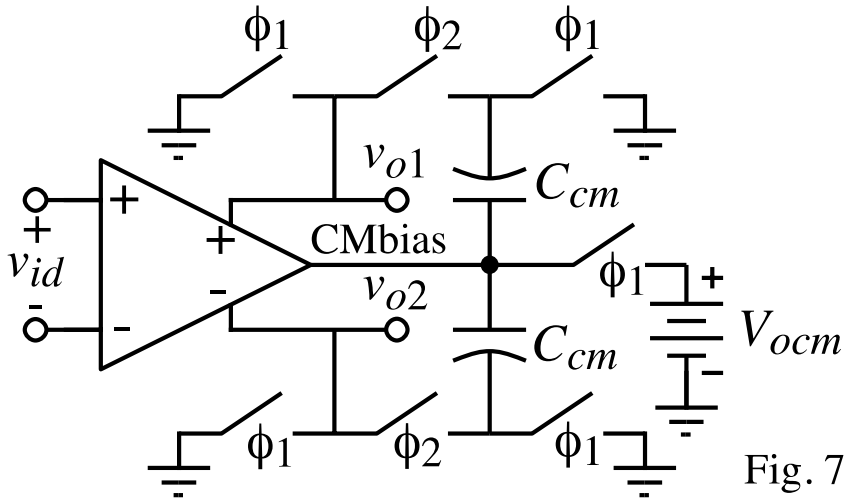


Fig. 7.3-14

Operation:

1.) During the ϕ_1 phase, both C_{cm} are charged to the desired value of V_{ocm} and CMbias = V_{ocm}.

2.) During the ϕ_2 phase, the C_{cm} capacitors are connected between the differential outputs and the CMbias node. The average value applied to the CMbias node will be V_{ocm}.

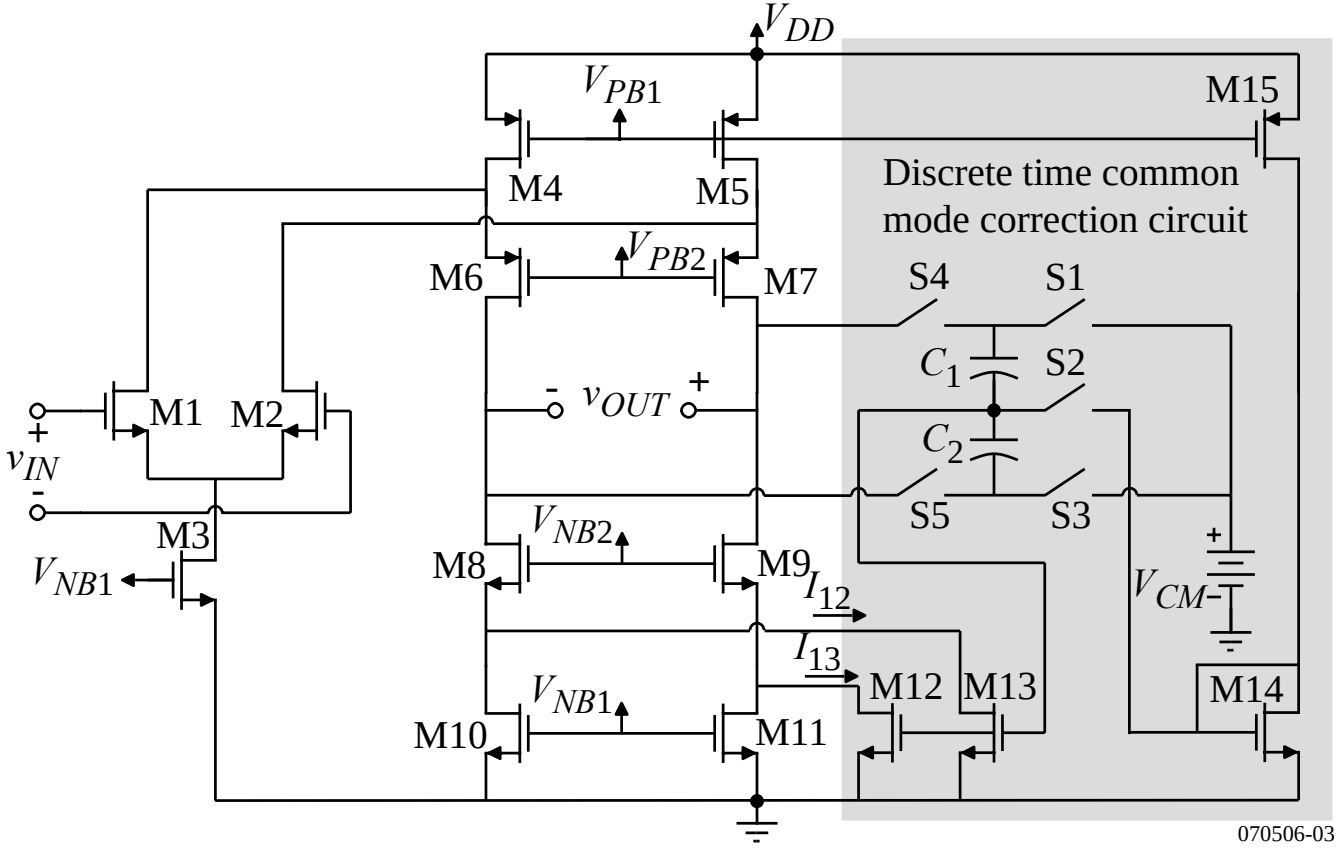
Example of a Common-Mode Output Voltage Stabilization Scheme for Discrete-Time Applications

Common mode adjustment phase:

Switches S1, S2 and S3 are closed. C_1 and C_2 are charged to the value necessary for I_{12} and I_{13} to keep the common mode output voltage at V_{CM}.

Amplification phase:

Switches S4 and S5 are closed. If the common mode output voltage is not at V_{CM}, the currents I_{12} and I_{13} will change to force the value of the common mode output voltage back to V_{CM}.

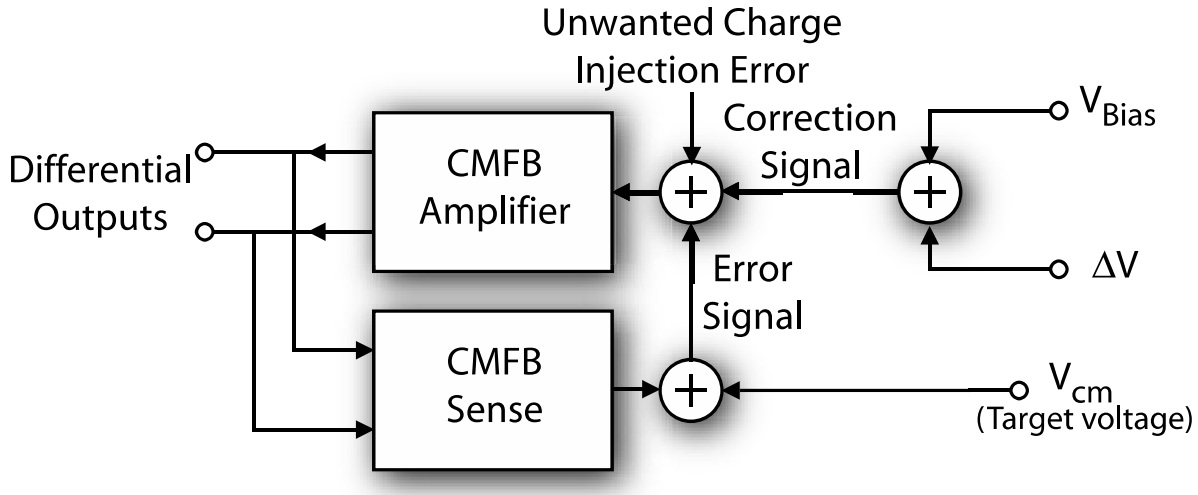


Correction of Channel Charge and Clock Feedthrough

In the discrete-time common mode correction schemes, the switches can introduce error due to channel charge and clock feedthrough.

Through simulation, these errors can be predicted and corrected by applying a correction signal superimposed upon the error signal to achieve the desired (target) common mode voltage.

General principle:



SUMMARY

- Advantages of differential output op amps:
  - 6 dB increase in signal amplitude
  - Cancellation of even harmonics
  - Cancellation of common mode signals including clock feedthrough
- Disadvantages of differential output op amps:
  - Need for common mode output voltage stabilization
  - Compensation of common mode feedback loop
  - Difficult to interface with single-ended circuits
- Most differential output op amps are truly balanced
- For push-pull outputs, the quiescent current should be well defined
- Common mode feedback schemes include,
  - Continuous time
  - Discrete time