LECTURE 26 – BUFFERED OP AMPS

LECTURE ORGANIZATION

Outline

- Introduction
- Open Loop Buffered Op Amps
- Closed Loop Buffered Op Amps
- Use of the BJT in Buffered Op Amps
- Summary

***CMOS Analog Circuit Design*, 3rd Edition Reference**

Pages 354-370

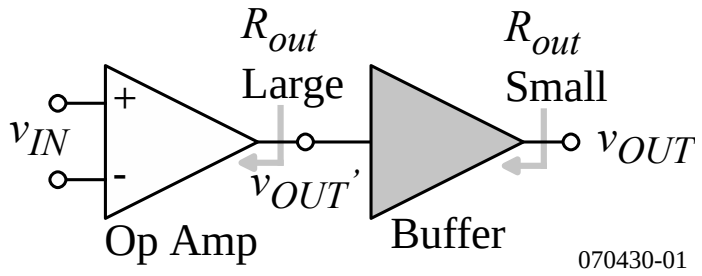
INTRODUCTION

Buffered Op Amps

What is a buffered op amp?

Buffered op amps are op amps with the ability to drive a low output resistance and/or a large output capacitance. This requires:

- An output resistance typically in the range of $10\Omega \leq R_o \leq 1000\Omega$
- Ability to sink and source sufficient current ($C_L \cdot SR$)



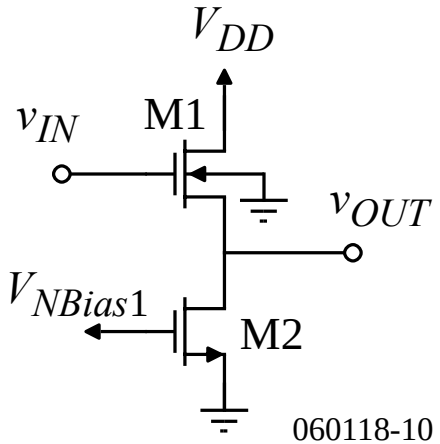
Types of buffered op amps:

- Open loop using output amplifiers
- Closed loop using negative shunt feedback to reduce the output resistance of the op amp

OPEN LOOP BUFFERED OP AMPS

The Class A Source Follower as a Buffer

- Simple
- Small signal gain $\approx \dfrac{g_m}{g_m + g_{mbs} + G_L} < 1$
- Low efficiency
- $R_{out} = \dfrac{1}{g_m + g_{mbs}} \approx 500$ to 1000Ω
- Level shift from input to output
- Maximum upper output voltage is limited
- Broadbanded as the pole and zero due to the source follower are close so compensation is typically not a problem



The Push-Pull Follower as a Buffer

- Voltage loss from 2 cascaded followers

$$A_v \approx \left(\frac{g_{m3}}{g_{m3}+g_{mbs3}}\right)\left(\frac{g_{m1}}{g_{m1}+g_{mbs1}+G_L}\right) < 1$$

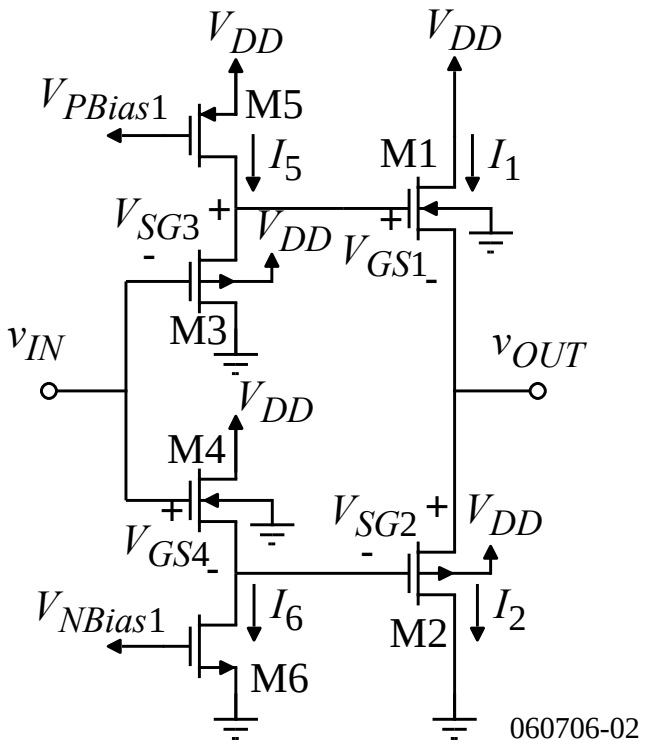
- Higher efficiency
- $R_{out} \approx \dfrac{0.5}{g_m + g_{mbs}} \approx 250 \text{ to } 500\Omega$
- Current in M1 and M2 determined by:

$$V_{GS4} + V_{SG3} = V_{GS1} + V_{SG2}$$

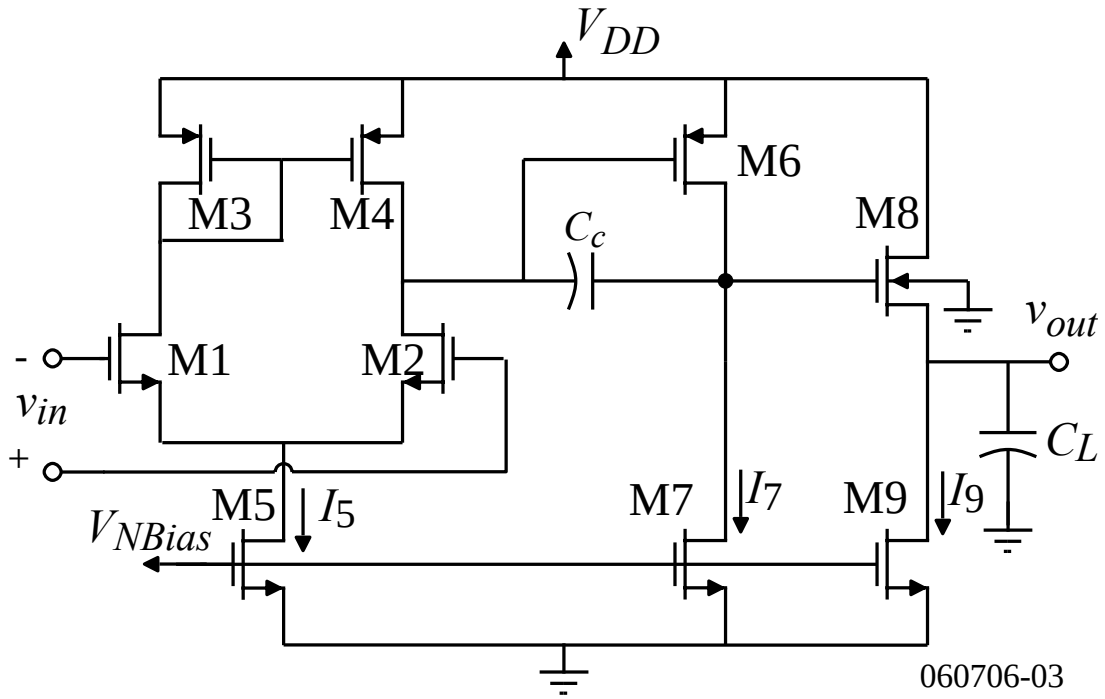
$$\sqrt{\frac{2I_6}{K_n'(W_4/L_4)}} + \sqrt{\frac{2I_5}{K_p'(W_3/L_3)}} = \sqrt{\frac{2I_1}{K_n'(W_1/L_1)}} + \sqrt{\frac{2I_2}{K_p'(W_2/L_2)}}$$

Use the W/L ratios to define I_1 and I_2 from I_5 and I_6

- Maximum positive and negative output voltages are limited



Two-Stage Op Amp with Follower



Power dissipation now becomes $(I_5 + I_7 + I_9)V_{DD}$

Gain becomes,

$$A_v = \left(\frac{g_{m1}}{g_{ds2}+g_{ds4}}\right)\left(\frac{g_{m6}}{g_{ds6}+g_{ds7}}\right)\left(\frac{g_{m8}}{g_{m8}+ g_{mbs8}+g_{ds8}+g_{ds9}}\right)$$

Source-Follower, Push-Pull Output Op Amp

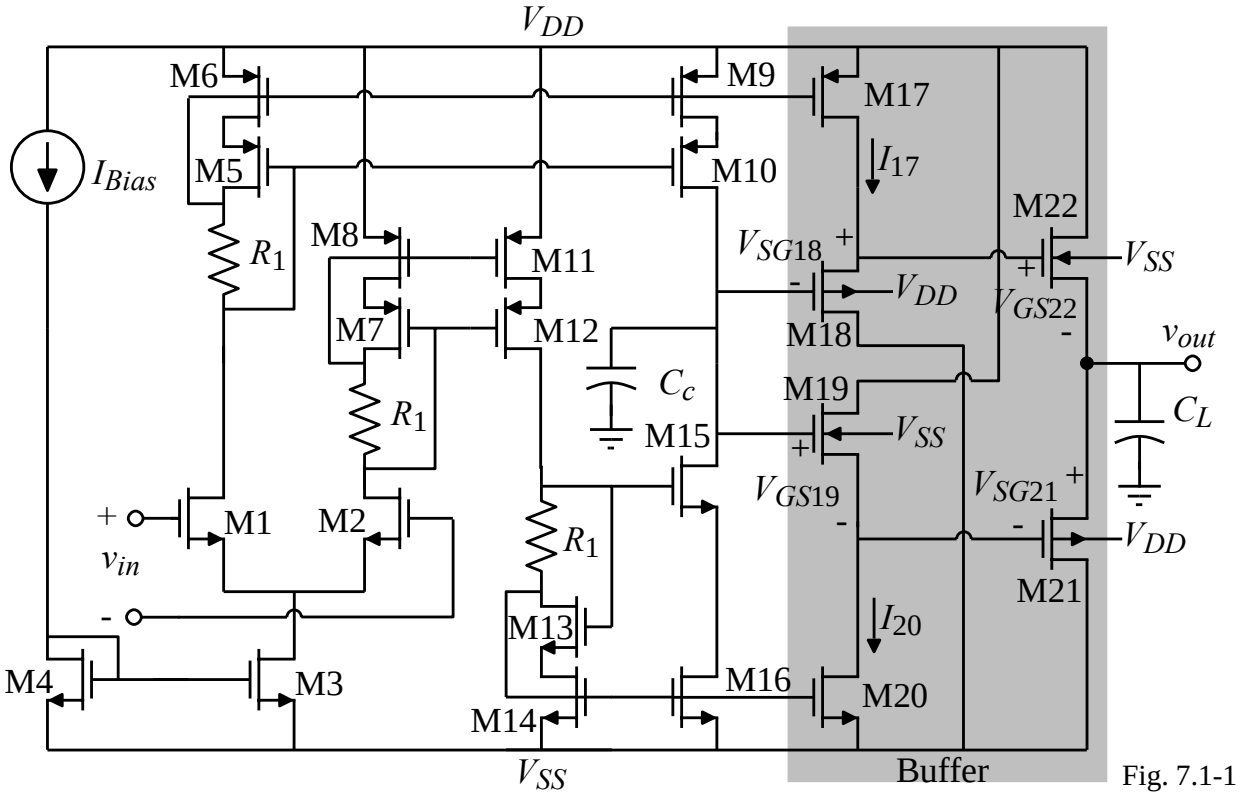


Fig. 7.1-1

$R_{out} \approx \frac{1}{g_{m21}+g_{m22}} \leq 1000\Omega$, $A_v(0)$=65dB (I_{Bias}=50μA), and GB = 60MHz for C_L = 1pF

Note the bias currents through M18 and M19 vary with the signal.

Compensation of Op Amps with Output Amplifiers

Compensation of a three-stage amplifier:

This op amp introduces a third pole, p'_3

(what about zeros?)

With no compensation,

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{-A_{vo}}{\left(\frac{s}{p'_1} - 1\right)\left(\frac{s}{p'_2} - 1\right)\left(\frac{s}{p'_3} - 1\right)}$$

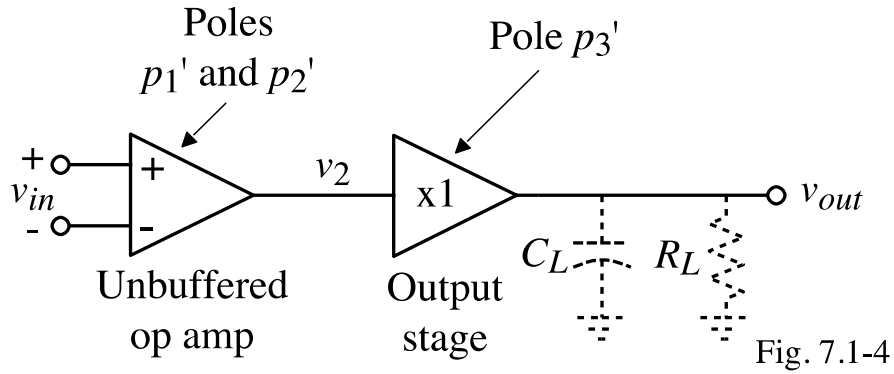
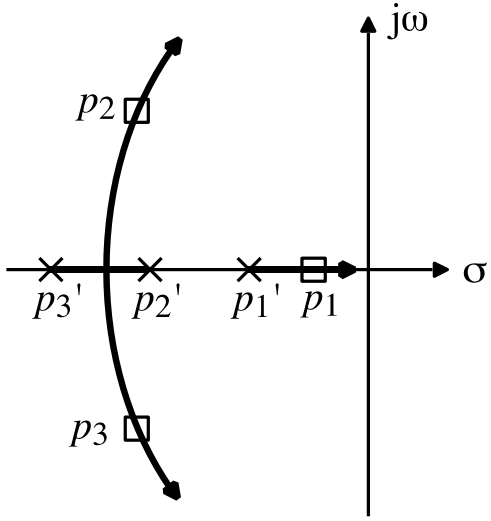
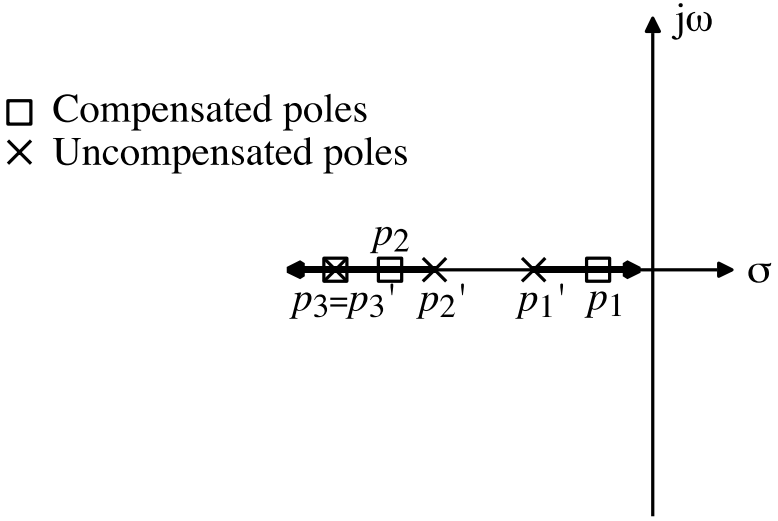


Fig. 7.1-4

Illustration of compensation choices:



Miller compensation applied around both the second and the third stage.

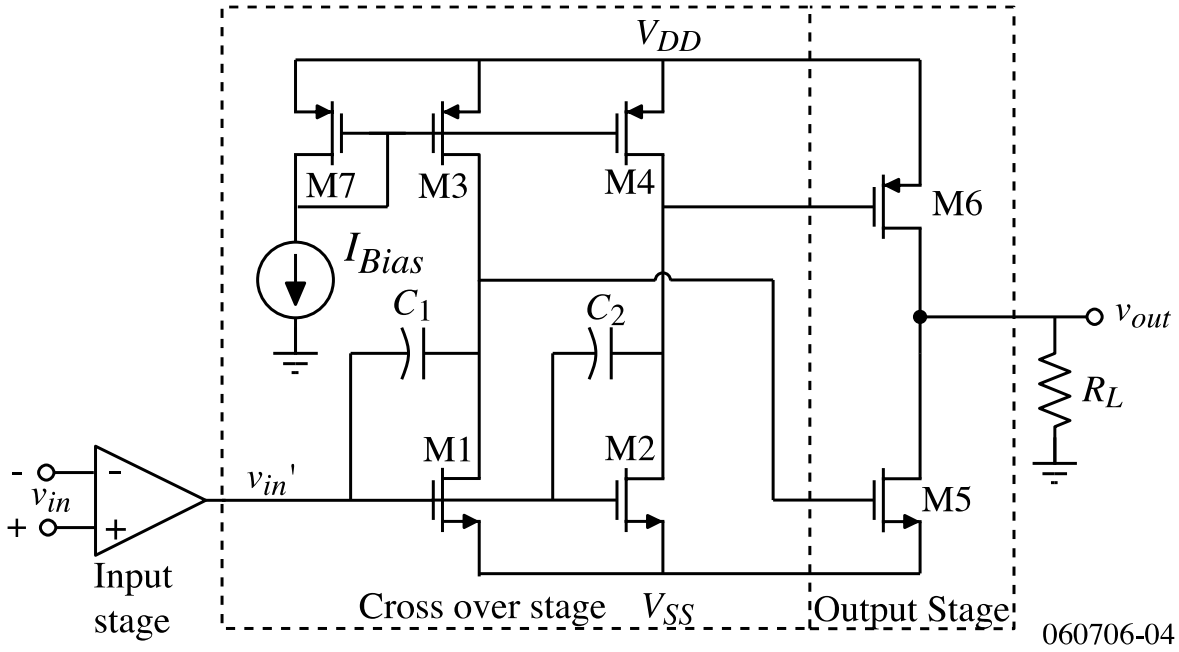


Miller compensation applied around the second stage only.

Fig. 7.1-5

Crossover-Inverter, Buffer Stage Op Amp

Principle: If the buffer has high output resistance and voltage gain (common source), this is okay if when loaded by a small R_L the gain of this stage is approximately unity.



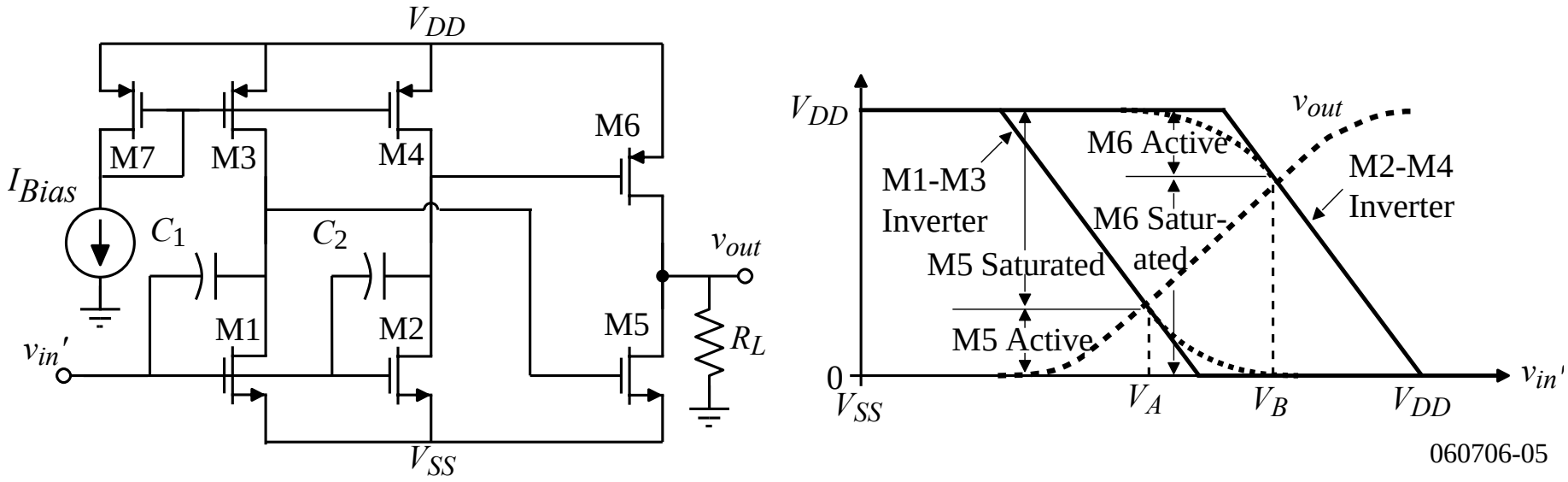
- This buffer trades gain for the ability to drive a low load resistance
- The load resistance should be fixed in order to avoid changes in the buffer gain
- The push-pull common source output will give good output voltage swing capability

Crossover-Inverter, Buffer Stage Op Amp - Continued

How does the output buffer work?

The two inverters, M1-M3 and M2-M4 are designed to work over different regions of the buffer input voltage, v_{in}'.

Consider the idealized voltage transfer characteristic of the crossover inverters:



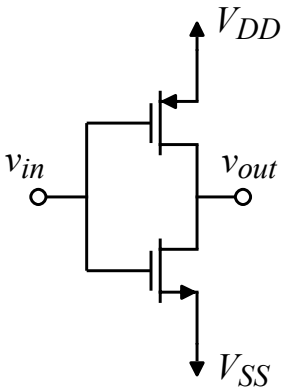
Crossover voltage ≡ $V_C = V_B - V_A \geq 0$

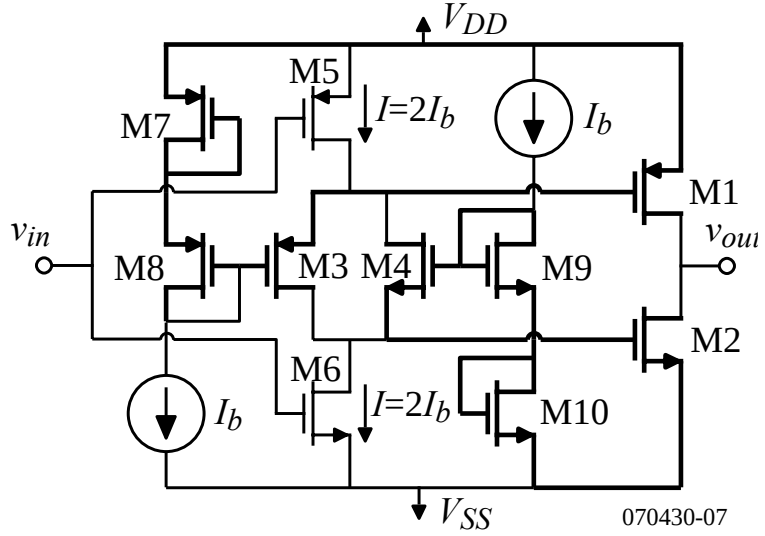
V_C is designed to be small and positive for worst case variations in processing.

Large Output Current Buffer

In the case where the load consists of a large capacitor, the ability to sink and source a large current is much more important than reducing the output resistance. Consequently, the common-source, push-pull is ideal if the quiescent current can be controlled.

A possible implementation:





If $W_4/L_4 = W_9/L_9$ and $W_3/L_3 = W_8/L_8$, then the quiescent currents in M1 and M2 can be determined by the following relationship:

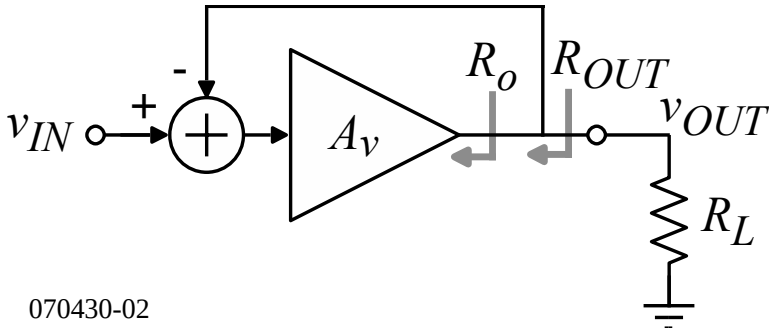
$$I_1 = I_2 = I_b\left(\frac{W_1/L_1}{W_7/L_7}\right) = I_b\left(\frac{W_2/L_2}{W_{10}/L_{10}}\right)$$

When v_{in} is increased, M6 turns off M2 and turns on M1 to source current. Similarly, when v_{in} is decreased, M5 turns off M1 and turns on M2 to sink current.

CLOSED LOOP BUFFERED OP AMPS

Principle

Use negative shunt feedback to reduce the output resistance of the buffer.

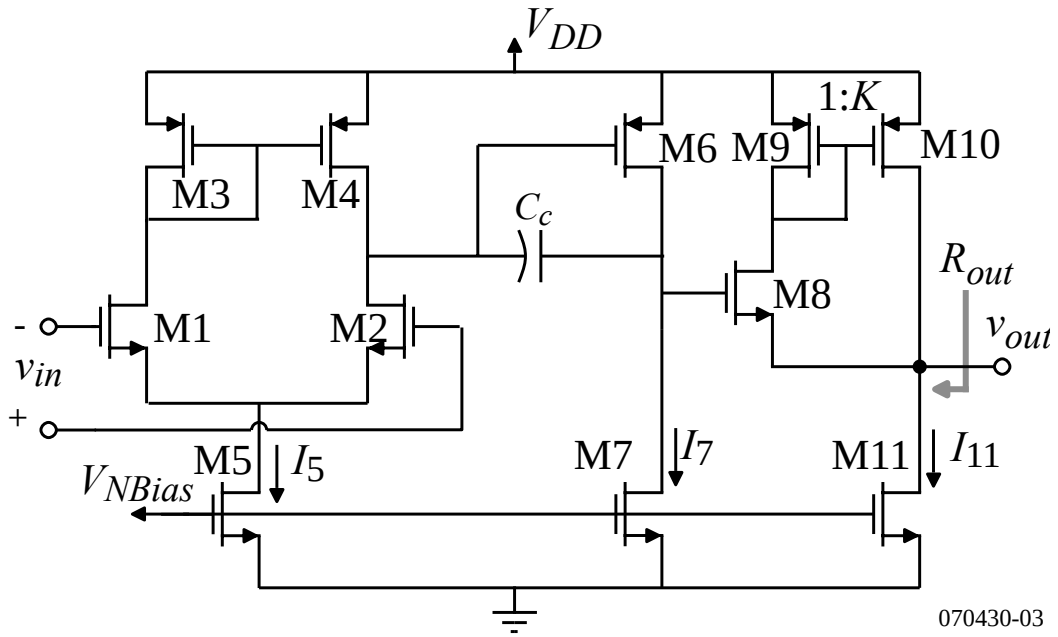


- Output resistance

$$R_{OUT} = \frac{R_o}{1 + A_v}$$

- Watch out for when small R_L causes A_v to decrease.
- The bandwidth will be limited by the feedback (i.e. at high frequencies, the gain of A_v decreases causing the output resistance to increase.

Two Stage Op Amp with a Gain Boosted, Source Follower Buffer



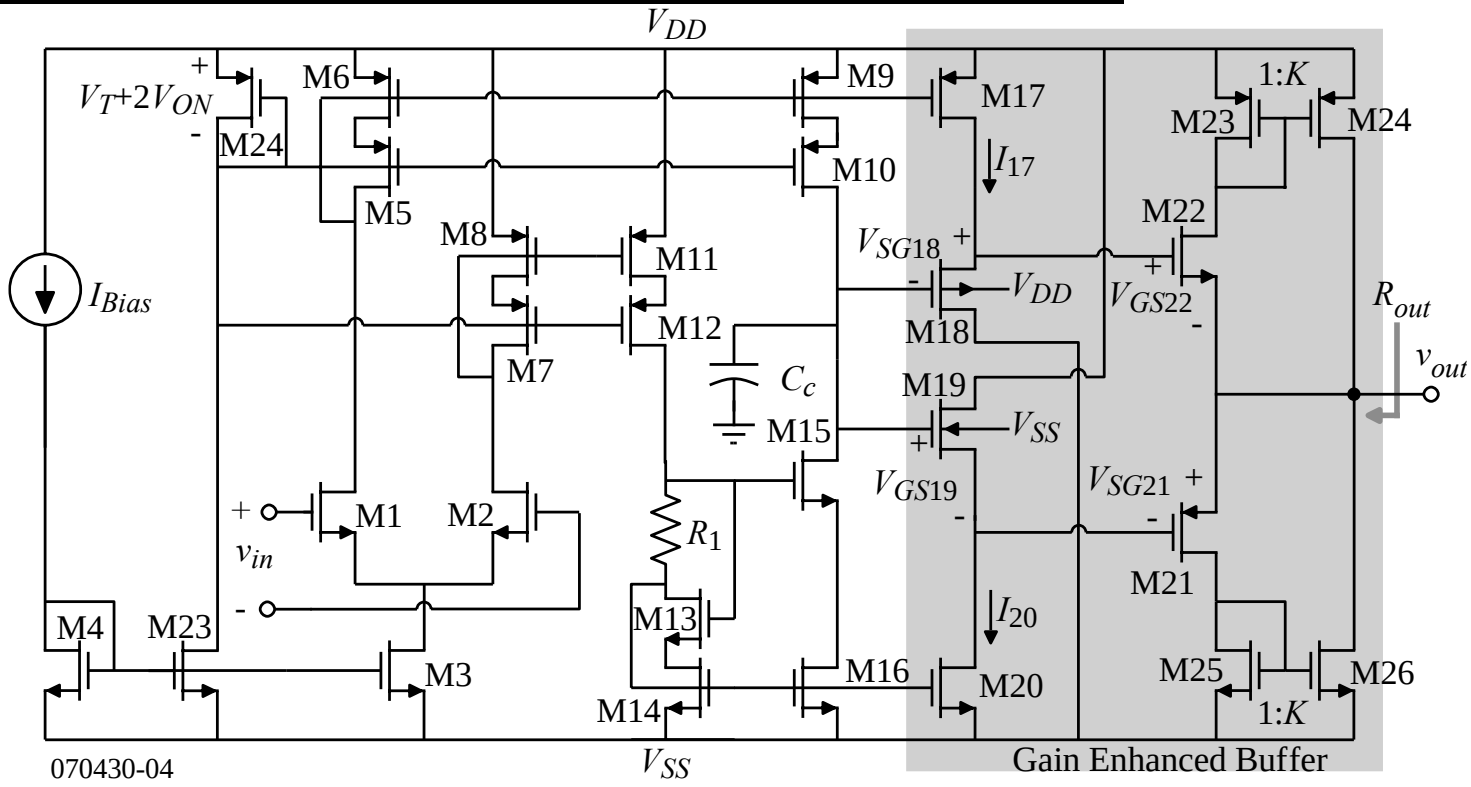
$$R_{out} \approx \frac{1}{g_{m8}K}$$

Power dissipation now becomes $(I_5 + I_7 + I_{11})V_{DD}$

Gain becomes,

$$A_v = \left(\frac{g_{m1}}{g_{ds2}+g_{ds4}}\right)\left(\frac{g_{m6}}{g_{ds6}+g_{ds7}}\right)\left(\frac{g_{m8}K}{g_{m8}K+ g_{mbs8}K +G_L}\right)$$

Gain Boosted, Source-Follower, Push-Pull Output Op Amp



$$R_{out} \approx \frac{1}{K(g_{m21}+g_{m22})} \approx \frac{1000\Omega}{K} \approx 100\Omega$$

$A_v(0)$=65dB (I_{Bias}=50μA)

Note the bias currents through M18 and M19 vary with the signal.

Common Source, Push Pull Buffer with Shunt Feedback

To get low output resistance using MOSFETs, negative feedback must be used.

Ideal implementation:

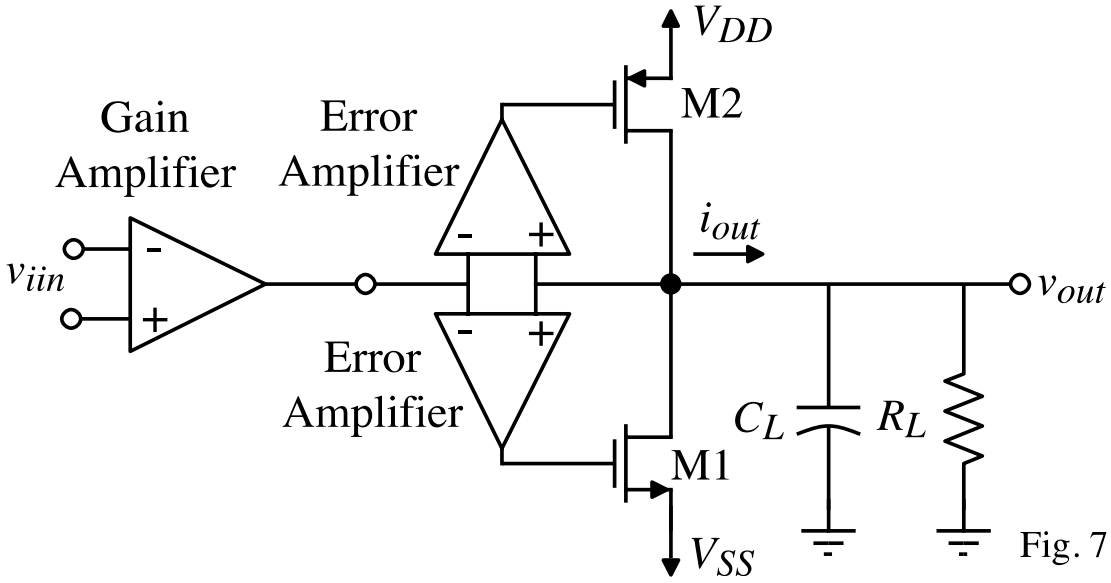


Fig. 7.1-5A

Comments:

- The output resistance will be equal to $r_{ds1}||r_{ds2}$ divided by the loop gain
- If the error amplifiers are not perfectly matched, the bias current in M1 and M2 is not defined

Low Output Resistance Op Amp - Continued

Offset correction circuitry:

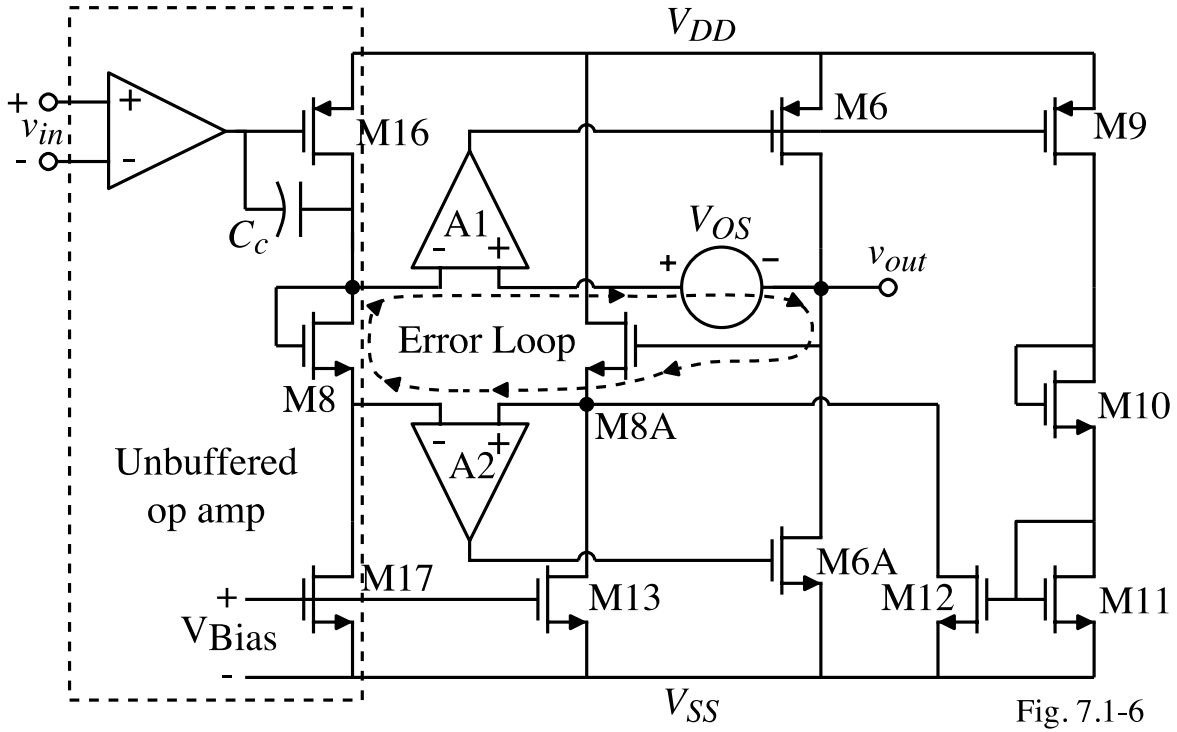


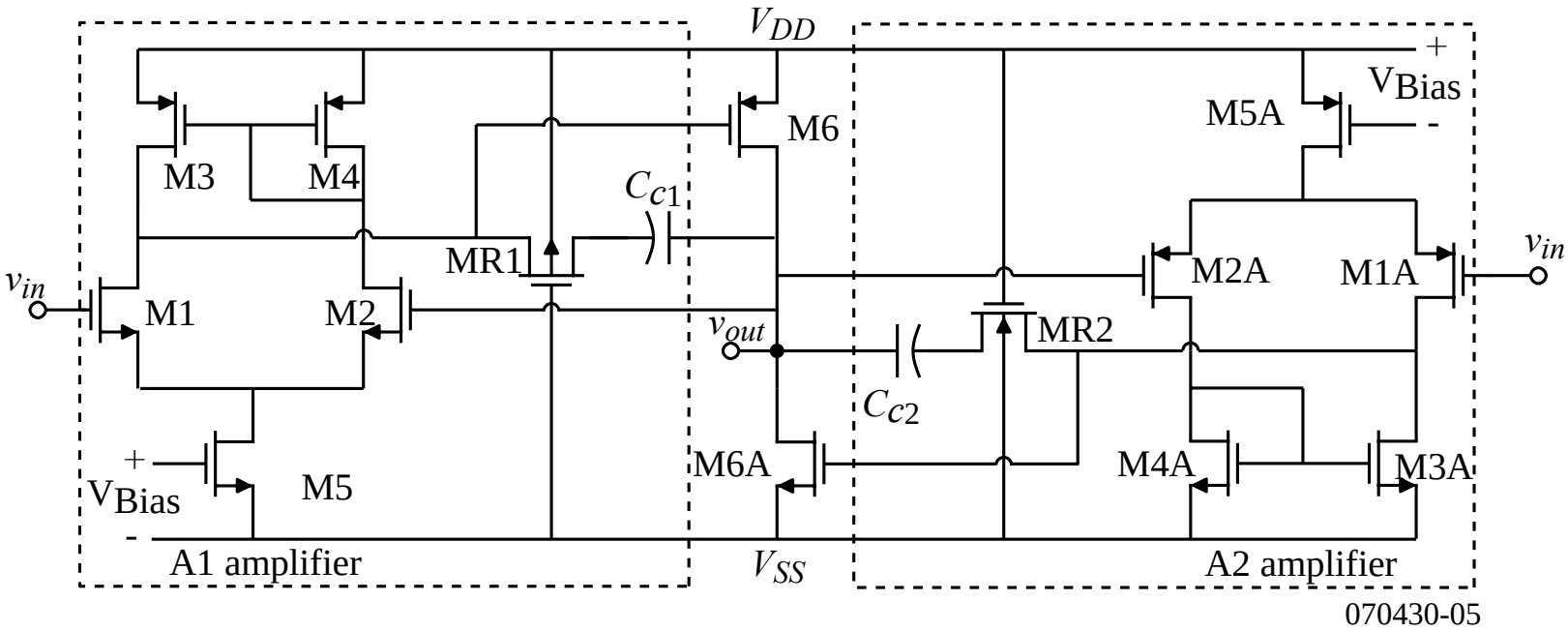
Fig. 7.1-6

The feedback circuitry of the two error amplifiers tries to insure that the voltages in the loop sum to zero. Without the M9-M12 feedback circuit, there is no way to adjust the output for any error in the loop. The circuit works as follows:

When V_{OS} is positive, M6 tries to turn off and so does M6A. I_{M9} reduces thus reducing I_{M12}. A reduction in I_{M12} reduces I_{M8A} thus decreasing V_{GS8A}. V_{GS8A} ideally decreases by an amount equal to V_{OS}. A similar result holds for negative offsets and offsets in *EA*2.

Low Output Resistance Op Amp - Continued

Error amplifiers:



Basically a two-stage op amp with the output push-pull transistors as the second-stage of the op amp.

Low Output Resistance Op Amp - Complete Schematic

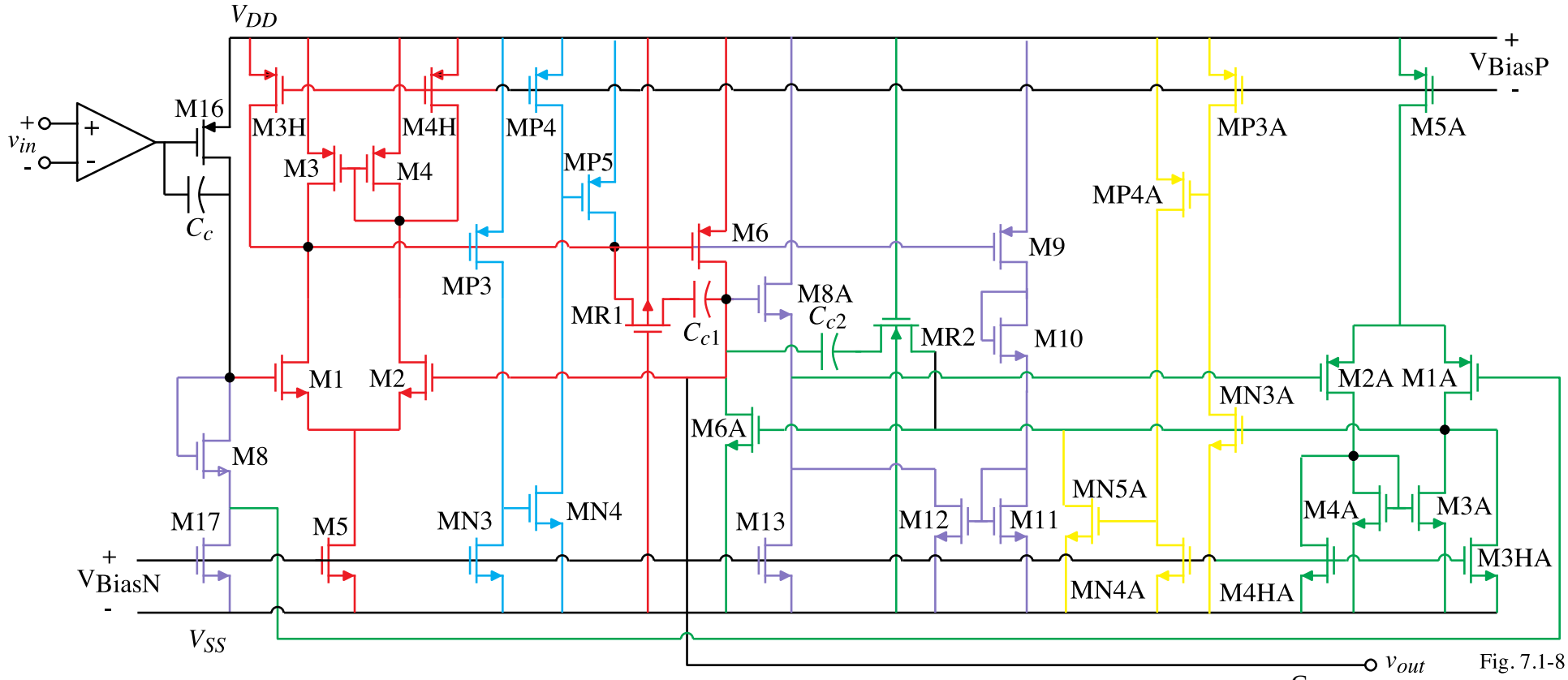


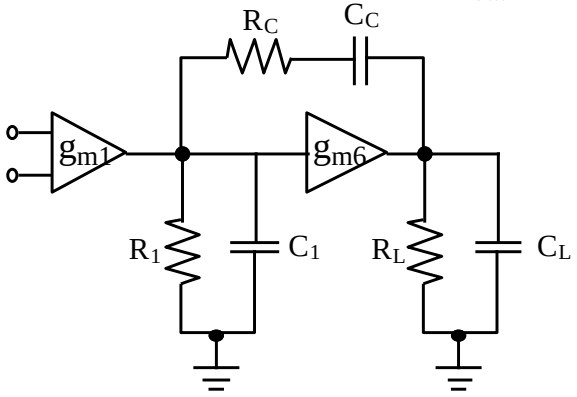
Fig. 7.1-8

Short circuit protection(max. output ±60mA):

MP3-MN3-MN4-MP4-MP5

MN3A-MP3A-MP4A-MN4A-MN5A

$$R_{out} \approx \frac{r_{ds6} \| r_{ds6A}}{\text{Loop Gain}} \approx \frac{50\text{k}\Omega}{5000} = 10\Omega$$



Simpler Implementation of Negative Feedback to Achieve Low Output Resistance

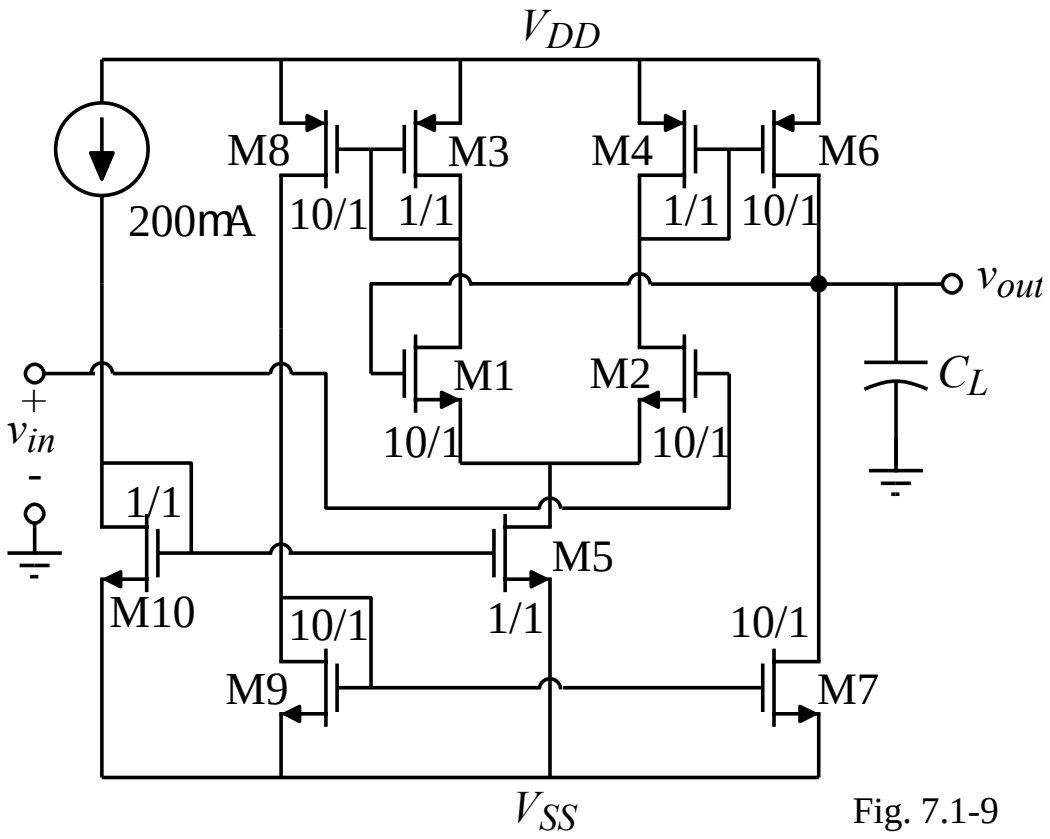


Fig. 7.1-9

Output Resistance:

$$R_{out} = \frac{R_o}{1+LG}$$

where

$$R_o = \frac{1}{g_{ds6}+g_{ds7}}$$

and

$$|LG| = \frac{g_{m2}}{2g_{m4}}(g_{m6}+g_{m7})R_o$$

Therefore, the output resistance is:

$$R_{out} = \frac{1}{(g_{ds6}+g_{ds7})\left[1+\left(\frac{g_{m2}}{2g_{m4}}\right)(g_{m6}+g_{m7})R_o\right]}$$

Example 26-1 - Low Output Resistance Using Shunt Negative Feedback Buffer

Find the output resistance of above op amp using the model parameters of $K_N' = 120\mu A/V^2$, $K_P' = 25\mu A/V^2$, $\lambda_N = 0.06V^{-1}$ and $\lambda_P = 0.08V^{-1}$.

Solution

The current flowing in the output transistors, M6 and M7, is 1mA which gives R_o of

$$R_o = \frac{1}{(\lambda_N+\lambda_P)1mA} = \frac{1000}{0.14} = 7.143k\Omega$$

To calculate the loop gain, we find that

$$g_{m2} = \sqrt{2K_N'\cdot 10\cdot 100\mu A} = 490\mu S$$

$$g_{m4} = \sqrt{2K_P'\cdot 1\cdot 100\mu A} = 70.7\mu S$$

and

$$g_{m6} = \sqrt{2K_P'\cdot 10\cdot 1000\mu A} = 707\mu S$$

Therefore, the loop gain is

$$|LG| = \frac{490}{2\cdot 70.7}\ (0.707+0.071)7.143 = 19.26$$

Solving for the output resistance, R_{out}, gives

$$R_{out} = \frac{7.143k\Omega}{1 + 19.26} = 353\Omega \quad \text{(Assumes that } R_L \text{ is large)}$$

USE OF THE BJT IN BUFFERED OP AMPS

Substrate BJTs

Illustration of an NPN substrate BJT available in a p-well CMOS technology:

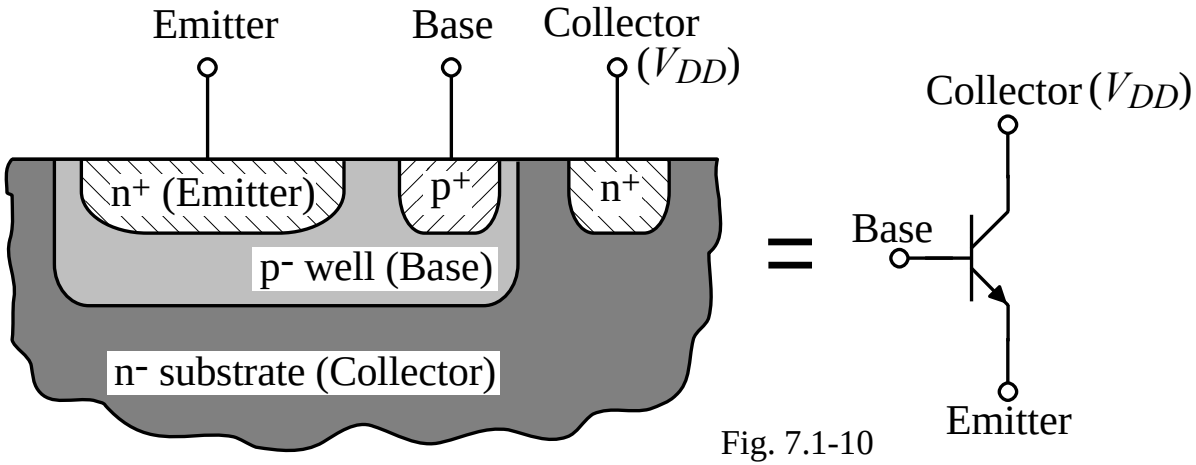


Fig. 7.1-10

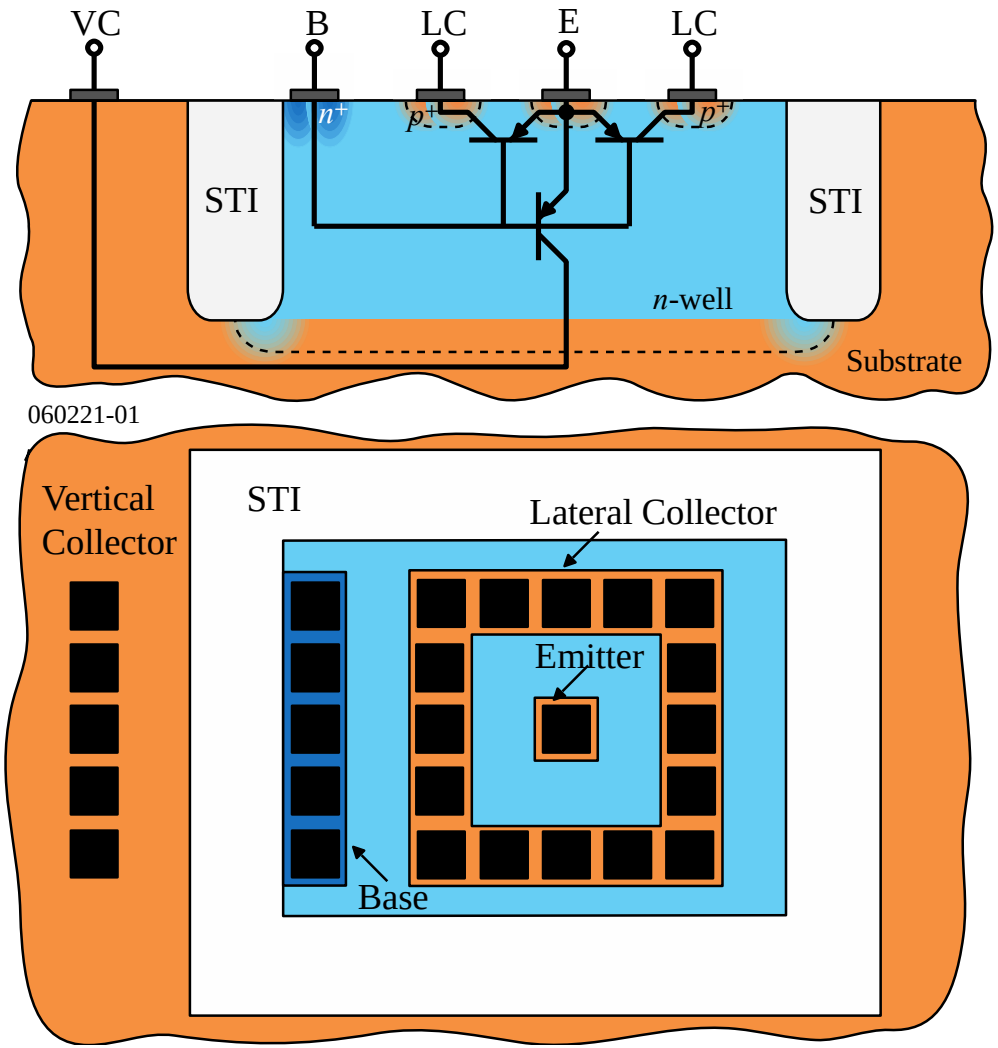
Comments:

- g_m of the BJT is larger than the FET so that the output resistance w/o feedback is lower
- Collector current will be flowing in the substrate
- Current is required to drive the BJT
- Only an NPN or a PNP bipolar transistor is available

A Lateral Bipolar Transistor

n-well CMOS technology:

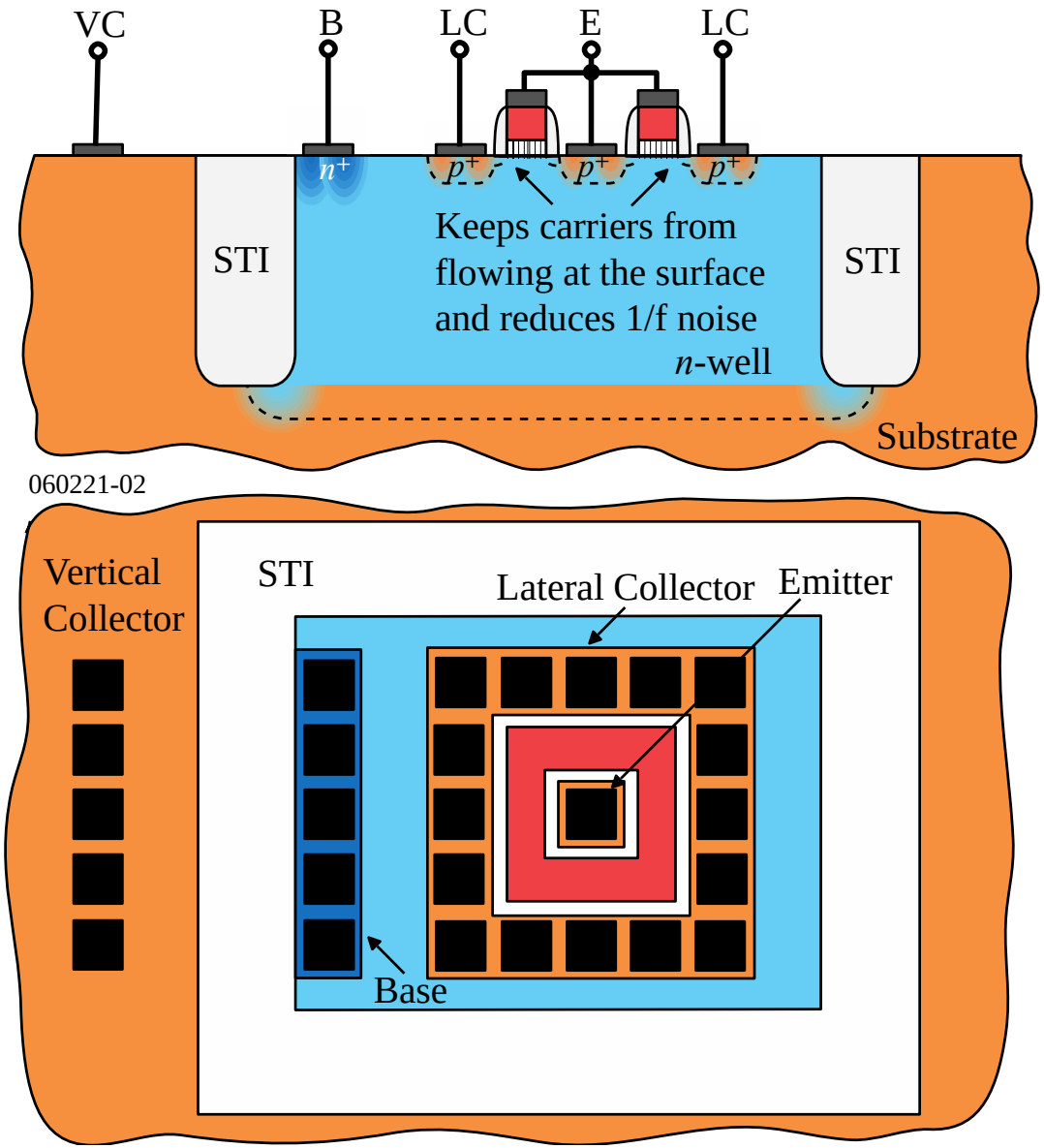
- It is desirable to have the lateral collector current much larger than the vertical collector current.
- Triple well technology allows the current of the vertical collector to avoid flowing in the substrate.
- Lateral BJT generally has good matching.



A Field-Aided Lateral BJT

Use minimum channel length to enhance beta:

$ß_F \approx 50$ to 100 depending on the process



Two-Stage Op Amp with a Class-A BJT Output Buffer Stage

Purpose of the M8-M9 source follower:

1.) Reduce the output resistance (includes whatever is seen from the base to ground divided by $1+\beta_F$)

2.) Reduces the output load at the drains of M6 and M7

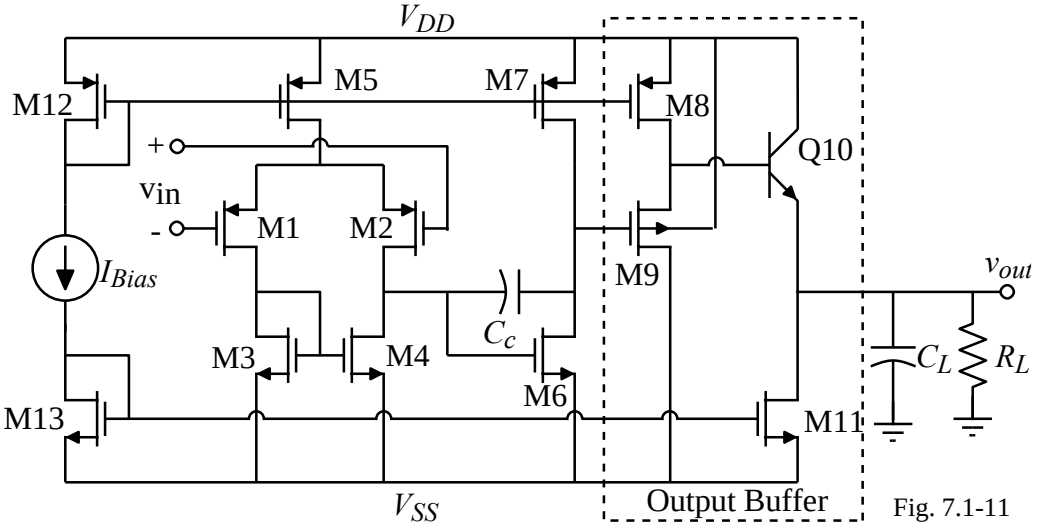


Fig. 7.1-11

Small-signal output resistance : $R_{out} \approx \dfrac{r_{\pi 10} + (1/g_{m9})}{1+ß_F} = \dfrac{1}{g_{m10}} + \dfrac{1}{g_{m9}(1+ß_F)}$

= 51.6Ω+6.7Ω = 58.3Ω where I_{10}=500µA, I_8=100µA, W_9/L_9=100 and $ß_F$ is 100

$$v_{OUT}(\text{max}) = V_{DD} - V_{SD8}(\text{sat}) - v_{BE10} = V_{DD} - \sqrt{\frac{2K_P'}{I_8(W_8/L_8)}} - V_t \ln\left(\frac{I_{c10}}{I_{s10}}\right)$$

Voltage gain:

$$\frac{v_{out}}{v_{in}} \approx \left(\frac{g_{m1}}{g_{ds2}+g_{ds4}}\right)\left(\frac{g_{m6}}{g_{ds6}+g_{ds7}}\right)\left(\frac{g_{m9}}{g_{m9}+g_{mbs9}+g_{ds8}+g_{\pi 10}}\right)\left(\frac{g_{m10}R_L}{1+g_{m10}R_L}\right)$$

Compensation will be more complex because of the additional stages.

Example 26-2 - Designing the Class-A, Buffered Op Amp

Use an *n*-well, 0.25µm CMOS technology to design an op amp using a class-A, BJT output stage to give the following specifications. Assume the channel length is to be 0.5µm. The FETs have the model parameters of $K_N' = 120\mu A/V^2$, $K_P' = 25\mu A/V^2$, $V_{TN} = |V_{TP}| = 0.5V$, $\lambda_N = 0.06V^{-1}$ and $\lambda_P = 0.08V^{-1}$ along with the BJT parameters of $I_S = 10^{-14}A$ and $ß_F = 50$.

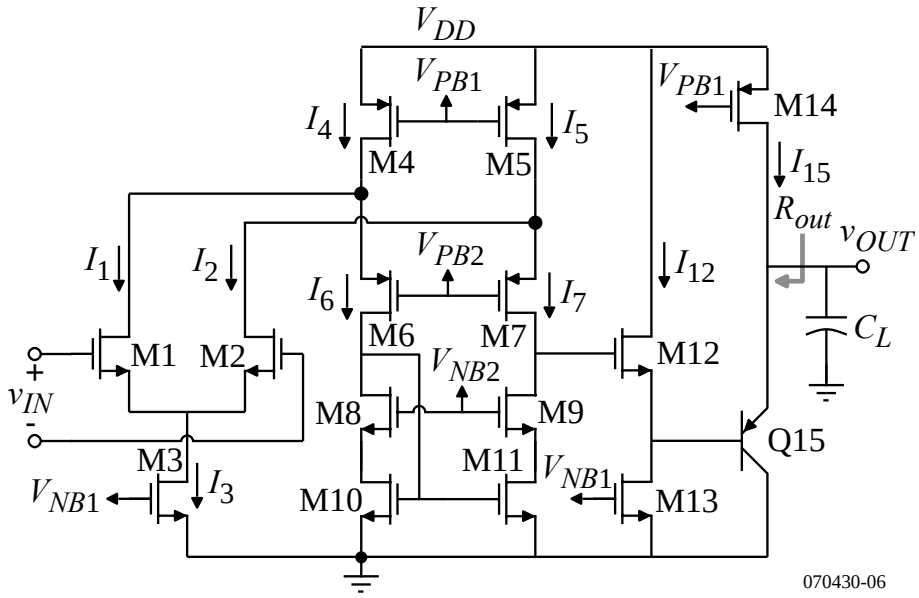
$V_{DD} = 2.5V$ $V_{SS} = 0V$ GB = 10MHz $A_{vd}(0) \geq 2500V/V$ Slew rate $\geq 10V/\mu s$

$R_L = 500\Omega$ $R_{out} \leq 50\Omega$ $C_L = 100pF$ $ICMR = +1V$ to $2V$

Solution

A quick comparison shows that the specifications of this problem are similar to the folded cascode op amp that was designed in Ex. 24-4. Borrowing that design for this example results in the following op amp.

Therefore, the goal of this example will be the design of M12 through Q15 to satisfy the slew rate and output resistance requirements.



Example 26-2 – Continued

BJT follower (Q15):

SR = 10V/μs and 100pF capacitor give I_{15} = 1mA.

$\therefore$ Assuming the gate of M14 is connected to the gate of M5, the W/L ratio of M14 becomes

$W_{14}/L_{14} = (1000\mu A/125\mu A)160 = 1280 \quad \Rightarrow \quad W_{14} = 640\mu m$

$I_{15} = 1mA \quad \Rightarrow \quad 1/g_{m15} = 0.0258V/1mA = 25.8\Omega$

MOS follower:

To source 1mA, the BJT requires 20μA ($ß$ =50) from the MOS follower (M12-M13).

Therefore, select a bias current of 100μA for M13. If the gates of M3 and M13 are connected together, then

$W_{13}/L_{13} = (100\mu A/100\mu A)15 = 15 \quad \Rightarrow \quad W_{13} = 7.5\mu m$

To get R_{out} = 50Ω, if $1/g_{m15}$ is 25.8Ω, then design g_{m12} as

$$\frac{1}{g_{m15}} = \frac{1}{g_{m12}(1+ß_F)} = 24.2\Omega \quad \rightarrow \quad g_{m12} = \frac{1}{(24.2\Omega)(1+ß_F)} = \frac{1}{24.2\cdot 51} = 810\mu S$$

$\therefore$ g_{m12} and $I_{12} \Rightarrow W/L = 27.3 \approx 30 \Rightarrow W_{12} = 15\mu m$

Example 26-2 - Continued

To calculate the voltage gain of the MOS follower we need to find g_{mbs9} ($\gamma_N = 0.4\sqrt{\text{V}}$).

$$\therefore \qquad g_{mbs12} = \frac{g_{m12}\gamma_N}{2\sqrt{2\phi_F + V_{BS12}}} = \frac{810 \cdot 0.4}{2\sqrt{0.5+0.55}} = 158\mu\text{S}$$

where we have assumed that the value of V_{SB12} is approximately 1.25V – 0.7V = 0.55V.

$$\therefore \qquad A_{MOS} = \frac{810\mu\text{S}}{810\mu\text{S}+158\mu\text{S}+6\mu\text{S}+8\mu\text{S}} = 0.825$$

The voltage gain of the BJT follower is

$$A_{BJT} = \frac{500}{25.8+500} = 0.951 \text{ V/V}$$

Thus, the gain of the op amp is

$$A_{vd}(0) = (4{,}680)(0.825)(0.951) = 3{,}672 \text{ V/V}$$

The power dissipation of this amplifier is,

$$P_{diss.} = 2.5\text{V}(125\mu\text{A}+125\mu\text{A}+100\mu\text{A}+1000\mu\text{A}) = 3.375\text{mW}$$

The signal swing across the 500Ω load resistor will be restricted to ±0.5V due to the 1000μA output current limit.

SUMMARY

- A buffered op amp requires an output resistance between $10\Omega \leq R_o \leq 1000\Omega$
- Output resistance using MOSFETs only can be reduced by,
  - Source follower output ($1/g_m$)
  - Negative shunt feedback (frequency is a problem in this approach)
- Use of substrate (or lateral) BJT's can reduce the output resistance because g_m is larger than the g_m of a MOSFET
- Adding a buffer stage to lower the output resistance will most likely complicate the compensation of the op amp