LECTURE 25 – SIMULATION AND MEASUREMENT OF OP AMPS

LECTURE ORGANIZATION

Outline

- Introduction
- Open Loop Gain
- *CMRR* and *PSRR*
- A general method of measuring A_{vd}, *CMRR*, and *PSRR*
- Other op amp measurements
- Simulation of a Two-Stage Op Amp
- Summary

***CMOS Analog Circuit Design*, 3rd Edition Reference**

Pages 328-341

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INTRODUCTION

Simulation and Measurement Considerations

Objectives:

- The objective of simulation is to verify and optimize the design.
- The objective of measurement is to experimentally confirm the specifications.

Similarity between Simulation and Measurement:

- Same goals
- Same approach or technique

Differences between Simulation and Measurement:

- Simulation can idealize a circuit
  - All transistor electrical parameters are ideally matched
  - Ideal stimuli
- Measurement must consider all nonidealities
  - Physical and electrical parameter mismatches
  - Nonideal stimuli
  - Parasistics

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OPEN LOOP GAIN

Simulating or Measuring the Open-Loop Transfer Function of the Op Amp

Circuit (Darkened op amp identifies the op amp under test):

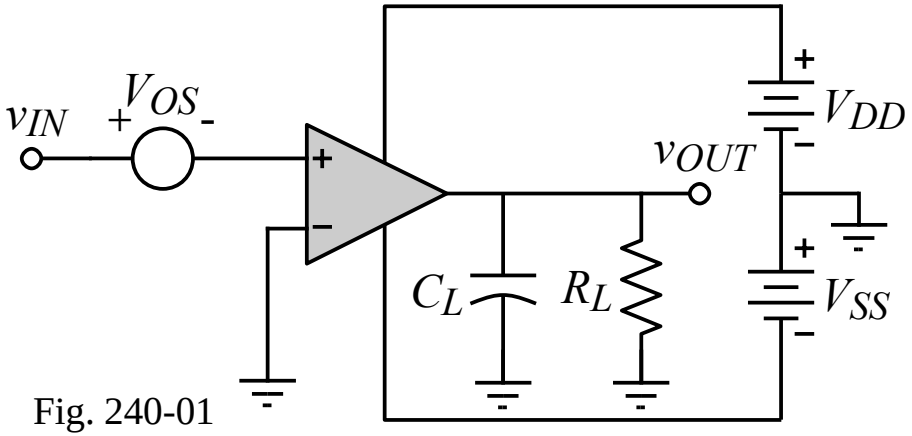

Fig. 240-01

Simulation:

This circuit will give the voltage transfer function curve. This curve should identify:

1.) The linear range of operation
2.) The gain in the linear range
3.) The output limits
4.) The systematic input offset voltage
5.) DC operating conditions, power dissipation
6.) When biased in the linear range, the small-signal frequency response can be obtained
7.) From the open-loop frequency response, the phase margin can be obtained (F = 1)

Measurement:

This circuit probably will not work unless the op amp gain is very low.

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A More Robust Method of Measuring the Open-Loop Frequency Response

Circuit:

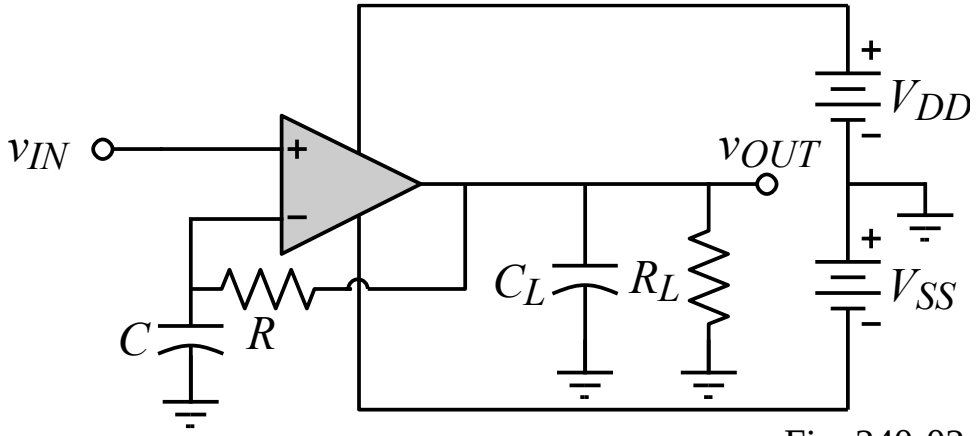

Fig. 240-02

Resulting Closed-Loop Frequency Response:

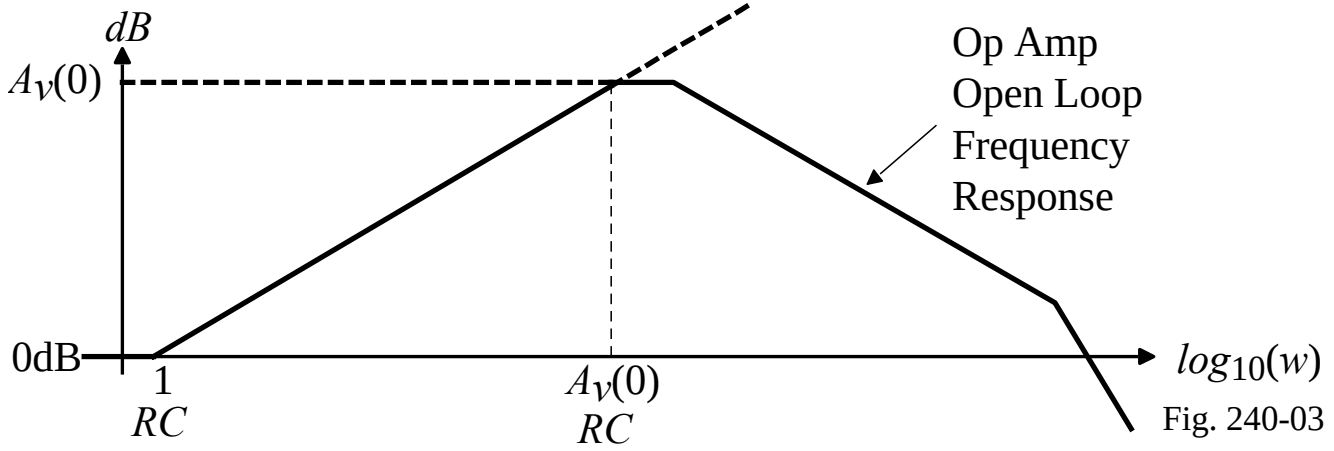

Fig. 240-03

Make the *RC* product as large as possible.

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CMRR AND *PSRR*

Simulation of the Common-Mode Voltage Gain

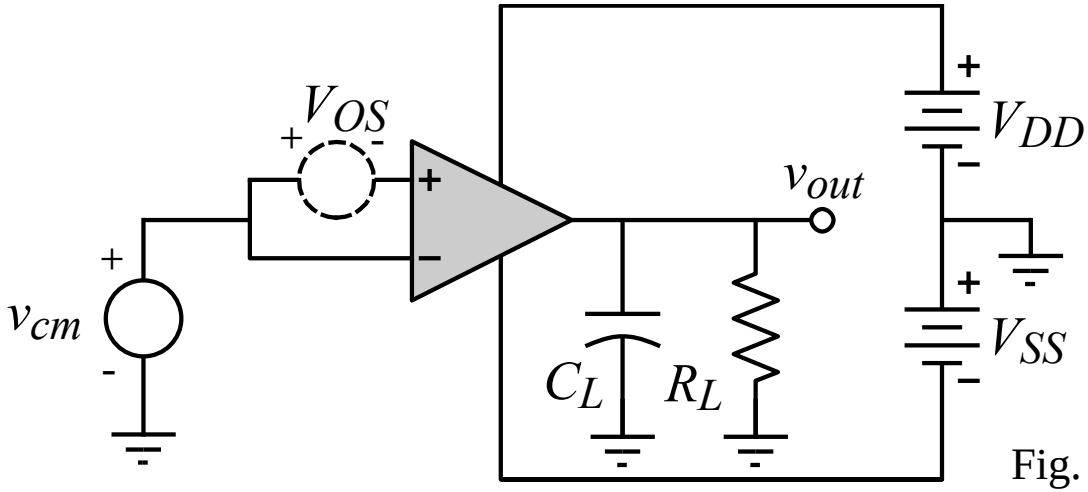

Fig. 6.6-5

Make sure that the output voltage of the op amp is in the linear region.

Divide (subtract dB) the result into the open-loop gain to get *CMRR*.

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Simulation of CMRR of an Op Amp

A simulation method that avoids dividing the differential gain by the common mode gain is given on this slide. For this method to work, the op amp should be balanced.

Consider the following:

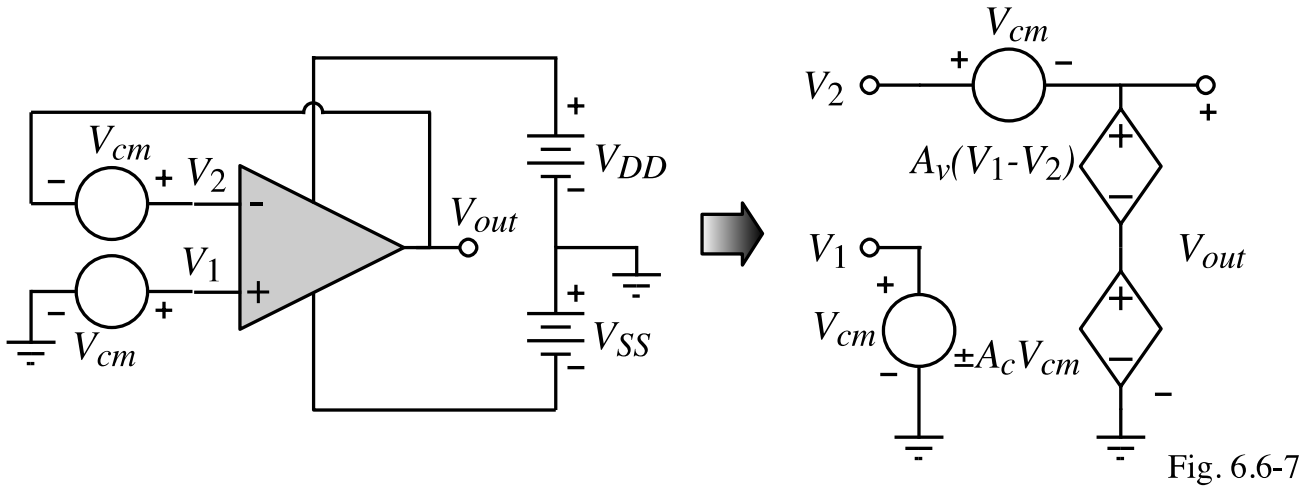

Fig. 6.6-7

$$V_{out} = A_v(V_1\text{-}V_2) \pm A_{cm}\left(\frac{V_1+V_2}{2}\right) = -A_V V_{out} \pm A_{cm} V_{cm}$$

$$V_{out} = \frac{\pm A_{cm}}{1+A_v} V_{cm} \approx \frac{\pm A_{cm}}{A_v} V_{cm}$$

$$\therefore \quad \boxed{|CMRR| = \frac{A_v}{A_{cm}} = \frac{V_{cm}}{V_{out}}}$$

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Direct Simulation of *PSRR*

Circuit:

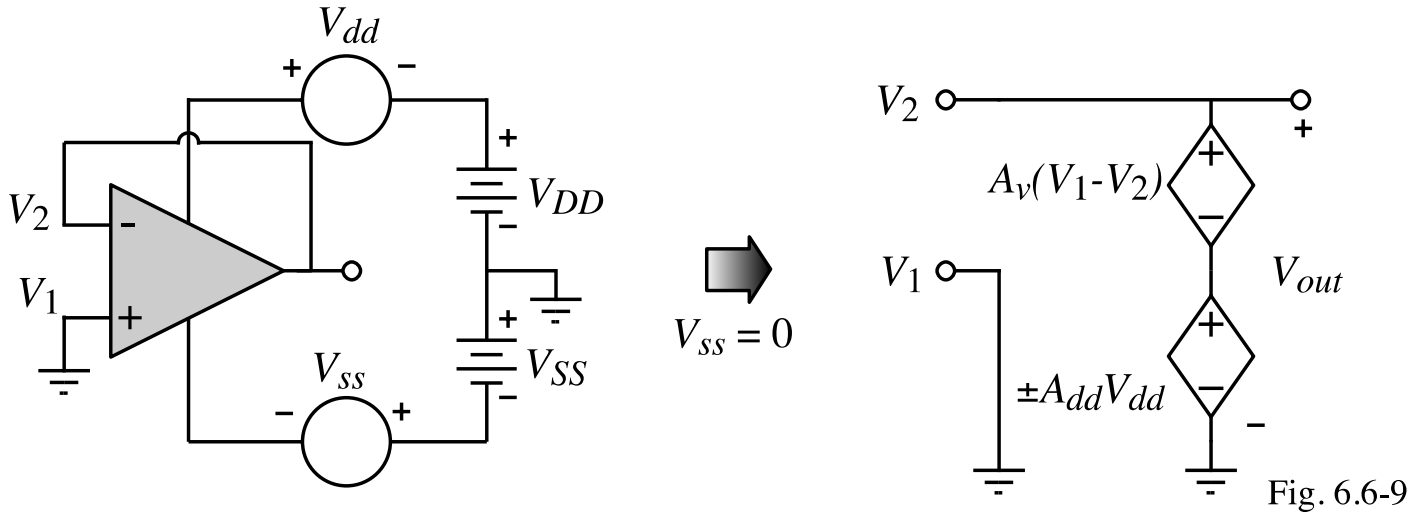

Fig. 6.6-9

$$V_{out} = A_v(V_1\text{-}V_2) \pm A_{dd}V_{dd} = -A_vV_{out} \pm A_{dd}V_{dd}$$

$$V_{out} = \frac{\pm A_{dd}}{1+A_v} V_{dd} \approx \frac{\pm A_{dd}}{A_v} V_{dd}$$

$$\therefore \quad \boxed{PSRR^+ = \frac{A_v}{A_{dd}} = \frac{V_{dd}}{V_{out}}} \quad \text{and} \quad \boxed{PSRR^- = \frac{A_v}{A_{ss}} = \frac{V_{ss}}{V_{out}}}$$

Works well as long as *CMRR* is much greater than 1.

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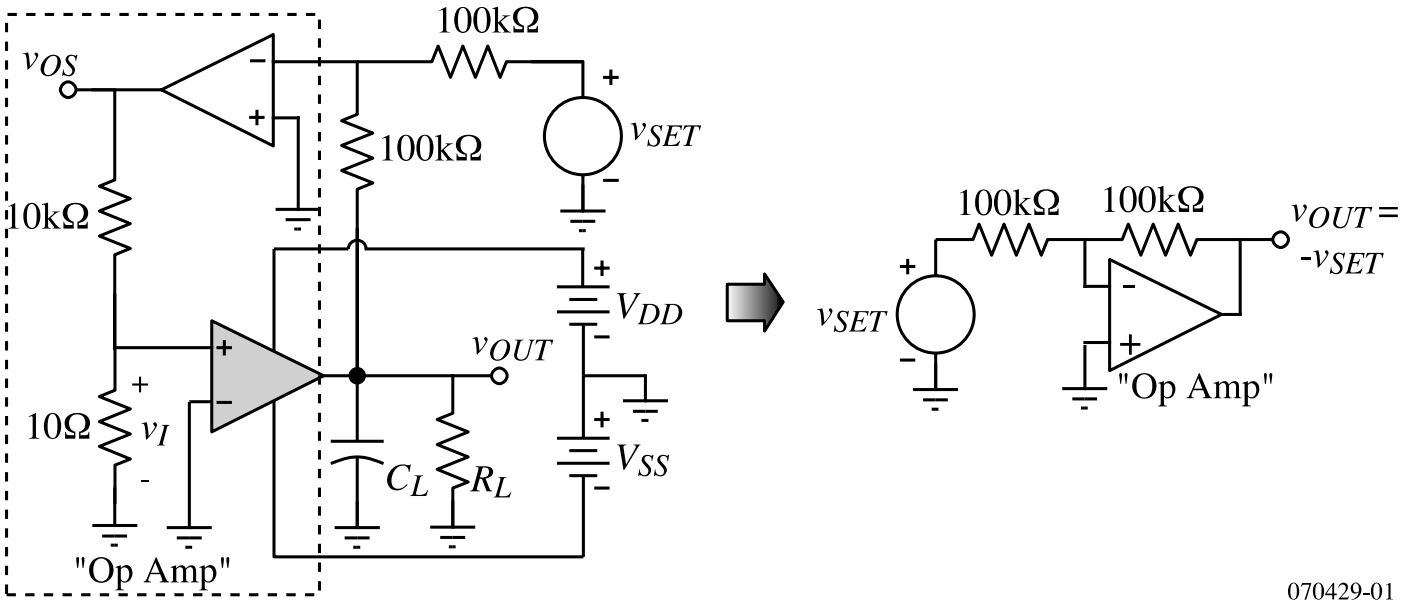
A GENERAL METHOD OF MEASURING A_{VD}, *CMRR*, AND *PSRR*

General Principle of the Measurement

Circuit:



The amplifier under test is shown as the darkened op amp.

Principle:

Apply the stimulus to the output of the op amp under test and see how the input responds. Note that:

$$v_{OUT} = -v_{SET} \quad \text{and} \quad v_I \approx \frac{v_{OS}}{1000}$$

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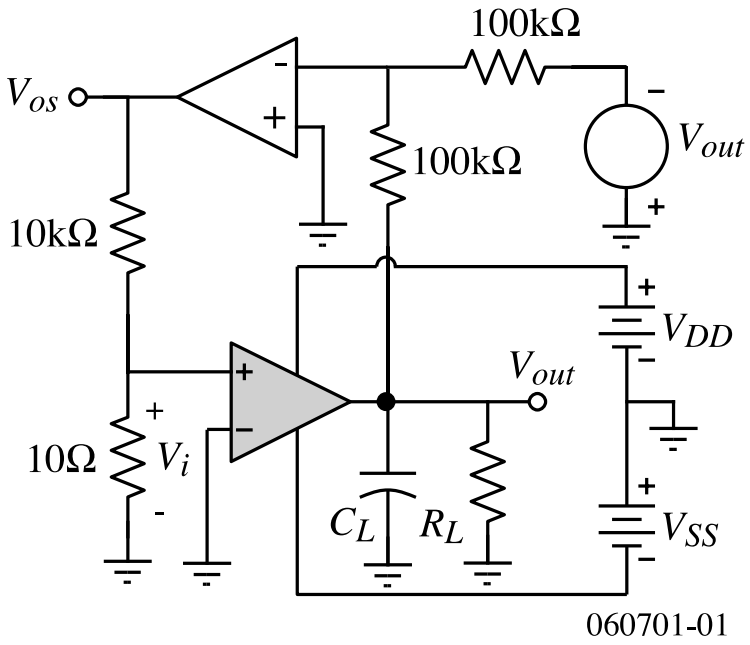
Measurement of Open-Loop Gain

Measurement configuration:



$$A_{vd} = \frac{V_{out}}{V_{id}} = \frac{V_{out}}{V_i}$$

$$V_{os} \approx 1000 V_i$$

Therefore, $$A_{vd} = \frac{1000 V_{out}}{V_{os}}$$

Sweep V_{out} as a function of frequency, invert the result and multiply by 1000 to get $A_{vd}(j\omega)$.

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Measurement of *CMRR*

Measurement Configuration:

Note that the whole amplifier is stimulated by V_{icm} while the input responds to this change.

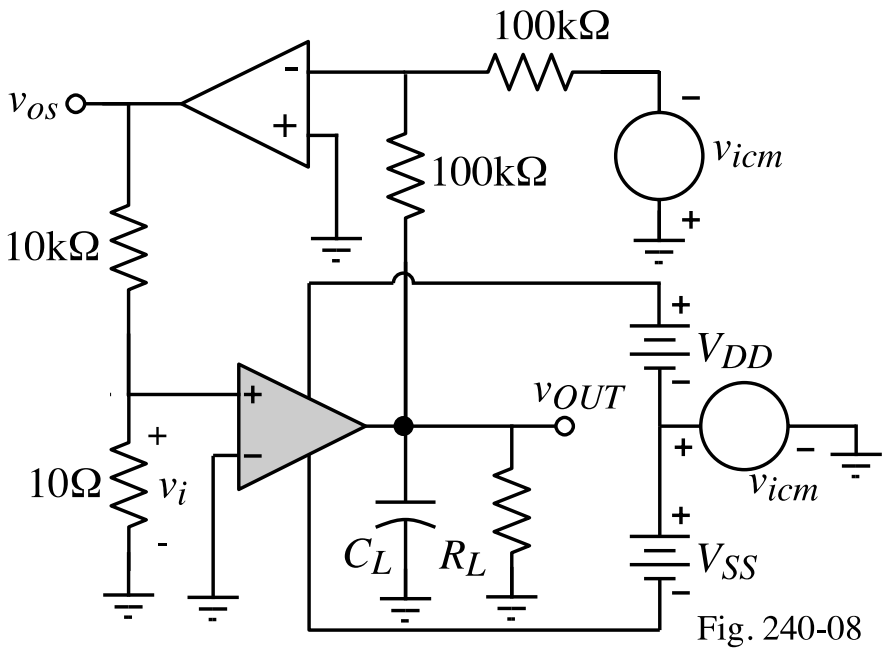

Fig. 240-08

The definition of the common-mode rejection ratio is

$$CMRR = \left|\frac{A_{vd}}{A_{cm}}\right| = \frac{(v_{out}/v_{id})}{(v_{out}/v_{icm})}$$

However, in the above circuit the value of v_{out} is the same so that we get

$$CMRR = \frac{v_{icm}}{v_{id}}$$

But $v_{id} = v_i$ and $v_{os} \approx 1000 v_i = 1000 v_{id} \Rightarrow v_{id} = \frac{v_{os}}{1000}$

Substituting in the previous expression gives, $$CMRR = \frac{v_{icm}}{\frac{v_{os}}{1000}} = \frac{1000\ v_{icm}}{v_{os}}$$

Make a frequency sweep of V_{icm}, invert the result and multiply by 1000 to get *CMRR*.

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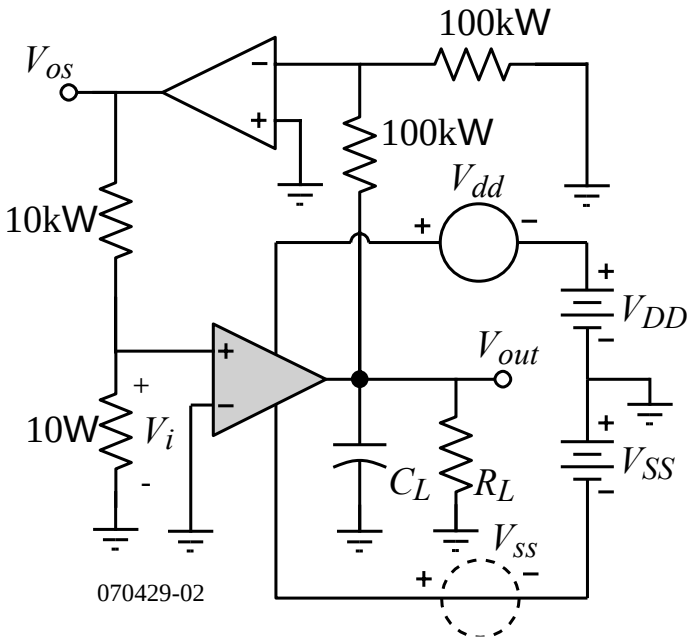
Measurement of *PSRR*

Measurement Configuration:



The definition of the positive power supply rejection ratio is

$$PSRR^+ = \left|\frac{A_{vd}}{A_{dd}}\right| = \frac{(V_{out}/V_{id})}{(V_{out}/V_{dd})}$$

However, in the above circuit the value of V_{out} is the same so that we get

$$PSRR^+ = \frac{V_{dd}}{V_{id}}$$

But $V_{id} = V_i$ and $V_{os} \approx 1000V_i = 1000V_{id}$ $\Rightarrow$ $V_{id} = \frac{V_{os}}{1000}$

Substituting in the previous expression gives, $PSRR^+ = \frac{V_{dd}}{\frac{V_{os}}{1000}} = \frac{1000\ V_{dd}}{V_{os}}$

Make a frequency sweep of V_{dd}, invert the result and multiply by 1000 to get $PSRR^+$.

(Same procedure holds for $PSRR^-$.)

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OTHER OP AMP MEASUREMENTS

Simulation or Measurement of *ICMR*

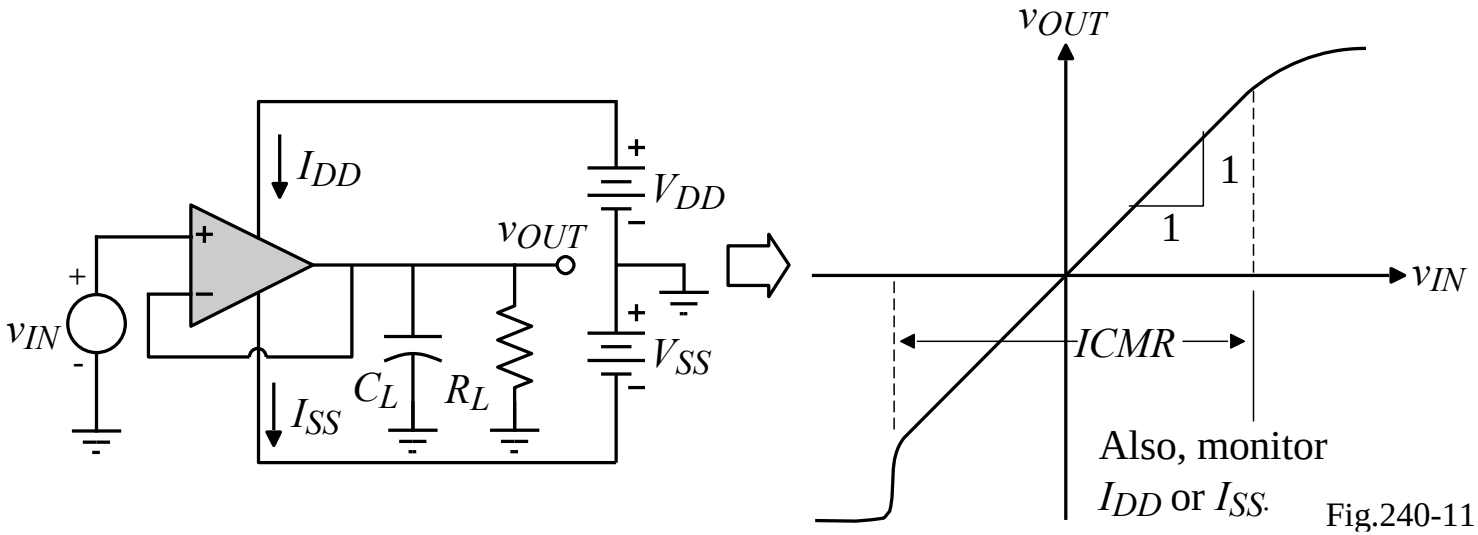

Fig.240-11

Initial jump in sweep is due to the turn-on of M5.

Should also plot the current in the input stage (or the power supply current).

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Measurement or Simulation of Slew Rate and Settling Time

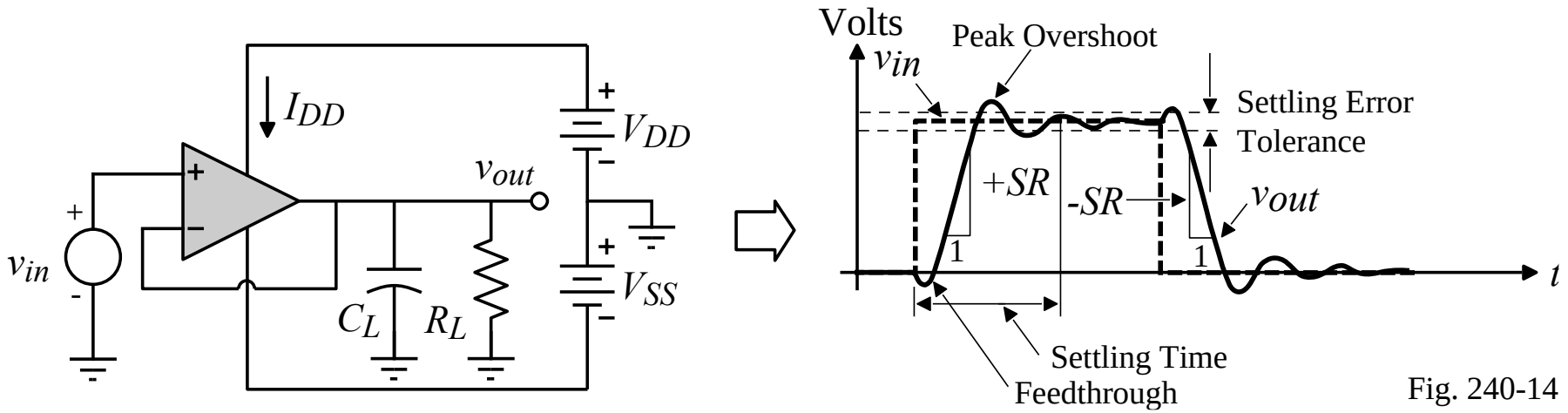

Fig. 240-14

If the slew rate influences the small signal response, then make the input step size small enough to avoid slew rate (i.e. less than 0.5V for MOS).

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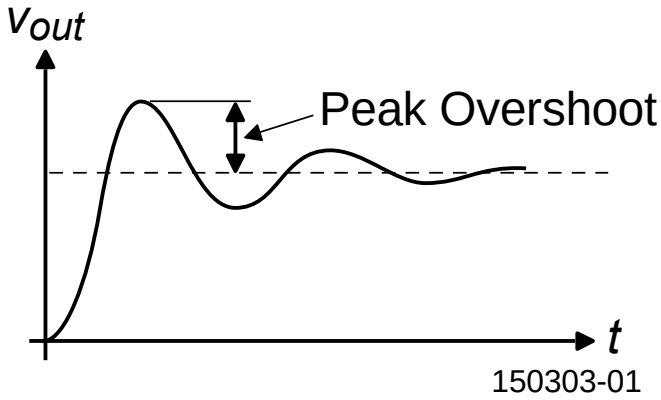
Phase Margin and Peak Overshoot Relationship

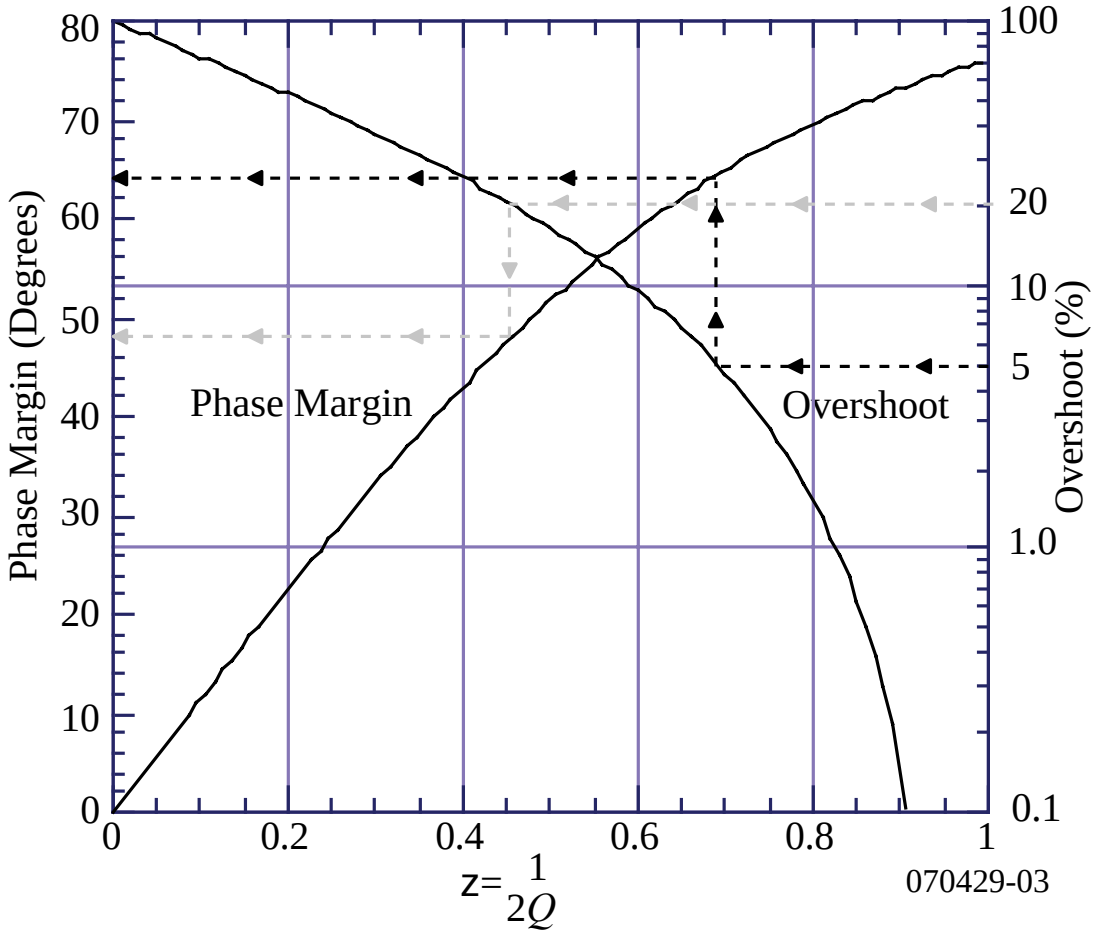
It can be shown (Appendix D of the 3rd edition of text) that:

Phase Margin (Degrees) = $57.2958 cos^{-1}[\sqrt{4\zeta^4+1} - 2\zeta^2]$

Overshoot (%) = $100\ exp\left(\frac{-\pi\zeta}{\sqrt{1-\zeta^2}}\right)$



For example, a 5% overshoot corresponds to a phase margin of approximately 64°.



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SIMULATION OF A TWO-STAGE CMOS OP AMP

Example 25-1 Simulation of a Two-Stage CMOS Op Amp

An op amp designed using the procedure described in Lecture 23 is to be simulated by SPICE. The device parameters to be used are those of Tables 3.1-2 and 3.2-1 of the textbook *CMOS Analog Circuit Design*.

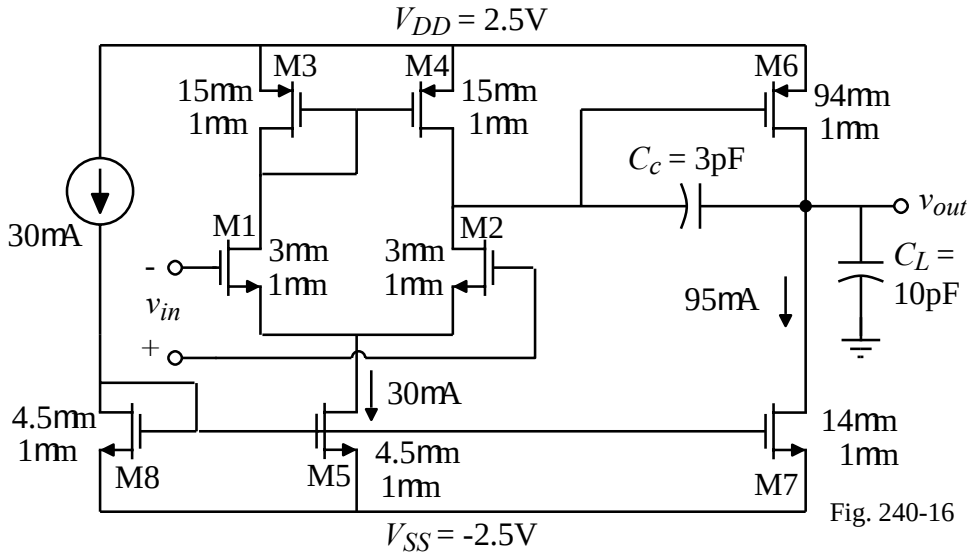

Fig. 240-16

The specifications of this op amp are as follows where the channel length is to be 1μm and the load capacitor is C_L = 10pF:

A_V > 3000V/V	V_{DD} = 2.5V	V_{SS} = -2.5V
GB = 5MHz	SR > 10V/μs	60° phase margin
V_{out} range = ±2V	$ICMR$ = -1 to 2V	$P_{diss} \leq$ 2mW

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Example 25-1 – Continued

Bulk Capacitance Calculation:

If the values of the area and perimeter of the drain and source of each transistor are known, then the simulator will calculate the values of C_{BD} and C_{Bs}. Since there is no layout yet, we estimate the values of the area and perimeter of the drain and source of each transistor as:

$$AS = AD \cong W[L1 + L2 + L3]$$

$$PS = PD \cong 2W + 2[L1 + L2 + L3]$$

where $L1$ is the minimum allowable distance between the polysilicon and a contact in the moat (2µm), $L2$ is the length of a minimum-size square contact to moat (2µm), and $L3$ is the minimum allowable distance between a contact to moat and the edge of the moat (2µm). (These values will be found from the physical design rules for the technology).

For example consider M1:

$$AS = AD = (3\mu m)x(2\mu m+2\mu m+2\mu m) = 18\mu m^2$$

$$PS = PD = 2x3\mu m + 2x6\mu m = 19\mu m$$

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Example 25-1 - Continued

Op Amp Subcircuit:

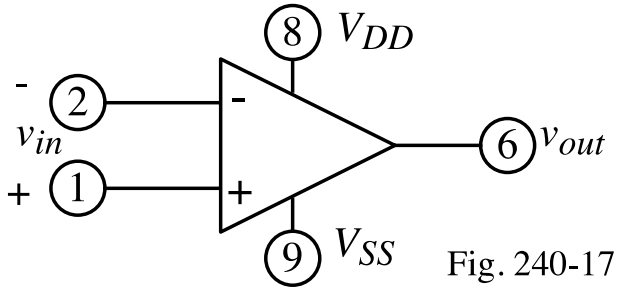

Fig. 240-17

```
.SUBCKT OPAMP 1 2 6 8 9
M1 4 2 3 3 NMOS1 W=3U L=1U AD=18P AS=18P PD=18U PS=18U
M2 5 1 3 3 NMOS1 W=3U L=1U AD=18P AS=18P PD=18U PS=18U
M3 4 4 8 8 PMOS1 W=15U L=1U AD=90P AS=90P PD=42U PS=42U
M4 5 4 8 8 PMOS1 W=15U L=1U AD=90P AS=90P PD=42U PS=42U
M5 3 7 9 9 NMOS1 W=4.5U L=1U AD=27P AS=27P PD=21U PS=21U
M6 6 5 8 8 PMOS1 W=94U L=1U AD=564P AS=564P PD=200U PS=200U
M7 6 7 9 9 NMOS1 W=14U L=1U AD=84P AS=84P PD=40U PS=40U
M8 7 7 9 9 NMOS1 W=4.5U L=1U AD=27P AS=27P PD=21U PS=21U
CC 5 6 3.0P
.MODEL NMOS1 NMOS VTO=0.70 KP=110U GAMMA=0.4 LAMBDA=0.04 PHI=0.7
+MJ=0.5 MJSW=0.38 CGBO=700P CGSO=220P CGDO=220P CJ=770U CJSW=380P
+LD=0.016U TOX=14N
.MODEL PMOS1 PMOS VTO=-0.7 KP=50U GAMMA=0..57 LAMBDA=0.05 PHI=0.8
+MJ=0.5 MJSW=.35 CGBO=700P CGSO=220P CGDO=220P CJ=560U CJSW=350P +LD=0.014U TOX=14N
IBIAS 8 7 30U
.ENDS
```


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Example 25-1 - Continued

PSPICE Input File for the Open-Loop Configuration:

```
EXAMPLE 25-1 OPEN LOOP CONFIGURATION
.OPTION LIMPTS=1000
VIN+ 1 0 DC 0 AC 1.0
VDD 4 0 DC 2.5
VSS 0 5 DC 2.5
VIN - 2 0 DC 0
CL 3 0 10P
X1 1 2 3 4 5 OPAMP
        ⋮
(Subcircuit of previous slide)
        ⋮
.OP
.TF V(3) VIN+
.DC VIN+ -0.005 0.005 100U
.PRINT DC V(3)
.AC DEC 10 1 10MEG
.PRINT AC VDB(3) VP(3)
.PROBE      (This entry is unique to PSPICE)
.END
```


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Example 25-1 - Continued

Open-loop transfer characteristic:

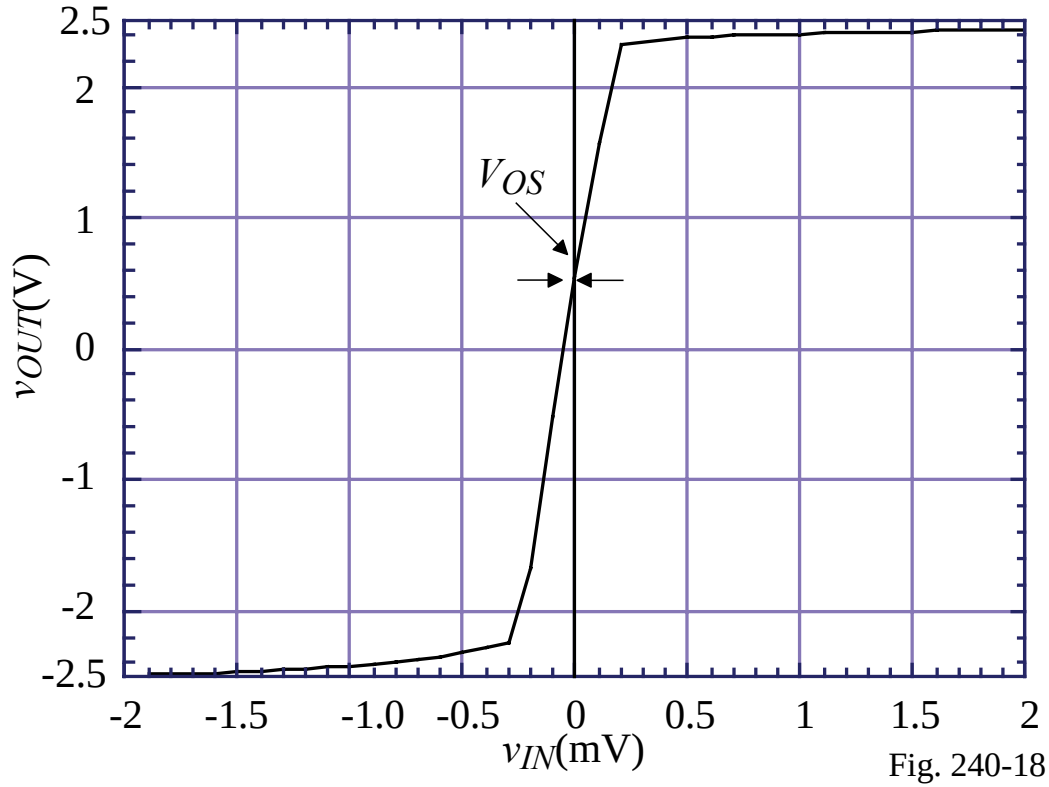

Fig. 240-18

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Example 25-1 - Continued

Open-loop transfer frequency response:

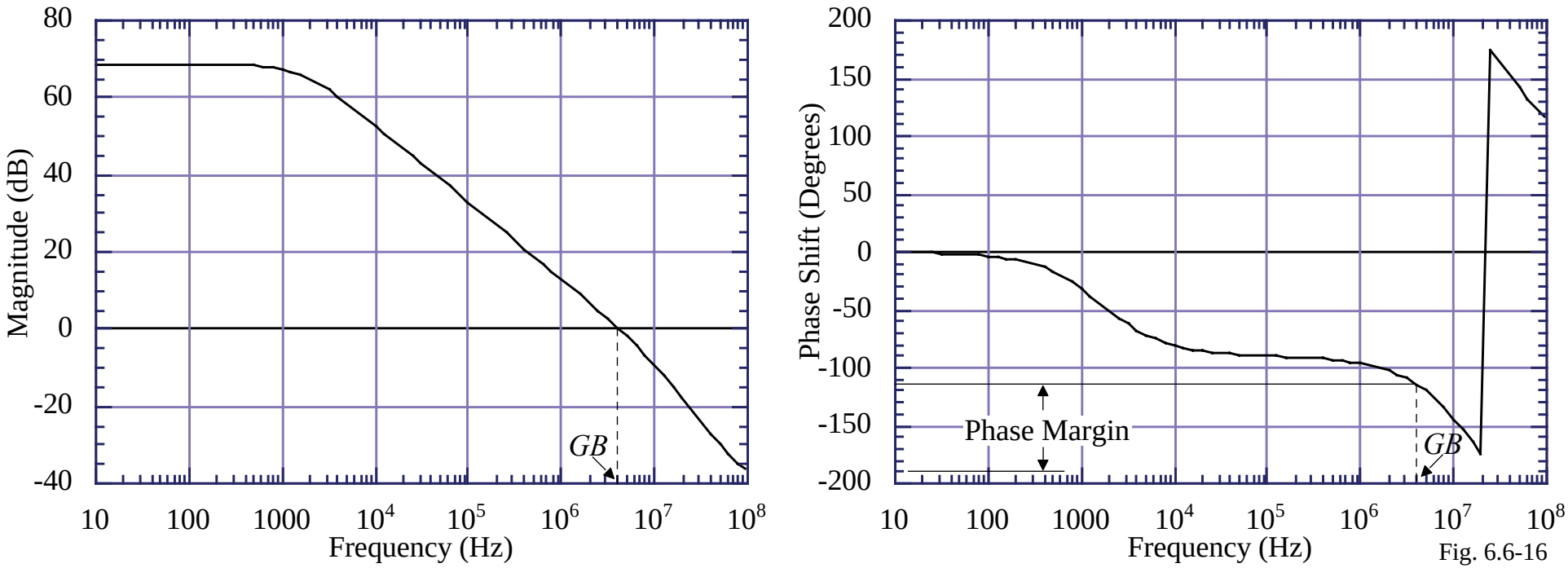

Fig. 6.6-16

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Example 25-1 - Continued

Input common mode range:

```
EXAMPLE 25-1 UNITY GAIN CONFIGURATION.
.OPTION LIMPTS=501
VIN+ 1 0 PWL(0 -2 10N -2 20N 2 2U 2 2.01U -2 4U  -2 4.01U
+ -.1 6U -.1 6.0 1U .1 8U .1 8.01U -.1  10U -.1)
VDD 4 0 DC 2.5 AC 1.0
VSS 0 5 DC 2.5

CL 3 0 20P
X1 1 3 3 4 5 OPAMP
        ⋮
(Subcircuit of Table 6.6-1)
        ⋮
.DC VIN+ -2.5 2.5  0.1
.PRINT DC V(3)
.TRAN 0.05U 10U 0 10N
.PRINT TRAN V(3) V(1)
.AC DEC 10 1 10MEG
.PRINT AC VDB(3) VP(3)
.PROBE   (This entry is unique to PSPICE)
.END
```

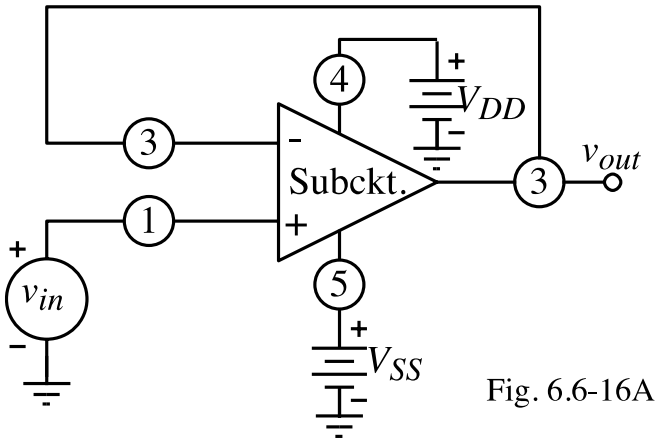

Fig. 6.6-16A

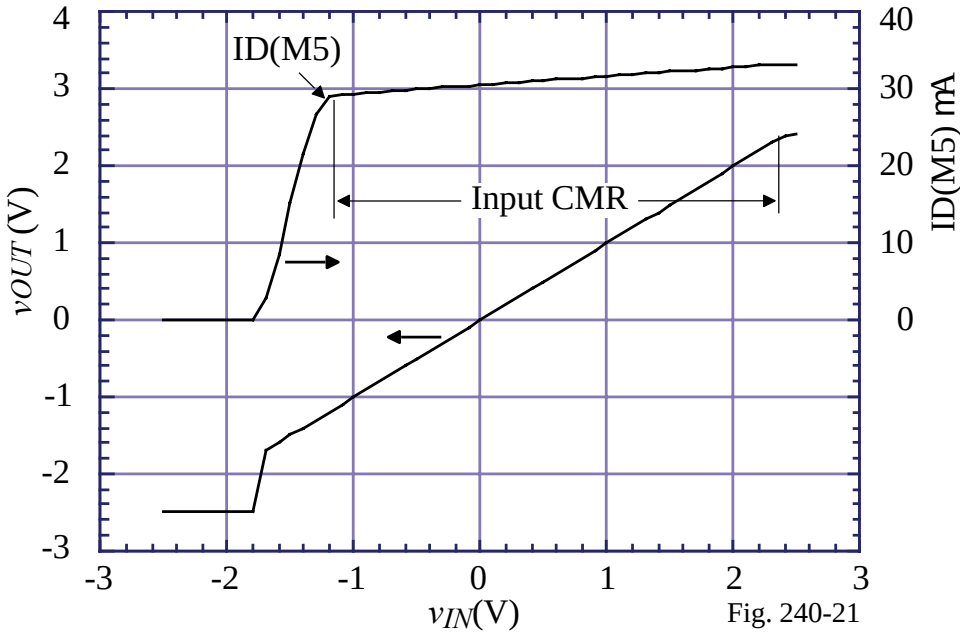

Fig. 240-21

Note the usefulness of monitoring the current in the input stage to determine the lower limit of the *ICMR*.

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Example 25-1 - Continued

Positive *PSRR*:

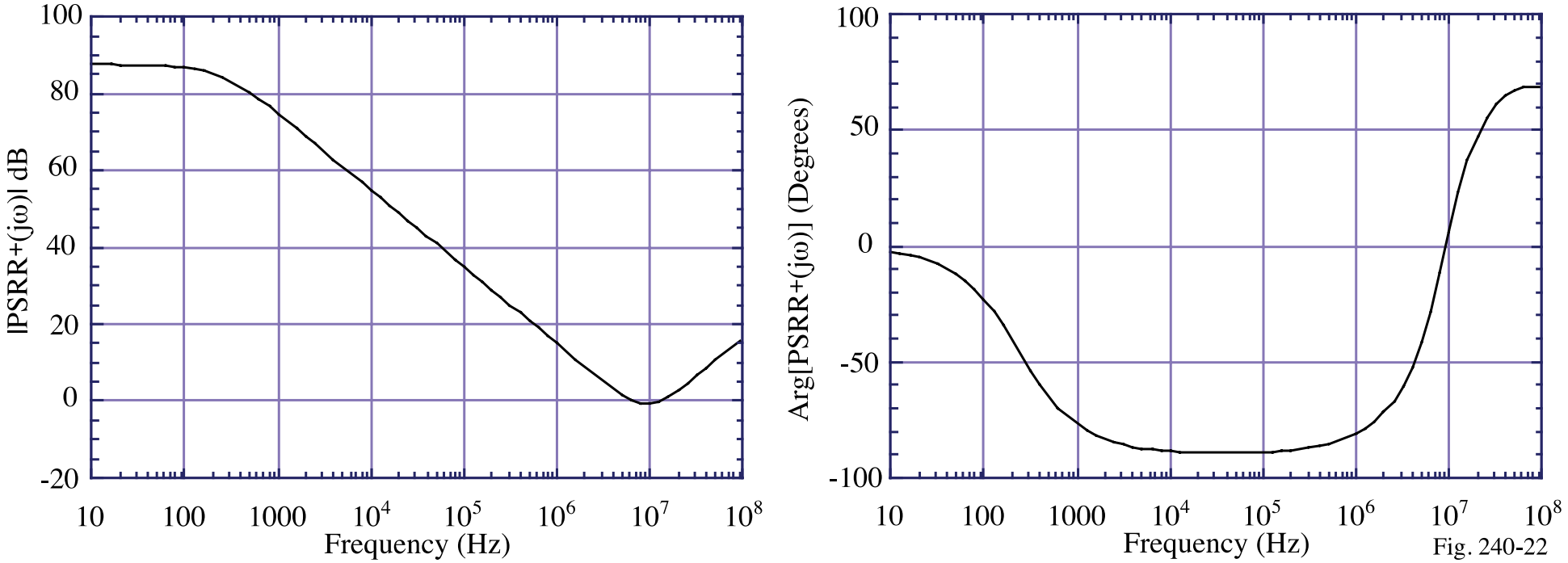

Fig. 240-22

This $PSRR^+$ is poor because of the Miller capacitor. The degree of $PSRR^+$ deterioration will be better shown when compared with the $PSRR^-$.

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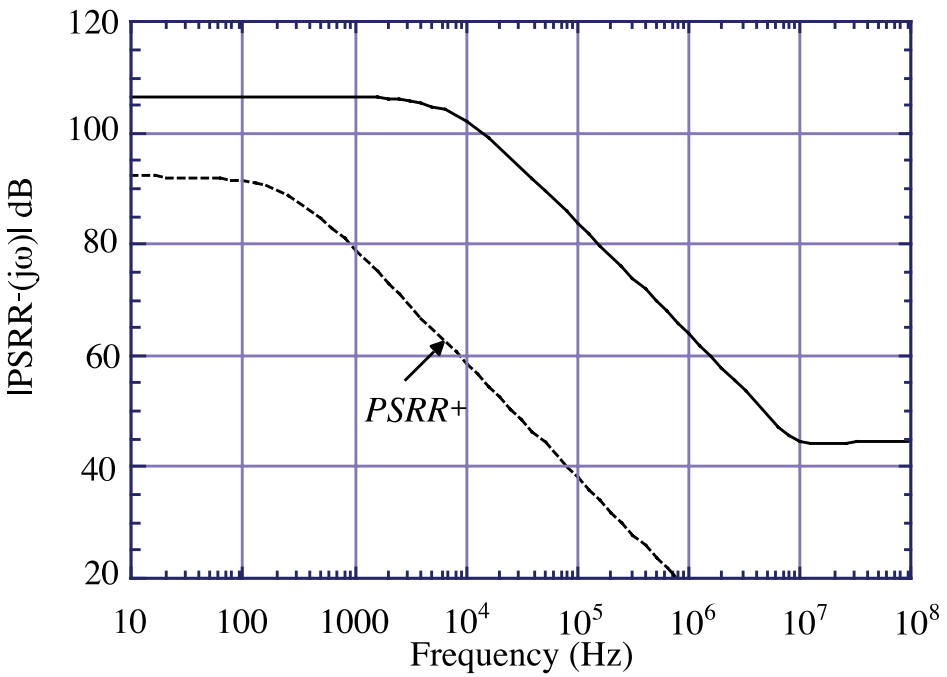
Example 25-1 - Continued

Negative *PSRR*:



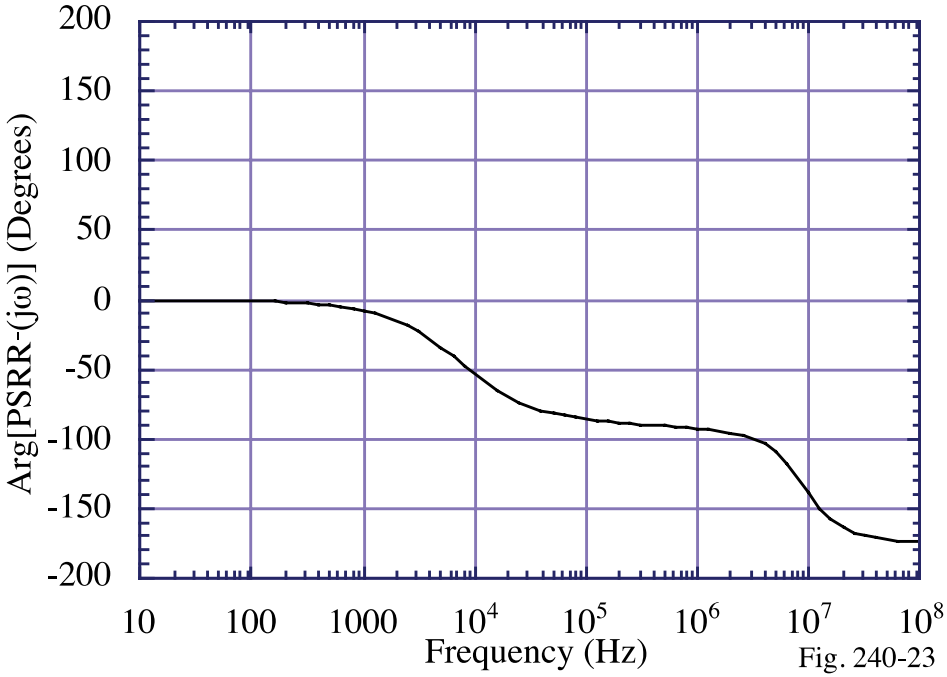


Fig. 240-23

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Example 25-1 - Continued

Large-signal and small-signal transient response:

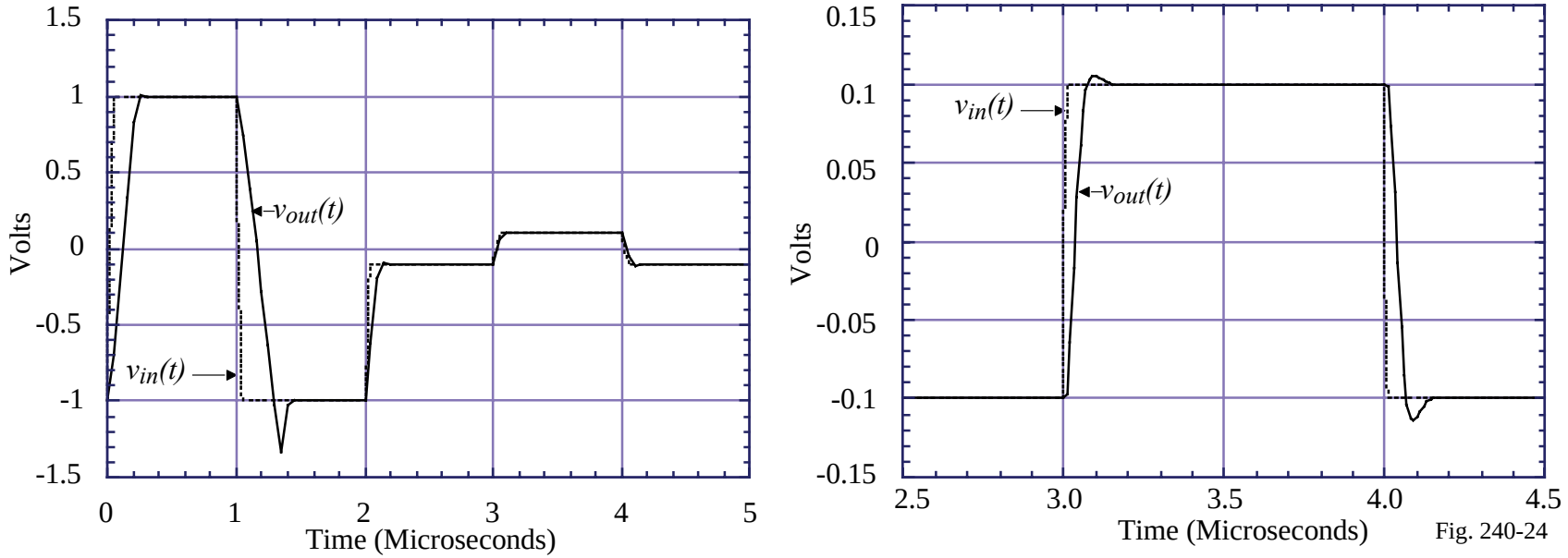

Fig. 240-24

Why the negative overshoot on the slew rate?

If M7 cannot sink sufficient current then the output stage slews and only responds to changes at the output via the feedback path which involves a delay.

Note that $-dv_{out}/dt \approx -2V/0.3\mu s = -6.67V/\mu s$. For a 10pF capacitor this requires 66.7µA and only 95µA-66.7µA = 28µA is available for C_c. For the positive slew rate, M6 can provide whatever current is required by the capacitors and can immediately respond to changes at the output.

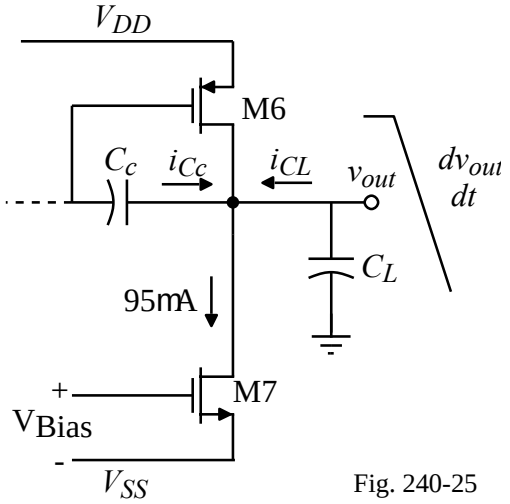

Fig. 240-25

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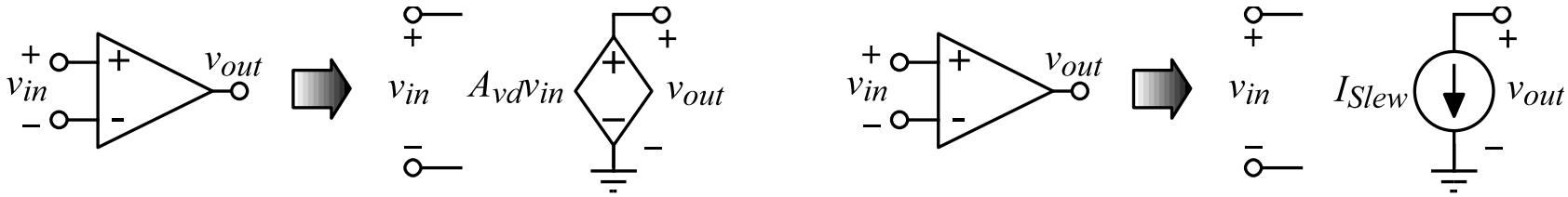
Example 25-1 - Continued

Insight into slewing:

When an op amp slews, the input loses control of the output.

In the above example, the current in M6 is zero and any change in the input of the op amp has no influence on the output current.

Simple op amp models:



Op Amp not Slewing

Op Amp Slewing

120403-01

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Example 25-1 - Continued

Comparison of the Simulation Results with the Specifications of Example 25-1:

Specification (Power supply = ±2.5V)	Design	Simulation
Open Loop Gain	>5000	10,000
GB (MHz)	5 MHz	5 MHz
Input CMR (Volts)	-1V to 2V	-1.2 V to 2.4 V,
Slew Rate (V/µsec)	>10 (V/µsec)	+10, -7(V/µsec)
P_{diss} (mW)	< 2mW	0.625mW
V_{out} range (V)	±2V	+2.3V, -2.2V
$PSRR^+$ (0) (dB)	-	87
$PSRR^-$ (0) (dB)	-	106
Phase margin (degrees)	60°	65°
Output Resistance (kΩ)	-	122.5kΩ

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Relative Overshoots of Ex. 25-1

Why is the negative-going overshoot larger than the positive-going overshoot on the small-signal transient response of a previous slide?

Consider the following circuit and waveform:

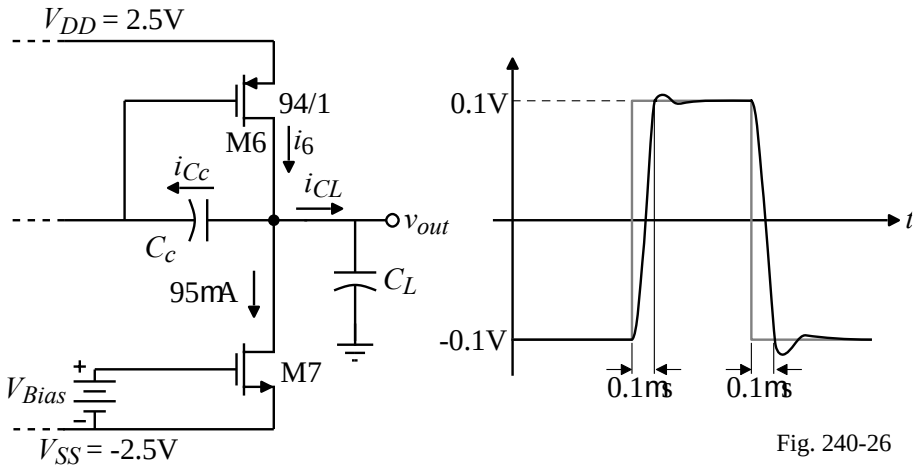

Fig. 240-26

During the rise time,

$i_{CL} = C_L(dv_{out}/dt) = 10\text{pF}(0.2\text{V}/0.1\mu\text{s}) = 20\mu\text{A}$ and $i_{Cc} = 3\text{pf}(2\text{V}/\mu\text{s}) = 6\mu\text{A}$

$\therefore\ i_6 = 95\mu\text{A} + 20\mu\text{A} + 6\mu\text{A} = 121\mu\text{A} \Rightarrow g_{m6} = 1066\mu\text{S}$ (nominal was 942.5μS)

During the fall time, $i_{CL} = C_L(-dv_{out}/dt) = 10\text{pF}(-0.2\text{V}/0.1\mu\text{s}) = -20\mu\text{A}$

and $i_{Cc} = -3\text{pf}(2\text{V}/\mu\text{s}) = -6\mu\text{A}$

$\therefore\ i_6 = 95\mu\text{A} - 20\mu\text{A} - 6\mu\text{A} = 69\mu\text{A} \Rightarrow g_{m6} = 805\mu\text{S}$

The dominant pole is $p_1 \approx (R_I g_{m6} R_{II} C_c)^{-1}$ but the GB is $g_{mI}/C_c = 94.25\mu\text{S}/3\text{pF} = 31.42\text{x}10^6$ rads/sec and stays constant. Thus we must look elsewhere for the reason. Recall that $p_2 \approx g_{m6}/C_L$ which explains the difference.

$\therefore\ p_2(95\mu\text{A}) = 94.25\text{x}10^6$ rads/sec, $p_2(121\mu\text{A}) = 106.6\ \text{x}10^6$ rads/sec, and $p_2(69\mu\text{A}) = 80.05\ \text{x}10^6$ rads/sec. Thus, phase margin is less during the fall time than the rise time.

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SUMMARY

- Simulation and measurement of op amps has both similarities and differences
- Measurement of open loop gain is very challenging – the key is to keep the quiescent point output of the op amp well defined
- The method of stimulating the output of the op amp or power supplies and letting the input respond results in a robust method of measuring open loop gain, *CMRR*, and *PSRR*
- Carefully investigate any deviations or aberrations from expected behavior in the simulation and experimental results
- Be alert for when the small-signal model calculations are influenced by the large signal performance

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