LECTURE 24 – CASCODE OP AMPS

LECTURE ORGANIZATION

Outline

- Lecture Organization
- Single Stage Cascode Op Amps
- Two Stage Cascode Op Amps
- Summary

***CMOS Analog Circuit Design*, 3rd Edition Reference**

Pages 310-328

Cascode Op Amps

Why cascode op amps?

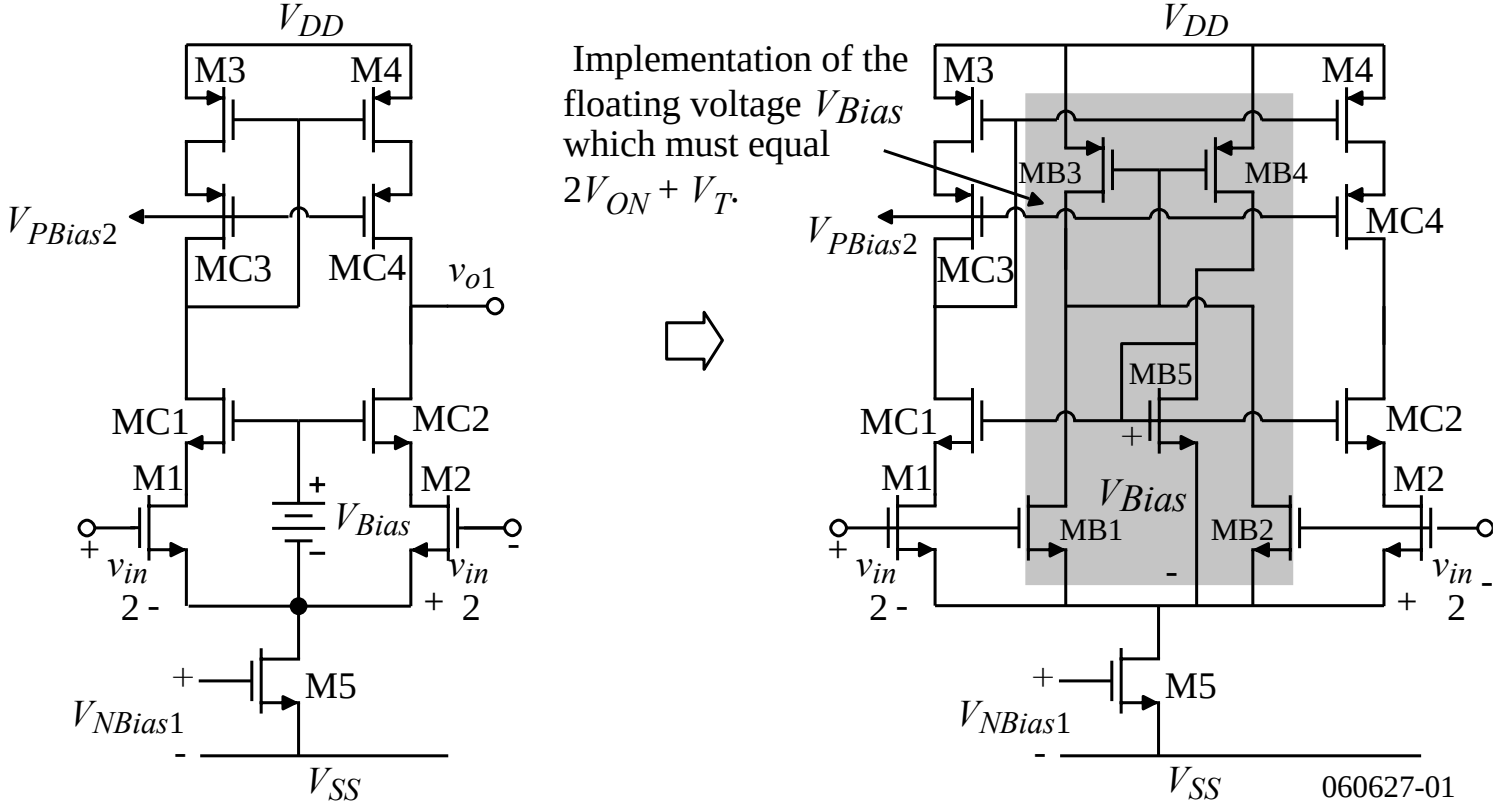
- Control of the frequency behavior
- Can get more gain by increasing the output resistance of a stage
- In the past section, *PSRR* of the two-stage op amp was insufficient for many applications
- A two-stage op amp can become unstable for large load capacitors (if nulling resistor is not used)
- The cascode op amp leads to wider *ICMR* and/or smaller power supply requirements

Where Should the Cascode Technique be Used?

- First stage -
  Good noise performance
  Requires level translation to second stage
  Degrades the Miller compensation
- Second stage -
  Self compensating
  Increases the efficiency of the Miller compensation
  Increases *PSRR*

SINGLE STAGE CASCODE OP AMPS

Simple Single Stage Cascode Op Amp



R_{out} of the first stage is $R_I \approx (g_{mC2}r_{dsC2}r_{ds2})||(g_{mC4}r_{dsC4}r_{ds4})$

Voltage gain = $\frac{v_{o1}}{v_{in}} = g_{m1}R_I$ [The gain is increased by approximately $0.5(g_{MC}r_{dsC})$]

As a single stage op amp, the compensation capacitor becomes the load capacitor.

Example 24-1 Single-Stage, Cascode Op Amp Performance

Assume all W/L ratios are 10 μm/1 μm, and that $I_{DS1} = I_{DS2} =$ 50 μA of single stage op amp. Find the voltage gain of this op amp and the value of C_I if GB = 10 MHz. Use K_N' = 120μA/V^2, K_P' = 25μA/V^2, V_{TN} = 0.5V, V_{TP} = -0.5V, $\lambda_N = 0.06\text{V}^{-1}$ and $\lambda_P = 0.08\text{V}^{-1}$.

Solution

The device transconductances are

$g_{m1} = g_{m2} = g_{mI} = 346.4\ \mu\text{S}$

$g_{mC1} = g_{mC2} = 346.4\mu\text{S}$

$g_{mC3} = g_{mC4} = 158.1\ \mu\text{S}$.

The output resistance of the NMOS and PMOS devices is 0.333 MΩ and 0.25 MΩ, respectively.

$\therefore$ $R_I = 7.86\ \text{M}\Omega$

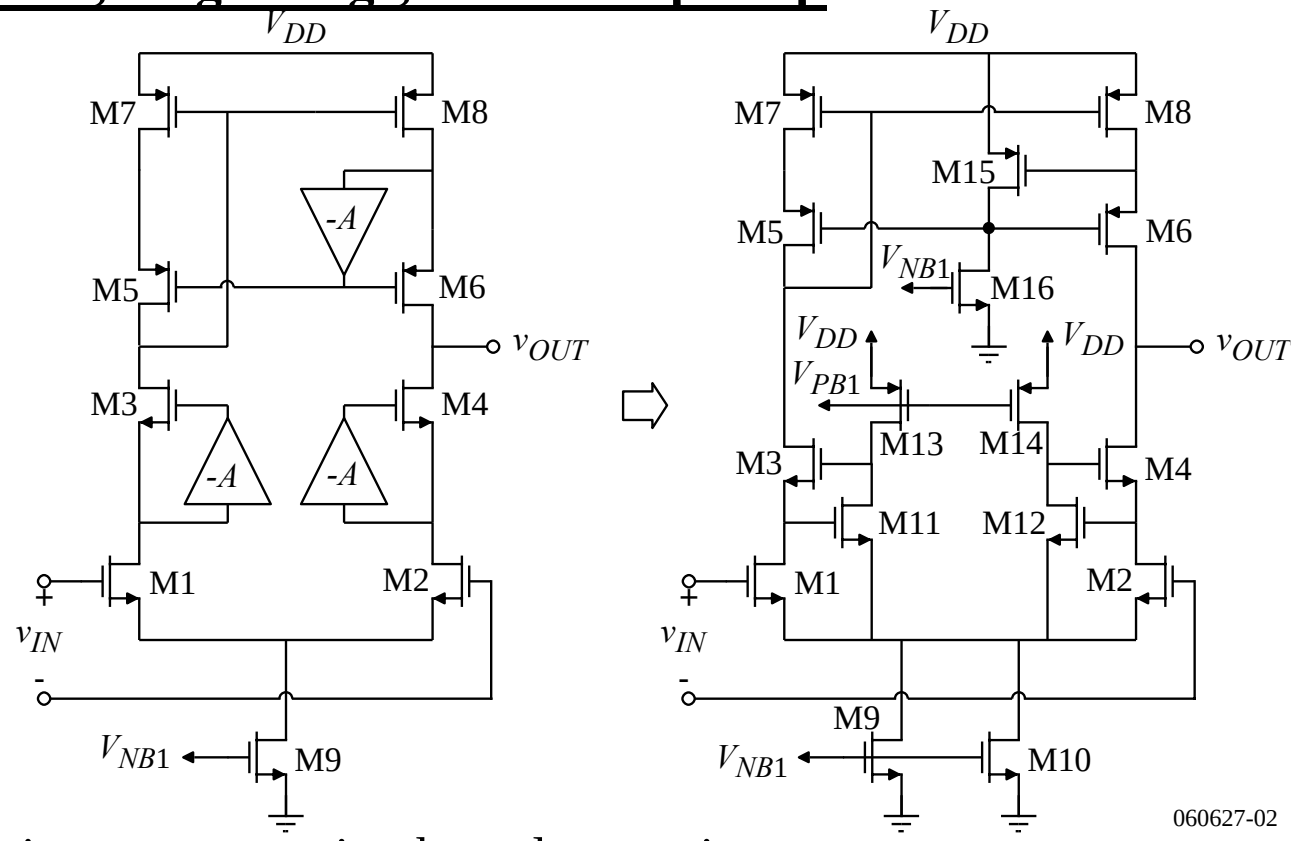
$A_V(0) = 2{,}722$ V/V.

For a unity-gain bandwidth of 10 MHz, the value of C_I is 5.51 pF.

What happens if a 100pF capacitor is attached to this op amp?

GB goes from 10MHz to 0.551MHz.

Enhanced Gain, Single Stage, Cascode Op Amp



From inspection, we can write the voltage gain as,

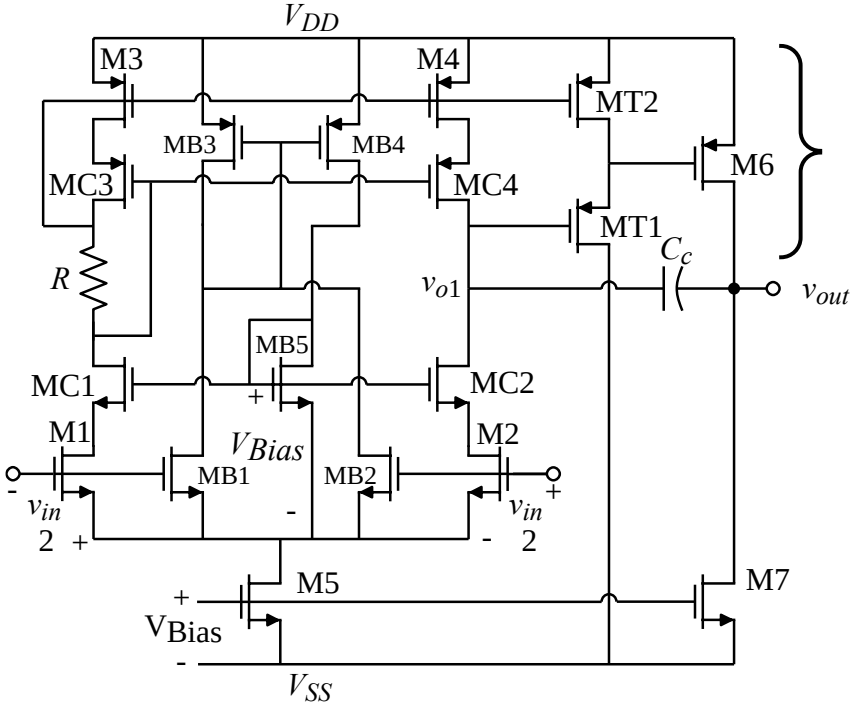
$$A_v = \frac{v_{OUT}}{v_{IN}} = g_{m1}R_{out} \qquad \text{where} \qquad R_{out} = (Ar_{ds6}g_{m6}r_{ds8}) \| (Ar_{ds2}g_{m4}r_{ds4})$$

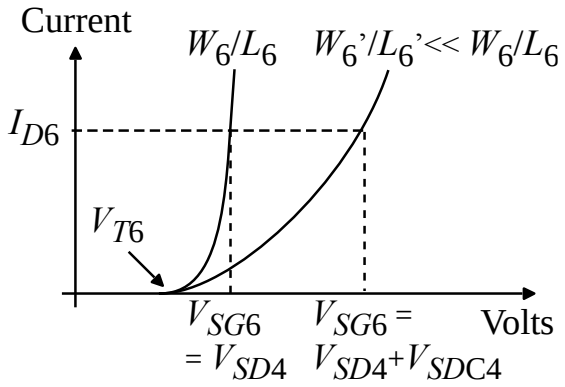
If $r_{dsn} \approx r_{dsp}$, then $A \approx g_m r_{ds}/2$ and the voltage gain would be equal to 100K to 500,K.

Output is not optimized for maximum signal swing.

TWO-STAGE, CASCODE OP AMPS

Two-Stage Op Amp with a Cascoded First-Stage





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- MT1 and MT2 are required for level shifting from the first-stage to the second.
- The $PSRR^+$ is not improved by MT1
- Internal loop pole at the gate of M6 may cause the Miller compensation to fail.
- The voltage gain of this op amp could easily be 100,000V/V

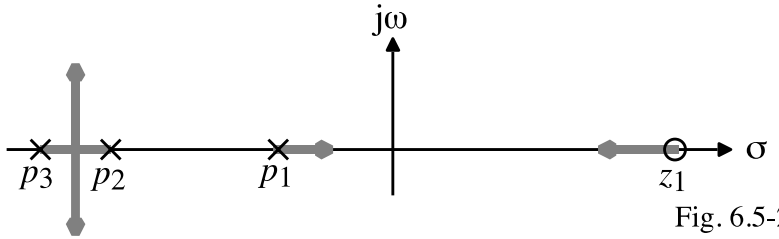


Fig. 6.5-2A

Implementation of Gain in C_c Feedback Loop Using the Previous Amplifier

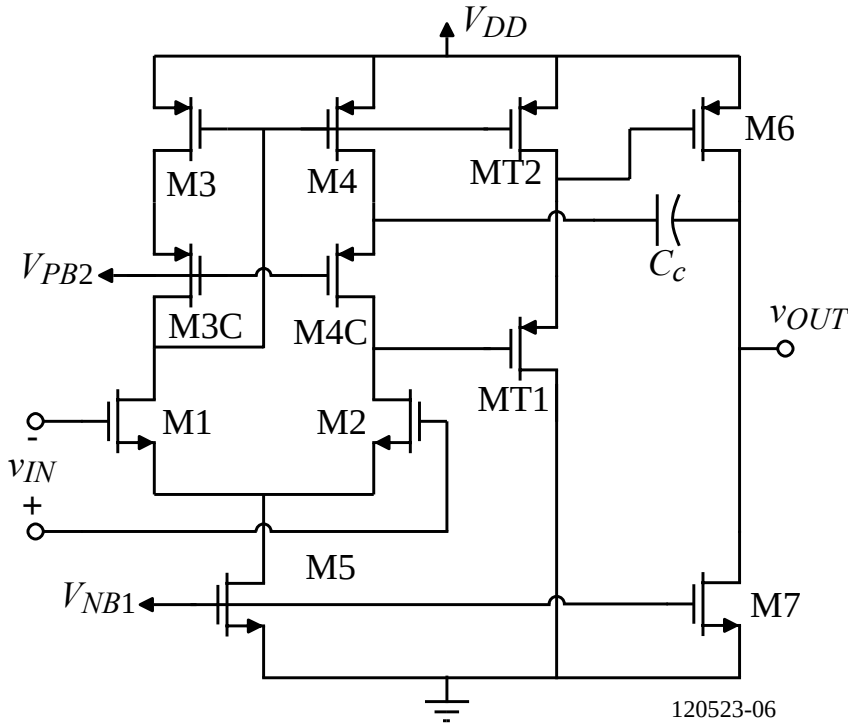
In Lecture 23, we showed that a common-gate amplifier in the compensation feedback prevented feed forward and moved the output pole further away from the origin.

Modifying the previous amplifier:

Connecting C_c to the source of M4C results in two improvements:

1.) MC4 gives gain in the compensation feedback path pushing the output pole further away from the origin.

2.) The compensation capacitor, C_c, is disconnected from the gate of MT1 eliminating the poor PSRR.



Two-Stage Op Amp with a Cascode Second-Stage

$$A_v = g_{mI}g_{mII}R_IR_{II}$$

where $g_{mI} = g_{m1} = g_{m2}$, $g_{mII} = g_{m6}$,

$$R_I = \frac{1}{g_{ds2} + g_{ds4}} = \frac{2}{(\lambda_2 + \lambda_4)I_{D5}}$$

and

$$R_{II} = (g_{mC6}r_{dsC6}r_{ds6})\|(g_{mC7}r_{dsC7}r_{ds7})$$

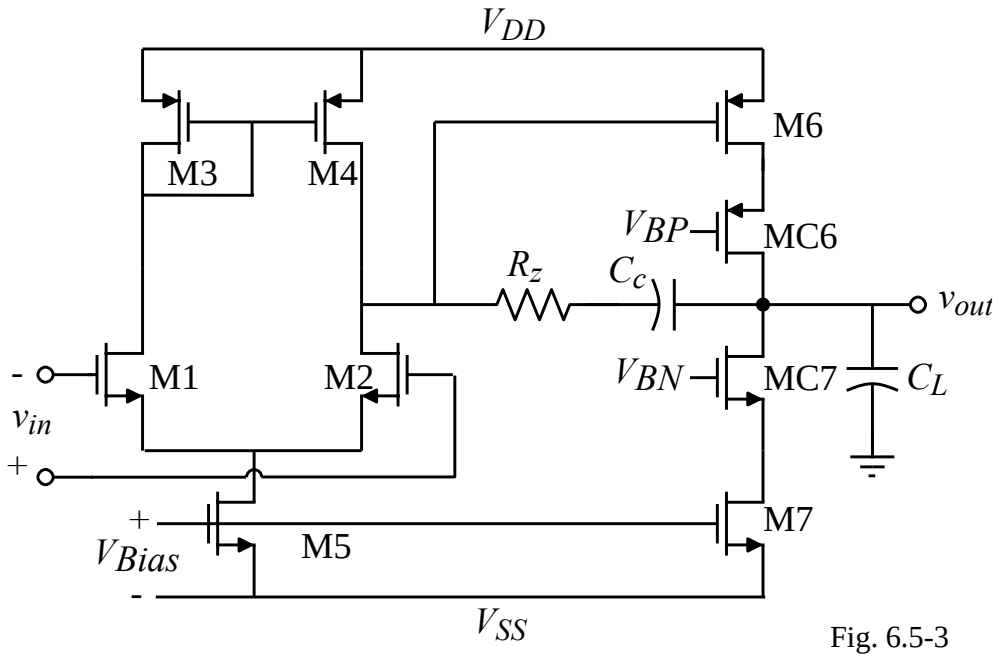
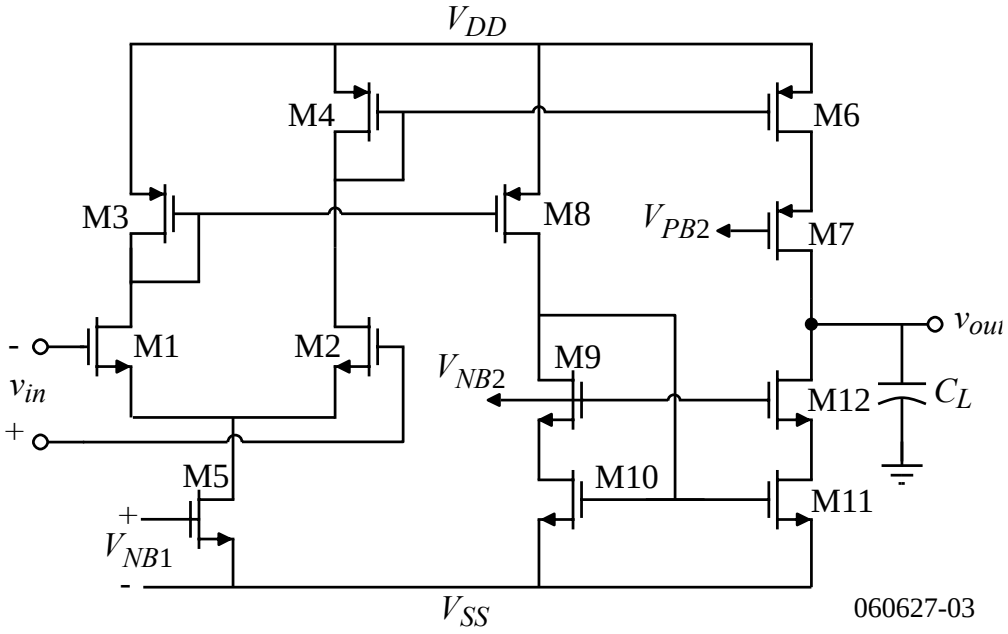


Fig. 6.5-3

Comments:

- The second-stage gain has greatly increased improving the Miller compensation
- The overall gain is approximately $(g_m r_{ds})^3$ if $r_{dsn} >> r_{dsp}$ or if $r_{dsp} >> r_{dsn}$
- Output pole, p_2, is approximately the same if C_c is constant
- The zero RHP is the same if C_c is constant
- PSRR is poor unless the Miller compensation is removed (then the op amp becomes self compensated)

A Balanced, Two-Stage Op Amp using a Cascode Output Stage



$$v_{out} = \left(\frac{g_{m1}g_{m8}}{g_{m3}}\frac{v_{in}}{2} + \frac{g_{m2}g_{m6}}{g_{m4}}\frac{v_{in}}{2}\right)R_{II}$$

$$= \left(\frac{g_{m1}}{2}+\frac{g_{m2}}{2}\right)kv_{in}\,R_{II} = g_{m1}\cdot k\cdot R_{II}$$

where

$R_{II} = (g_{m7}r_{ds7}r_{ds6})\|(g_{m12}r_{ds12}r_{ds11})$

and

$$k = \frac{g_{m8}}{g_{m3}} = \frac{g_{m6}}{g_{m4}}$$

This op amp is balanced because the drain-to-ground loads for M1 and M2 are identical.

TABLE 1 - Design Relationships for Balanced, Cascode Output Stage Op Amp.

Slew rate $= \frac{I_{out}}{C_L}$	$GB = \frac{g_{m1}g_{m8}}{g_{m3}C_L}$	$A_v = \frac{1}{2}\left(\frac{g_{m1}g_{m8}}{g_{m3}} + \frac{g_{m2}g_{m6}}{g_{m4}}\right)R_{II}$
$V_{in}(\max) = V_{DD} - \left[\frac{I_5}{\beta_3}\right]^{1/2} - \lvert V_{TO3}\rvert(\max) + V_{T1}(\min)$		$V_{in}(\min) = V_{SS} + V_{DS5} + \left[\frac{I_5}{\beta_1}\right]^{1/2} + V_{T1}(\min)$

Technological Implications of the Cascode Configuration

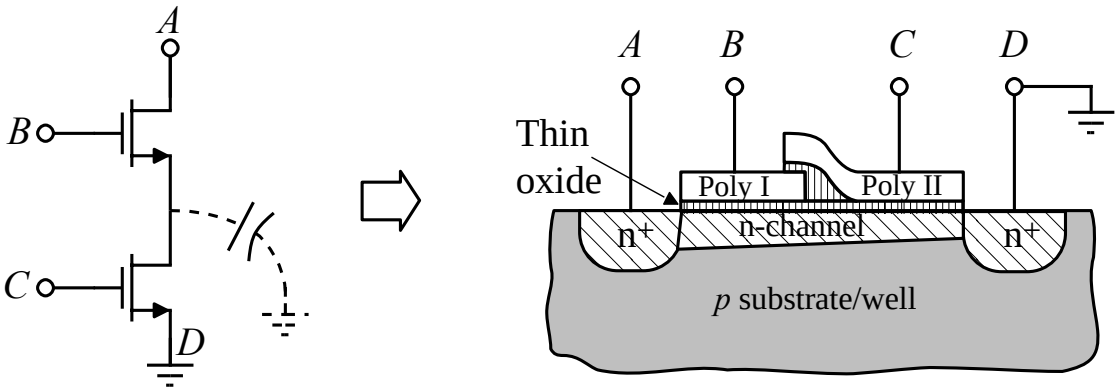


Fig. 6.5-5

If a double poly CMOS process is available, inter-node parasitics can be minimized. As an alternative, one should keep the drain/source between the transistors to a minimum area.

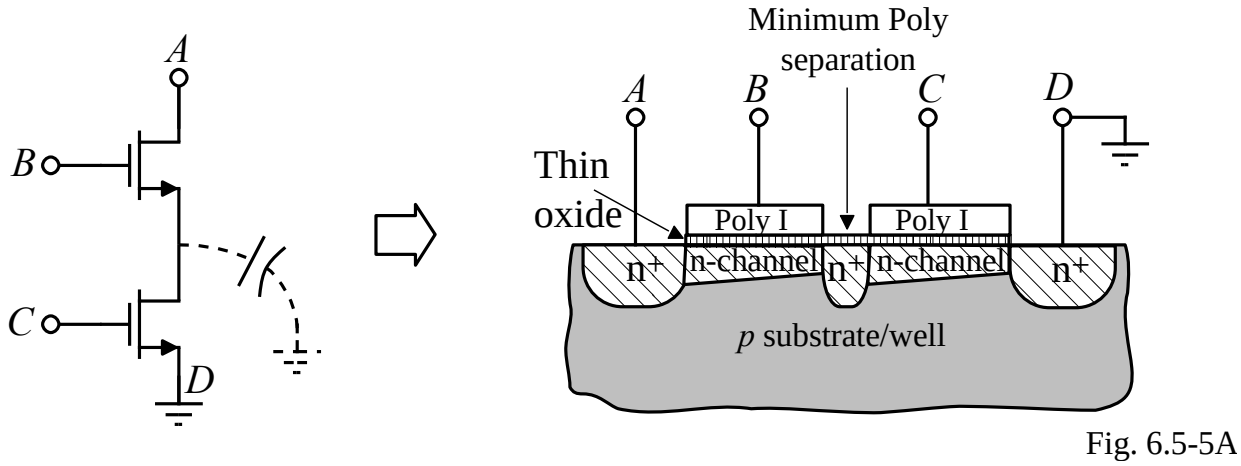
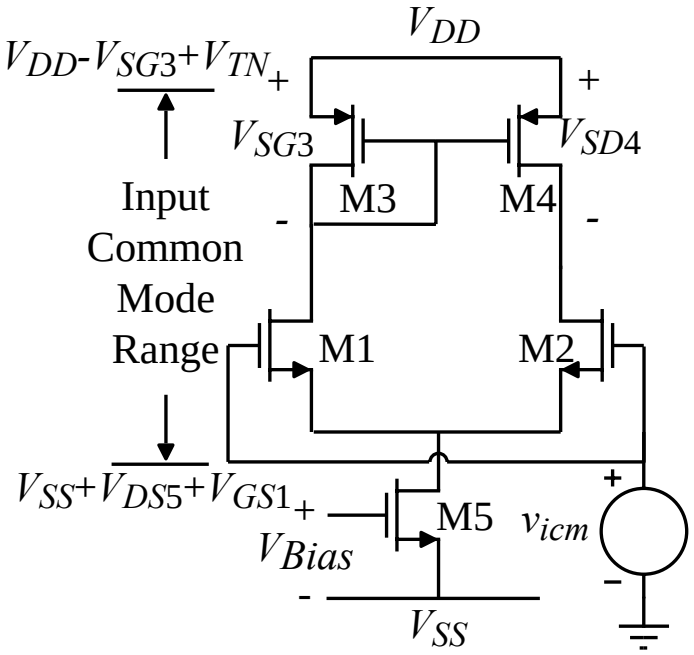
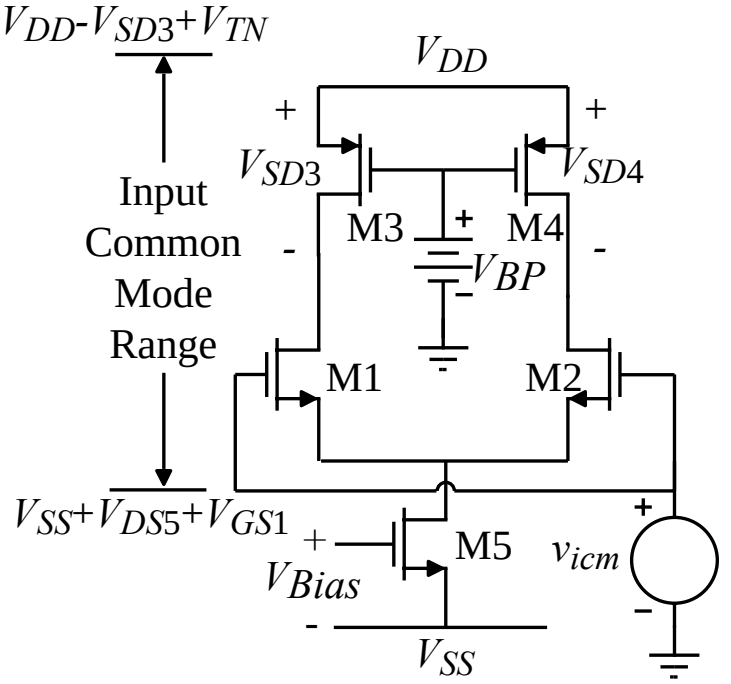


Fig. 6.5-5A

Input Common Mode Range for Two Types of Differential Amplifier Loads



Differential amplifier with a current mirror load.



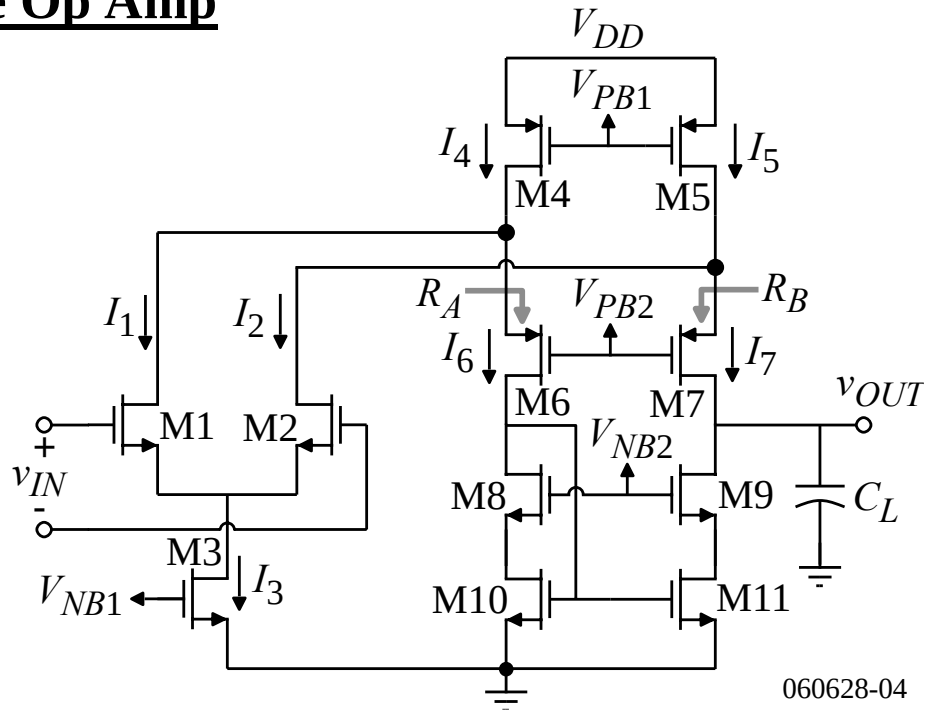
Differential amplifier with current source loads.

Fig. 6.5-6

In order to improve the ICMR, it is desirable to use current source (sink) loads without losing half the gain.

The resulting solution is the *folded* cascode op amp.

The Folded Cascode Op Amp



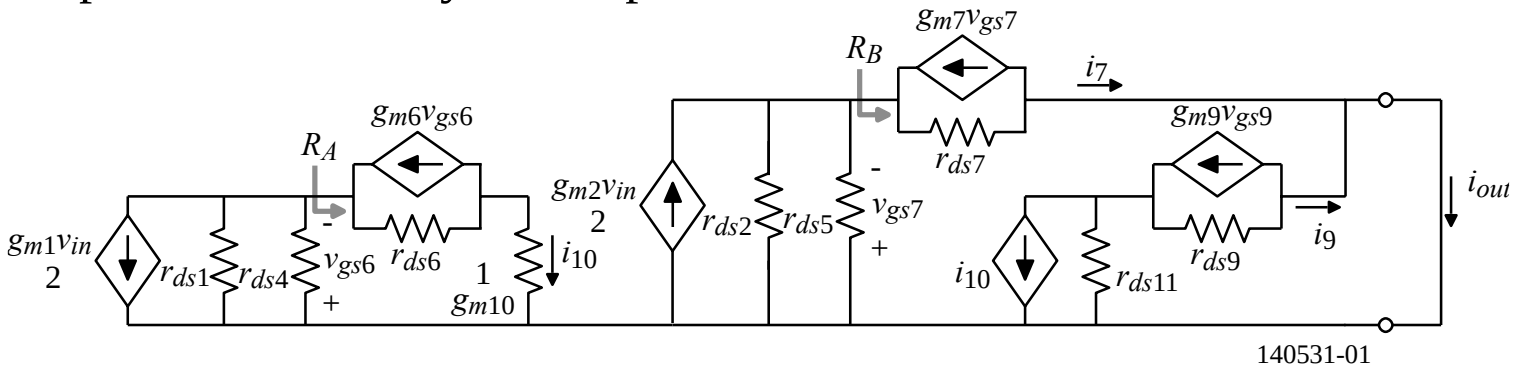
Comments:

- I_4 and I_5, should be designed so that I_6 and I_7 never become zero (i.e. I_4=I_5=1.5I_3)
- This amplifier is nearly balanced (would be exactly if R_A was equal to R_B)
- Self compensating
- Poor noise performance, the gain occurs at the output so all intermediate transistors contribute to the noise along with the input transistors. (Some first stage gain can be achieved if R_A and R_B are greater than g_{m1} or g_{m2}.

Small-Signal Analysis of the Folded Cascode Op Amp

Model:

The easiest way to analyze this amplifier is to first find the short-circuit output current and multiple this current by the output resistance.



With the output short-circuited, $R_A \approx 1/g_{m6}$ and $R_B \approx 1/g_{m7}$. Therefore the currents i_7 and i_9 can be written as,

$$i_7 = \frac{g_{m2}(r_{ds2}\|r_{ds5})v_{in}}{2[R_B + (r_{ds2}\|r_{ds5})]} \approx \frac{g_{m2}v_{in}}{2} \quad \text{and} \quad i_9 \approx -i_{10} = \frac{g_{m1}(r_{ds1}\|r_{ds4})v_{in}}{2[R_A + (r_{ds1}\|r_{ds4})]} \approx \frac{g_{m1}v_{in}}{2}$$

The output resistance with the short-circuit removed is,

$$R_{out} \approx (g_{m9}r_{ds9}r_{ds11})\|[\, g_{m7}r_{ds7}(r_{ds2}\|\, r_{ds5})]$$

Finally,

$$v_{out} = (i_7 + i_9)R_{out} = \left(\frac{g_{m1}v_{in}}{2} + \frac{g_{m2}v_{in}}{2}\right)R_{out} = g_{m1}R_{out} = g_{m2}R_{out}$$

Intuitive Analysis of the Folded Cascode Op Amp

Assume that a voltage of ΔV is applied. We know that

$$R_A(\text{M6}) \approx 1/g_{m6} \text{ and } R_B(\text{M7}) \approx 1/g_{m7}$$

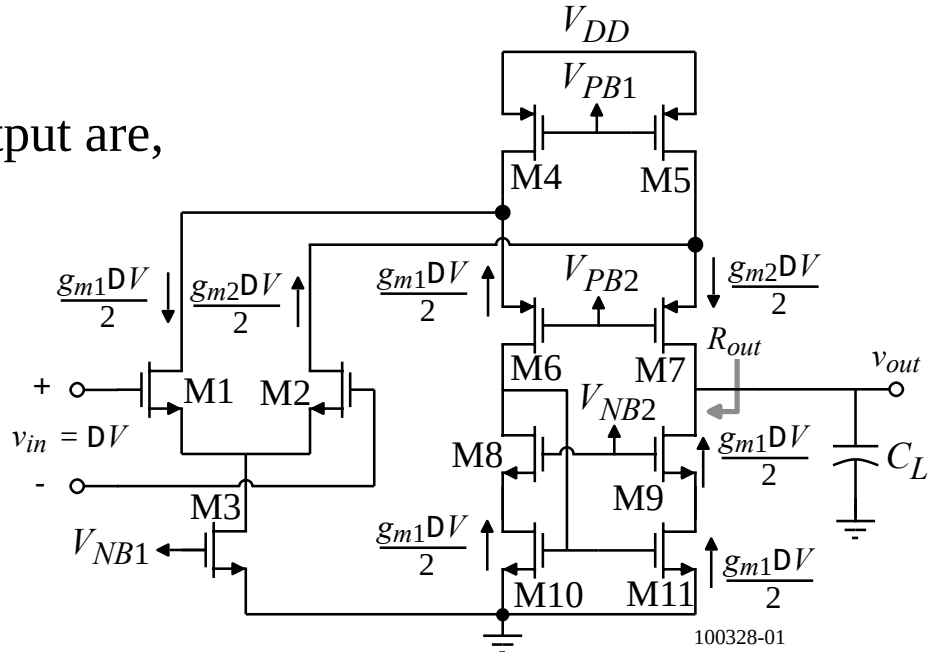
The currents flowing to the short-circuited output are,

$$\frac{g_{m1}\Delta V}{2} + \frac{g_{m2}\Delta V}{2}$$

The output resistance is approximately,

$$R_{out} \approx (g_{m9}r_{ds9}r_{ds11}) \| [\, g_{m7}r_{ds7}(r_{ds2} \| r_{ds5})]$$

$$\approx \left(\frac{g_m r_{ds}^2}{3}\right) \text{ if } r_{dsn} \approx r_{dsp}$$



Therefore, the approximate voltage gain is,

$$\frac{v_{out}}{v_{in}} = \left(\frac{g_{m1}}{2} + \frac{g_{m2}}{2}\right) R_{out} \approx g_m R_{out} = \left(\frac{g_m^2 r_{ds}^2}{3}\right)$$

The GB is,

$$GB = \frac{A_v(0)}{|p_1|} = \frac{g_m R_{out}}{|R_{out} C_L|} = \frac{g_m}{C_L}$$

Frequency Response of the Folded Cascode Op Amp

The frequency response of the folded cascode op amp is determined primarily by the output pole which is given as

$$p_{out} = \frac{-1}{R_{out}C_{out}}$$

where C_{out} is the capacitance connected from the output to ground.

All other poles must be greater than $GB = g_{m1}/C_{out}$.

The approximate expressions for each pole is (ignoring C_{gd}):

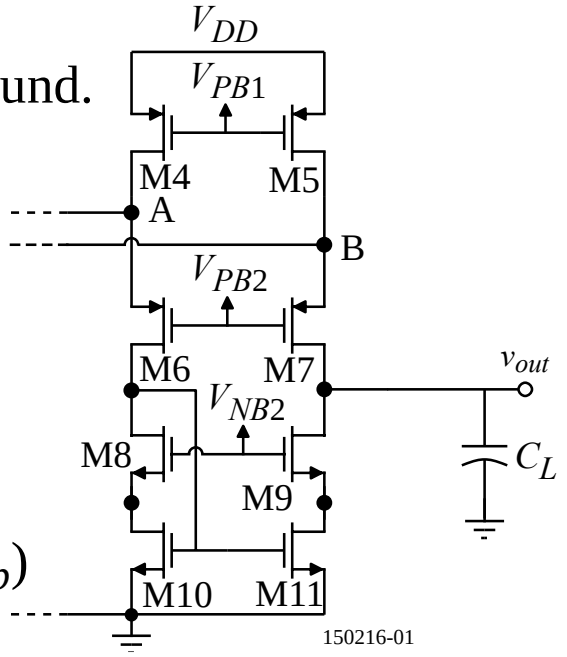
1.) Pole at node A: $p_A \approx - g_{m6}/(C_{gs}+ 2C_{db})$

2.) Pole at node B: $p_B \approx - g_{m7}/(C_{gs}+ 2C_{db})$

3.) Pole at drain of M6: $p_6 \approx -g_{m10}/(2C_{gs}+ 2C_{db})$

4.) Pole at source of M8: $p_8 \approx -(g_{m8}r_{ds8}g_{m10})/(C_{gs}+ C_{db})$

5.) Pole at source of M9: $p_9 \approx -g_{m9}/(C_{gs}+ C_{db})$



where the approximate expressions are found by the reciprocal product of the resistance and parasitic capacitance seen to ground from a given node. One might feel that because R_B is approximately r_{ds} that this pole also might be small. However, at frequencies where this pole has influence, C_{out}, causes R_{out} to be much smaller making p_B also non-dominant.

Example 24-3 - Folded Cascode, CMOS Op Amp

Assume that all $g_{mN} = g_{mP} = 100\mu S$, $r_{dsN} = 2M\Omega$, $r_{dsP} = 1M\Omega$, and $C_L = 10pF$. Find all of the small-signal performance values for the folded-cascode op amp.

$$R_{out} = (g_{m9}r_{ds9}r_{ds11})\|[g_{m7}r_{ds7}(r_{ds5}\|r_{ds2})] = 400M\Omega\|[(100)(0.667M\Omega)] = 57.143M\Omega$$

$$\frac{v_{out}}{v_{in}} = g_{mN}R_{out} = (100)(57.143) = 5{,}714.3 \text{ V/V}$$

$$|p_{out}| = \frac{1}{R_{out}C_{out}} = \frac{1}{57.143M\Omega \cdot 10pF} = 1{,}750 \text{ rads/sec.} \Rightarrow 278Hz \Rightarrow GB = 1.21MHz$$

PSRR of the Folded Cascode Op Amp

Consider the following circuit used to model the $PSRR^-$:

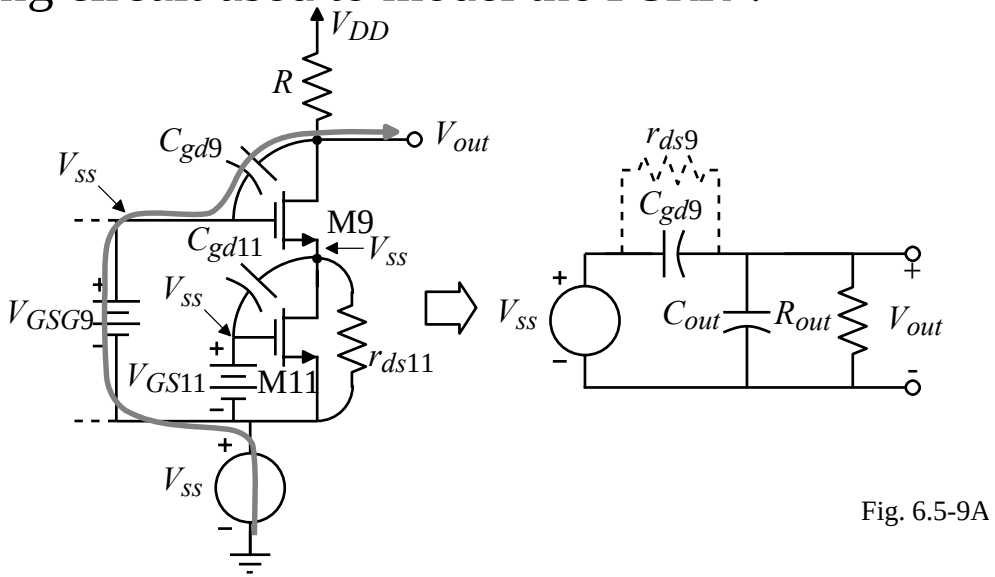


Fig. 6.5-9A

This model assumes that gate, source and drain of M11 and the gate and source of M9 all vary with V_{SS}.

We shall examine V_{out}/V_{ss} rather than $PSRR^-$. (Small V_{out}/V_{ss} will lead to large $PSRR^-$.)

The transfer function of V_{out}/V_{ss} can be found as

$$\frac{V_{out}}{V_{ss}} \approx \frac{sC_{gd}9R_{out}}{sC_{out}R_{out}+1} \quad \text{for } C_{gd}9 < C_{out}$$

The approximate $PSRR^-$ is sketched on the next page.

Frequency Response of the PSRR- of the Folded Cascode Op Amp

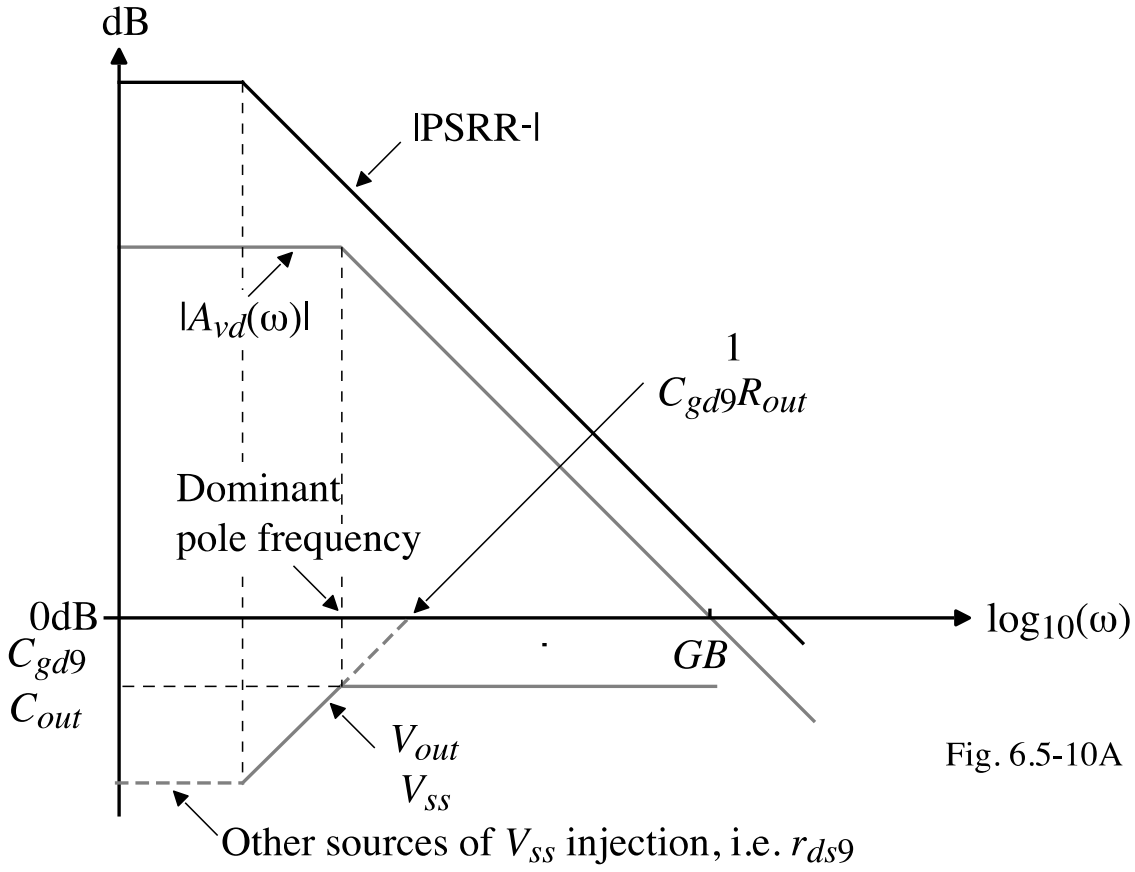


Fig. 6.5-10A

We see that the PSRR of the cascode op amp is much better than the two-stage op amp without any modifications to improve the PSRR.

Design Approach for the Folded-Cascode Op Amp

Step	Relationship	Design Equation/Constraint	Comments
1	Slew Rate	$I_3 = SR \cdot C_L$	
2	Bias currents in output cascodes	$I_4 = I_5 = 1.2I_3$ to $1.5I_3$	Avoid zero current in cascodes
3	Maximum output voltage, v_{out}(max)	$S_5=\frac{2I_5}{K_P' V_{SD5}^2}$, $S_7=\frac{2I_7}{K_P' V_{SD7}^2}$, ($S_4=S_5$ and $S_6=S_7$)	V_{SD5}(sat)=V_{SD7}(sat) = 0.5[V_{DD}-V_{out}(max)]
4	Minimum output voltage, v_{out}(min)	$S_{11}=\frac{2I_{11}}{K_N' V_{DS11}^2}$, $S_9=\frac{2I_9}{K_N' V_{DS9}^2}$, ($S_{10}=S_{11}$ and $S_8=S_9$)	V_{DS9}(sat)=V_{DS11}(sat) = 0.5[V_{out}(min)-V_{SS}]
5	$GB = \frac{g_{m1}}{C_L}$	$S_1=S_2=\frac{g_{m1}^2}{K_N' I_3}=\frac{GB^2 C_L^2}{K_N' I_3}$	
6	Minimum input CM	$S_3 = \frac{2I_3}{K_N'\left(V_{in}(\min)-V_{SS}-\sqrt{(I_3/K_N' S_1)}-V_{T1}\right)^2}$	
7	Maximum input CM	$S_4 = S_5 = \frac{2I_4}{K_P'\left(V_{DD}-V_{in}(\max)+V_{T1}\right)}^2$	S_4 and S_5 must meet or exceed value in step 3
8	Differential Voltage Gain	$\frac{v_{out}}{v_{in}} = \left(\frac{g_{m1}}{2}+\frac{g_{m2}}{2}\right)R_{out} = g_{mI}R_{out}$	
9	Power dissipation	$P_{diss} = (V_{DD}-V_{SS})(I_3+I_{10}+I_{11})$	

Example 24-4 Design of a Folded-Cascode Op Amp

Design a folded-cascode op amp if the slew rate is 10V/μs, the load capacitor is 10pF, the maximum and minimum output voltages are 2V and 0.5V for a 2.5V power supply, the *GB* is 10MHz, the minimum input common mode voltage is +1V and the maximum input common mode voltage is 2.5V. The differential voltage gain should be greater than 3,000V/V and the power dissipation should be less than 5mW. Use K_N'=120μA/V^2, K_P'= 25μA/V^2, $V_{TN} = |V_{TP}| = 0.5$V, $\lambda_N = 0.06\text{V}^{-1}$, and $\lambda_P = 0.08\text{V}^{-1}$. Let $L = 0.5\ \mu$m.

Solution

Following the approach outlined above, $I_3 = SR \cdot C_L = 10\text{x}10^6 \cdot 10^{-11} = 100\mu\text{A}$.

Select $I_4 = I_5 = 125\mu\text{A}$.

Next, we see that the value of $0.5(V_{DD}\text{-}V_{out}(\text{max}))$ is 0.5V/2 or 0.25V. Thus,

$$S_4 = S_5 = \frac{2 \cdot 125\mu\text{A}}{25\mu\text{A/V}^2 \cdot (0.25\text{V})^2} = \frac{2 \cdot 125 \cdot 16}{25} = 160$$

and assuming worst case currents in M6 and M7 gives,

$$S_6 = S_7 = \frac{2 \cdot 125\mu\text{A}}{25\mu\text{A/V}^2 (0.25\text{V})^2} = \frac{2 \cdot 125 \cdot 16}{25} = 160$$

The value of $0.5(V_{out}(\text{min})\text{-}|V_{SS}|)$ is 0.25V which gives the value of S_8, S_9, S_{10} and S_{11} as

$$S_8 = S_9 = S_{10} = S_{11} = \frac{2 \cdot I_8}{K_N' V_{DS8}^2} = \frac{2 \cdot 125}{120 \cdot (0.25)^2} = 20$$

Example 24-4 - Continued

In step 5, the value of GB gives S_1 and S_2 as

$$S_1 = S_2 = \frac{GB^2 \cdot C_L^2}{K_N' I_3} = \frac{(20\pi \text{x} 10^6)^2 (10^{-11})^2}{120\text{x}10^{-6} \cdot 100\text{x}10^{-6}} = 32.9 \approx 33$$

The minimum input common mode voltage defines S_3 as

$$S_3 = \frac{2I_3}{K_N'\left(V_{in}(\text{min}) - V_{SS} - \sqrt{\frac{I_3}{K_N' S_1}} - V_{T1}\right)^2} = \frac{200\text{x}10^{-6}}{120\text{x}10^{-6}\left(1.0+0-\sqrt{\frac{100}{120 \cdot 33}} - 0.5\right)^2} \approx 15$$

We need to check that the values of S_4 and S_5 are large enough to satisfy the maximum input common mode voltage. The maximum input common mode voltage of 2.5 requires

$$S_4 = S_5 \geq \frac{2I_4}{K_P'[V_{DD} - V_{in}(\text{max}) + V_{T1}]^2} = \frac{2 \cdot 125\mu\text{A}}{25\mu\text{A/V}^2[0.5\text{V}]^2} = 40$$

which is less than 160. In fact, with $S_4 = S_5 = 160$, the maximum input common mode voltage is 2.75V.

The power dissipation is found to be

$$P_{diss} = 2.5\text{V}(125\mu\text{A}+125\mu\text{A}) = 0.625\text{mW}$$

Example 24-4 - Continued

The small-signal voltage gain requires the following values to evaluate:

S_4, S_5: $g_m = \sqrt{2\cdot 125\cdot 25\cdot 160} = 1000\mu S$ and $g_{ds} = 125x10^{-6}\cdot 0.08 = 10\mu S$

S_6, S_7: $g_m = \sqrt{2\cdot 75\cdot 25\cdot 160} = 774.6\mu S$ and $g_{ds} = 75x10^{-6}\cdot 0.08 = 6\mu S$

S_8, S_9, S_{10}, S_{11}: $g_m = \sqrt{2\cdot 75\cdot 120\cdot 20} = 600\mu S$ and $g_{ds} = 75x10^{-6}\cdot 0.06 = 4.5\mu S$

S_1, S_2: $g_{mI} = \sqrt{2\cdot 50\cdot 120\cdot 33} = 629\mu S$ and $g_{ds} = 50x10^{-6}(0.06) = 3\mu S$

Thus,

$$R_{II} \approx g_{m9}r_{ds9}r_{ds11} = (600\mu S)\left(\frac{1}{4.5\mu S}\right)\left(\frac{1}{4.5\mu S}\right) = 29.63M\Omega$$

$$R_{out} \approx 29.63M\Omega \| (774.6\mu S)\left(\frac{1}{6\mu S}\right)\left(\frac{1}{10\mu S+3\mu S}\right) = 7.44M\Omega$$

The small-signal, differential-input, voltage gain is

$$A_{vd} = g_{mI}R_{out} = (629)(7.44) = 4{,}680 \text{ V/V}$$

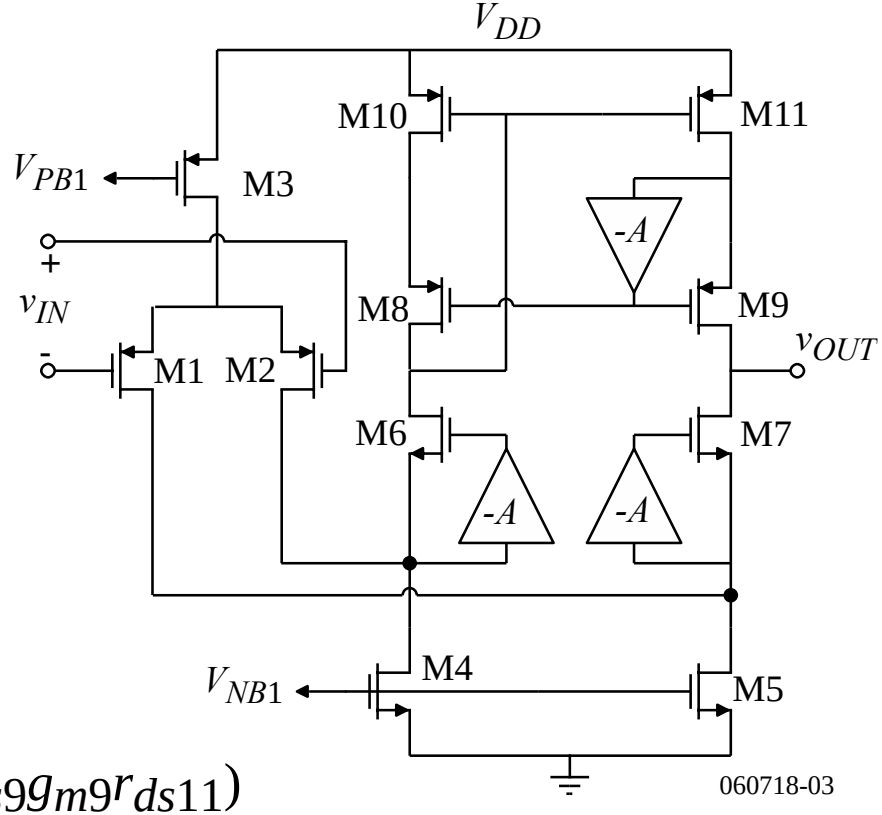
The gain is slightly larger than the specified 3,000 V/V.

Comments on Folded Cascode Op Amps

- Good PSRR
- Good ICMR
- Self compensated
- Can cascade an output stage to get extremely high gain with lower output resistance (use Miller compensation in this case)
- Need first stage gain for good noise performance
- Widely used in telecommunication circuits where large dynamic range is required

Enhanced-Gain, Folded Cascode Op Amps

If more gain is needed, the folded cascode op amp can be enhanced to boost the output impedance even higher as follows.



Voltage gain = $g_{m1}R_{out}$,

where

$$R_{out} \approx [Ar_{ds7}g_{m7}(r_{ds1}\|r_{ds5})]\| (Ar_{ds9}g_{m9}r_{ds11})$$

If $r_{dsn} >> r_{dsp}$ or if $r_{dsp} >> r_{dsn}$, then $A \approx g_m r_{ds}$ and the voltage gain would be in the range of 100,000 to 500,000.

Note that to achieve maximum output swing, it will be necessary to make sure that M5 and M11 are biased with $V_{DS} = V_{DS}$(sat).

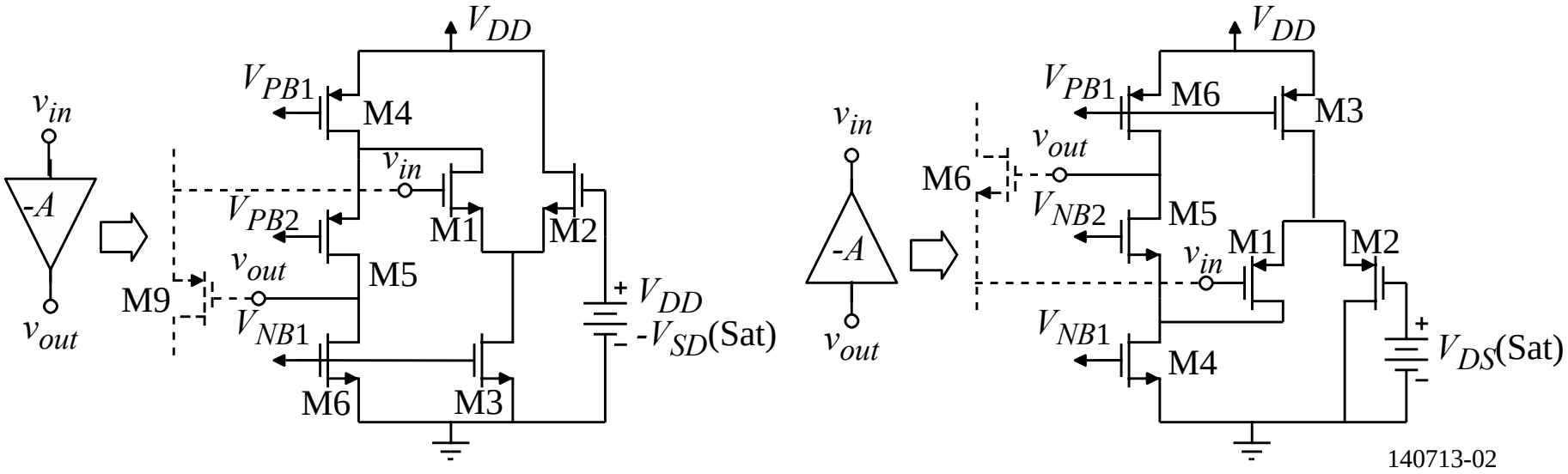
What are the Enhancement Amplifiers?

Requirements:

1.) Need a gain of $g_m r_{ds}$.

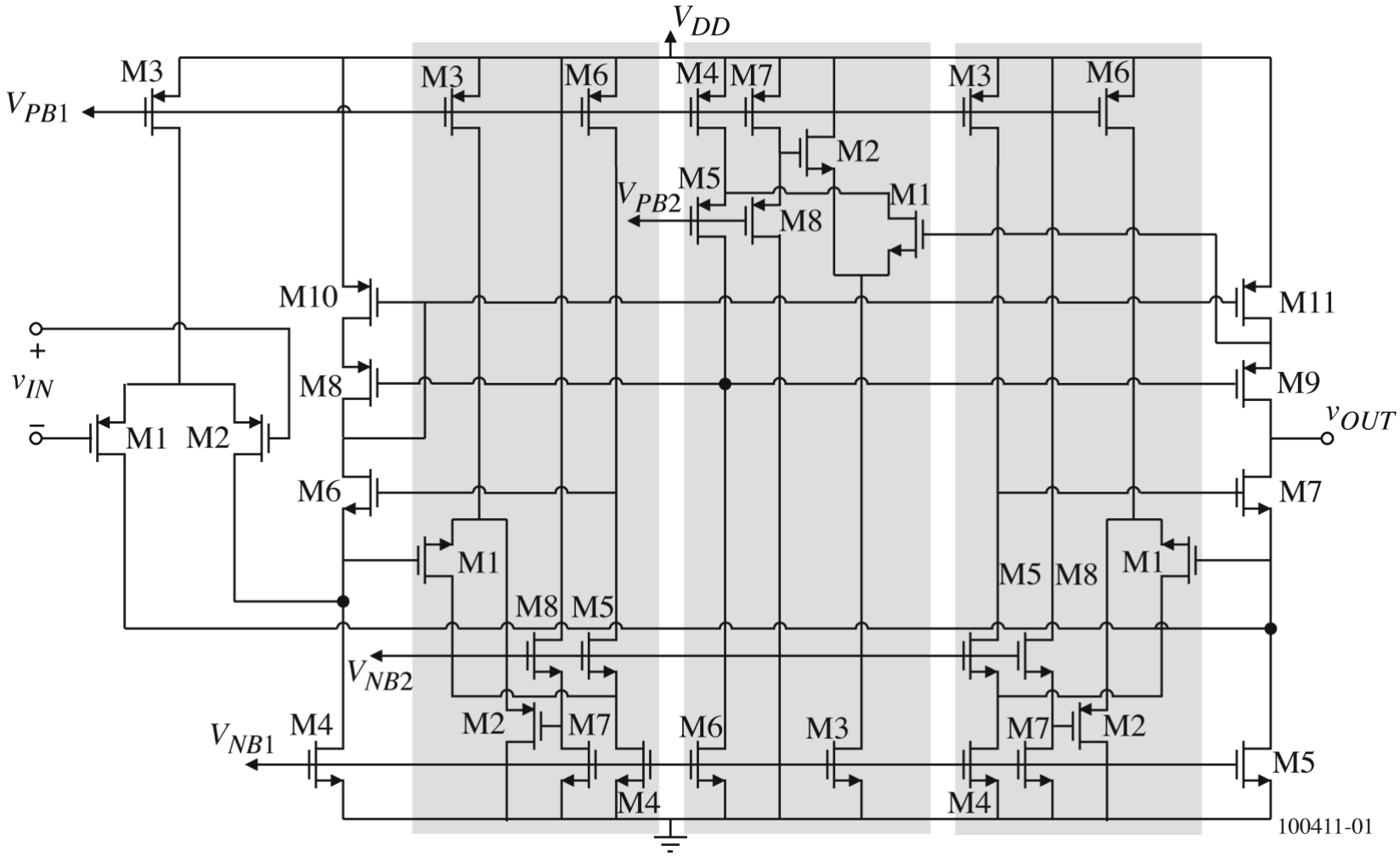
2.) Must be able to set the dc voltage at its input to get wide-output voltage swing.

Possible Enhancement Amplifiers:



Enhanced-Gain, Folded Cascode Op Amp

Detailed realization:

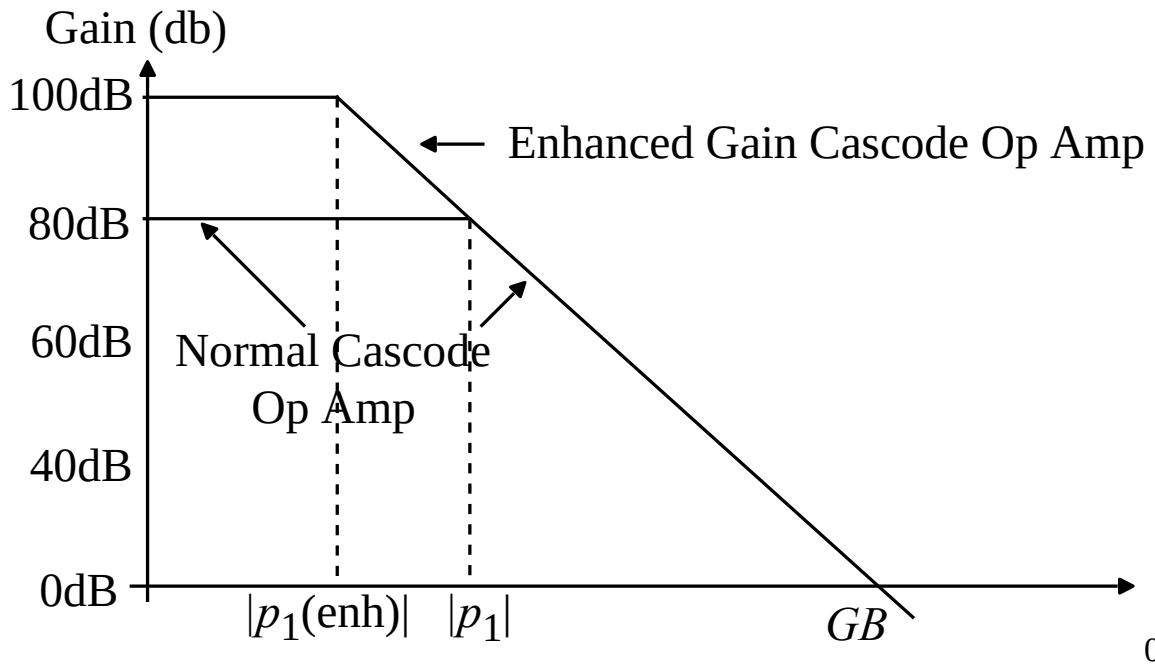


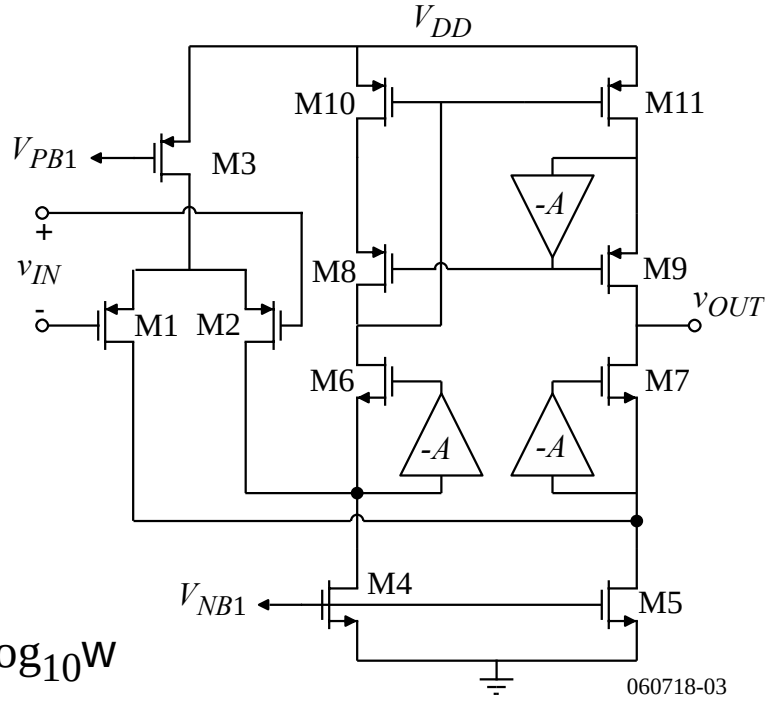
Frequency Response of the Enhanced Gain Cascode Op Amps

Normally, the frequency response of the cascode op amps would have one dominant pole at the output. The frequency response would be,

$$A_v(s) = g_{m1}\left(\frac{R_{out}(1/sC_{out})}{R_{out}+1/sC_{out}}\right) = \frac{g_{m1}R_{out}}{sR_{out}C_{out}+1} = \frac{g_{m1}R_{out}}{1-\frac{s}{p_1}}$$

If the amplifier used to boost the output resistance had no frequency dependence then the frequency response would be as follows.





SUMMARY

- Cascode op amps give additional flexibility to the two-stage op amp
  - Increase the gain
  - Control the dominant and nondominant poles
- Enhanced gain, cascode amplifiers provide additional gain and are used when high gains are needed
- Folded cascode amplifier is an attractive alternate to the two-stage op amp
  - Wider ICMR
  - Self compensating
  - Good PSRR