LECTURE 23 – DESIGN OF TWO-STAGE OP AMPS

LECTURE OUTLINE

Outline

- Steps in Designing an Op Amp
- Design Procedure for a Two-Stage Op Amp
- Design Example of a Two-Stage Op Amp
- Right Half Plane Zero
- PSRR of the Two-Stage Op Amp
- Summary

***CMOS Analog Circuit Design*, 3rd Edition Reference**

Pages 286-309

STEPS IN DESIGNING A CMOS OP AMP

Design Inputs

Boundary conditions:

1. Process specification (V_T, K', C_{ox}, etc.)
2. Supply voltage and range
3. Supply current and range
4. Operating temperature and range

Requirements:

1. Gain
2. Gain bandwidth
3. Settling time
4. Slew rate
5. Common-mode input range, *ICMR*
6. Common-mode rejection ratio, *CMRR*
7. Power-supply rejection ratio, *PSRR*
8. Output-voltage swing
9. Output resistance
10. Offset
11. Noise
12. Layout area

Outputs of Op Amp Electrical Design

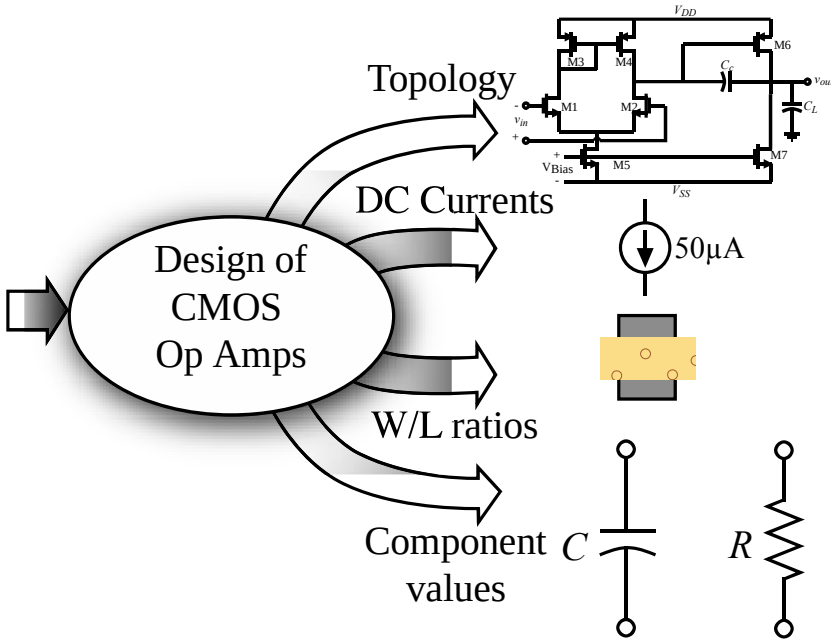
The basic outputs are:

1.) The topology

2.) The dc currents

3.) The *W* and *L* values of transistors

4.) The values of components



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Some Practical Thoughts on Op Amp Design

1.) Decide upon a suitable topology.
- Experience is a great help
- The topology should be the one capable of meeting most of the specifications
- Try to avoid "inventing" a new topology but start with an existing topology

2.) Determine the type of compensation needed to meet the specifications.
- Consider the load and stability requirements
- Use some form of Miller compensation or a self-compensated approach

3.) Design dc currents and device sizes for proper dc, ac, and transient performance.
- This begins with hand calculations based upon approximate design equations.
- Compensation components are also sized in this step of the procedure.
- After each device is sized by hand, a circuit simulator is used to fine tune the design

Two basic steps of design:

1.) "First-cut" - this step is to use hand calculations to propose a design that has potential of satisfying the specifications. Design robustness is developed in this step.

2.) Optimization - this step uses the computer to refine and optimize the design.

A DESIGN PROCEDURE FOR THE TWO-STAGE CMOS OP AMP

Unbuffered, Two-Stage CMOS Op Amp

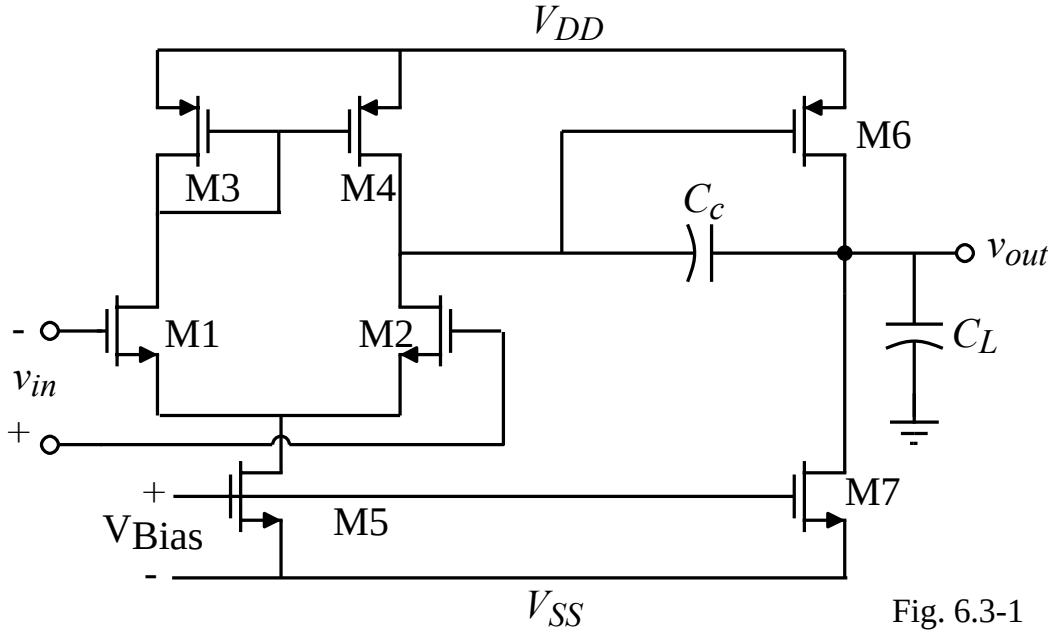


Fig. 6.3-1

Notation:

$$S_i = \frac{W_i}{L_i} = W/L \text{ of the ith transistor}$$

DC Balance Conditions for the Two-Stage Op Amp

For best performance, keep all transistors in saturation.

M4 is the only transistor that cannot be forced into saturation by internal connections or external voltages.

Therefore, we develop conditions to force M4 to be in saturation.

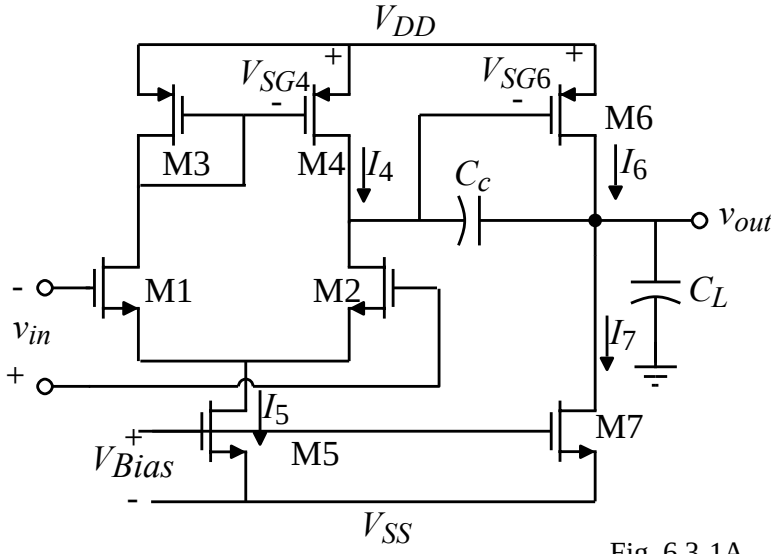


Fig. 6.3-1A

1.) First *assume* that $V_{SG4} = V_{SG6}$. This will cause "proper mirroring" in the M3-M4 mirror. Also, the gate and drain of M4 are at the same potential so that M4 is "guaranteed" to be in saturation.

2.) *If* $V_{SG4} = V_{SG6}$, then $I_6 = \left(\frac{S_6}{S_4}\right) I_4$

3.) However, $I_7 = \left(\frac{S_7}{S_5}\right) I_5 = \left(\frac{S_7}{S_5}\right) (2I_4)$

4.) For balance, I_6 must equal $I_7 \Rightarrow$ $\boxed{\frac{S_6}{S_4} = \frac{2S_7}{S_5}}$ called the "balance conditions"

5.) So if the balance conditions are satisfied, then $V_{DG4} = 0$ and M4 is saturated.

Summary of the Design Relationships for the Two-Stage Op Amp

Slew rate $SR = \frac{I_5}{C_c}$ (Assuming $I_7 >> I_5$ and $C_L > C_c$)

First-stage gain $A_{v1} = \frac{g_{m1}}{g_{ds2} + g_{ds4}} = \frac{2g_{m1}}{I_5(l_2 + l_4)}$

Second-stage gain $A_{v2} = \frac{g_{m6}}{g_{ds6} + g_{ds7}} = \frac{g_{m6}}{I_6(l_6 + l_7)}$

Gain-bandwidth $GB = \frac{g_{m1}}{C_c}$

Output pole $p_2 = \frac{-g_{m6}}{C_L}$

RHP zero $z_1 = \frac{g_{m6}}{C_c}$

60° phase margin requires that $g_{m6} = 2.2g_{m2}(C_L/C_c)$ if all other roots are $\geq 10GB$.

Positive ICMR $V_{\text{in(max)}} = V_{DD} - \sqrt{\frac{I_5}{b_3}} - |V_{T03}|(\text{max}) + V_{T1}(\text{min})$

Negative ICMR $V_{\text{in(min)}} = V_{SS} + \sqrt{\frac{I_5}{b_1}} + V_{T1}(\text{max}) + V_{DS5}(\text{sat})$

Op Amp Specifications

The following design procedure assumes that specifications for the following parameters are given.

1. Gain at dc, $A_v(0)$
2. Gain-bandwidth, GB
3. Phase margin (or settling time)
4. Input common-mode range, ICMR
5. Load Capacitance, C_L
6. Slew-rate, SR
7. Output voltage swing
8. Power dissipation, P_{diss}

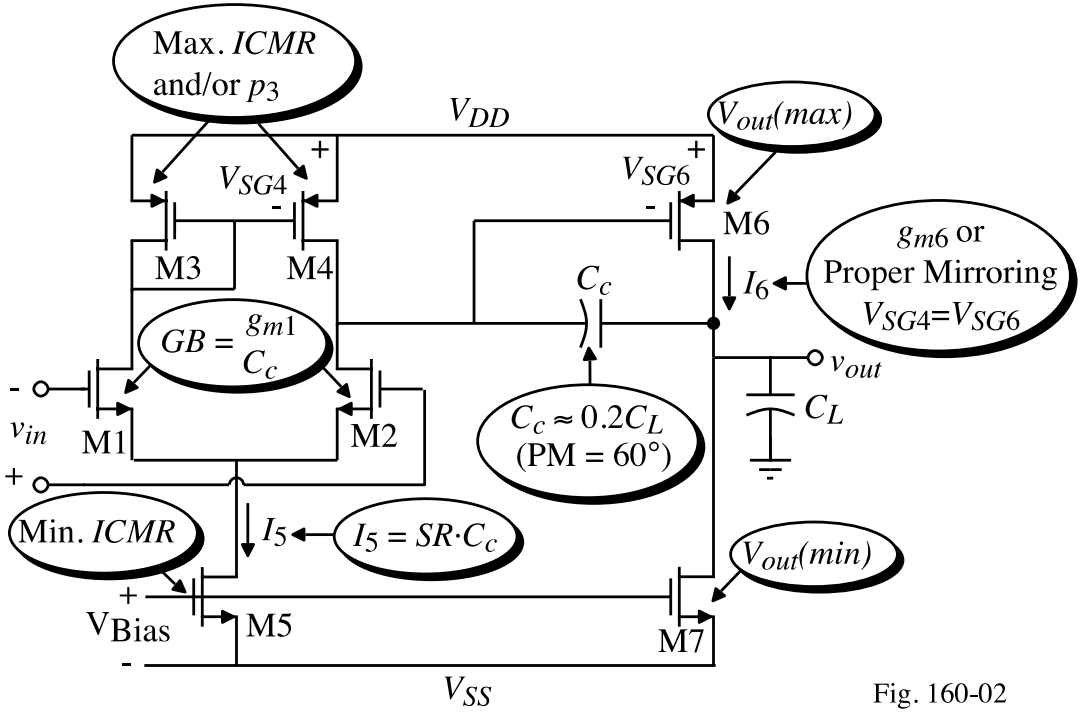


Fig. 160-02

Unbuffered Op Amp Design Procedure

This design procedure assumes that the gain at dc (A_v), unity gain bandwidth (GB), input common mode range (V_{in}(min) and V_{in}(max)), load capacitance (C_L), slew rate (SR), settling time (T_s), output voltage swing (V_{out}(max) and V_{out}(min)), and power dissipation (P_{diss}) are given. Choose the smallest device length which will keep the channel modulation parameter constant and give good matching for current mirrors.

1. From the desired phase margin, choose the minimum value for C_c, i.e. for a 60° phase margin we use the following relationship. This assumes that $z \geq 10GB$.

$$C_c > 0.22C_L$$

2. Determine the minimum value for the "tail current" (I_5) from

$$I_5 = SR \cdot C_c$$

3. Design for S_3 from the maximum input voltage specification.

$$S_3 = \frac{I_5}{K'_3[V_{DD} - V_{in}(\max) - |V_{T03}|(\max) + V_{T1}(\min)]^2}$$

4. Verify that the pole of M3 due to C_{gs3} and C_{gs4} ($= 0.67W_3L_3C_{ox}$) will not be dominant by assuming it to be greater than 10 GB

$$\frac{g_{m3}}{2C_{gs3}} > 10GB.$$

Unbuffered Op Amp Design Procedure - Continued

5. Design for S_1 (S_2) to achieve the desired GB.

$$g_{m1} = GB \cdot C_c \rightarrow S_2 = \frac{g_{m1}^2}{K'_1 I_5}$$

6. Design for S_5 from the minimum input voltage. First calculate $V_{DS5}(\text{sat})$ then find S_5.

$$V_{DS5}(\text{sat}) = V_{in}(\text{min}) - V_{SS} - \sqrt{\frac{I_5}{\beta_1}} - V_{T1}(\text{max}) \geq 100 \text{ mV} \rightarrow S_5 = \frac{2I_5}{K'_5[V_{DS5}(\text{sat})]^2}$$

7. Find S_6 by letting the second pole (p_2) be equal to 2.2 times GB and assuming that $V_{SG4} = V_{SG6}$.

$$g_{m6} = 2.2 g_{m2}(C_L/C_c) \quad \text{and} \quad \frac{g_{m6}}{g_{m4}} = \frac{\sqrt{2K_P' S_6 I_6}}{\sqrt{2K_P' S_4 I_4}} = \sqrt{\frac{S_6 I_6}{S_4 I_4}} = \frac{S_6}{S_4} \rightarrow S_6 = \frac{g_{m6}}{g_{m4}} S_4$$

8. Calculate I_6 from

$$I_6 = \frac{g_{m6}^2}{2K'_6 S_6}$$

Check to make sure that S_6 satisfies the $V_{out}(\text{max})$ requirement and adjust as necessary.

9. Design S_7 to achieve the desired current ratios between I_5 and I_6.

$S_7 = (I_6/I_5)S_5$ (Check the minimum output voltage requirements)

Unbuffered Op Amp Design Procedure - Continued

10. Check gain and power dissipation specifications.

$$A_v = \frac{2g_{m2}g_{m6}}{I_5(\lambda_2 + \lambda_4)I_6(\lambda_6 + \lambda_7)} \qquad P_{diss} = (I_5 + I_6)(V_{DD} + |V_{SS}|)$$

11. If the gain specification is not met, then the currents, I_5 and I_6, can be decreased or the W/L ratios of M2 and/or M6 increased. The previous calculations must be rechecked to insure that they are satisfied. If the power dissipation is too high, then one can only reduce the currents I_5 and I_6. Reduction of currents will probably necessitate increase of some of the W/L ratios in order to satisfy input and output swings.

12. Simulate the circuit to check to see that all specifications are met.

Unbuffered Op Amp Design Summary

Step	Design Equations	Comments
1	Let $C_c \geq 0.2C_L$	PM = 60° and RHP Z=10*GB*
2	$I_5 \geq SR \cdot C_c$	Assumes SR limited by C_c
3	$\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{I_5}{K_3'\left[V_{DD} - V_{in}(\max) - \lvert V_{T3}\rvert + V_{T1}\right]^2}$	Maximum input common mode range
4	$g_{m1} = GB \cdot C_c \quad \rightarrow \quad \frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{g_{m1}^2}{K_1' I_5}$	*GB* defines the W/L of M1 and M2
5	$\frac{W_5}{L_5} = \frac{2I_5}{K_5' V_{DS5}(sat)^2}$	Minimum input common mode range
6	$\frac{W_6}{L_6} = \frac{g_{m6}}{g_{m4}} \frac{W_4}{L_4}$	DC balance conditions
7	$I_6 = \frac{g_{m6}^2}{2K_6'(W_6/L_6)}$	PM = 60° and p_2 = 2.2*GB* give $g_{m6} \approx 10 g_{m1}$
8	$\frac{W_7}{L_7} = \max\left[\frac{I_6}{I_5}\frac{W_5}{L_5}, \frac{2I_7}{K_7' V_{DS7}(sat)^2}\right]$	Determines the current in M7
9	Check gain and power dissipation and iterate if necessary	$A_v = \frac{2g_{m1}g_{m6}}{I_5(\lambda_2 + \lambda_4) I_6(\lambda_6 + \lambda_7)}$ and $P_{diss} = (I_5 + I_6)(V_{DD} + \lvert V_{SS}\rvert)$

DESIGN EXAMPLE OF A TWO-STAGE OP AMP

Example 23-1 - Design of a Two-Stage Op Amp

If K_N'=120μA/V^2, K_P'= 25μA/V^2, $V_{TN} = |V_{TP}|$ = 0.5±0.15V, λ_N = 0.06V^{-1}, and λ_P = 0.08V^{-1}, design a two-stage, CMOS op amp that meets the following specifications. Assume the channel length is to be 0.5μm and the load capacitor is C_L = 10pF.

A_V > 3000V/V	V_{DD} =2.5V	GB = 5MHz	SR > 10V/μs
60° phase margin	0.5V<V_{out} range < 2V	$ICMR$ = 1.25V to 2V	P_{diss} ≤ 2mW

Solution

1.) The first step is to calculate the minimum value of the compensation capacitor C_c,

$$C_c > (2.2/10)(10\text{ pF}) = 2.2\text{ pF}$$

2.) Choose C_c as 3pF. Using the slew-rate specification and C_c calculate I_5.

$$I_5 = (3\text{x}10^{-12})(10\text{x}10^6) = 30\ \mu\text{A}$$

3.) Next calculate $(W/L)_3$ using ICMR requirements (use worst case thresholds ±0.15V).

$$(W/L)_3 = \frac{30\text{x}10^{-6}}{(25\text{x}10^{-6})[2.5 - 2 - .65 + 0.35]^2} = 30 \quad \rightarrow \quad \boxed{(W/L)_3 = (W/\text{L})_4 = 30}$$

Example 23-1 - Continued

4.) Now we can check the value of the mirror pole, p_3, to make sure that it is in fact greater than $10GB$. Assume the C_{ox} = 6fF/μm^2. The mirror pole can be found as

$$p_3 \approx \frac{-g_{m3}}{2C_{gs3}} = \frac{-\sqrt{2K'_pS_3I_3}}{2(0.667)W_3L_3C_{ox}} = -1.25\text{x}10^9\text{(rads/sec)}$$

or 199 MHz. Thus, p_3, is not of concern in this design because $p_3 >> 10GB$.

5.) The next step in the design is to calculate g_{m1} to get

$$g_{m1} = (5\text{x}10^6)(2\pi)(3\text{x}10^{-12}) = 94.25\mu\text{S}$$

Therefore, $(W/L)_1$ is

$$(W/L)_1 = (W/L)_2 = \frac{g_{m1}^2}{2K'_NI_1} = \frac{(94.25)^2}{2\cdot120\cdot15} = 2.47 \approx 3.0 \Rightarrow \boxed{(W/L)_1 = (W/L)_2 = 3}$$

6.) Next calculate V_{DS5},

$$V_{DS5} = 1.25 - \sqrt{\frac{30\text{x}10^{-6}}{120\text{x}10^{-6}\cdot3}} - .65 = 0.31\text{V}$$

Using V_{DS5} calculate $(W/L)_5$ from the saturation relationship.

$$(W/L)_5 = \frac{2(30\text{x}10\text{-}6)}{(120\text{x}10\text{-}6)(0.31)^2} = 5.16 \approx 6 \qquad \rightarrow \qquad \boxed{(W/L)_5 = 6}$$

Example 23-1 - Continued

7.) For 60° phase margin, we know that

$$g_{m6} \geq 10 g_{m1} \geq 942.5\mu S$$

Assuming that $g_{m6} = 942.5\mu S$ and knowing that $g_{m4} = 150\mu S$, we calculate $(W/L)_6$ as

$$(W/L)_6 = 30\,\frac{942.5\text{x}10^{-6}}{(150\text{x}10^{-6})} = 188.5 \approx 190 \qquad \boxed{(W/L)_6 = 190}$$

8.) Calculate I_6 using the small-signal g_m expression:

$$I_6 = \frac{(942.5\text{x}10^{-6})^2}{(2)(25\text{x}10^{-6})(188.5)} = 94.2\mu A \approx 95\mu A$$

Calculating $(W/L)_6$ based on V_{out}(max), gives a value of 15. Since 190 exceeds the specification and gives better phase margin, we choose $(W/L)_6 = 190$ and $I_6 = 95\mu A$. With $I_6 = 95\mu A$ the power dissipation is $P_{diss} = 2.5V \cdot (30\mu A + 95\mu A) = 0.3125mW$

9.) Finally, calculate $(W/L)_7$

$$(W/L)_7 = 6\left(\frac{95\text{x}10^{-6}}{30\text{x}10^{-6}}\right) = 19 \approx 20 \qquad \rightarrow \qquad \boxed{(W/L)_7 = 20}$$

Let us check the V_{out}(min) specification although the W/L of M7 is so large that this is probably not necessary. The value of V_{out}(min) is

$$V_{out}(\text{min}) = V_{DS7}(\text{sat}) = \sqrt{(2 \cdot 95)/(120 \cdot 20)} = 0.281V$$

which is less than required. At this point, the first-cut design is complete.

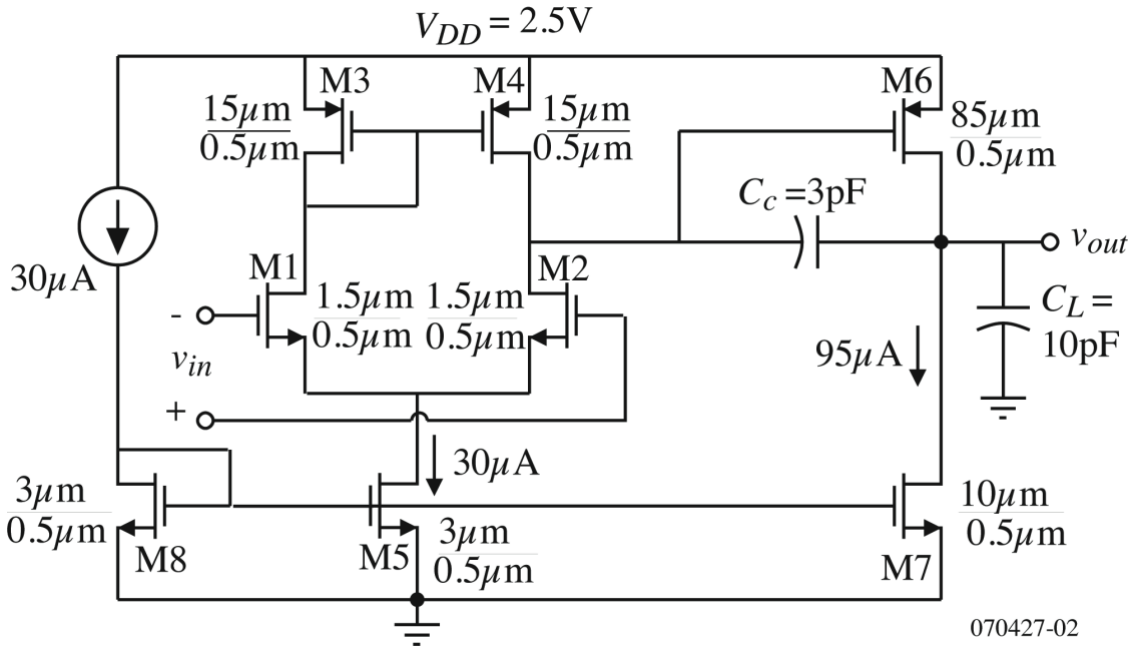
Example 23-1 - Continued

10.) Now check to see that the gain specification has been met

$$A_v = \frac{(94.25\text{x}10\text{-}6)(942.5\text{x}10\text{-}6)}{15\text{x}10\text{-}6(.06 + .08)95\text{x}10\text{-}6(.06 + .08)} = 3{,}180\text{V/V}$$

which barely exceeds the specifications. Since we are at 2xL_{min}, it won't do any good to increase the channel lengths. Decreasing the currents or increasing W_6/L_6 will help.

The figure below shows the results of the first-cut design. The W/L ratios shown do not account for the lateral diffusion discussed above. The next phase requires simulation.

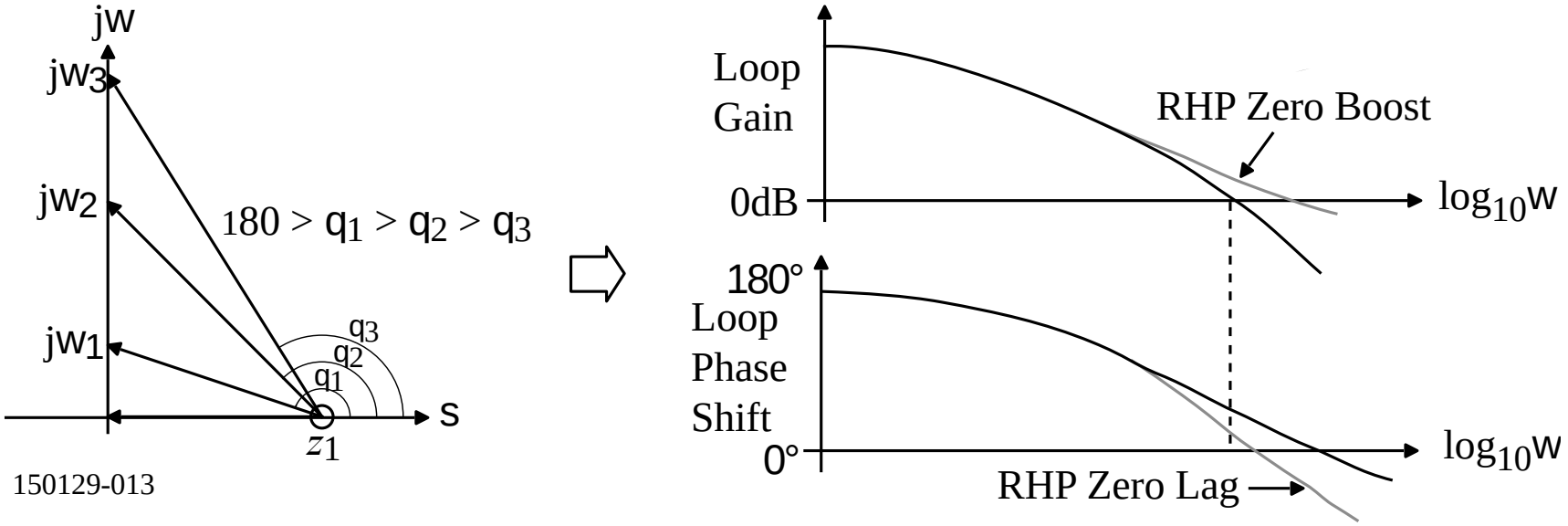


RIGHT-HALF PLANE ZERO

Controlling the Right-Half Plane Zero

Why is the RHP zero a problem?

Because it boosts the magnitude but lags the phase - the worst possible combination for stability.



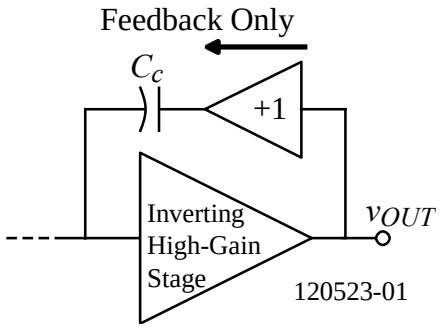
Solution of the problem:

The compensation comes from the *feedback path* through C_c, but the RHP zero comes from the *feedforward path* through C_c so eliminate the feedforward path!

Elimination of the Feedforward Path through the Miller Capacitor

1.) Removing the feedforward path.

Roots: Dominant pole and output pole.

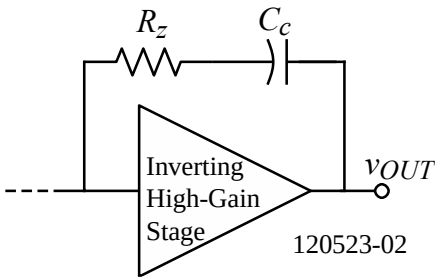


2.) Controlling the RHP zero location using a nulling resistor†.

Roots:

a.) Dominant pole (Miller pole)

b.) Output pole



c.) Pole due to R_z and first stage output capacitance, $p_4 \approx \dfrac{-1}{R_z C_I}$

d.) Controllable zero, $z_1 = \dfrac{1}{C_c(1/g_{mII} - R_z)}$

Note that z_1 can be placed anywhere on the real axis.

† W.J. Parrish, "An Ion Implanted CMOS Amplifier for High Performance Active Filters", Ph.D. Dissertation, 1976, Univ. of CA, Santa Barbara.

A Design Procedure that Allows the RHP Zero to Cancel the Output Pole, p_2

We desire that $z_1 = p_2$ in terms of the previous notation.

Therefore,

$$\frac{1}{C_c(1/g_{mII} - R_z)} = \frac{-g_{mII}}{C_{II}}$$

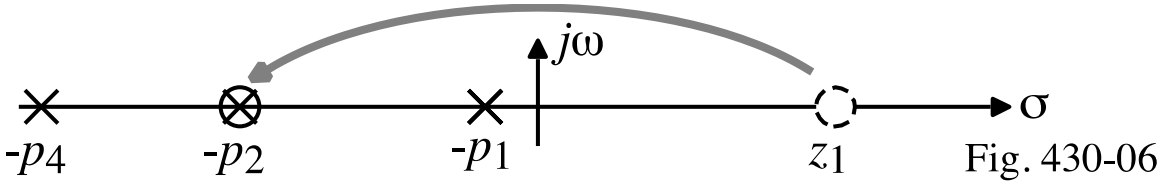


Fig. 430-06

The value of R_z can be found as

$$R_z = \left(\frac{C_c + C_{II}}{C_c}\right)(1/g_{mII})$$

With p_2 canceled, the remaining roots are p_1 and p_4(the pole due to R_z) . For unity-gain stability, all that is required is that

$$|p_4| > A_v(0)|p_1| = \frac{A_v(0)}{g_{mII}R_{II}R_IC_c} = \frac{g_{mI}}{C_c} \qquad \text{and} \qquad (1/R_zC_I) > (g_{mI}/C_c) = GB$$

Substituting R_z into the above inequality and assuming $C_{II} >> C_c$ results in

$$C_c > \sqrt{\frac{g_{mI}}{g_{mII}} C_IC_{II}}$$

This procedure gives excellent stability for a fixed value of C_{II} ($\approx C_L$).

Unfortunately, as C_L changes, p_2 changes and the zero must be readjusted to cancel p_2.

Using the Nulling Resistor in the Miller Compensated Two-Stage Op Amp

Circuit:

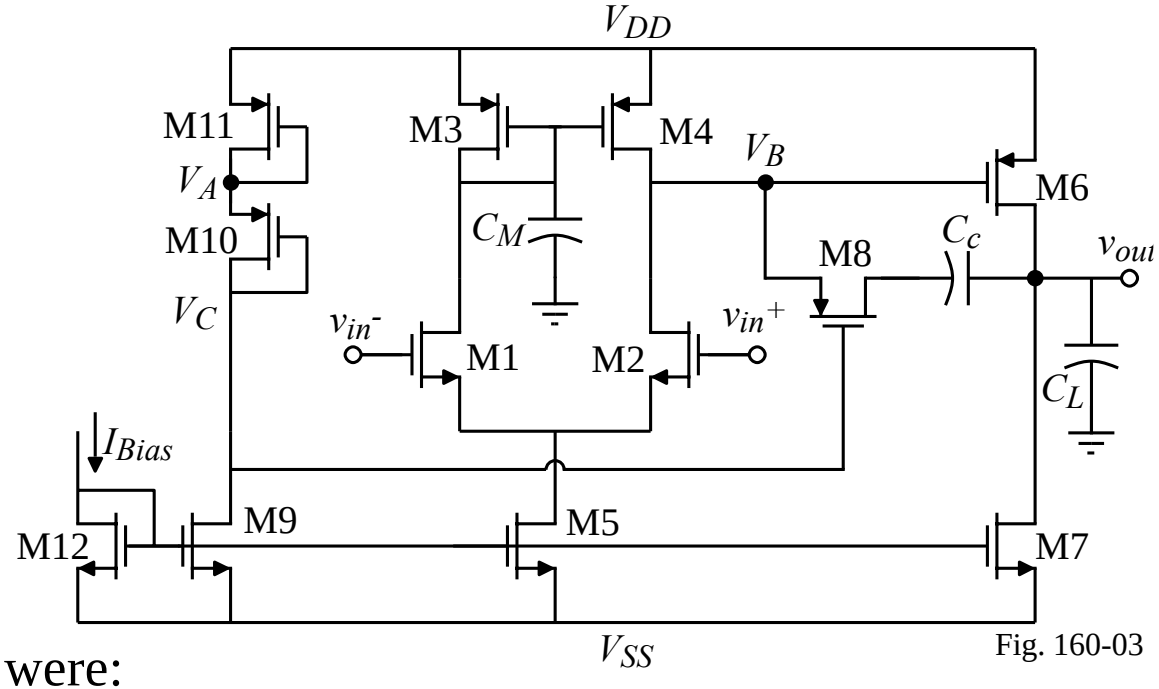


Fig. 160-03

We saw earlier that the roots were:

$$p_1 = -\frac{g_{m2}}{A_v C_c} = -\frac{g_{m1}}{A_v C_c} \qquad p_2 = -\frac{g_{m6}}{C_L}$$

$$p_4 = -\frac{1}{R_z C_I} \qquad z_1 = \frac{-1}{R_z C_c - C_c/g_{m6}}$$

where $A_v = g_{m1} g_{m6} R_I R_{II}$.

(Note that p_4 is the pole resulting from the nulling resistor compensation technique.)

Design of the Nulling Resistor (M8)

For the zero to be on top of the second pole (p_2), the following relationship must hold

$$R_Z = \frac{1}{g_{m6}}\left(\frac{C_L + C_c}{C_c}\right) = \left(\frac{C_c+C_L}{C_c}\right)\frac{1}{\sqrt{2K'_P S_6 I_6}}$$

The resistor, R_z, is realized by the transistor M8 which is operating in the active region because the dc current through it is zero. Therefore, R_z, can be written as

$$R_z = \frac{v_{DS8}}{i_{D8}}\bigg|_{V_{DS8}=0} = \frac{1}{K'_P S_8(V_{SG8}-|V_{TP}|)}$$

The bias circuit is designed so that voltage V_A is equal to V_B.

$$\therefore \quad |V_{GS10}| - |V_T| = |V_{GS8}| - |V_T| \Rightarrow \quad V_{SG11} = V_{SG6} \qquad \Rightarrow \quad \left(\frac{W_{11}}{L_{11}}\right) = \left(\frac{I_{10}}{I_6}\right)\left(\frac{W_6}{L_6}\right)$$

In the saturation region

$$|V_{GS10}| - |V_T| = \sqrt{\frac{2(I_{10})}{K'_P(W_{10}/L_{10})}} = |V_{GS8}| - |V_T|$$

$$\therefore \quad R_z = \frac{1}{K'_P S_8}\sqrt{\frac{K'_P S_{10}}{2I_{10}}} = \frac{1}{S_8}\sqrt{\frac{S_{10}}{2K'_P I_{10}}}$$

Equating the two expressions for R_Z gives $\left(\frac{W_8}{L_8}\right) = \left(\frac{C_c}{C_L + C_c}\right)\sqrt{\frac{S_{10}S_6 I_6}{I_{10}}}$

Example 23-2 - RHP Zero Compensation

Use results of Ex. 23-1 and design compensation circuitry so that the RHP zero is moved from the RHP to the LHP and placed on top of the output pole p_2. Use device data given in Ex. 23-1.

Solution

The task at hand is the design of transistors M8, M9, M10, M11, and bias current I_{10}. The first step in this design is to establish the bias components. In order to set V_A equal to V_B, then V_{SG11} must equal V_{SG6}. Therefore,

$$S_{11} = (I_{11}/I_6)S_6$$

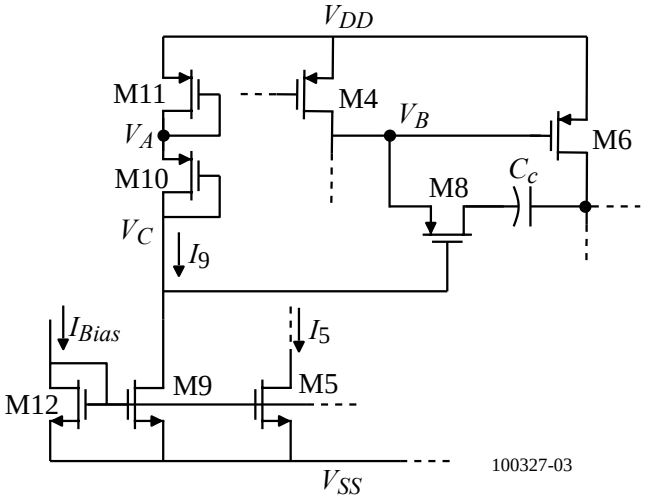
Choose $I_{11} = I_{10} = I_9 = 15\mu A$ which gives $S_{11} = (15\mu A/95\mu A)190 = 30$.

The aspect ratio of M10 is essentially a free parameter, and will be set equal to 1. There must be sufficient supply voltage to support the sum of V_{SG11}, V_{SG10}, and V_{DS9}. The ratio of I_{10}/I_5 determines the (W/L) of M9. This ratio is

$$(W/L)_9 = (I_{10}/I_5)(W/L)_5 = (15/30)(6) = 3$$

Now $(W/L)_8$ is determined to be

$$(W/L)_8 = \left(\frac{3pF}{3pF+10pF}\right)\sqrt{\frac{1\cdot 190\cdot 95\mu A}{15\mu A}} = 8$$



Example 23-2 - Continued

It is worthwhile to check that the RHP zero has been moved on top of p_2. To do this, first calculate the value of R_z. V_{SG8} must first be determined. It is equal to V_{SG10}, which is

$$V_{SG10} = \sqrt{\frac{2I_{10}}{K'_P S_{10}}} + |V_{TP}| = \sqrt{\frac{2\cdot 15}{25\cdot 1}} + 0.5 = 1.595\text{V}$$

Next determine R_z.

$$R_z = \frac{1}{K'_P S_8 (V_{SG10} - |V_{TP}|)} = \frac{10^6}{25\cdot 8(1.595-.7)} = 4.564\text{k}\Omega$$

The location of z_1 is calculated as

$$z_1 = \frac{-1}{(4.564 \text{ x } 10^3)(3\text{x}10^{-12}) - \frac{3\text{x}10^{-12}}{950\text{x}10^{-6}}} = -94.91\text{x}10^6 \text{ rads/sec}$$

The output pole, p_2, is

$$p_2 = -\frac{950\text{x}10^{-6}}{10\text{x}10^{-12}} = -95\text{x}10^6 \text{ rads/sec}$$

Thus, we see that for all practical purposes, the output pole is canceled by the zero that has been moved from the RHP to the LHP.

The results of this design are summarized below where $L = 0.5\mu\text{m}$.

$W_8 = 4\mu\text{m}$ $W_9 = 1.5\mu\text{m}$ $W_{10} = 0.5\mu\text{m}$ and $W_{11} = 15\ \mu\text{m}$

An Alternate Form of Nulling Resistor

To cancel p_2,

$$z_1 = p_2 \rightarrow \quad R_z = \frac{C_c+C_L}{g_{m6A}C_C} = \frac{1}{g_{m6B}}$$

Which gives

$$g_{m6B} = g_{m6A}\left(\frac{C_c}{C_c+C_L}\right)$$

In the previous example,

$g_{m6A} = 950\mu S$, $C_c = 3pF$

and $C_L = 10pF$.

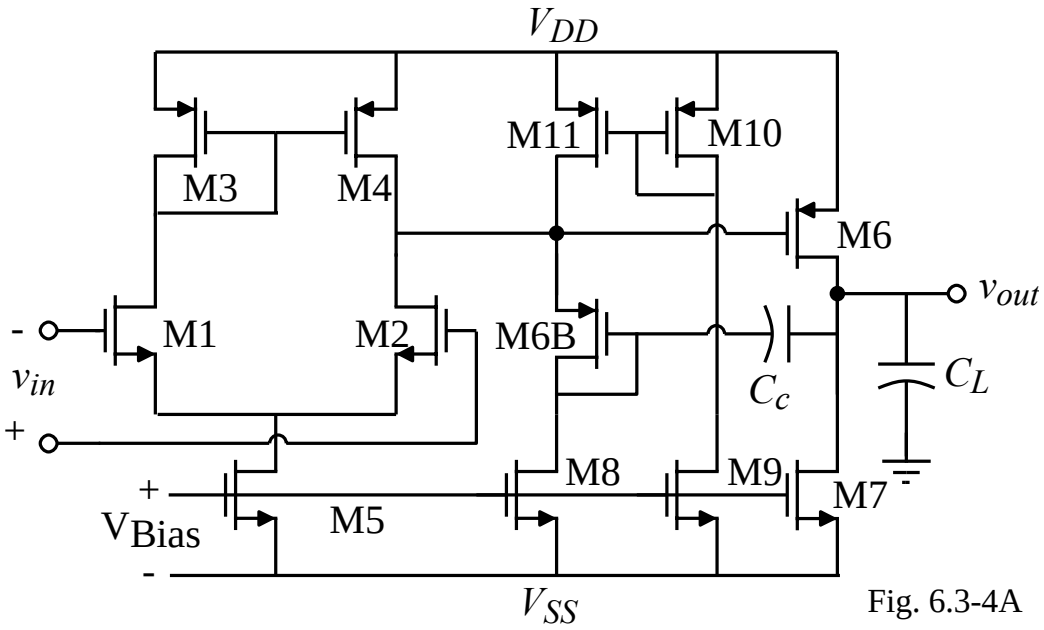


Fig. 6.3-4A

Choose $I_{6B} = 10\mu A$ to get

$$g_{m6B} = \frac{g_{m6A}C_c}{C_c + C_L} \rightarrow \sqrt{\frac{2K_PW_{6B}I_{6B}}{L_{6B}}} = \left(\frac{C_c}{C_c+C_L}\right)\sqrt{\frac{2K_PW_{6A}I_{D6}}{L_{6A}}}$$

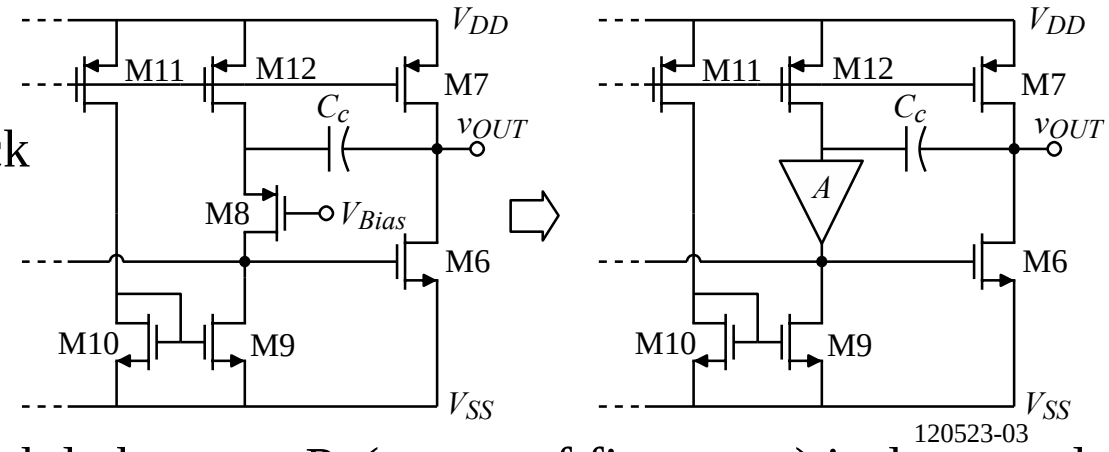
or

$$\frac{W_{6B}}{L_{6B}} = \left(\frac{3}{13}\right)^2\frac{I_{6A}}{I_{6B}}\frac{W_{6A}}{L_{6A}} = \left(\frac{3}{13}\right)^2\left(\frac{95}{10}\right)(190) = 96.12 \rightarrow W_{6B} = 48\mu m$$

Increasing the Magnitude of the Output Pole†

The magnitude of the output pole, p_2, can be increased by introducing gain in the Miller capacitor feedback path as shown where,

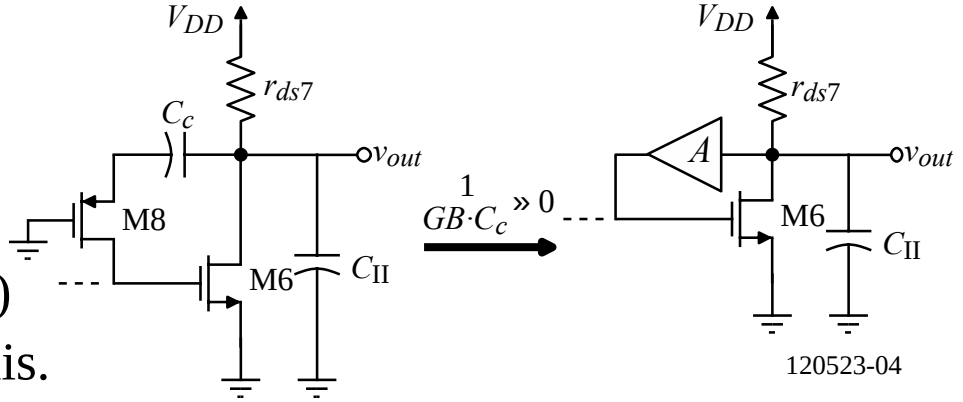
$$A \approx g_{m8}(r_{ds8}||r_{ds9}||r_{ds2}||r_{ds4}).$$



The roots become,

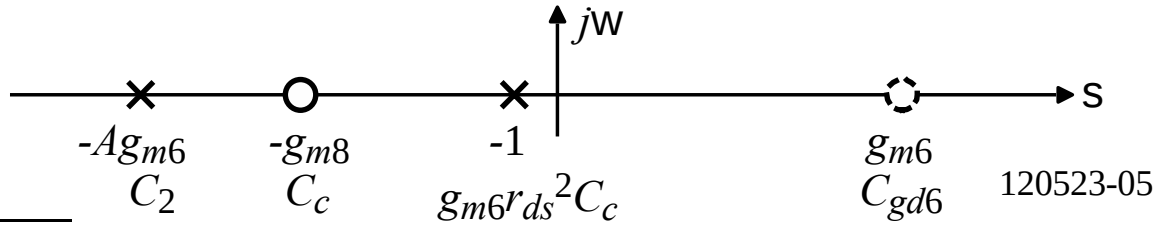
1.) The dominant pole increased slightly because R_I (output of first stage) is decreased.

2.) The output pole is increased by a factor of A to get new $p_2 \approx \dfrac{-Ag_{m6}}{C_{II}}$



3.) The pole at the source of M8 ($-g_{m8}/C_c$) becomes a zero on the negative real axis.

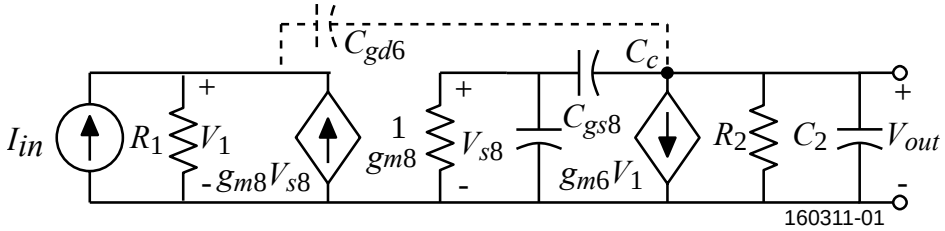
Roots:



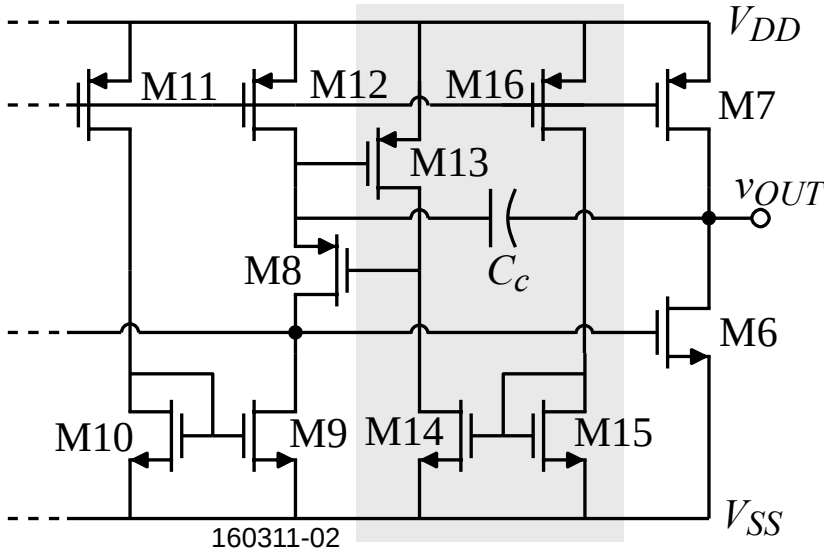
† B.K. Ahuja, "An Improved Frequency Compensation Technique for CMOS Operational Amplifiers," *IEEE J. of Solid-State Circuits*, Vol. SC-18, No. 6 (Dec. 1983) pp. 629-633.

Issues with the Previous Method†

The previous technique assumed that the gate-source capacitance of M8 could be neglected. Unfortunately, this assumption ignores a pair of complex poles near the unity gain frequency. Below is the small signal model with the capacitance that causes this that includes C_{gs8}.



The solution proposed in the reference below is to decrease the impedance at the source of M8 by using a negative feedback loop. Below is a possible solution that will have better phase margin.



† Uday Dasgupta, "Issues with 'Ahuja' Frequency Compensation Technique," Proc. of IEEE Inter. Symposium on Radio Frequency Integration Technology, Jan. 9, 2009, pp. 326-329.

POWER SUPPLY REJECTION RATIO OF THE TWO-STAGE OP AMP

What is *PSRR*?

$$PSRR = \frac{A_v(V_{dd}=0)}{A_{dd}(V_{in}=0)}$$

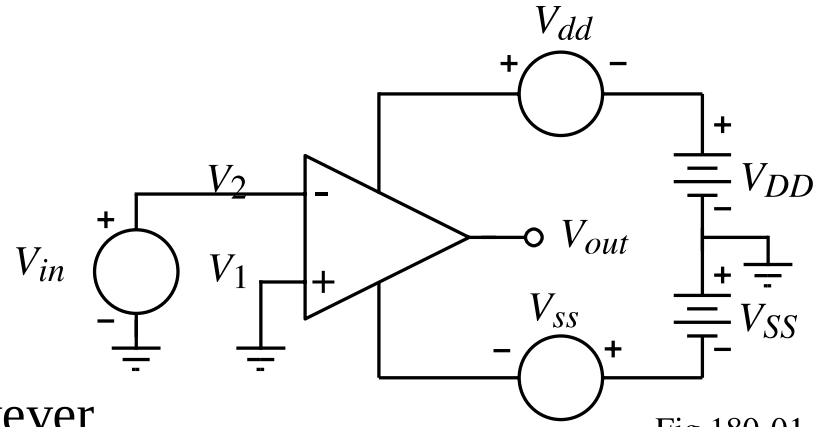


Fig.180-01

How do you calculate *PSRR*?

You could calculate A_v and A_{dd} and divide, however

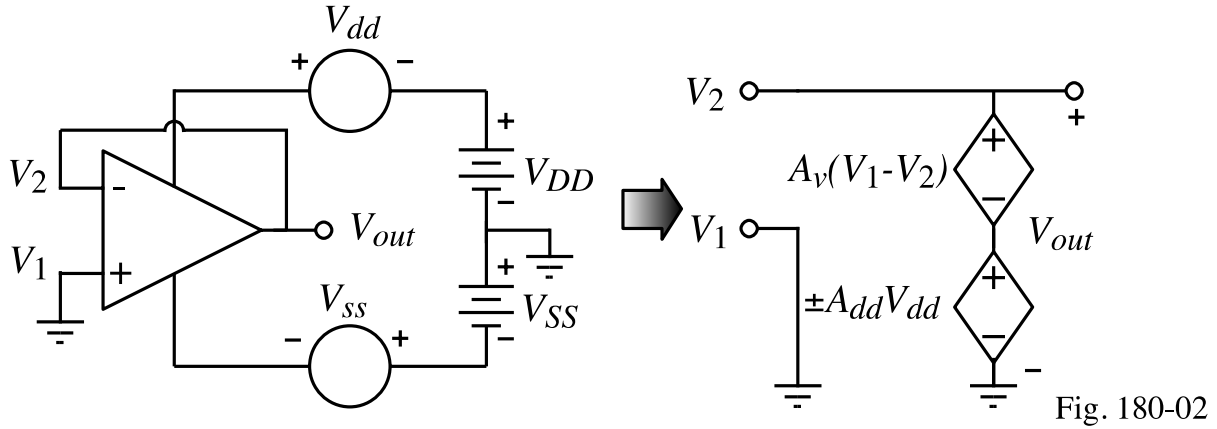


Fig. 180-02

$$V_{out} = A_{dd}V_{dd} + A_v(V_1-V_2) = A_{dd}V_{dd} - A_vV_{out} \quad \rightarrow \quad V_{out}(1+A_v) = A_{dd}V_{dd}$$

$$\therefore \quad \frac{V_{out}}{V_{dd}} = \frac{A_{dd}}{1+A_v} \approx \frac{A_{dd}}{A_v} = \frac{1}{PSRR^+} \quad \text{(Good for frequencies up to } GB\text{)}$$

Approximate Model for *PSRR*+

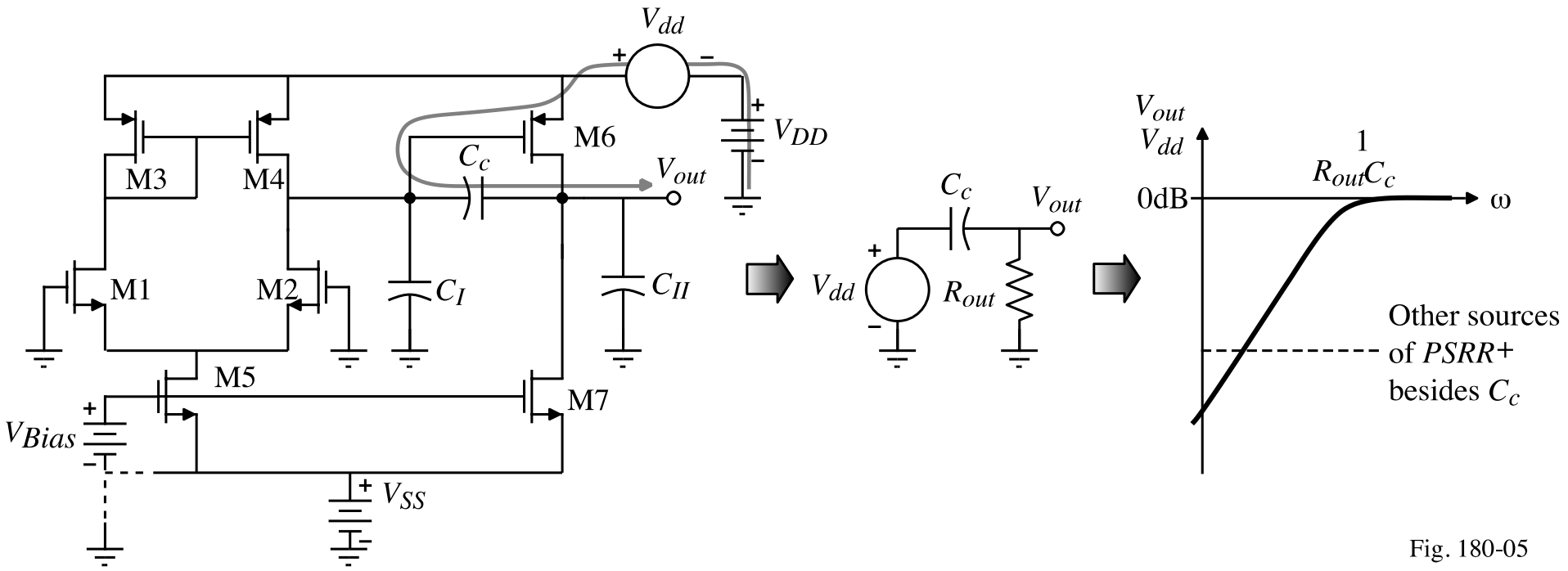


Fig. 180-05

1.) The M7 current sink causes V_{SG6} to act like a battery.

2.) Therefore, V_{dd} couples from the source to gate of M6.

3.) The path to the output is through any capacitance from gate to drain of M6.

Conclusion:

The Miller capacitor C_C couples the positive power supply ripple directly to the output.

Must reduce or eliminate C_C.

Approximate Model for $PSRR^-$

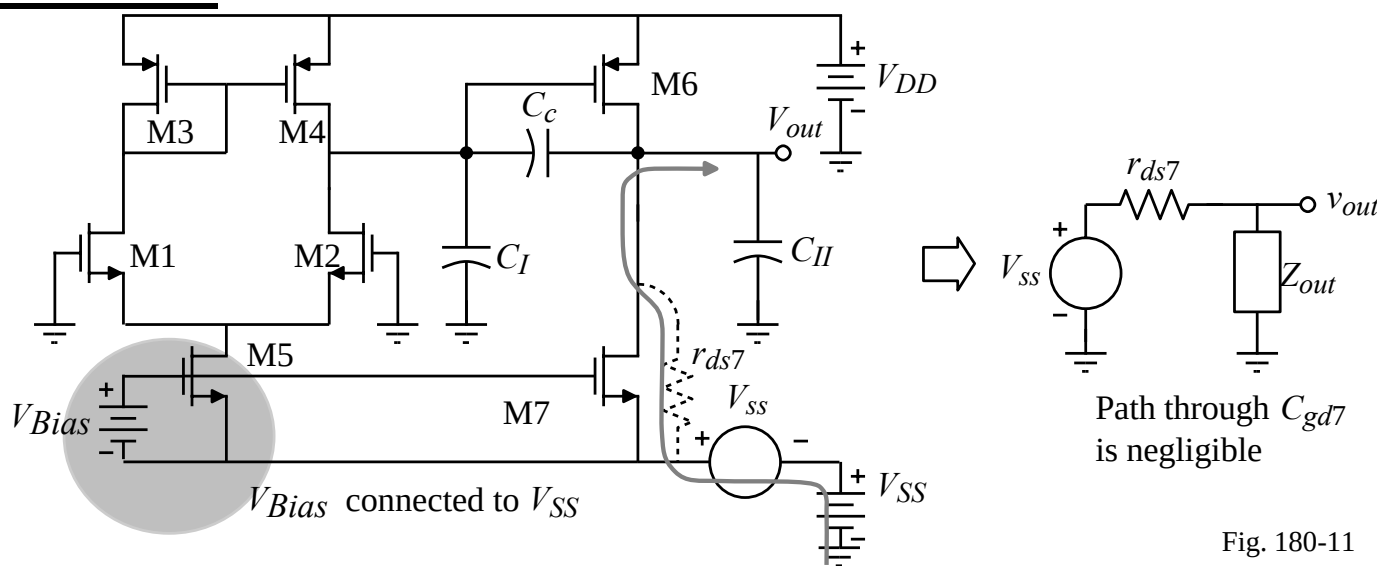
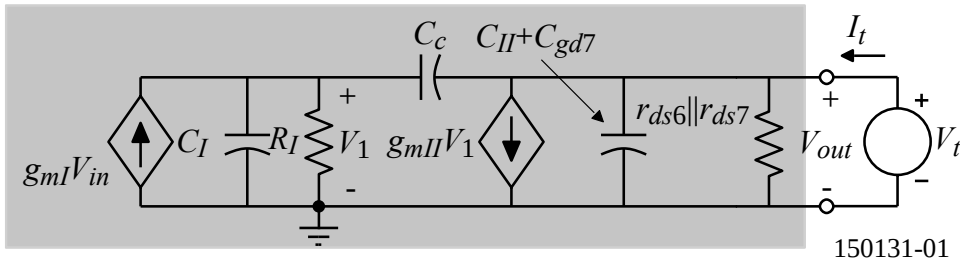


Fig. 180-11

What is Z_{out}?

$$Z_{out} = \frac{V_t}{I_t} \Rightarrow I_t = g_{mII}V_1 = g_{mII}\left(\frac{g_{mI}V_t}{G_I+sC_I+sC_c}\right)$$

Thus, $$Z_{out} = \frac{G_I+s(C_I+C_c)}{g_{mI}g_{MII}}$$



150131-01

$$\therefore \frac{V_{out}}{V_{ss}} = \frac{1+\frac{r_{ds7}}{Z_{out}}}{1} = \frac{s(C_c+C_I) + G_I+g_{mI}g_{mII}r_{ds7}}{s(C_c+C_I) + G_I} \quad \Rightarrow \quad \text{Pole at } \frac{-G_I}{C_c+C_I}$$

The negative *PSRR* is much better than the positive *PSRR*.

SUMMARY

- The output of the design of an op amp is
  - Schematic
  - DC currents
  - W/L ratios
  - Component values
- Design procedures provide an organized approach to creating the dc currents, *W*/*L* ratios, and the component values
- The right-half plane zero causes the Miller compensation to deteriorate
- Methods for eliminating the influence of the RHP zero are:
  - Nulling resistor
  - Increasing the magnitude of the output pole
- The *PSRR* of the two-stage op amp is poor because of the Miller capacitance, however, methods exist to eliminate this problem
- The two-stage op amp is a very general and flexible op amp