LECTURE 19 – DIFFERENTIAL AMPLIFIER

LECTURE ORGANIZATION

Outline

- Characterization of a differential amplifier
- Differential amplifier with a current mirror load
- Differential amplifier with MOS diode loads
- An intuitive method of small signal analysis
- Large signal performance of differential amplifiers
- Differential amplifiers with current source loads
- Design of differential amplifiers
- Summary

***CMOS Analog Circuit Design*, 3rd Edition Reference**

Pages 198-217

CHARACTERIZATION OF A DIFFERENTIAL AMPLIFIER

What is a Differential Amplifier?

A differential amplifier is an amplifier that amplifies the difference between two voltages and rejects the average or common mode value of the two voltages.

Differential and common mode voltages:

v_1 and v_2 are called *single-ended* voltages. They are voltages referenced to ac ground.

The *differential-mode* input voltage, v_{ID}, is the voltage difference between v_1 and v_2.

The *common-mode* input voltage, v_{IC}, is the average value of v_1 and v_2 .

$$\therefore \quad v_{ID} = v_1 - v_2 \quad \text{and} \quad v_{IC} = \frac{v_1+v_2}{2} \quad \Rightarrow \; v_1 = v_{IC} + 0.5v_{ID} \quad \text{and} \quad v_2 = v_{IC} - 0.5v_{ID}$$

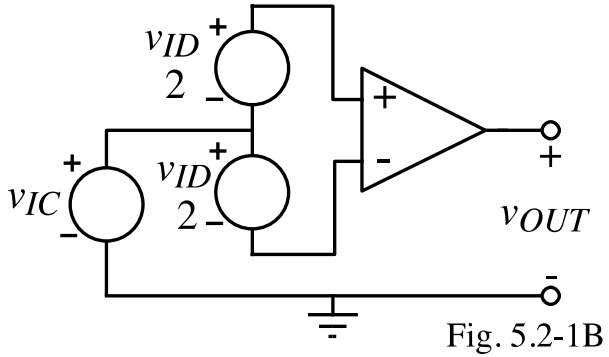


Fig. 5.2-1B

$$v_{OUT} = A_{VD}v_{ID} \pm A_{VC}v_{IC} = A_{VD}(v_1 - v_2) \pm A_{VC}\left(\frac{v_1 + v_2}{2}\right)$$

where

A_{VD} = differential-mode voltage gain

A_{VC} = common-mode voltage gain

Differential Amplifier Definitions

- Common mode rejection rato (*CMRR*)

$$CMRR = \left|\frac{A_{VD}}{A_{VC}}\right|$$

CMRR is a measure of how well the differential amplifier rejects the common-mode input voltage in favor of the differential-input voltage.

- Input common-mode range (*ICMR*)

The input common-mode range is the range of common-mode voltages over which the differential amplifier continues to sense and amplify the difference signal with the same gain.

Typically, the *ICMR* is defined by the common-mode voltage range over which all MOSFETs remain in the saturation region.

- Output offset voltage (V_{OS}(out))

The output offset voltage is the voltage which appears at the output of the differential amplifier when the input terminals are connected together.

- Input offset voltage (V_{OS}(in) = V_{OS})

The input offset voltage is equal to the output offset voltage divided by the differential voltage gain.

$$V_{OS} = \frac{V_{OS}(\text{out})}{A_{VD}}$$

Transconductance Characteristic of the Differential Amplifier

Consider the following n-channel differential amplifier (called a source-coupled pair). Where should bulk be connected? Consider a p-well, CMOS technology:

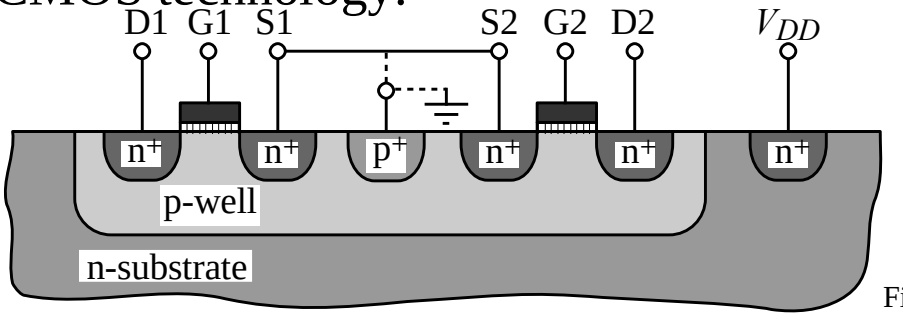


Fig. 5.2-3

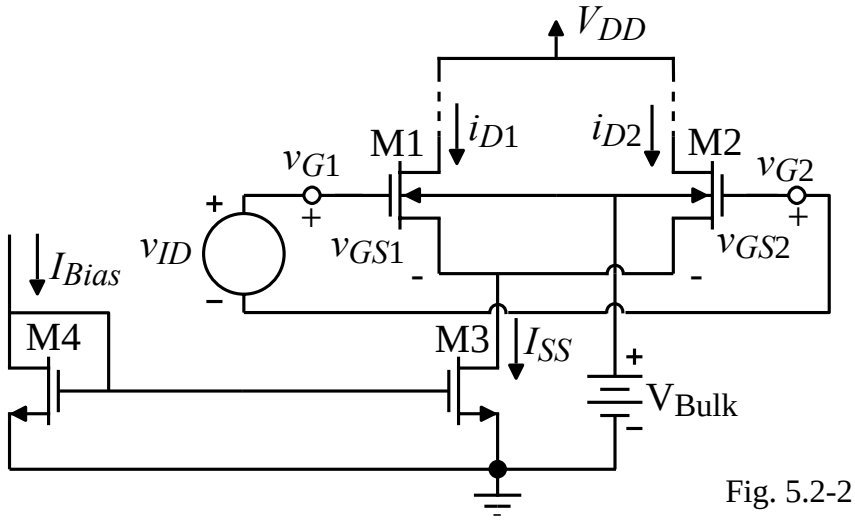
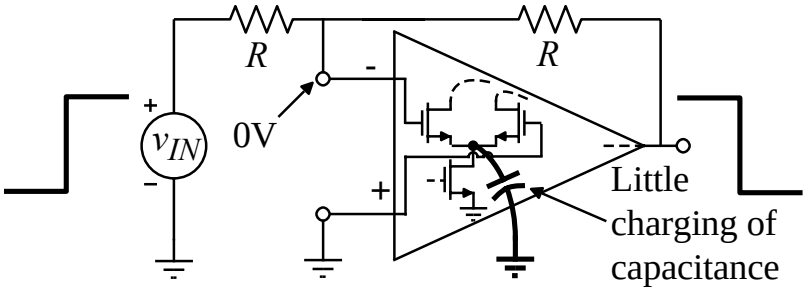


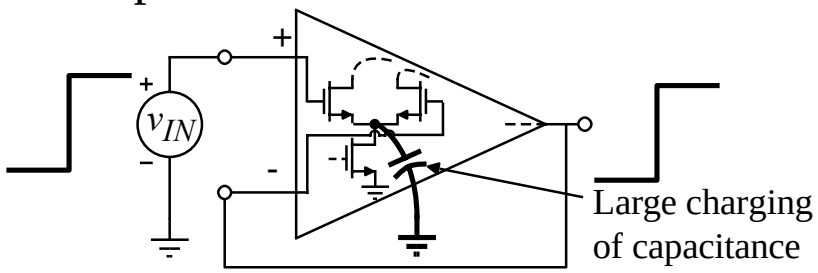
Fig. 5.2-2

1.) Bulks connected to the sources: No modulation of V_T but large common mode parasitic capacitance.

2.) Bulks connected to ground: Smaller common mode parasitic capacitors, but modulation of V_T.

What are the implications of a large common mode capacitance?





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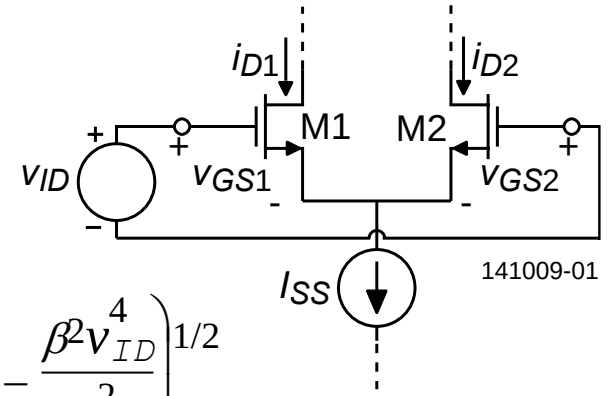
Transconductance Characteristic of the Differential Amplifier - Continued

Defining equations:

$$v_{ID} = v_{GS1} - v_{GS2} = \sqrt{\frac{2i_{D1}}{\beta}} - \sqrt{\frac{2i_{D2}}{\beta}} \quad \text{and} \quad I_{SS} = i_{D1} + i_{D2}$$



Solution:

$$i_{D1} = \frac{I_{SS}}{2} + \frac{I_{SS}}{2}\left(\frac{\beta v_{ID}^2}{I_{SS}} - \frac{\beta^2 v_{ID}^4}{4I_{SS}^2}\right)^{1/2} \quad \text{and} \quad i_{D2} = \frac{I_{SS}}{2} - \frac{I_{SS}}{2}\left(\frac{\beta v_{ID}^2}{I_{SS}} - \frac{\beta^2 v_{ID}^4}{4I_{SS}^2}\right)^{1/2}$$

which are valid for $v_{ID} < 2(I_{SS}/\beta)^{1/2}$.

Illustration of the result:

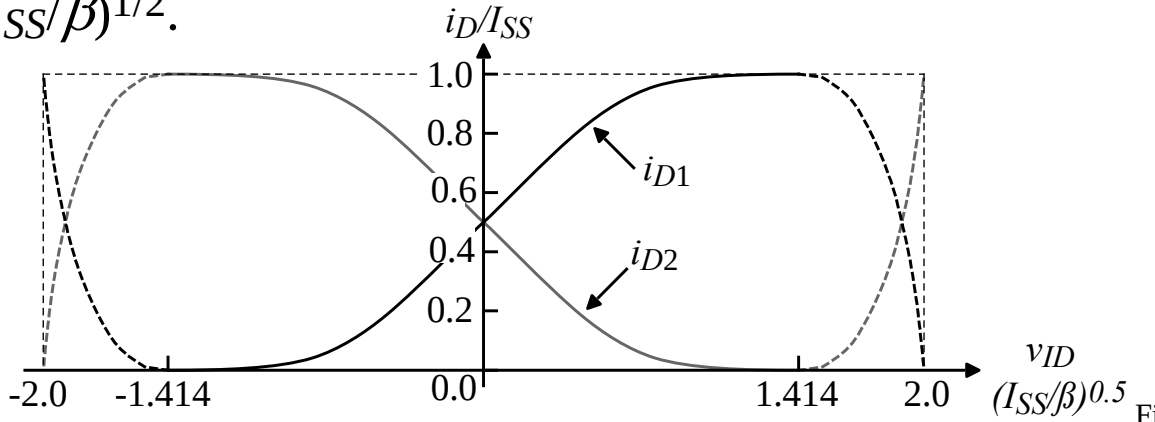


Fig. 5.2-4

Differentiating i_{D1} (or i_{D2}) with respect to v_{ID} and setting V_{ID} =0V gives

$$g_m = \frac{di_{D1}}{dv_{ID}}(V_{ID} = 0) = \sqrt{\frac{\beta I_{SS}}{4}} = \sqrt{\frac{K'_1 I_{SS} W_1}{4L_1}}$$ (half the g_m of an inverting amplifier)

DIFFERENTIAL AMPLIFIER WITH A CURRENT MIRROR LOAD

Voltage Transfer Characteristic of the Differential Amplifier

In order to obtain the voltage transfer characteristic, a load for the differential amplifier must be defined. We will select a current mirror load as illustrated below.

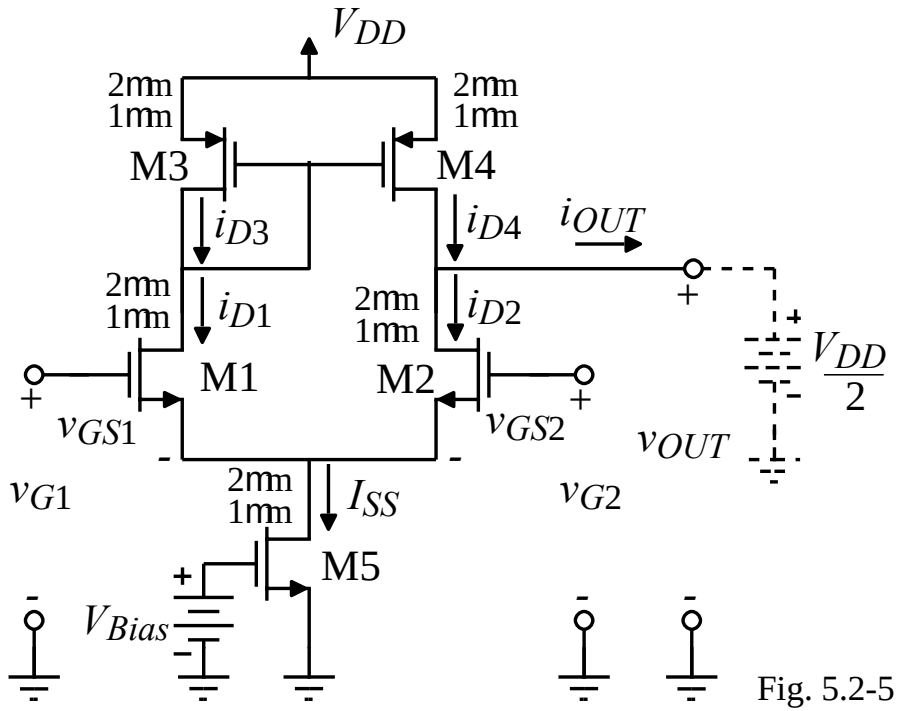


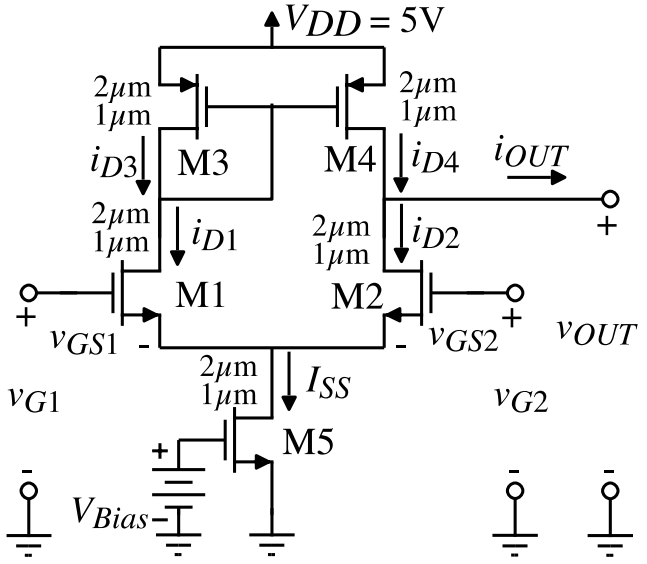
Fig. 5.2-5

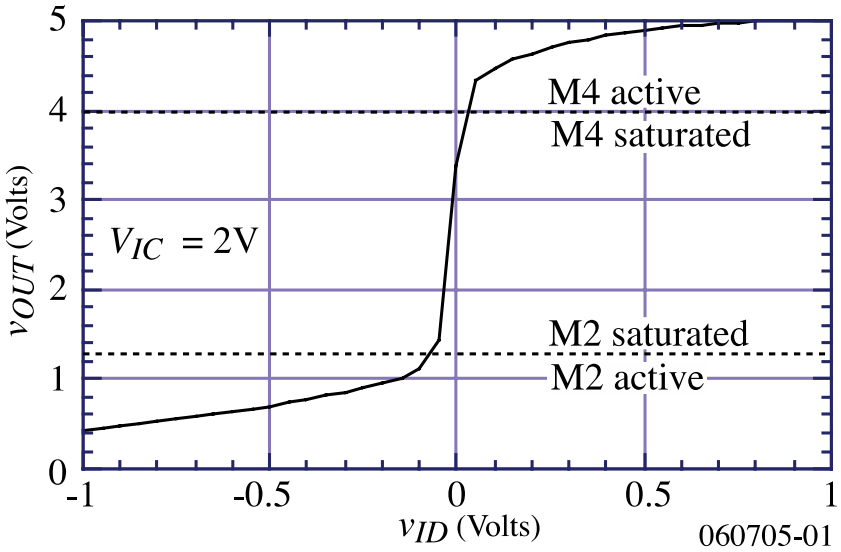
Note that output signal to ground is equivalent to the differential output signal due to the current mirror.

The short-circuit, transconductance is given as

$$g_m = \frac{di_{OUT}}{dv_{ID}}(V_{ID}=0) = \sqrt{\beta I_{SS}} = \sqrt{\frac{K'_1 I_{SS} W_1}{L_1}}$$

Voltage Transfer Function of the Differential Amplifer with a Current Mirror Load





Regions of operation of the transistors:

M2 is saturated when,

$$v_{DS2} \geq v_{GS2} - V_{TN} \rightarrow v_{OUT} - V_{S1} \geq V_{IC} - 0.5v_{ID} - V_{S1} - V_{TN} \rightarrow v_{OUT} \geq V_{IC} - V_{TN}$$

where we have assumed that the region of transition for M2 is close to $v_{ID} = 0$V.

M4 is saturated when,

$$v_{SD4} \geq v_{SG4} - |V_{TP}| \rightarrow V_{DD} - v_{OUT} \geq V_{SG4} - |V_{TP}| \rightarrow v_{OUT} \leq V_{DD} - V_{SG4} + |V_{TP}|$$

The regions of operations shown on the voltage transfer function assume $I_{SS} = 100\mu A$.

Note: $V_{SG4} = \sqrt{\frac{2 \cdot 50}{50 \cdot 2}} + |V_{TP}| = 1 + |V_{TP}| \quad \Rightarrow \quad v_{OUT} \leq 5 - 1 - 0.7 + 0.7 = 4V$

Input Common Mode Range (ICMR)

ICMR is found by setting $v_{ID} = 0$ and varying v_{IC} until one of the transistors leaves the saturation.

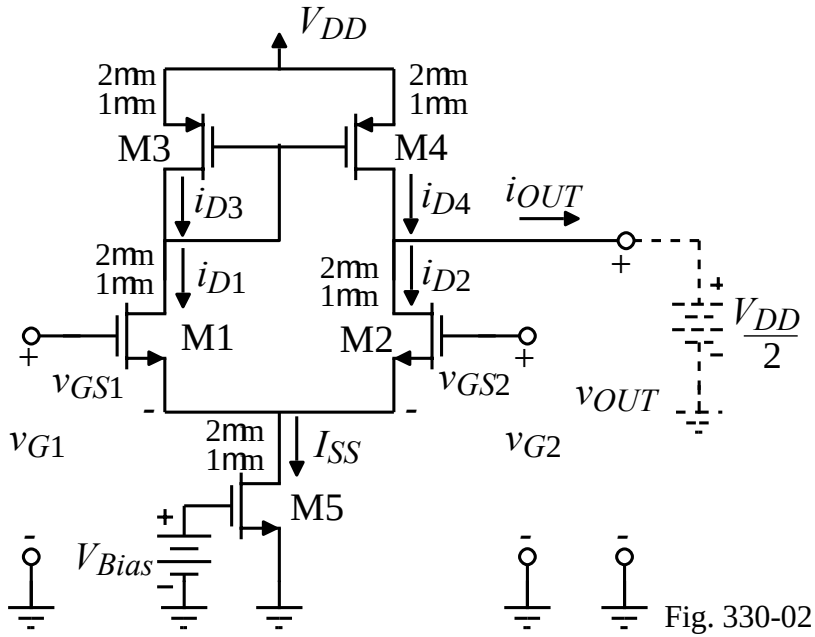


Fig. 330-02

Highest Common Mode Voltage

Path from G1 through M1 and M3 to V_{DD}:

$$V_{IC}(\max) = V_{G1}(\max) = V_{G2}(\max)$$
$$= V_{DD} - V_{SG3} - V_{DS1}(\text{sat}) + V_{GS1}$$

or

$$V_{IC}(\max) = V_{DD} - V_{SG3} + V_{TN1}$$

Path from G2 through M2 and M4 to V_{DD}:

$$V_{IC}(\max)' = V_{DD} - V_{SD4}(\text{sat}) - V_{DS2}(\text{sat}) + V_{GS2}$$
$$= V_{DD} - V_{SD4}(\text{sat}) + V_{TN2}$$

$\therefore$ $\boxed{V_{IC}(\max) = V_{DD} - V_{SG3} + V_{TN1}}$

Lowest Common Mode Voltage (Assume a V_{SS} for generality)

$$\boxed{V_{IC}(\min) = V_{SS} + V_{DS5}(\text{sat}) + V_{GS1} = V_{SS} + V_{DS5}(\text{sat}) + V_{GS2}}$$

where we have assumed that $V_{GS1} = V_{GS2}$ during changes in the input common mode voltage.

Small-Signal Analysis of the Differential-Mode of the Diff. Amp

A requirement for differential-mode operation is that the differential amplifier is balanced†.

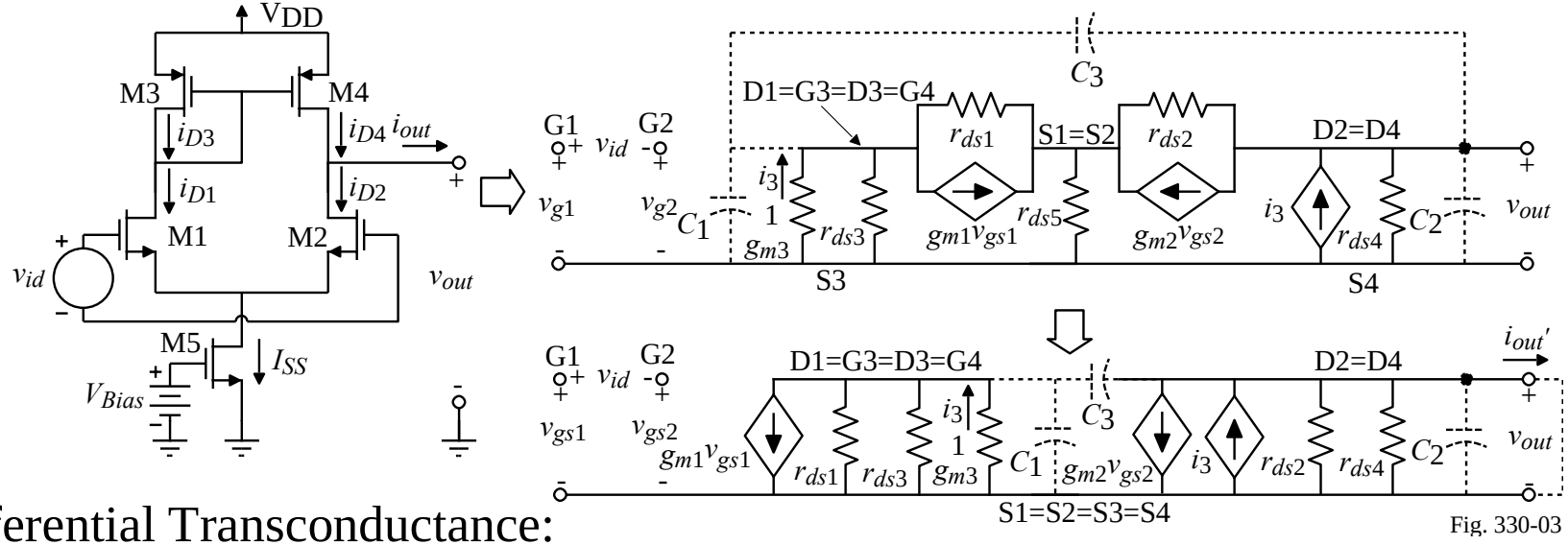


Fig. 330-03

Differential Transconductance:

Assume that the output of the differential amplifier is an ac short.

$$i_{\text{out}}' = \frac{g_{m1}g_{m3}r_{p1}}{1+g_{m3}r_{p1}}v_{gs1} - g_{m2}v_{gs2} \approx g_{m1}v_{gs1} - g_{m2}v_{gs2} = g_{md}v_{id}$$

where $g_{m1} = g_{m2} = g_{md}$, $r_{p1} = r_{ds1} \,||\, r_{ds3}$ and i'_{out} designates the output current into a short circuit.

† It can be shown that the current mirror causes this requirement to be invalid because the drain loads are not matched. However, we will continue to use the assumption regardless.

Small-Signal Analysis of the Differential-Mode of the Diff. Amplifier - Continued

Output Resistance:

$$r_{out} = \frac{1}{g_{ds2} + g_{ds4}} = r_{ds2} \| r_{ds4}$$

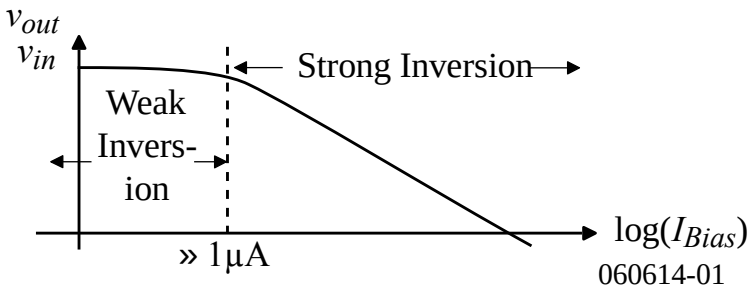
Differential Voltage Gain:

$$A_v = \frac{v_{out}}{v_{id}} = \frac{g_{md}}{g_{ds2} + g_{ds4}}$$

If we assume that all transistors are in saturation and replace the small signal parameters of g_m and r_{ds} in terms of their large-signal model equivalents, we achieve

$$A_v = \frac{v_{out}}{v_{id}} = \frac{(K'_1 I_{SS} W_1/L_1)^{1/2}}{(\lambda_2 + \lambda_4)(I_{SS}/2)} = \frac{2}{\lambda_2 + \lambda_4}\left(\frac{K'_1 W_1}{I_{SS} L_1}\right)^{1/2} \propto \frac{1}{\sqrt{I_{SS}}}$$

Note that the small-signal gain is inversely proportional to the square root of the bias current!



Example:

If W_1/L_1 = 2μm/1μm and I_{SS} = 50μA (10μA), then

A_v(n-channel) = 46.6V/V (104.23V/V)

A_v(p-channel) = 31.4V/V (70.27V/V)

$$r_{out} = \frac{1}{g_{ds2} + g_{ds4}} = \frac{1}{25\mu A \cdot 0.09 V^{-1}} = 0.444 M\Omega \ (2.22 M\Omega)$$

Common Mode Analysis for the Current Mirror Load Differential Amplifier

The current mirror load differential amplifier is not a good example for common mode analysis because the current mirror rejects the common mode signal.

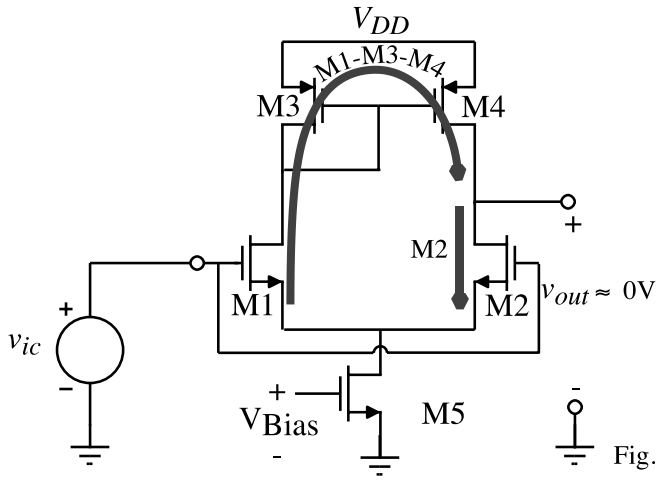


Fig. 5.2-8A

$$\begin{bmatrix}\text{Total common}\\ \text{mode Output}\\ \text{due to } v_{ic}\end{bmatrix} = \begin{bmatrix}\text{Common mode}\\ \text{output due to}\\ \text{M1-M3-M4 path}\end{bmatrix} - \begin{bmatrix}\text{Common mode}\\ \text{output due to}\\ \text{M2 path}\end{bmatrix}$$

Therefore:

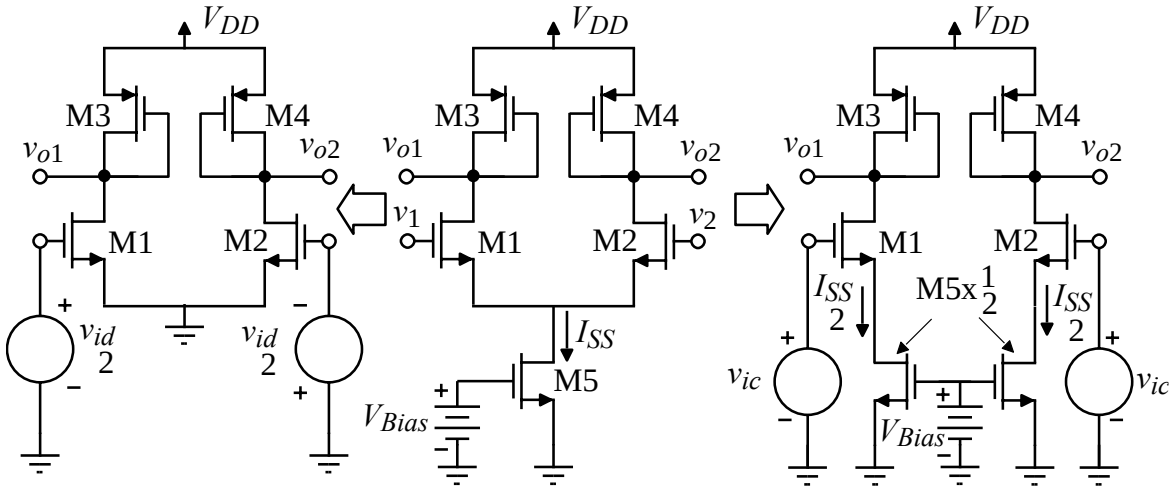
- The common mode output voltage should ideally be zero.
- Any voltage that exists at the output is due to mismatches in the gain between the two different paths.

DIFFERENTIAL AMPLIFIER WITH MOS DIODE LOADS

Small-Signal Analysis of the Common-Mode of the Differential Amplifier

The common-mode gain of the differential amplifier with a current mirror load is ideally zero.

To illustrate the common-mode gain, we need a different type of load so we will consider the following:



Differential-Mode Analysis:

$$\frac{v_{o1}}{v_{id}} \approx -\frac{g_{m1}}{2g_{m3}} \qquad \text{and} \quad \frac{v_{o2}}{v_{id}} \approx +\frac{g_{m2}}{2g_{m4}}$$

Note that these voltage gains are half of the active load inverter voltage gain.

Small-Signal Analysis of the Common-Mode of the Differential Amplifier – Cont'd

Common-Mode Analysis:

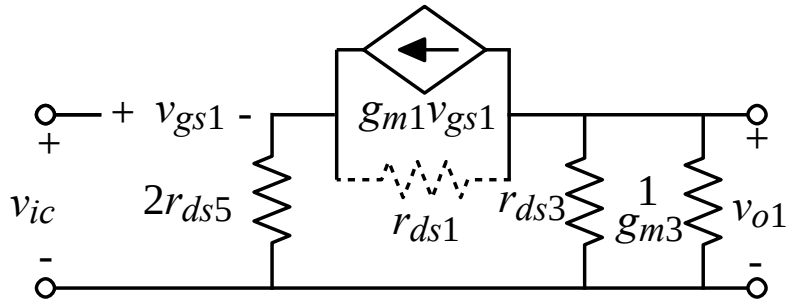


Fig. 330-06

Assume that r_{ds1} is large and can be ignored (greatly simplifies the analysis).

$\therefore \quad v_{gs1} = v_{g1} - v_{s1} = v_{ic} - 2g_{m1}r_{ds5}v_{gs1}$

Solving for v_{gs1} gives

$$v_{gs1} = \frac{v_{ic}}{1 + 2g_{m1}r_{ds5}}$$

The single-ended output voltage, v_{o1}, as a function of v_{ic} can be written as

$$\frac{v_{o1}}{v_{ic}} = -\frac{g_{m1}[r_{ds3}\|(1/g_{m3})]}{1 + 2g_{m1}r_{ds5}} \approx -\frac{(g_{m1}/g_{m3})}{1 + 2g_{m1}r_{ds5}} \approx -\frac{g_{ds5}}{2g_{m3}}$$

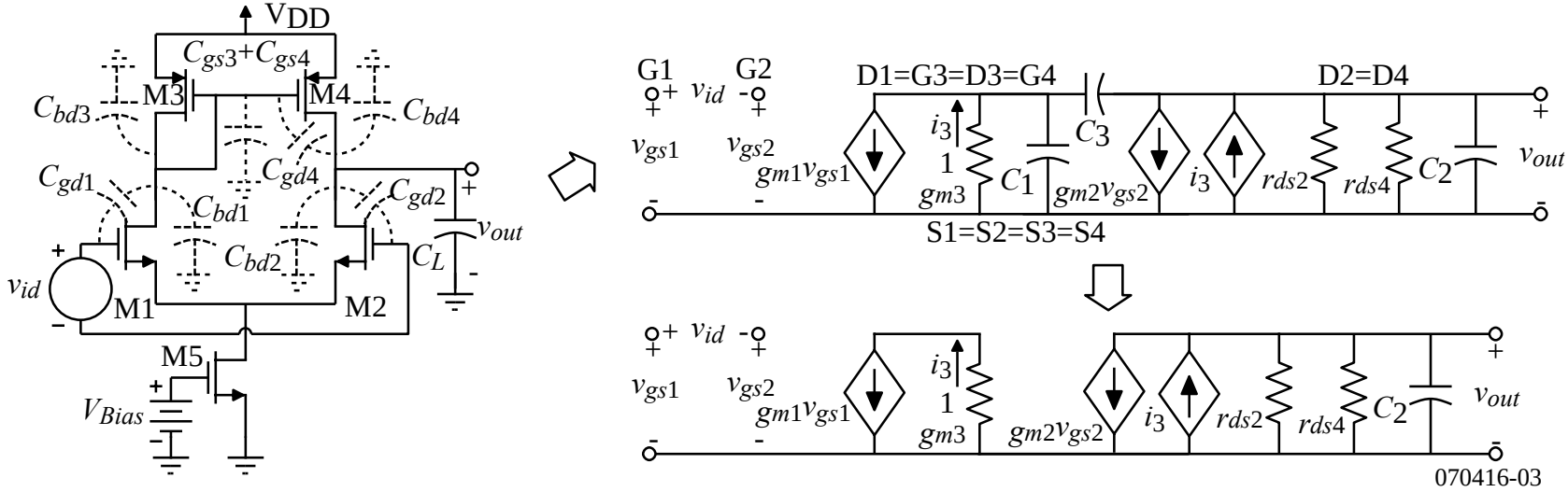
Common-Mode Rejection Ratio (*CMRR*):

$$CMRR = \frac{|v_{o1}/v_{id}|}{|v_{o1}/v_{ic}|} = \frac{g_{m1}/2g_{m3}}{g_{ds5}/2g_{m3}} = g_{m1}r_{ds5}$$

How could you easily increase the *CMRR* of this differential amplifier?

Frequency Response of the Differential Amplifier

Back to the current mirror load differential amplifier:



Ignore the zeros that occur due to C_{gd1}, C_{gd2} and C_{gd4}.

$C_1 = C_{gd1}+C_{bd1}+C_{bd3}+C_{gs3}+C_{gs4}$, $C_2 = C_{bd2}+C_{bd4}+C_{gd2}+C_L$ and $C_3 = C_{gd4}$

The poles are $p_1 = -g_{m3}/C_1$ and $p_2 = -(g_{ds2}+g_{ds4})/C_2$. Since $|p_1| >> |p_2|$, then we can write

$$V_{out}(s) \approx \frac{g_{m1}}{g_{ds2}+g_{ds4}}\left(\frac{\omega_2}{s+\omega_2}\right)[V_{gs1}(s) - V_{gs2}(s)] \quad \text{where } \omega_2 \approx \frac{g_{ds2}+g_{ds4}}{C_2}$$

The approximate frequency response of the differential amplifier reduces to

$$\frac{V_{out}(s)}{V_{id}(s)} \cong \left(\frac{g_{m1}}{g_{ds2}+g_{ds4}}\right)\left(\frac{\omega_2}{s+\omega_2}\right)$$

SMALL SIGNAL PERFORMANCE OF THE DIFFERENTIAL AMPLIFIER

Simplification of Small Signal Analysis

Small signal analysis is used so often in analog circuit design that it becomes desirable to find faster ways of performing this important analysis.

Intuitive Analysis (or Schematic Analysis)

Technique:

1.) Identify the transistor(s) that convert the input voltage to current (these transistors are called *transconductance transistors*).

2.) Trace the currents to where they flow into an equivalent resistance to ground.

3.) Multiply this resistance by the current to get the voltage at this node to ground.

4.) Repeat this process until the output is reached.

Simple Example:

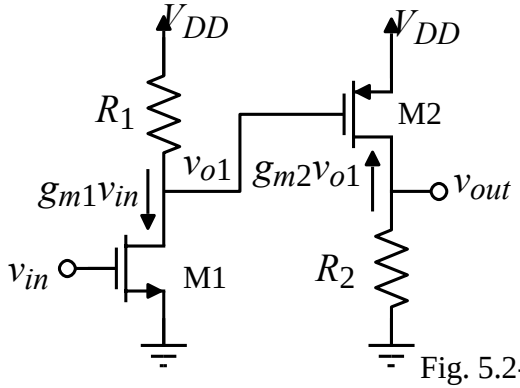


Fig. 5.2-10C

$$v_{o1} = -(g_{m1}v_{in})\,R_1 \quad \rightarrow \quad v_{out} = -(g_{m2}v_{o1})R_2 \quad \rightarrow \quad v_{out} = (g_{m1}R_1 g_{m2}R_2)v_{in}$$

Intuitive Analysis of the Current-Mirror Load Differential Amplifier

1.) $i_1 = 0.5g_{m1}v_{id}$ and $i_2 = -0.5g_{m2}v_{id}$

2.) $i_3 = i_1 = 0.5g_{m1}v_{id}$

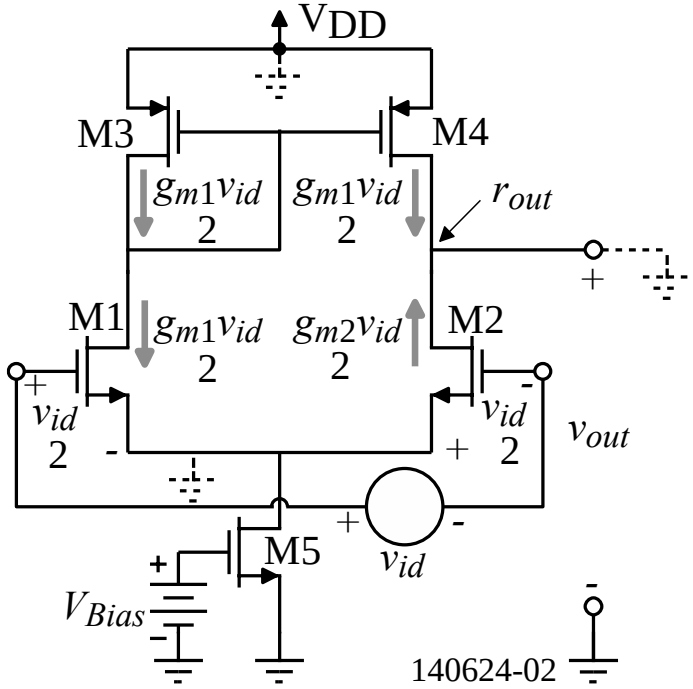
3.) $i_4 = i_3 = 0.5g_{m1}v_{id}$

4.) The short-circuit output current is

$i_4 - i_2 = 0.5g_{m1}v_{id} + 0.5g_{m2}v_{id} = g_{m1}v_{id}$

4.) The resistance at the output node, r_{out}, is

$r_{ds2} \| r_{ds4}$ or $\dfrac{1}{g_{ds2} + g_{ds4}}$



5.) $\therefore \; v_{out} = (0.5g_{m1}v_{id} + 0.5g_{m2}v_{id})r_{out}$

$$= \frac{g_{m1}v_{in}}{g_{ds2}+g_{ds4}} = \frac{g_{m2}v_{in}}{g_{ds2}+g_{ds4}} \quad \Rightarrow \quad \frac{v_{out}}{v_{in}} = \frac{g_{m1}}{g_{ds2}+g_{ds4}}$$

Some Concepts to Help Extend the Intuitive Method of Small-Signal Analysis

1.) Approximate the output resistance of any cascode circuit as

$$R_{out} \approx (g_{m2}r_{ds2})r_{ds1}$$

where M1 is a transistor cascoded by M2.

2.) If there is a resistance, R, in series with the source of the transconductance transistor, let the effective transconductance be

$$g_{m(eff)} = \frac{g_m}{1+g_mR}$$

Proof:

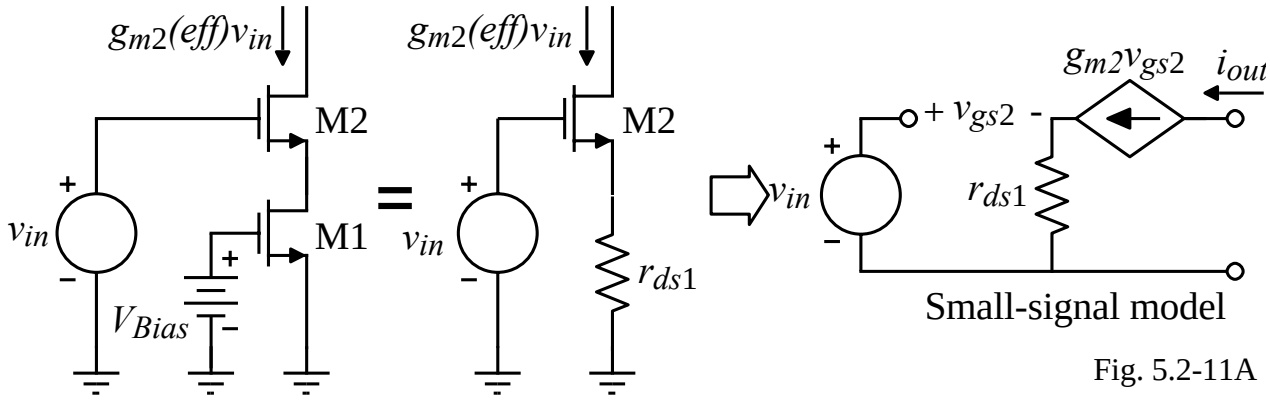


Fig. 5.2-11A

$$\therefore\ v_{gs2} = v_{g2} - v_{s2} = v_{in} - (g_{m2}r_{ds1})v_{gs2} \Rightarrow v_{gs2} = \frac{v_{in}}{1+g_{m2}r_{ds1}}$$

Thus, $i_{out} = \dfrac{g_{m2} v_{in}}{1 + g_{m2} r_{ds1}} = g_{m2}(eff)\, v_{in}$

Noise Analysis of the Differential Amplifier

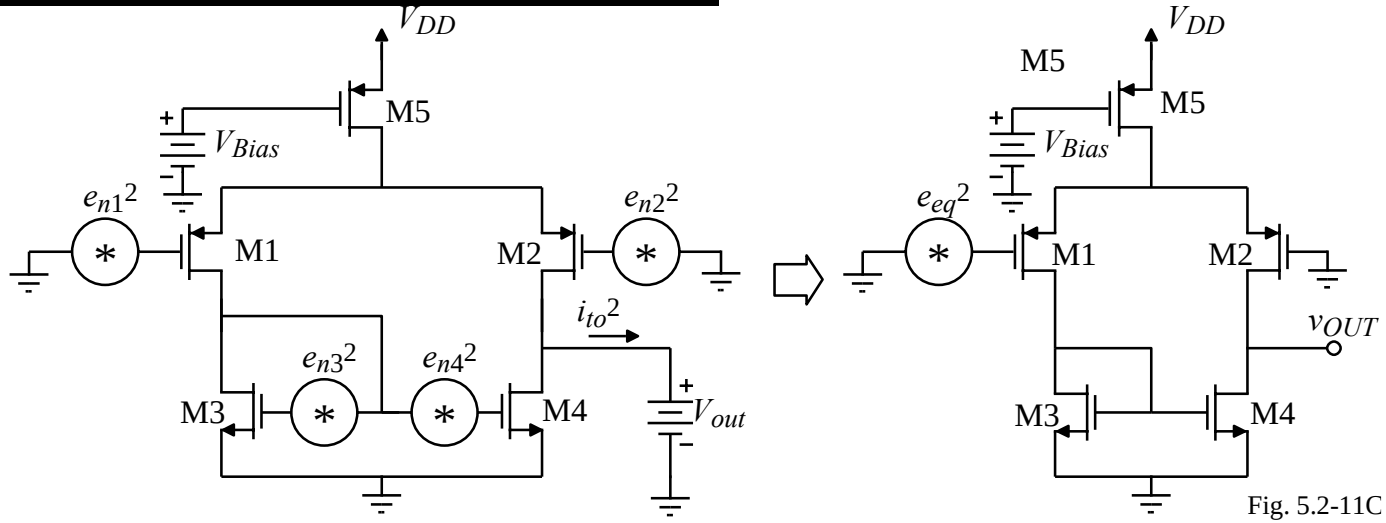


Fig. 5.2-11C

Solve for the total output-noise current to get,

$$i_{to}^2 = g_{m1}^2 e_{n1}^2 + g_{m2}^2 e_{n2}^2 + g_{m3}^2 e_{n3}^2 + g_{m4}^2 e_{n4}^2$$

This output-noise current can be expressed in terms of an equivalent input noise voltage, e_{eq}^2, given as $i_{to}^2 = g_{m1}^2 e_{eq}^2$

Equating the above two expressions for the total output-noise current gives,

$$e_{eq}^2 = e_{n1}^2 + e_{n2}^2 + \left(\frac{g_{m3}}{g_{m1}}\right)^2 \left[e_{n3}^2 + e_{n4}^2\right]$$

1/f Noise ($e_{n1}^2 = e_{n2}^2$ and $e_{n3}^2 = e_{n4}^2$):

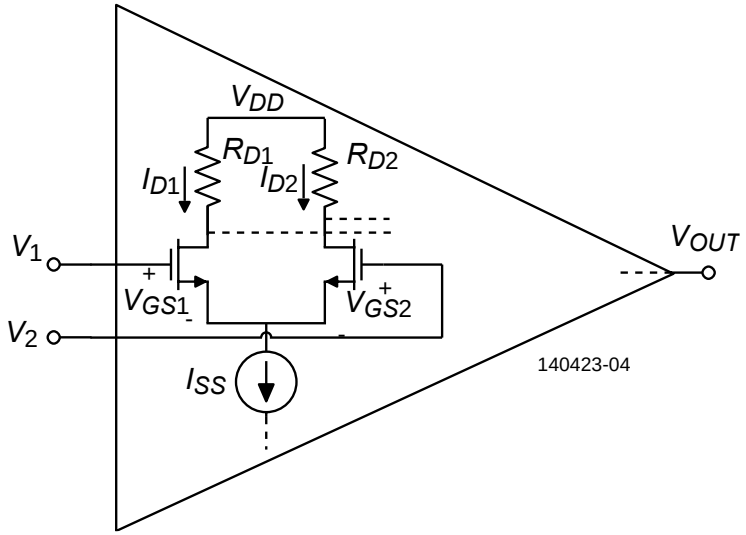
$$e_{eq}^2(1/f) = \frac{2B_P}{fW_1L_1}\left[1 + \left(\frac{K'_N B_N}{K'_P B_P}\right)\left(\frac{L_1}{L_3}\right)^2\right]$$

Thermal Noise ($e_{n1}^2 = e_{n2}^2$ and $e_{n3}^2 = e_{n4}^2$):

$$e_{eq}^2(th) = \frac{16kT}{3[2K'_1(W/L)_1 I_1]^{1/2}}\left[1 + \sqrt{\frac{W_3L_1K'_3}{L_3W_1K'_1}}\right]$$

CMOS Input Offset Voltage - Strong Inversion

Circuit:



Input Offset Voltage:

$$V_{IO} = V_{GS1} - V_{GS2} = V_{T1} - V_{T2} + \sqrt{\left(\frac{2I_{D1}}{K'}\cdot\frac{L_1}{W_1}\right)} - \sqrt{\left(\frac{2I_{D2}}{K'}\cdot\frac{L_2}{W_2}\right)}$$

But $I_{D1}R_{D1} = I_{D2}R_{D2}$, therefore

$$V_{IO} = \Delta V_T + \sqrt{\frac{2L_1}{W_1}}\left[\sqrt{I_{D2}R_{D2}} - \sqrt{\frac{I_{D2}}{K_2}}\right] = \Delta V_T + \sqrt{\frac{2I_DL_1}{W_1}}\left[\sqrt{\frac{R_{D2}}{K_1R_{D1}}} - \sqrt{\frac{1}{K_2}}\right]$$

where $I_{D1} \approx I_{D2} = I_D$ and $\Delta V_T = V_{T1}\text{-}V_{T2}$.

Assuming matched geometries, $W_1/L_1 = W_2/L_2 = W/L$,

$$V_{IO} = \Delta V_T + \sqrt{\frac{2I_DL}{W}}\left[\sqrt{\frac{R_{D2}}{K_1R_{D1}}} - \sqrt{\frac{1}{K_2}}\right]$$

CMOS Input Offset Voltage - Strong Inversion

Define the following,

$$R_{D1} = R + 0.5\Delta R,\ R_{D2} = R - 0.5\Delta R,\ K_1 = K + 0.5\Delta K, \text{ and } K_2 = K - 0.5\Delta K$$

where $R = 0.5(R_{D1} + R_{D2})$, $\Delta R = R_{D1} - R_{D2}$, $K = 0.5(K_1 + K_2)$, and $\Delta K = K_1 - K_2$.

Substituting these relationships into the expression for V_{IO} gives,

$$V_{IO} = \Delta V_T + \sqrt{\frac{2I_D L}{W}}\left[\sqrt{\frac{R - 0.5\Delta R}{(K + 0.5\Delta K)(R + 0.5\Delta R)}} - \sqrt{\frac{1}{K - 0.5\Delta K}}\right]$$

Factoring out R and K gives,

$$V_{IO} = \Delta V_T + \sqrt{\frac{2I_D L}{KW}}\left[\sqrt{\frac{1 - 0.5\Delta R/R}{(1 + 0.5\Delta K/K)(1 + 0.5\Delta R/R)}} - \sqrt{\frac{1}{1 - 0.5\Delta K/K}}\right]$$

Approximating $1/(1 \pm \varepsilon)$ as $1 \mp \varepsilon$ results in,

$$V_{IO} \approx \Delta V_T + \sqrt{\frac{2I_D L}{KW}}\left[\sqrt{(1 - 0.5\Delta R/R)(1 - 0.5\Delta K/K)(1 - 0.5\Delta R/R)} - \sqrt{1 + 0.5\Delta K/K}\right]$$

Finally, multiplying terms and ignoring higher order terms and letting $\sqrt{x} \approx 0.5x$ gives,

$$V_{IO} \approx \Delta V_T - \frac{1}{2}\left[\frac{\Delta R}{R} + \frac{\Delta K}{K}\right]\sqrt{\frac{2I_D L}{KW}} = \Delta V_T - \frac{1}{2}\left[\frac{\Delta R}{R} + \frac{\Delta K}{K}\right](V_{GS} - V_T)$$

CMOS Input Offset Voltage Temperature Drift – Strong Inversion

Assumptions:

Drain current is constant, $\Delta R/R$ and $\Delta K/K$ have very little temperature dependence.

Therefore only ΔV_T and K will considered in the expression below

$$V_{IO} \approx \Delta V_T - \frac{1}{2}\left[\frac{\Delta R}{R} + \frac{\Delta K}{K}\right]\sqrt{\frac{2I_D L}{KW}}$$

Assuming $V_T(T) = V_T(T_o) - \alpha(T - T_o)$ and $K(T) = kT^{-1.5}$, then we get,

$$\frac{\Delta V_T}{dT} = \frac{d}{dT}\left[V_{T1} - \alpha_1(T - T_o) - V_{T2} + \alpha_2(T - T_o)\right] = \alpha_2 - \alpha_1 = \Delta\alpha \approx 0$$

and

$$\frac{d}{dT}\sqrt{\frac{2I_D L}{KW}} = \sqrt{\frac{2I_D L}{KW}}\left(-\frac{3}{2}\frac{T^{-2.5}}{T^{-1.5}}\right) = -\frac{3}{2T}\sqrt{\frac{2I_D L}{KW}}$$

Therefore,

$$\frac{dV_{IO}}{dT} = \frac{3}{4T}\left[\frac{\Delta R}{R} + \frac{\Delta K}{K}\right]\sqrt{\frac{2I_D L}{KW}} = \frac{3}{4T}\left[\frac{\Delta R}{R} + \frac{\Delta K}{K}\right](V_{GS} - V_T) = \frac{1}{400}\frac{2}{100}\frac{1}{10} = 5\mu V/°C$$

Comments:

When the overdrive is large, the input offset voltage temperature drift will be larger

Typical values of dV_{IO}/dT are 1-10μV/°C

CMOS Input Offset Voltage Temperature Drift – Weak Inversion

Repeating the previous analysis with the following model for the transistors

$$i_D = I_{T1}\frac{W}{L}\exp\left(\frac{V_{GS} - V_T}{nV_t}\right)$$

gives,

$$V_{IO} = V_{GS1} - V_{GS2} = V_{T1} + nV_t \ln\left(\frac{i_{D1}L_1}{I_{T1}W_1}\right) - V_{T2} + nV_t \ln\left(\frac{i_{D2}L_2}{I_{T2}W_2}\right) = \Delta V_T + nV_t \ln\left(\frac{i_{D1}L_1 I_{T2}W_2}{i_{D2}L_2 I_{T1}W_1}\right)$$

But $i_{D1}R_{D1} = i_{D2}R_{D2}$ and $W_1/L_1 = W_2/L_2 = W/L$ which gives,

$$V_{IO} = \Delta V_T + \ln\left(\frac{R_{D2}I_{T2}}{R_{D1}I_{T1}}\right)$$

Define the following,

$R_{D1} = R + 0.5\Delta R$, $R_{D2} = R - 0.5\Delta R$, $I_{T1} = I_T + 0.5\Delta I_T$, and $I_{T2} = I_T - 0.5\Delta I_T$

where $R = 0.5(R_{D1} + R_{D2})$, $\Delta R = R_{D1} - R_{D2}$, $I_T = 0.5(I_{T1} + I_{T2})$, and $\Delta I_T = I_{T1} - I_{T2}$.

Substituting these relationships into the expression for V_{IO} gives,

$$V_{IO} = \Delta V_T + nV_t \ln\left(\frac{(R - 0.5\Delta R)(I_T - 0.5\Delta I_T)}{(R + 0.5\Delta R)(I_T + 0.5\Delta I_T)}\right) = \Delta V_T + nV_t \ln\left(\frac{(1 - 0.5\Delta R/R)(1 - 0.5\Delta I_T/I_T)}{(1 + 0.5\Delta R/R)(1 + 0.5\Delta I_T/I_T)}\right)$$

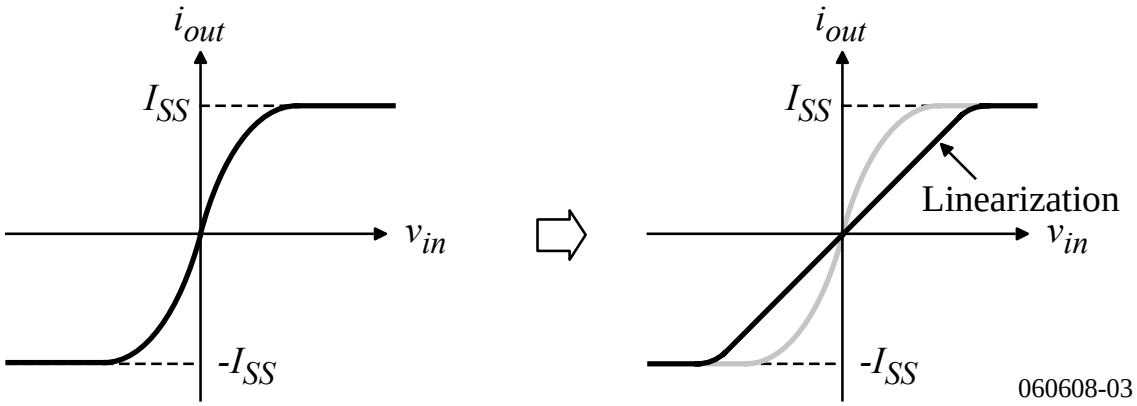
$$\approx \Delta V_T + nV_t \ln\left[(1 - 0.5\Delta R/R)^2(1 - 0.5\Delta I_T/I_T)^2\right] \approx \Delta V_T + nV_t \ln\left[1 - \Delta R/R - \Delta I_T/I_T\right]$$

$$\approx \Delta V_T - nV_t\left(\frac{\Delta R}{R} + \frac{\Delta I_T}{I_T}\right)$$

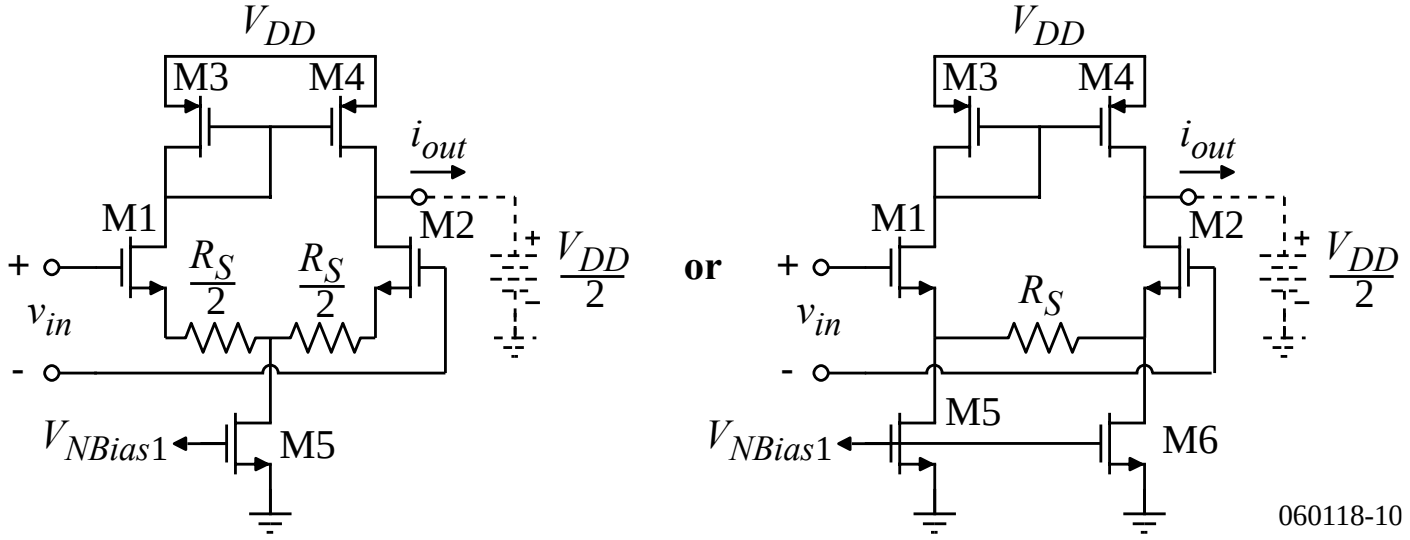
LARGE SIGNAL PERFORMANCE OF THE DIFFERENTIAL AMPLIFIER

Linearization of the Transconductance

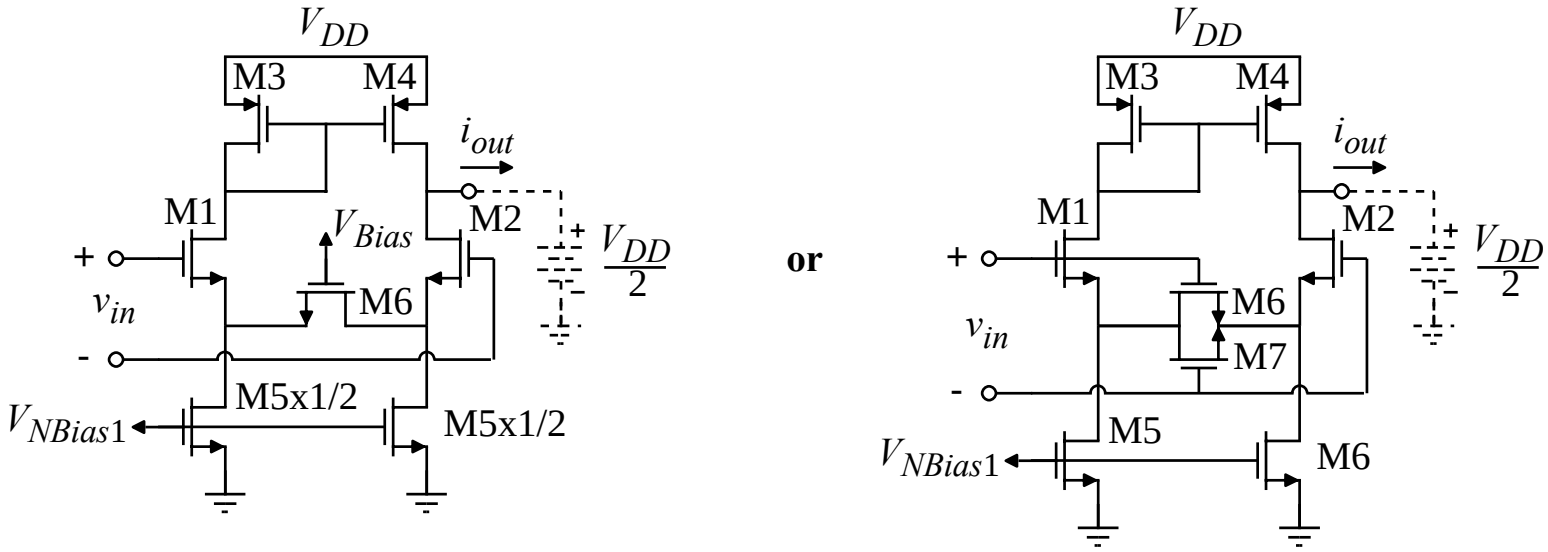
Goal:



Method (degeneration):



Linearization with Active Devices



M6 is in deep triode region 060608-05 M6 and M7 are in the triode region

Note that these transconductors on this slide and the last can all have a varying transconductance by changing the value of I_{SS}.

Slew Rate of the Differential Amplifier

Slew Rate (*SR*) = Maximum output-voltage rate (either positive or negative)

It is caused by, $i_{OUT} = C_L \frac{dv_{OUT}}{dt}$. When i_{OUT} is a constant, the rate is a constant.

Consider the following current-mirror load, differential amplifiers:

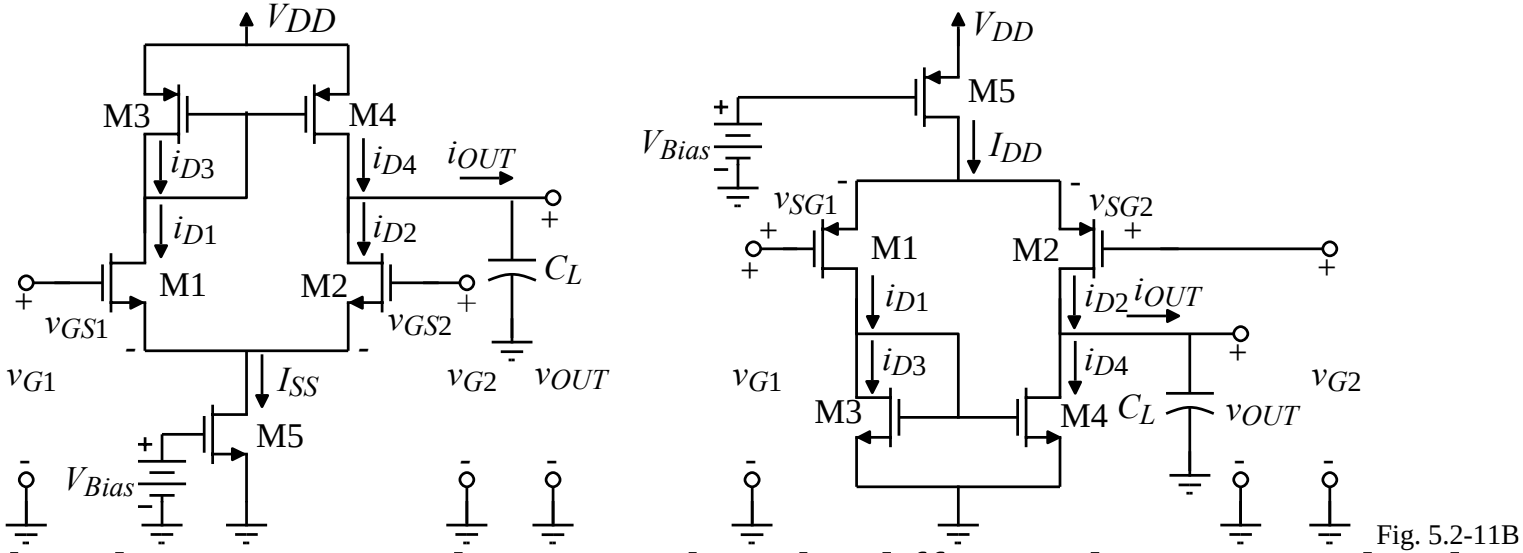


Fig. 5.2-11B

Note that slew rate can only occur when the differential input signal is large enough to cause I_{SS} (I_{DD}) to flow through only one of the differential input transistors.

$$SR = \frac{I_{SS}}{C_L} = \frac{I_{DD}}{C_L} \quad \Rightarrow \quad \text{If } C_L = 5\text{pF and } I_{SS} = 10\mu\text{A, the slew rate is } SR = 2\text{V}/\mu\text{s}.$$

(For the BJT differential amplifier slewing occurs at ±100mV whereas for the MOSFET differential amplifier it can be ±2V or more.)

DIFFERENTIAL AMPLIFIERS WITH CURRENT SOURCE LOADS

Current-Source Load Differential Amplifier

Gives a truly balanced differential amplifier.

Also, the upper input common-mode range is extended.

However, a problem occurs if $I_1 \neq I_3$ or if $I_2 \neq I_4$.

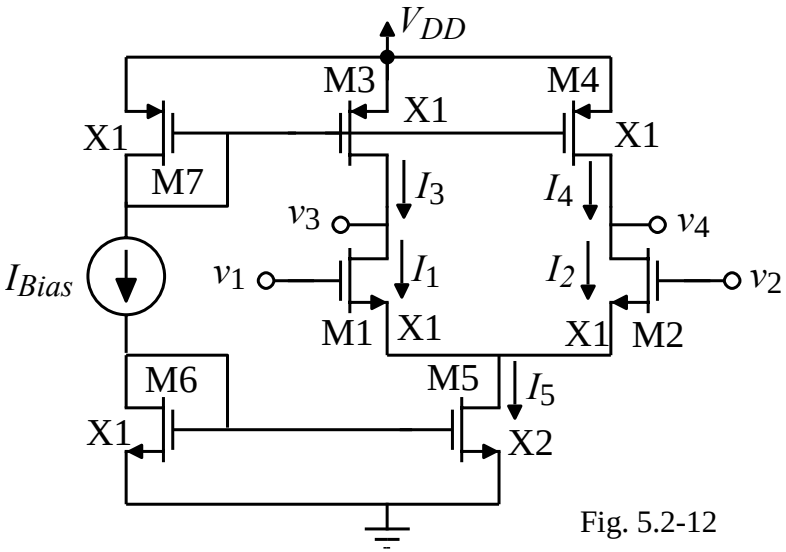
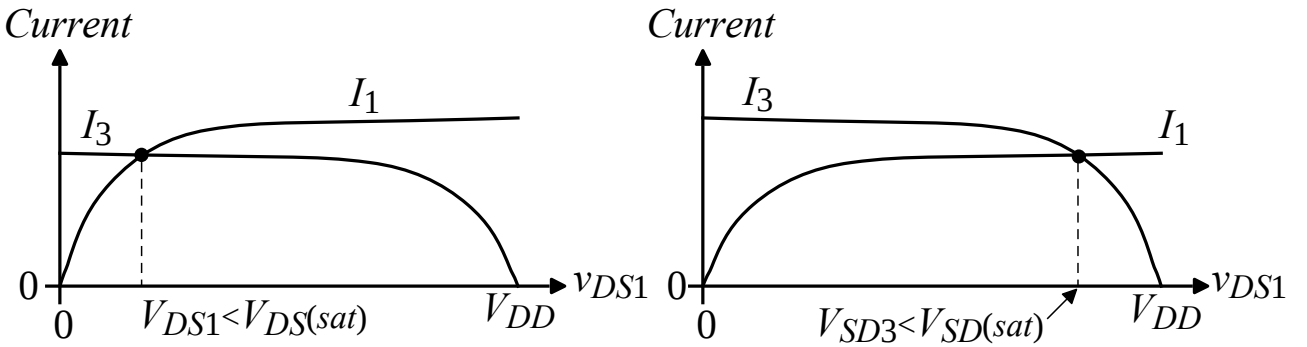


Fig. 5.2-12



(a.) $I_1 > I_3$. (b.) $I_3 > I_1$.

Fig. 5.2-13

A Differential-Output, Differential-Input Amplifier

Probably the best way to solve the current mismatch problem is through the use of common-mode feedback.

Consider the following solution to the previous problem.

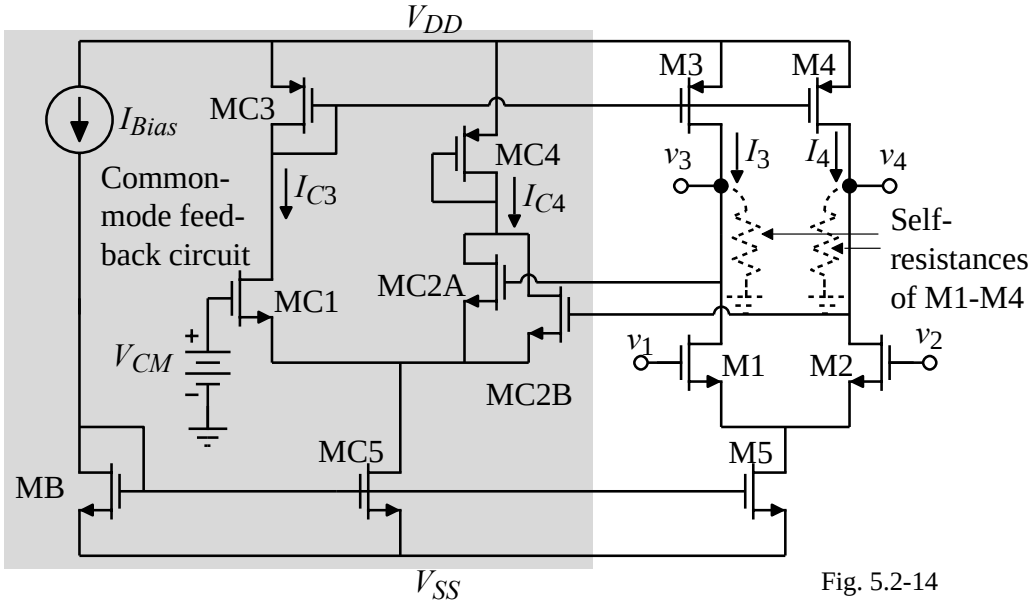


Fig. 5.2-14

Operation:

- Common mode output voltages are sensed at the gates of MC2A and MC2B and compared to V_{CM}.
- The current in MC3 provides the negative feedback to drive the common mode output voltage to the desired level.
- With large values of output voltage, this common mode feedback scheme has flaws.

Common-Mode Stabilization of the Diff.-Output, Diff.-Input Amplifier - Continued

The following circuit avoids the large differential output signal swing problems.

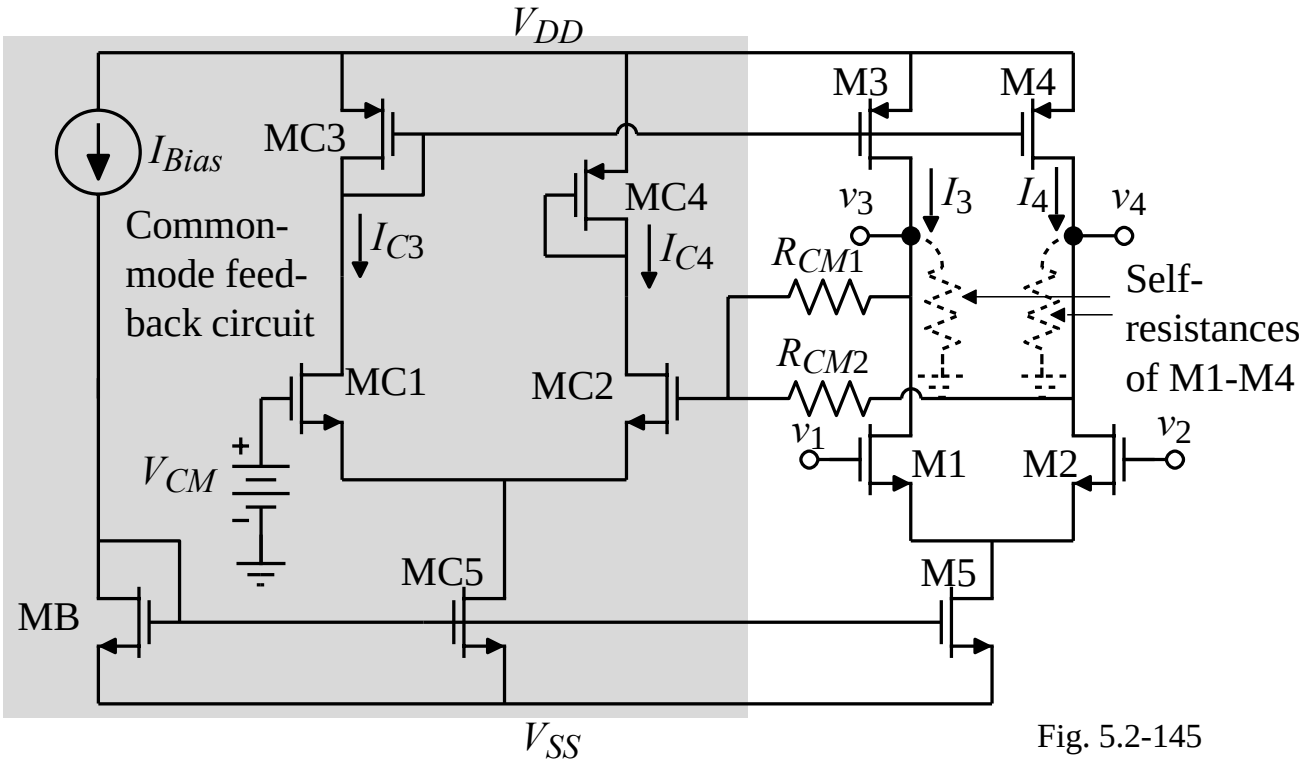


Fig. 5.2-145

Note that R_{CM1} and R_{CM2} must not load the output of the differential amplifier.

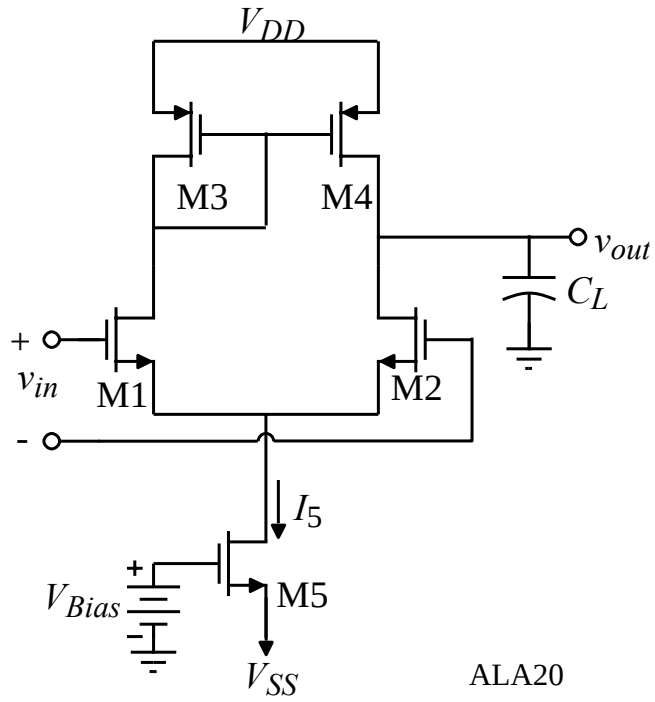
(We will examine more CM feedback schemes in Lecture 28.)

DESIGN OF DIFFERENTIAL AMPLIFIERS

Design of a CMOS Differential Amplifier with a Current Mirror Load

Design Considerations:

Constraints	Specifications
Power supply	Small-signal gain
Technology	Frequency response (C_L)
Temperature	ICMR
	Slew rate (C_L)
	Power dissipation



Relationships

$A_v = g_{m1}R_{out}$

$\omega_{-3dB} = 1/R_{out}C_L$

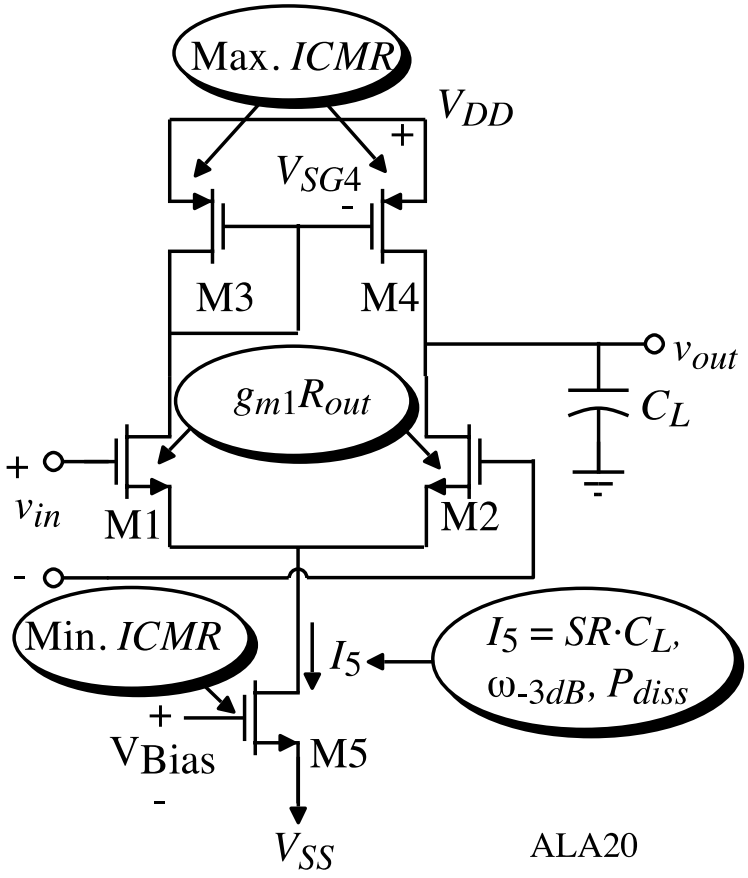
$V_{IC}(\max) = V_{DD} - V_{SG3} + V_{TN1}$

$V_{IC}(\min) = V_{SS} + V_{DS5}(\text{sat}) + V_{GS1} = V_{SS} + V_{DS5}(\text{sat}) + V_{GS2}$

$SR = I_{SS}/C_L$

$P_{diss} = (V_{DD}+|V_{SS}|)\text{x}(\text{All dc currents flowing from } V_{DD} \text{ or to } V_{SS})$

Design of a CMOS Differential Amplifier with a Current Mirror Load - Continued



Schematic-wise, the design procedure is illustrated as shown:

Procedure:

1.) Pick I_{SS} to satisfy the slew rate knowing C_L or the power dissipation

2.) Check to see if R_{out} will satisfy the frequency response, if not change I_{SS} or modify circuit

3.) Design W_3/L_3 (W_4/L_4) to satisfy the upper *ICMR*

4.) Design W_1/L_1 (W_2/L_2) to satisfy the gain

5.) Design W_5/L_5 to satisfy the lower *ICMR*

6.) Iterate where necessary

Example 19-1 - Design of a MOS Differential Amp. with a Current Mirror Load

Design the currents and W/L values of the current mirror load MOS differential amplifier to satisfy the following specifications: $V_{DD} = -V_{SS} = 2.5\text{V}$, $SR \geq 10\text{V/}\mu\text{s}$ (C_L=5pF), $f_{-3\text{dB}} \geq 100\text{kHz}$ (C_L=5pF), a small signal gain of 100V/V, $-1.5\text{V} \leq ICMR \leq 2\text{V}$ and $P_{diss} \leq 1\text{mW}$. Use the parameters of $K_N' = 110\mu\text{A/V}^2$, $K_P' = 50\mu\text{A/V}^2$, $V_{TN} = 0.7\text{V}$, $V_{TP} = -0.7\text{V}$, $\lambda_N = 0.04\text{V}^{-1}$ and $\lambda_P = 0.05\text{V}^{-1}$.

Solution

1.) To meet the slew rate, $I_{SS} \geq 50\mu\text{A}$. For maximum P_{diss}, $I_{SS} \leq 200\mu\text{A}$.

2.) $f_{-3\text{dB}}$ of 100kHz implies that $R_{out} \leq 318\text{k}\Omega$. Therefore $R_{out} = \dfrac{2}{(\lambda_N+\lambda_P)I_{SS}} \leq 318\text{k}\Omega$

$\therefore\ I_{SS} \geq 70\mu\text{A}$ Thus, pick $I_{SS} = 100\mu\text{A}$

3.) $V_{IC}(\text{max}) = V_{DD} - V_{SG3} + V_{TN1} \rightarrow 2\text{V} = 2.5 - V_{SG3} + 0.7$

$$V_{SG3} = 1.2\text{V} = \sqrt{\frac{2\cdot 50\mu\text{A}}{50\mu\text{A/V}^2(W_3/L_3)}} + 0.7$$

$$\therefore\ \frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{2}{(0.5)^2} = 8$$

Example 19-1 - Continued

4.) $100 = g_{m1}R_{out} = \dfrac{g_{m1}}{g_{ds2}+g_{ds4}} = \dfrac{\sqrt{2\cdot 110\mu A/V^2(W_1/L_1)}}{(0.04+0.05)\sqrt{50\mu A}} = 23.31\sqrt{\dfrac{W_1}{L_1}} \rightarrow \dfrac{W_1}{L_1} = \dfrac{W_2}{L_2} = 18.4$

5.) $V_{IC}(\text{min}) = V_{SS} + V_{DS5}(\text{sat}) + V_{GS1}$

$$-1.5 = -2.5 + V_{DS5}(\text{sat}) + \sqrt{\frac{2\cdot 50\mu A}{110\mu A/V^2(18.4)}} + 0.7$$

$$V_{DS5}(\text{sat}) = 0.3 - 0.222 = 0.0777 \Rightarrow \frac{W_5}{L_5} = \frac{2I_{SS}}{K_N' V_{DS5}(\text{sat})^2} = 150.6$$

We probably should increase W_1/L_1 to reduce V_{GS1}. If we choose $W_1/L_1 = 40$, then $V_{DS5}(\text{sat}) = 0.149\text{V}$ and $W_5/L_5 = 41$. (Larger than specified gain should be okay.)

SUMMARY

- Differential amplifiers are compatible with the matching properties of IC technology
- The differential amplifier has two modes of signal operation:
  - Differential mode
  - Common mode
- Differential amplifiers are excellent input stages for voltage amplifiers
- Differential amplifiers can have different loads including:
  - Current mirrors
  - MOS diodes
  - Current sources/sinks
  - Resistors
- The small signal performance of the differential amplifier is similar to the inverting amplifier in gain, output resistance and bandwidth
- The large signal performance includes slew rate and the linearization of the transconductance
- The design of CMOS analog circuits uses the relationships of the circuit to design the dc currents and the W/L ratios of each transistor