LECTURE 16 – CURRENT MIRRORS AND SIMPLE REFERENCES

LECTURE ORGANIZATION

Outline

- MOSFET current mirrors
- Improved current mirrors
- Voltage references with power supply independence
- Current references with power supply independence
- Temperature behavior of voltage and current references

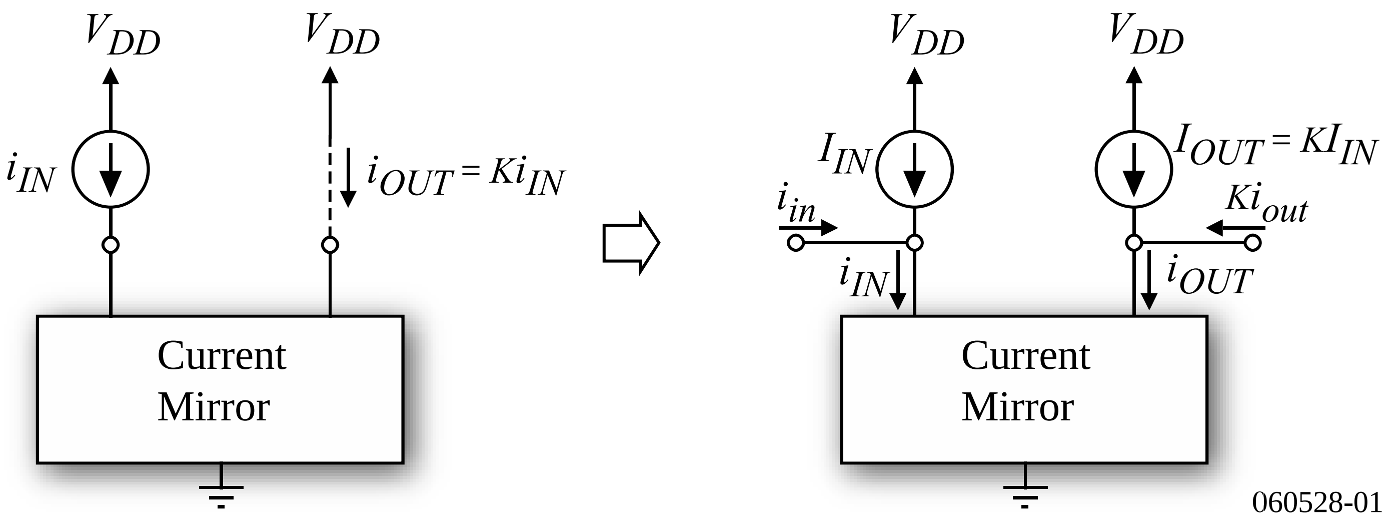
***CMOS Analog Circuit Design*, 3rd Edition Reference**

Pages 138-156

MOSFET CURRENT MIRRORS

What is a Current Mirror?

A current mirror replicates the input current of a current sink or current source as an output current. The output current may be identical to the input current or can be a scaled version of it.



The above current mirrors are referenced with respect to ground. Current mirrors can also be referenced with respect to V_{DD} and can source input and output currents.

Characterization of Current Mirrors

A current mirror is basically nothing more than a current amplifier. The ideal characteristics of a current amplifier are:

- Output current linearly related to the input current, $i_{out} = A_i i_{in}$
- Input resistance is zero
- Output resistance is infinity

Also, the characteristic V_{MIN} applies not only to the output but also the input.

- V_{MIN}(in) is the range of v_{in} over which the input resistance is not small
- V_{MIN}(out) is the range of v_{out} over which the output resistance is not large

Graphically:

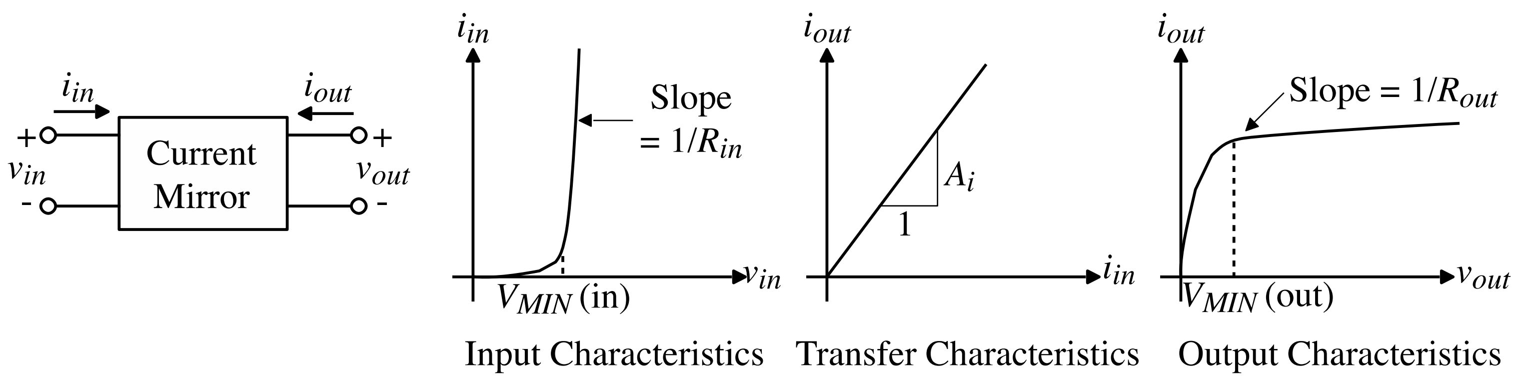


Fig. 300-01

Therefore, R_{out}, R_{in}, V_{MIN}(out), V_{MIN}(in), and A_i will characterize the current mirror.

Simple MOS Current Mirror

Circuit:

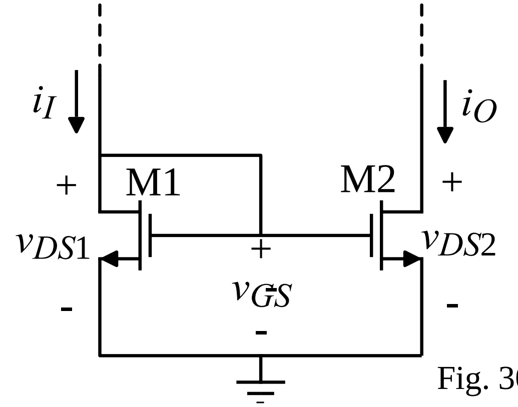


Fig. 300-02

Assume that $v_{DS2} > v_{GS} - V_{T2}$, then

$$\frac{i_O}{i_I} = \left(\frac{L_1W_2}{W_1L_2}\right)\left(\frac{V_{GS}-V_{T2}}{V_{GS}-V_{T1}}\right)^2\left[\frac{1+\lambda v_{DS2}}{1+\lambda v_{DS1}}\left(\frac{K_2'}{K_1'}\right)\right]$$

If the transistors are matched, then $K_1' = K_2'$ and $V_{T1} = V_{T2}$ to give,

$$\frac{i_O}{i_I} = \left(\frac{L_1W_2}{W_1L_2}\right)\left(\frac{1+\lambda v_{DS2}}{1+\lambda v_{DS1}}\right)$$

If $v_{DS1} = v_{DS2}$, then

$$\frac{i_O}{i_I} = \left(\frac{L_1W_2}{W_1L_2}\right)$$

Therefore the sources of error are:

1.) $v_{DS1} \neq v_{DS2}$

2.) M1 and M2 are not matched.

Influence of the Channel Modulation Parameter, λ

If the transistors are matched and the W/L ratios are equal, then

$$\frac{i_O}{i_I} = \frac{1 + \lambda v_{DS2}}{1 + \lambda v_{DS1}}$$

if the channel modulation parameter is the same for both transistors ($L_1 = L_2$).

Ratio error (%) versus drain voltage difference:

Note that one could use this effect to measure λ.

Measure V_{DS1}, V_{DS2}, i_I and i_O and solve the above equation for the channel modulation parameter, λ.

$$\lambda = \frac{\frac{i_O}{i_I} - 1}{v_{DS2} - \frac{i_O}{i_I}\lambda v_{DS1}}$$

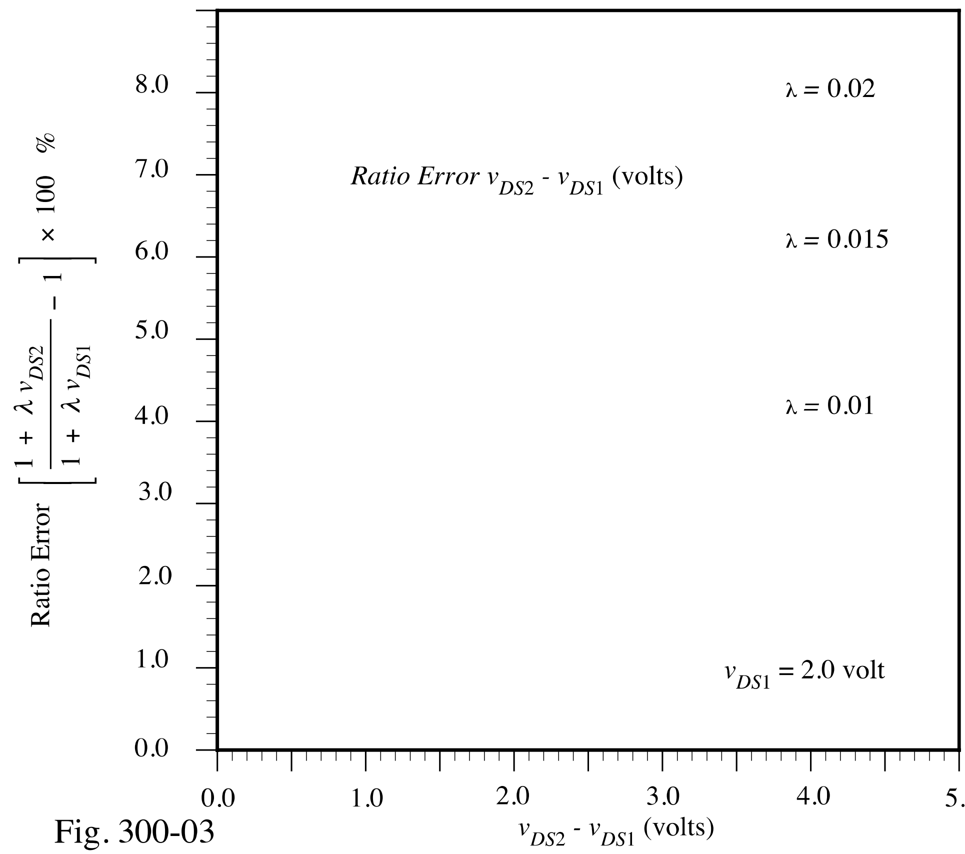
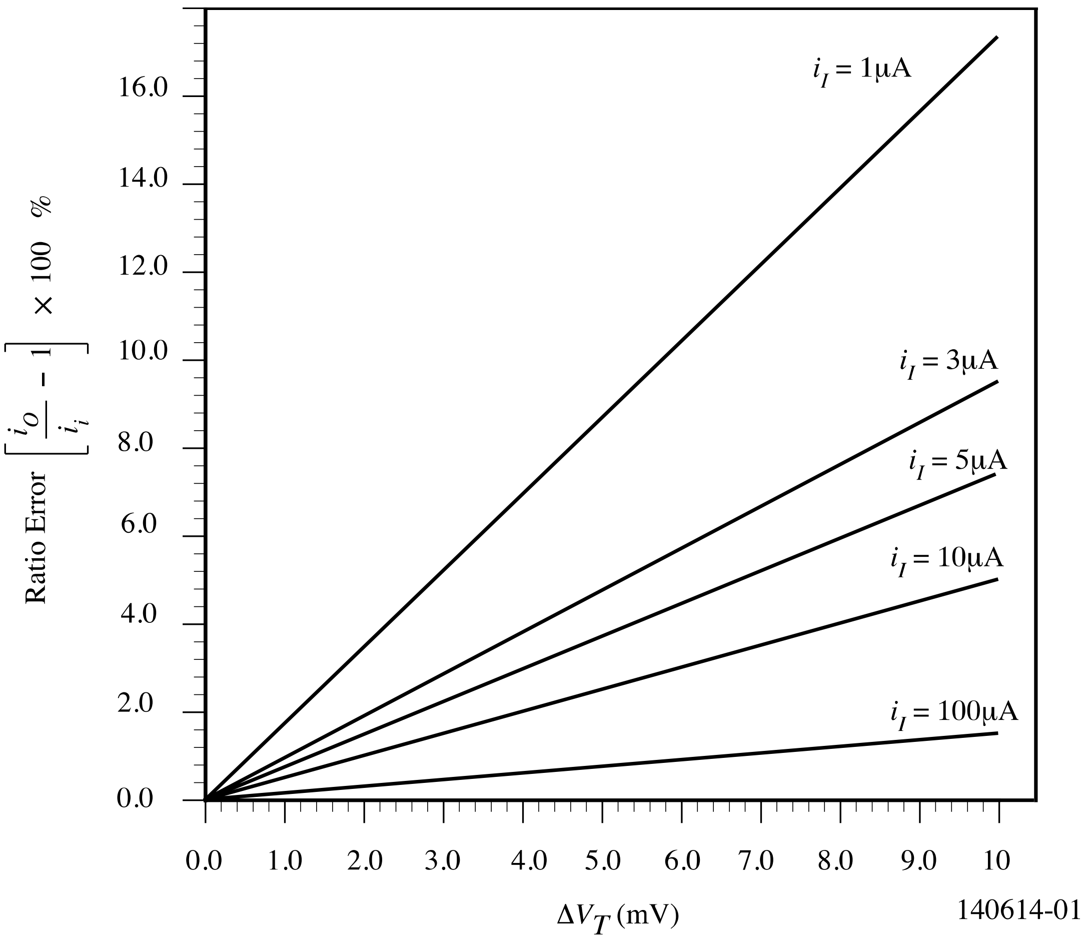


Fig. 300-03

Illustration of the Offset Voltage Error Influence

Assume that V_{T1} = 0.7V and $K'W/L$ = 110μA/V^2.



Key: Make the part of V_{GS} causing the current to flow, V_{ON}, more significant than V_T.

Example 16-1 – Aspect Ratio Errors in Current Mirrors

A layout is shown for a one-to-four current amplifier. Assume that the lengths are identical ($L_1 = L_2$) and find the ratio error if $W_1 = 5 \pm 0.1$ μm. The actual widths of the two transistors are

$$W_1 = 5 \pm 0.1\ \mu\text{m} \quad \text{and} \quad W_2 = 20 \pm 0.1\ \mu\text{m}$$

Solution

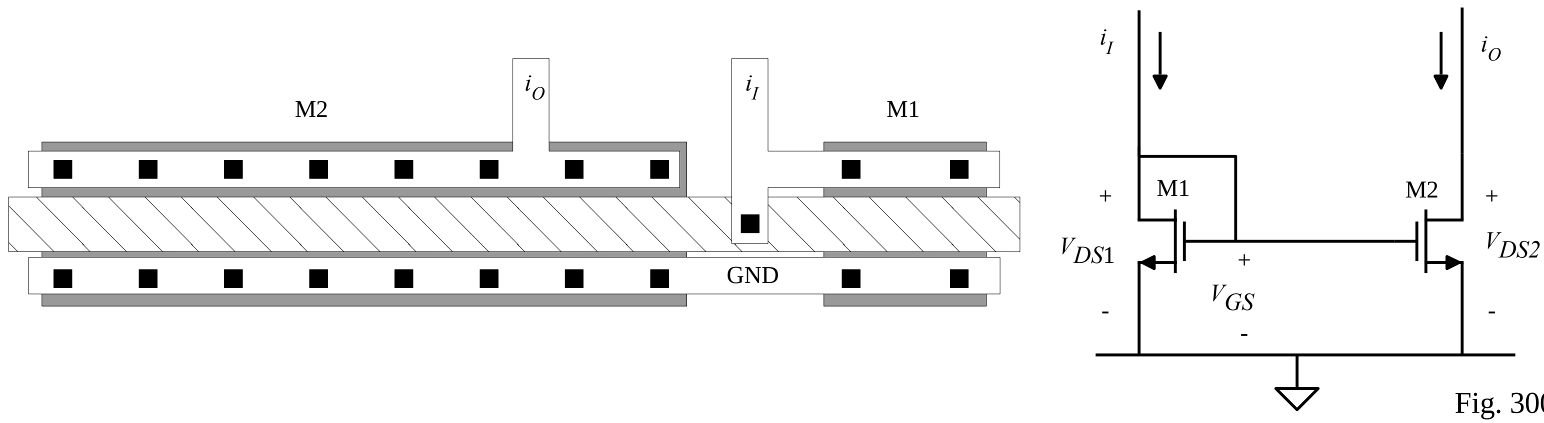


Fig. 300-5

We note that the tolerance is not multiplied by the nominal gain factor of 4.

The ratio of W_2 to W_1 and consequently the gain of the current amplifier is

$$\frac{i_O}{i_I} = \frac{W_2}{W_1} = \frac{20 \pm 0.1}{5 \pm 0.1} = 4\left(\frac{1 \pm (0.1/20)}{1 \pm (0.1/5)}\right) \approx 4\left(1 \pm \frac{0.1}{20}\right)\left(1 - \frac{\pm 0.1}{5}\right) \approx 4\left(1 \pm \frac{0.1}{20} - \frac{\pm 0.4}{20}\right) = 4 - (\pm 0.03)$$

where we have assumed that the variations would both have the same sign (correlated). It is seen that this ratio error is 0.75% of the desired current ratio or gain.

Example 16-2 – Reduction of the Aspect Ratio Errors in Current Mirrors

Use the layout technique illustrated below and calculate the ratio error of a current amplifier having the specifications of the previous example.

Solutions

The actual widths of M1 and M2 are

$$W_1 = 5 \pm 0.1\ \mu\text{m} \quad \text{and} \quad W_2 = 4(5 \pm 0.1)\ \mu\text{m}$$

The ratio of W_2 to W_1 and consequently the current gain is given below and is for all practical purposes independent of layout error.

$$\frac{i_O}{i_I} = \frac{4(5 \pm 0.1)}{5 \pm 0.1} = 4$$

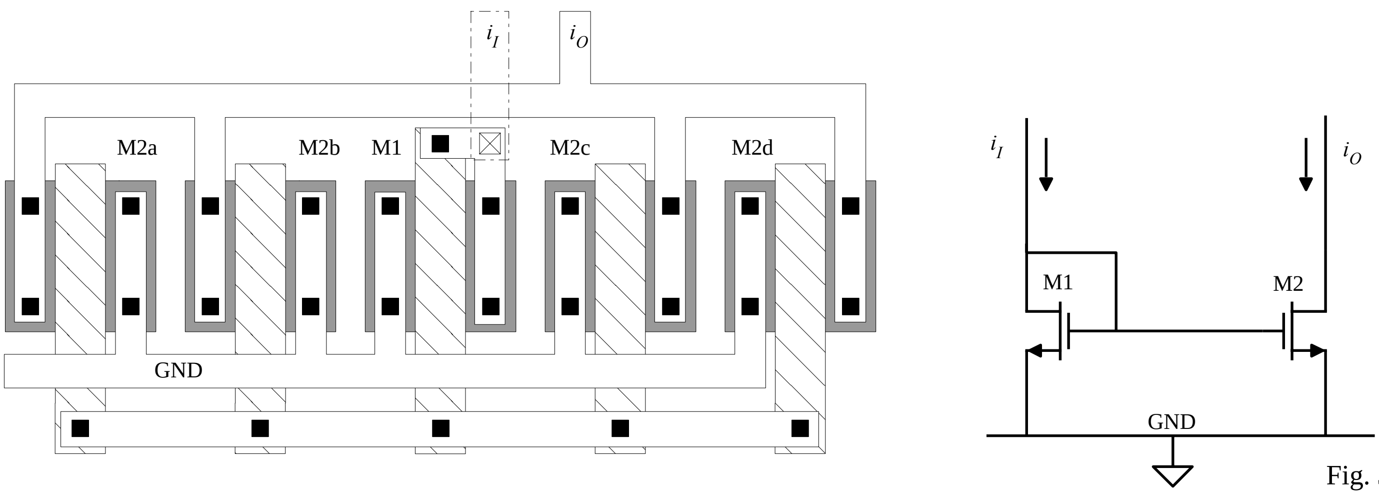


Fig. 300-6

Summary of the Simple MOS Current Mirror/Amplifier

- Minimum input voltage is $V_{MIN}(\text{in}) = V_T + V_{ON}$

    Okay, but could be reduced to V_{ON}.

    Principle:

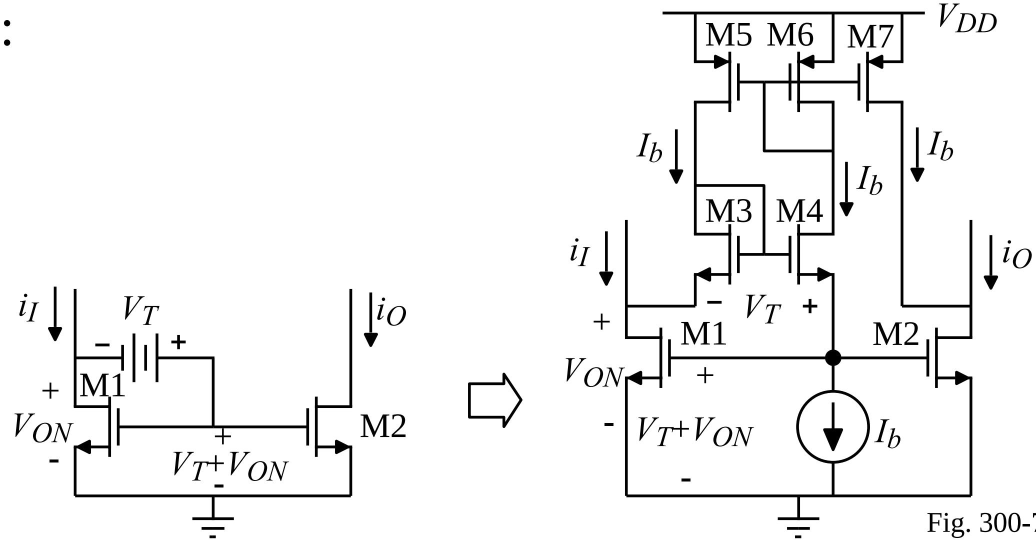


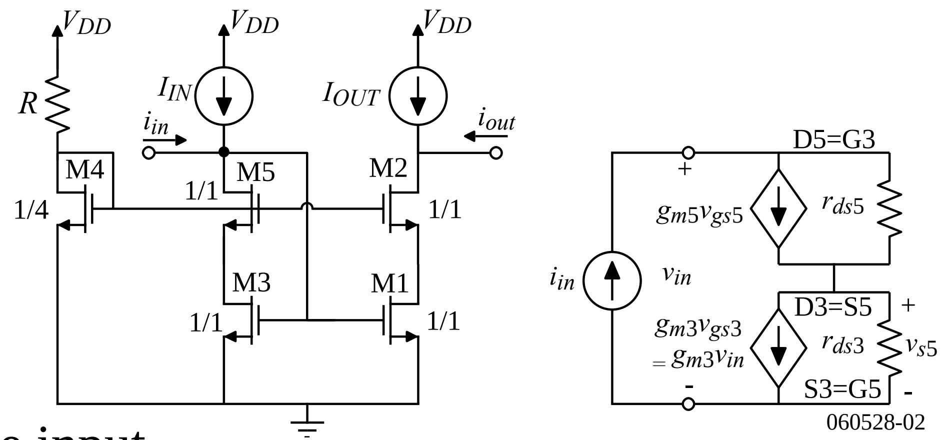
Fig. 300-7

    Will deal with later in low voltage op amps.

- Minimum output voltage is $V_{MIN}(\text{out}) = V_{ON}$
- Output resistance is $R_{out} = \dfrac{1}{\lambda I_D}$
- Input resistance is $R_{in} \approx \dfrac{1}{g_m}$
- Current gain accuracy is poor because $v_{DS1} \neq v_{DS2}$

IMPROVED CURRENT MIRRORS

Large Output Swing Cascode Current Mirror



- $R_{out} \approx g_{m2}r_{ds2}r_{ds1}$
- $R_{in} = \dfrac{v_{in}}{i_{in}} = \dfrac{r_{ds5} + r_{ds3} + r_{ds3}g_{m5}r_{ds5}}{g_{m3}r_{ds3}(1+g_{m5}r_{ds5})} \approx \dfrac{1}{g_{m3}}$

  An easier way to find R_{in}:

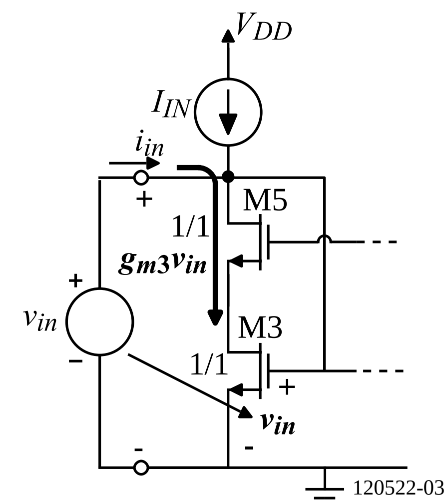
  1.) Apply a small voltage change, v_{in}, at the input.

  2.) Note that this voltage is equal to v_{gs3}.

  3.) This small voltage change causes a current change in the drain of M3 of $g_{m3}v_{gs3}$ or $g_{m3}v_{in}$.

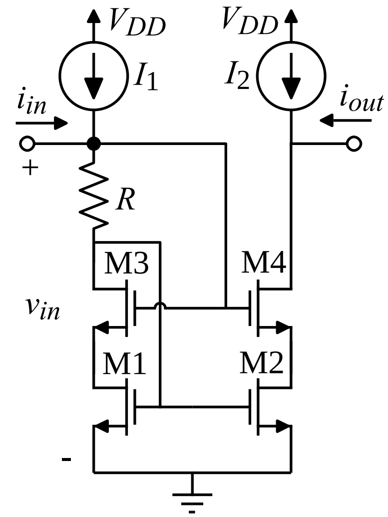
  4.) The current i_{in} is equal to $g_{m3}v_{in}$.

  5.) Therefore, dividing v_{in} by i_{in} gives $R_{in} = 1/g_{m3}$.

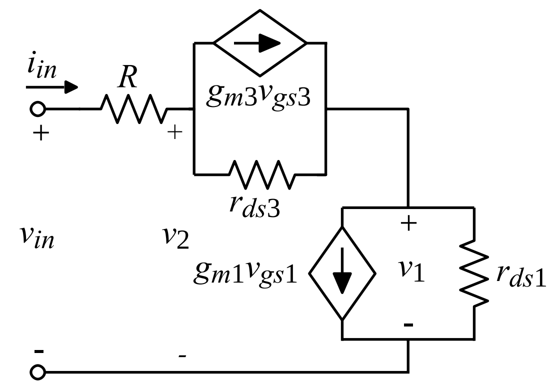


- V_{MIN}(out) = $2V_{ON}$
- V_{MIN}(in) = $V_T + V_{ON}$
- Current gain is excellent because $v_{DS1} = v_{DS3}$.

Self-Biased Cascode Current Mirror



Self-biased, cascode current mirror



Small-signal model to calculate R_{in}.

Fig. 310-03

- R_{in} = ?

$v_{in} = i_{in}R + r_{ds3}(i_{in}\text{-}g_{m3}v_{gs3})$
$\quad + r_{ds1}(i_{in}\text{-}g_{m1}v_{gs1})$

But,

$v_{gs1} = v_{in}\text{-}i_{in}R$

and

$$v_{gs3} = v_{in}\text{-}r_{ds1}(i_{in}\text{-}g_{m1}v_{gs1}) = v_{in}\text{-}r_{ds1}i_{in}+g_{m1}r_{ds1}(v_{in}\text{-}i_{in}R)$$

$$\therefore\ v_{in} = i_{in}R+r_{ds3}i_{in}\text{-}g_{m3}r_{ds3}[v_{in}\text{-}r_{ds1}i_{in}+g_{m1}r_{ds1}(v_{in}\text{-}i_{in}R)]+r_{ds1}[i_{in}\text{-}g_{m1}(v_{in}+i_{in}R)]$$

$$v_{in}[1+g_{m3}r_{ds3}+g_{m1}r_{ds1}g_{m3}r_{ds3}+g_{m1}r_{ds1}]$$
$$= i_{\text{in}}[R+r_{ds1}+r_{ds3}+g_{m3}r_{ds3}r_{ds1}+ g_{m1}r_{ds1}g_{m3}r_{ds3}R]$$

$$R_{in} = \frac{R + r_{ds1} + r_{ds3} + g_{m3}r_{ds3}r_{ds1} + g_{m1}r_{ds1}g_{m3}r_{ds3}R}{1 + g_{m3}r_{ds3} + g_{m1}r_{ds1}g_{m3}r_{ds3} + g_{m1}r_{ds1}} \approx \frac{1}{g_{m1}} + R$$

- $R_{out} \approx g_{m4}r_{ds4}r_{ds2}$
- V_{MIN}(in) = $V_T + 2V_{ON}$ •V_{MIN}(out) = $2V_{ON}$ • Current gain matching is excellent

MOS Regulated Cascode Current Mirror

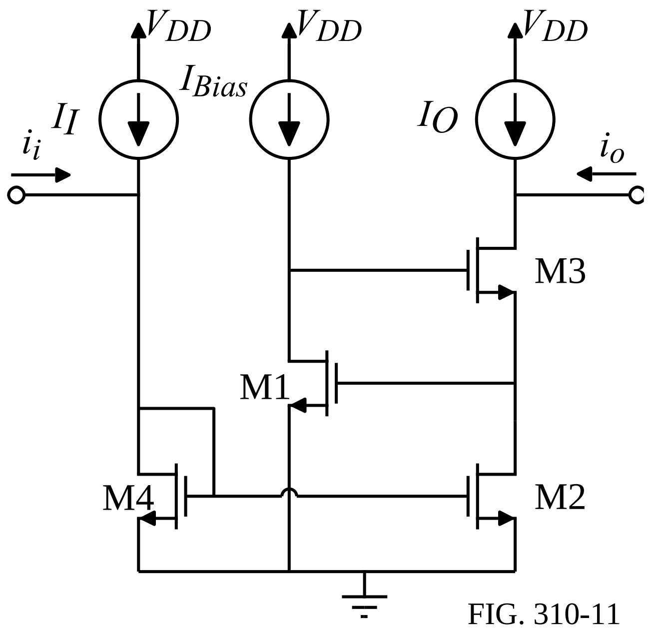


FIG. 310-11

- $R_{out} \approx g_m{}^2 r_{ds}{}^3$
- $R_{in} \approx \dfrac{1}{g_{m4}}$
- $V_{MIN}(\text{out}) = V_T + 2V_{ON}$ (Can be reduced to $2V_{ON}$)
- $V_{MIN}(\text{in}) = V_T + V_{ON}$ (Can be reduced to V_{ON})
- Current gain matching - good as long as $v_{DS4} = v_{DS2}$

Summary of MOS Current Mirrors

Current Mirror	Accuracy	Output Resistance	Input Resistance	Minimum Output Voltage	Minimum Input Voltage
Simple	Poor	r_{ds}	$\frac{1}{g_m}$	V_{ON}	V_T+V_{ON}
Wide Output Swing Cascode	Excellent	$g_m r_{ds}^2$	$\frac{1}{g_m}$	$2V_{ON}$	V_T+V_{ON}
Self-biased Cascode	Excellent	$g_m r_{ds}^2$	$R + \frac{1}{g_m}$	$2V_{ON}$	V_T+2V_{ON}
Regulated Cascode	Good-Excellent	$g_m^2 r_{ds}^3$	$\frac{1}{g_m}$	V_T+2V_{ON} (Can be $2V_{ON}$)	V_T+V_{ON} (Can be $\approx V_{ON}$)

VOLTAGE REFERENCES WITH POWER SUPPLY INDEPENDENCE

Power Supply Independence

How do you characterize power supply independence?

Use the concept of:

$$S_{V_{DD}}^{V_{REF}} = \frac{\partial V_{REF}/V_{REF}}{\partial V_{DD}/V_{DD}} = \frac{V_{DD}}{V_{REF}}\left(\frac{\partial V_{REF}}{\partial V_{DD}}\right)$$

Application of sensitivity to determining power supply dependence:

$$\frac{\Delta V_{REF}}{V_{REF}} = \left(S_{V_{DD}}^{V_{REF}}\right)\frac{\Delta V_{DD}}{V_{DD}}$$

Thus, the fractional change in the reference voltage is equal to the sensitivity times the fractional change in the power supply voltage.

For example, if the sensitivity is 1, then a 10% change in V_{DD} will cause a 10% change in V_{REF}.

Ideally, we want $S_{V_{DD}}^{V_{REF}}$ to be zero for power supply independence.

MOSFET-Resistance Voltage References

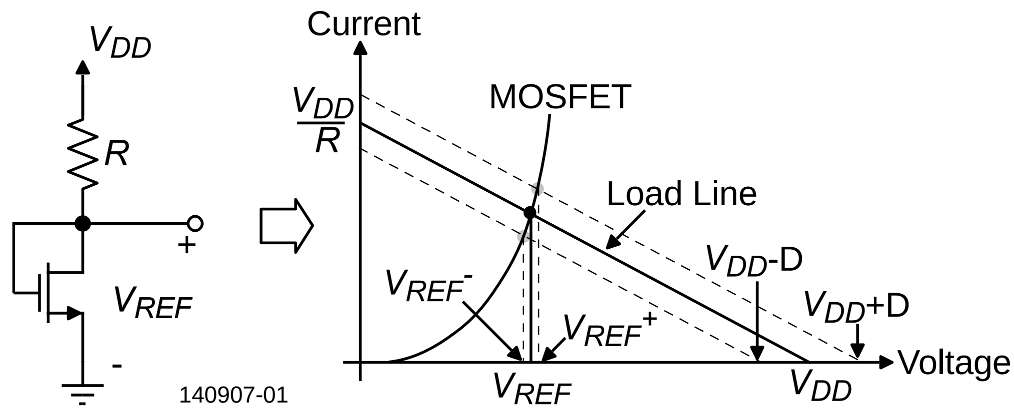
Simple MOS-R Voltage Reference

$$V_{REF} = V_{GS} = V_T + \sqrt{\frac{2(V_{DD}-V_{REF})}{\beta R}}$$

or

$$V_{REF} = V_T - \frac{1}{\beta R} + \sqrt{\frac{2(V_{DD}-V_T)}{\beta R} + \frac{1}{(\beta R)^2}}$$

$$S_{V_{DD}}^{V_{REF}} = \left(\frac{1}{\sqrt{1 + 2\beta(V_{DD}-V_T)R}}\right)\left(\frac{V_{DD}}{V_{REF}}\right)$$

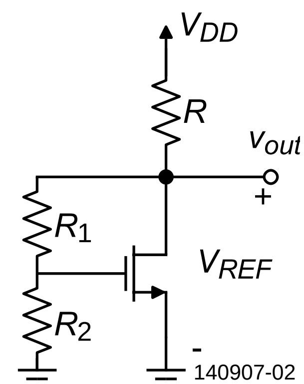


Assume V_{DD}=5V, W/L =100 and R=100kΩ, thus $V_{REF} \approx 0.7875$V and $S_{V_{DD}}^{V_{REF}} = 0.0653$

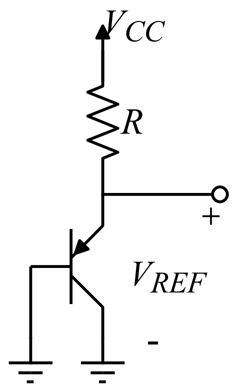
Higher Voltage Simple MOS-R Voltage Reference

This circuit allows V_{REF} to be larger. If the current in R_1 (and R_2) is small compared to the current flowing through the transistor, then

$$V_{REF} \approx \left(\frac{R_1 + R_2}{R_2}\right) V_{GS}$$



Bipolar-Resistance Voltage References



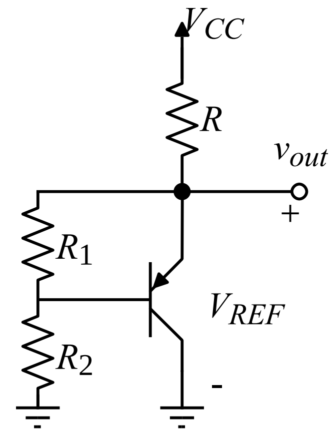


Fig. 370-04

$$V_{REF} = V_{EB} = \frac{kT}{q} \ln\left(\frac{I}{I_S}\right)$$

and $I = \dfrac{V_{CC} - V_{EB}}{R} \cong \dfrac{V_{CC}}{R}$

give $\quad V_{REF} \cong \dfrac{kT}{q} \ln\left(\dfrac{V_{CC}}{RI_S}\right)$

$$S_{V_{CC}}^{V_{REF}} = \frac{1}{\ln[V_{CC}/(RI_S)]} = \frac{1}{\ln(I/I_S)}$$

If $V_{CC} = 5\text{V}$, $R = 4.3\text{k}\Omega$ and $I_S = 1\text{fA}$, then $V_{REF} = 0.719\text{V}$.

Also, $S_{V_{CC}}^{V_{REF}} = 0.0362$

If the current in R_1 (and R_2) is small compared to the current flowing through the transistor, then

$$V_{REF} \approx \left(\frac{R_1 + R_2}{R_1}\right) V_{EB}$$

Can use diodes in place of the BJTs.

CURRENT REFERENCES WITH POWER SUPPLY INDEPENDENCE

Power Supply Independence

Again, we want

$$S_{V_{DD}}^{I_{REF}} = \frac{\partial I_{REF}/I_{REF}}{\partial V_{DD}/V_{DD}} = \frac{V_{DD}}{I_{REF}}\left(\frac{\partial I_{REF}}{\partial V_{DD}}\right)$$

to approach zero.

Therefore, as $S_{V_{DD}}^{I_{REF}}$ approaches zero, the change in I_{REF} as a function of a change in V_{DD} approaches zero.

Gate-Source Referenced Current Reference

The circuit below uses both positive and negative feedback to accomplish a current reference that is reasonably independent of power supply.

Circuit:

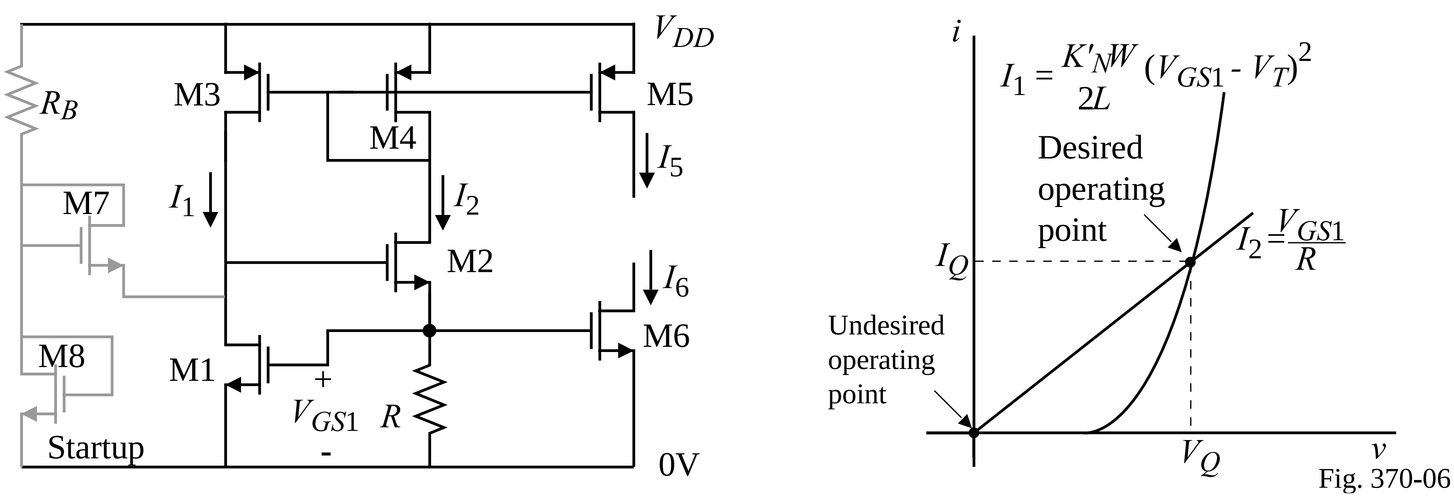


Fig. 370-06

Principle:

If M3 = M4, then $I_1 \approx I_2$. However, the M1-R loop gives $V_{GS1}=V_{T1} + \sqrt{\dfrac{2I_1}{K_N'(W_1/L_1)}}$

Solving these two equations gives $I_2 = \dfrac{V_{GS1}}{R} = \dfrac{V_{T1}}{R} + \left(\dfrac{1}{R}\right)\sqrt{\dfrac{2I_1}{K_N'(W_1/L_1)}}$

The output current, $I_{out}=I_1=I_2$ can be solved as $I_{out}= \dfrac{V_{T1}}{R} + \dfrac{1}{\beta_1 R^2} + \dfrac{1}{R}\sqrt{\dfrac{2V_{T1}}{\beta_1 R} + \dfrac{1}{(\beta_1 R)^2}}$

Simulation Results for the Gate-Source Referenced Current Reference

The current I_{D2} appears to be okay, why is I_{D1} increasing?

Apparently, the channel modulation on the current mirror M3-M4 is large.

At V_{DD} = 5V, V_{SD3} = 2.83V and V_{SD4} = 1.09V which gives $I_{D3} = 1.067 I_{D4} \approx 107\mu A$

Need to cascode the upper current mirror.

SPICE Input File:

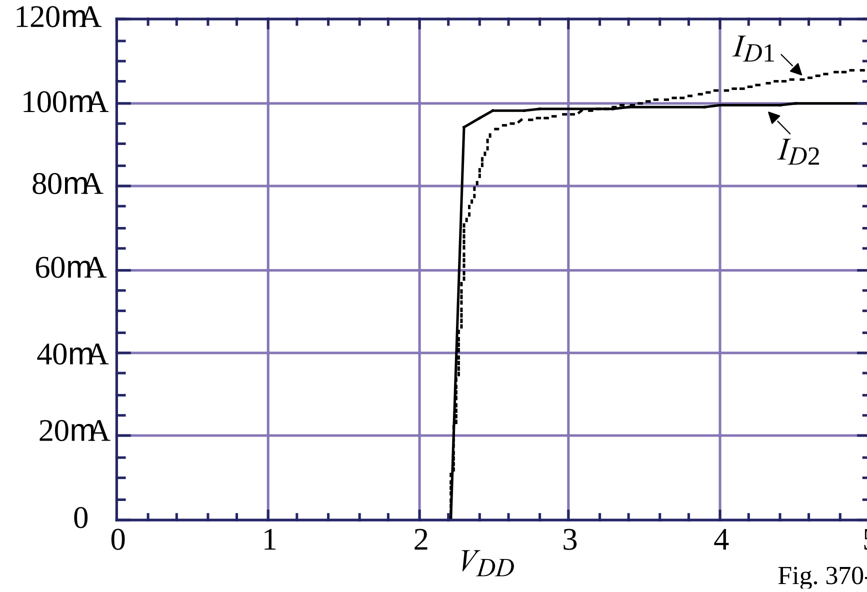
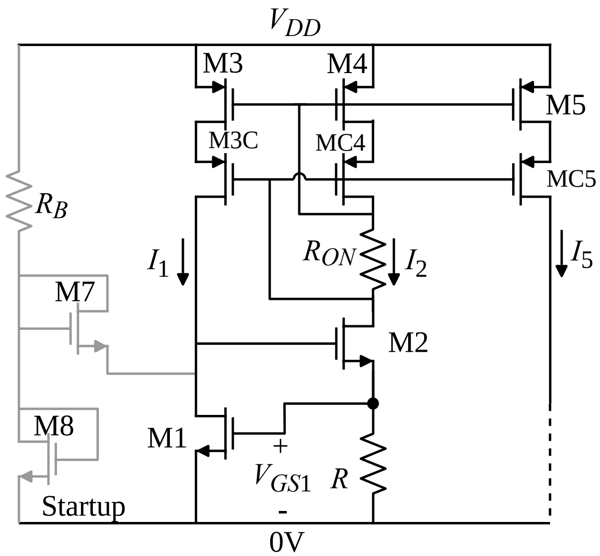


Fig. 370-07

```
Simple, Bootstrap Current Reference
VDD 1 0 DC 5.0
VSS 9 0 DC 0.0
M1 5 7 9 9 N W=20U L=1U
M2 3 5 7 9 N W=20U L=1U
M3 5 3 1 1 P W=25U L=1U
M4 3 3 1 1 P W=25U L=1U
M5 9 3 1 1 P W=25U L=1U
R 7 9 10KILOHM
M8 6 6 9 9 N W=1U L=1U
M7 6 6 5 9 N W=20U L=1U
RB 1 6 100KILOHM
.OP
.DC VDD 0 5 0.1
.MODEL N NMOS VTO=0.7 KP=110U
GAMMA=0.4 +PHI=0.7 LAMBDA=0.04
.MODEL P PMOS VTO=-0.7 KP=50U
GAMMA=0.57 +PHI=0.8 LAMBDA=0.05
.PRINT DC ID(M1) ID(M2) ID(M5)
.PROBE
.END
```


Cascoded Gate-Source Referenced Current Reference



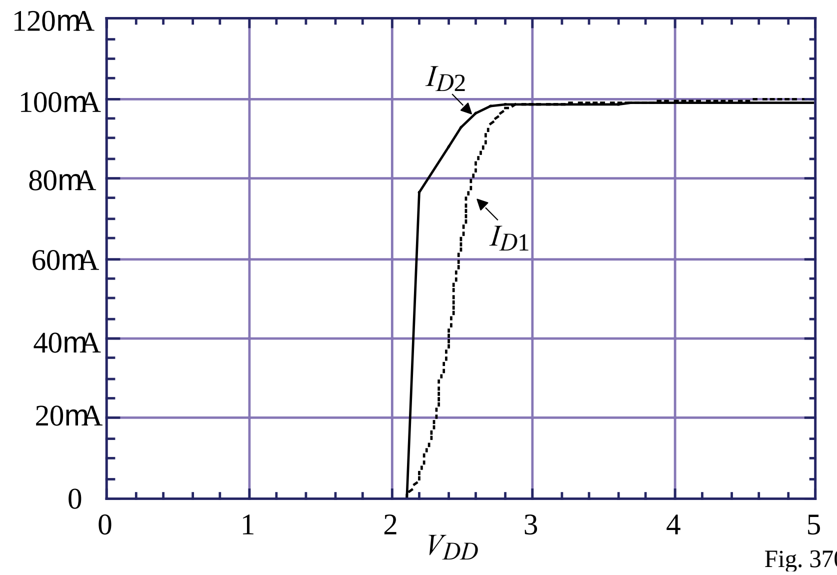
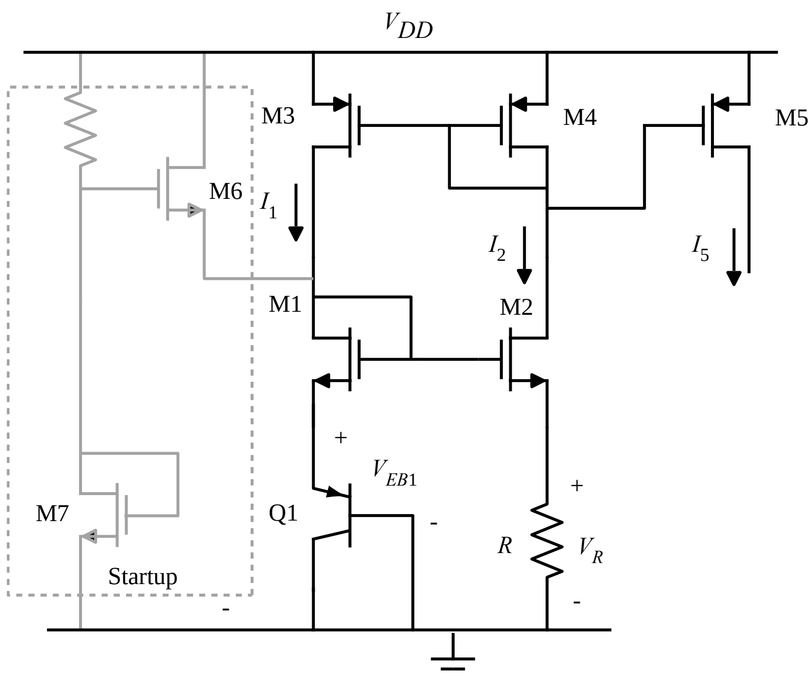


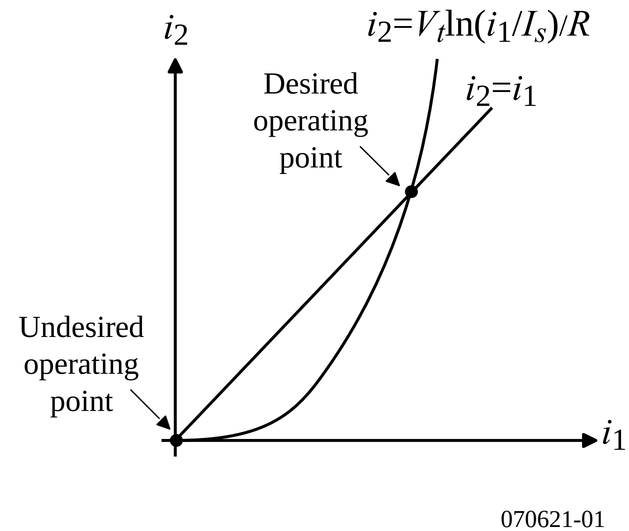
Fig. 370-08

SPICE Input File:

```
Cascode, Bootstrap Current Reference
VDD 1 0 DC 5.0
VSS 9 0 DC 0.0
M1 5 7 9 9 N W=20U L=1U
M2 4 5 7 9 N W=20U L=1U
M3 2 3 1 1 P W=25U L=1U
M4 8 3 1 1 P W=25U L=1U
M3C 5 4 2 1 P W=25U L=1U
MC4 3 4 8 1 P W=25U L=1U
RON 3 4 4KILOHM
M5 9 3 1 1 P W=25U L=1U
R 7 9 10KILOHM
M8 6 6 9 9 N W=1U L=1U
M7 6 6 5 9 N W=20U L=1U
RB 1 6 100KILOHM
.OP
.DC VDD 0 5 0.1
.MODEL N NMOS VTO=0.7 KP=110U
GAMMA=0.4 PHI=0.7 LAMBDA=0.04
.MODEL P PMOS VTO=-0.7 KP=50U
GAMMA=0.57 PHI=0.8 LAMBDA=0.05
.PRINT DC ID(M1) ID(M2) ID(M5)
.PROBE
.END
```

Base-Emitter Referenced Circuit





$$I_{out} = I_2 = \frac{V_{EB1}}{R}$$

BJT can be a MOSFET in weak inversion.

Low Voltage Gate-Source Referenced MOS Current Reference

The previous gate-source referenced circuits required at least 2 volts across the power supply before operating.

A low-voltage gate-source referenced circuit:

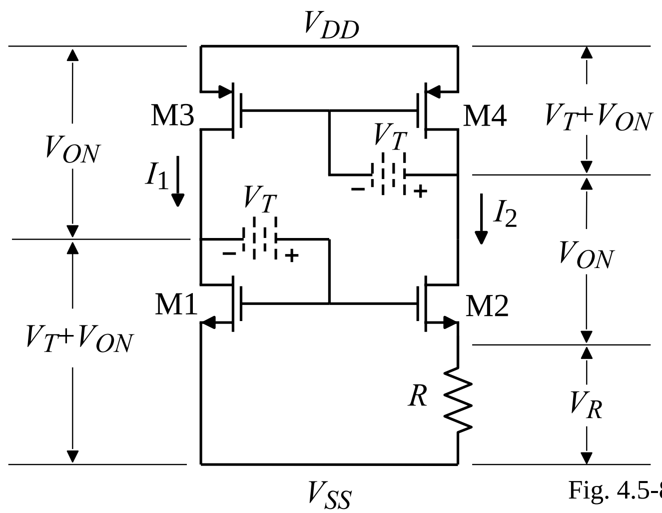


Fig. 4.5-8A

Without the batteries, V_T, the minimum power supply is $V_T+2V_{ON}+V_R$.

With the batteries, V_T, the minimum power supply is $2V_{ON}+V_R \approx 0.5\text{V}$

Summary of Power-Supply Independent References

- Reasonably good, simple voltage and current references are possible
- Best power supply sensitivity is approximately 0.01

  (10% change in power supply causes a 0.1% change in reference)

Type of Reference	$S_{V_{PP}}^{V_{REF}}$ or $S_{V_{PP}}^{I_{REF}}$
MOSFET-R	<1
BJT-R	<<1
Gate-source Referenced	<<1
Base-emitter Referenced	<<1

TEMPERATURE BEHAVIOR OF VOLTAGE AND CURRENT REFERENCES

Characterization of Temperature Dependence

The objective is to minimize the fractional temperature coefficient defined as,

$$TC_F = \frac{1}{V_{REF}}\left(\frac{V_{REF}}{T}\right) = \frac{1}{T} S_{T}^{V_{REF}} \text{ parts per million per °C or ppm/°C}$$

Temperature dependence of PN junctions:

$$\left.\begin{array}{l} i \approx I_s \exp\left(\dfrac{v}{V_t}\right) \\ I_s = KT^3 \exp\left(\dfrac{-V_{GO}}{V_t}\right) \end{array}\right\} \quad \frac{1}{I_s}\left(\frac{I_s}{T}\right) = \frac{(\ln I_s)}{T} = \frac{3}{T} + \frac{V_{GO}}{TV_t} \approx \frac{V_{GO}}{TV_t}$$

$$\frac{dv_{BE}}{dT} \approx \frac{V_{BE} - V_{GO}}{T} = \text{-2mV/°C at room temperature}$$

Temperature dependence of MOSFET in strong inversion:

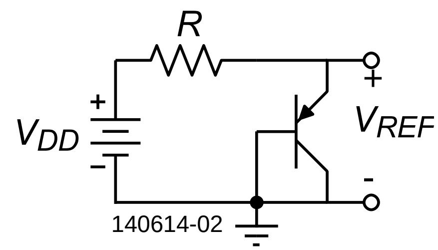
$$\left.\begin{array}{c} \dfrac{dv_{GS}}{dT} = \dfrac{dV_T}{dT} + \sqrt{\dfrac{2L}{WC_{ox}}}\dfrac{d}{dT}\left(\sqrt{\dfrac{i_D}{\mu_o}}\right) \\ \mu_o = KT^{-1.5} \\ V_T(T) = V_T(T_o) - \alpha(T-T_o) \end{array}\right\} \quad \frac{dv_{GS}}{dT} \approx -\alpha \approx -2.3\frac{\text{mV}}{\text{°C}}$$

Resistors: $(1/R)(dR/dT)$ ppm/°C

Bipolar-Resistance Voltage References

From previous work we know that,

$$V_{REF} = \frac{kT}{q}\,ln\left(\frac{V_{DD} - V_{REF}}{RI_s}\right)$$



However, not only is V_{REF} a function of T, but R and I_s are also functions of T.

$$\therefore \quad \frac{dV_{REF}}{dT} = \frac{k}{q}ln\left(\frac{V_{DD}\text{-}V_{REF}}{RI_s}\right) + \frac{kT}{q}\left(\frac{RI_s}{V_{DD}\text{-}V_{REF}}\right)\left[\frac{-1}{RI_s}\frac{dV_{REF}}{dT} - \left(\frac{V_{DD}\text{-}V_{REF}}{RI_s}\right)\left(\frac{dR}{RdT} + \frac{dI_s}{I_sdT}\right)\right]$$

$$= \frac{V_{REF}}{T} - \frac{V_t}{V_{DD}\text{-}V_{REF}}\frac{dV_{REF}}{dT} - V_t\left(\frac{dR}{RdT} + \frac{dI_s}{I_sdT}\right) = \frac{V_{REF}\text{-}V_{GO}}{T} - \frac{V_t}{V_{DD}\text{-}V_{REF}}\frac{dV_{REF}}{dT} - \frac{3V_t}{T} - \frac{V_t}{R}\frac{dR}{dT}$$

$$\therefore \quad \frac{dV_{REF}}{dT} = \frac{\dfrac{V_{REF}\text{-}V_{GO}}{T} - V_t\dfrac{dR}{RdT} - \dfrac{3V_t}{T}}{1 + \dfrac{V_t}{V_{DD}\text{-}V_{REF}}} \approx \frac{V_{REF}\text{-}V_{GO}}{T} - V_t\frac{dR}{RdT} - \frac{3V_t}{T}$$

$$TC_F = \frac{1}{V_{REF}}\frac{dV_{REF}}{dT} = \frac{V_{REF}\text{-}V_{GO}}{V_{REF}\cdot T} - \frac{V_t}{V_{REF}}\frac{dR}{RdT} - \frac{3V_t}{V_{REF}\cdot T}$$

If V_{REF} = 0.6V, V_t = 0.026V, and the R is polysilicon, then at 27°K the TC_F is

$$TC_F = \frac{0.6\text{-}1.205}{0.6\cdot 300} - \frac{0.026\cdot 0.0015}{0.6} - \frac{3\cdot 0.026}{0.6\cdot 300} = 33110^{-6}\text{-}65\text{x}10^{-6}\text{-}433\text{x}10^{-6} = \text{-}3859\text{ppm/°C}$$

MOSFET Resistor Voltage Reference

From previous results we know that

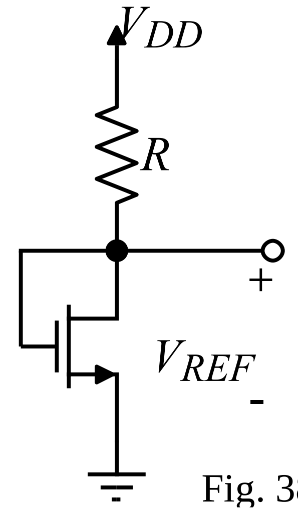


Fig. 380-02

$$V_{REF} = V_{GS} = V_T + \sqrt{\frac{2(V_{DD}-V_{REF})}{\beta R}}$$

or $$V_{REF} = V_T - \frac{1}{\beta R} + \sqrt{\frac{2(V_{DD}-V_T)}{\beta R} + \frac{1}{(\beta R)^2}}$$

Note that V_{REF}, V_T, β, and R are all functions of temperature.

It can be shown that the TC_F of this reference is

$$\frac{dV_{\mathrm{REF}}}{dT} = \frac{-\alpha + \sqrt{\frac{V_{DD}-V_{\mathrm{REF}}}{2\beta R}}\left(\frac{1.5}{T} - \frac{1}{R}\frac{dR}{dT}\right)}{1 + \frac{1}{\sqrt{2\beta R\,(V_{DD}-V_{\mathrm{REF}})}}}$$

$$\therefore \quad TC_F = \frac{-\alpha + \sqrt{\frac{V_{DD}-V_{\mathrm{REF}}}{2\beta R}}\left(\frac{1.5}{T} - \frac{1}{R}\frac{dR}{dT}\right)}{V_{REF}\left(1 + \frac{1}{\sqrt{2\beta R\,(V_{DD}-V_{\mathrm{REF}})}}\right)}$$

Example 16-3 - Calculation of MOSFET-Resistor Voltage Reference TC_F

Calculate the temperature coefficient of the MOSFET-Resistor voltage reference where W/L=2, V_{DD}=5V, R=100kΩ using the parameters of Table 3.1-2. The resistor, R, is polysilicon and has a temperature coefficient of 1500 ppm/°C.

Solution

First, calculate V_{REF} . Note that $\beta R = 220\text{x}10^{-6}\text{x}10^{5} = 22$ and $\frac{dR}{RdT} = 1500\text{ppm/°C}$

$$\therefore \quad V_{REF} = 0.7 - \frac{1}{22} + \sqrt{\frac{2(5-0.7)}{22} + \left(\frac{1}{22}\right)^2} = 1.281\text{V}$$

Now,
$$\frac{dV_{REF}}{dT} = \frac{-2.3\text{x}10^{-3} + \sqrt{\frac{5-1.281}{2(22)}}\left(\frac{1.5}{300} - 1500\text{x}10^{-6}\right)}{1 + \frac{1}{\sqrt{2(22)\,(5-1.281)}}} = -1.189\text{x}10^{-3}\text{V/°C}$$

The fractional temperature coefficient is given by

$$TC_F = -1.189\text{x}10^{-3}\left(\frac{1}{1.281}\right) = -928\text{ ppm/°C}$$

Gate-Source and Base-Emitter Referenced Current Source/Sinks

Gate-source referenced source:

The output current was given as, $I_{out} = \frac{V_{T1}}{R} + \frac{1}{\beta_1 R^2} + \frac{1}{R}\sqrt{\frac{2V_{T1}}{\beta_1 R} + \frac{1}{(\beta_1 R)^2}}$

Although we could grind out the derivative of I_{out} with respect to T, the temperature performance of this circuit is not that good to spend the time to do so. Therefore, let us assume that $V_{GS1} \approx V_{T1}$ which gives

$$I_{out} \approx \frac{V_{T1}}{R} \qquad \Rightarrow \qquad \frac{dI_{out}}{dT} = \frac{1}{R}\frac{dV_{T1}}{dT} - \frac{1}{R^2}\frac{dR}{dT}$$

In the resistor is polysilicon, then

$$TC_F = \frac{1}{I_{out}}\frac{dI_{out}}{dT} = \frac{1}{V_{T1}}\frac{dV_{T1}}{dT} - \frac{1}{R}\frac{dR}{dT} = \frac{-\alpha}{V_{T1}} - \frac{1}{R}\frac{dR}{dT} = \frac{-2.3\text{x}10^{-3}}{0.7} - 1.5\text{x}10^{-3} = -4786\text{ppm/°C}$$

Base-emitter referenced source:

The output current was given as, $I_{out} = I_2 = \frac{V_{BE1}}{R}$

The $TC_F = \frac{1}{V_{BE1}}\frac{dV_{BE1}}{dT} - \frac{1}{R}\frac{dR}{dT}$

If V_{BE1} = 0.6V and R is poly, then the $TC_F = \frac{1}{0.6}(-2\text{x}10^{-3}) - 1.5\text{x}10^{-3} = -4833\text{ppm/°C}$.

Low V_{DD} Current Reference

Consider the following circuit with all transistors having a W/L = 10. This is a bootstrapped reference which creates a V_{bias} independent of V_{DD}. The two key equations are:

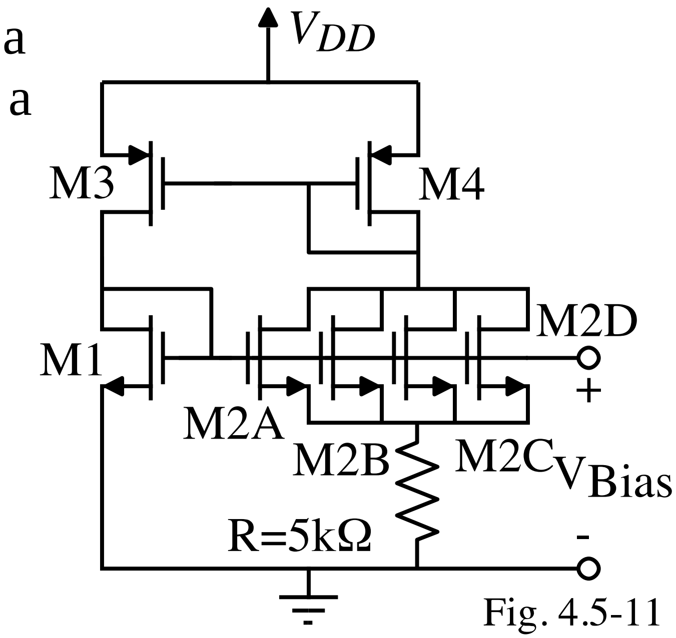


Fig. 4.5-11

$$I_3 = I_4 \Rightarrow I_1 = I_2$$

and

$$V_{GS1} = V_{GS2} + I_2R$$

Solving for I_2 gives:

$$I_2 = \frac{V_{GS1}-V_{GS2}}{R} = \frac{1}{R}\left(\sqrt{\frac{2I_1}{ß_1}} - \sqrt{\frac{2I_2}{ß_2}}\right) = \frac{\sqrt{2I_1}}{R\sqrt{ß_1}}\left(1 - \frac{1}{2}\right)$$

$$\therefore \quad \sqrt{I_2} = \frac{1}{R\sqrt{2ß_1}} \quad \Rightarrow \quad \boxed{I_2 = I_1 = \frac{1}{2ß_1R^2}} = \frac{1}{2\cdot110\text{x}10^{-6}\cdot10\cdot25\text{x}10^6} = 18.18\mu\text{A}$$

Now, V_{bias} can be written as

$$V_{bias}=V_{GS1}=\sqrt{\frac{2I_2}{ß_1}}+V_{TN} = \frac{1}{ß_1R}+V_{TN} = \frac{1}{110\text{x}10^{-6}\cdot10\cdot5\text{x}10^3} + 0.7 = 0.1818+0.7=0.8818\text{V}$$

Any transistor with $V_{GS} = V_{bias}$ will have a current flow that is given by $1/2ßR^2$.

Therefore, $$g_m = \sqrt{2Iß} = \sqrt{\frac{2ß}{2ßR^2}} = \frac{1}{R} \quad \Rightarrow \quad \boxed{g_m = \frac{1}{R}}$$

Summary of Reference Performance

Type of Reference	$S_{V_{DD}}^{V_{REF}}$	TC_F	Comments
MOSFET-R	<1	>1000ppm/°C	
BJT-R	<<1	>1000ppm/°C	
Gate-Source Referenced	Good if currents are matched	>1000ppm/°C	Requires start-up circuit
Base-emitter Referenced	Good if currents are matched	>1000ppm/°C	Requires start-up circuit

- A MOSFET can have zero temperature dependence of i_D for a certain v_{GS}
- If one is careful, very good independence of power supply can be achieved
- None of the above references have really good temperature independence

Consider the following example:

A 10 bit ADC has a reference voltage of 1V. The LSB is approximately 0.001V. Therefore, the voltage reference must be stable to within 0.1%. If a 100°C change in temperature is experienced, then the TC_F must be 0.001%/C or multiplying by 10^4 requires a TC_F = 10ppm/°C.