LECTURE 15 – RESISTOR IMPLEMENTATIONS AND CURRENT SINKS AND SOURCES

LECTURE ORGANIZATION

Outline

- Resistor implementations
- Simple current sinks and sources
- Improved performance current sinks and sources
- Summary

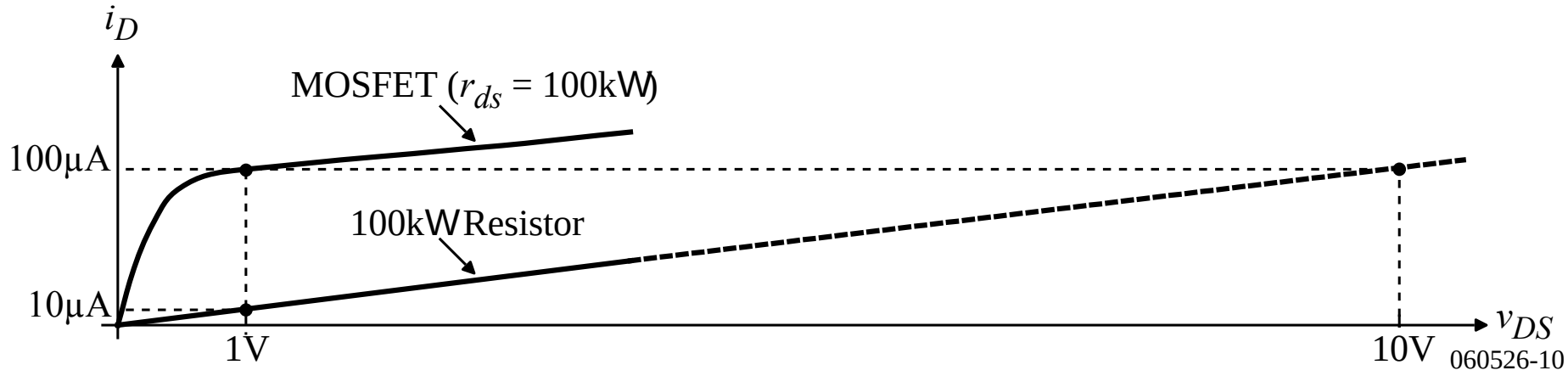
***CMOS Analog Circuit Design*, 3rd Edition Reference**

Pages 128-138

RESISTOR IMPLEMENTATION USING MOSFETS

Real Resistors versus MOSFET Resistors

- Smaller in area than actual resistors
- Can pass a large current through a large resistance without a large voltage drop



$$\text{AC resistance} = \frac{v_{ds}}{i_d} = \frac{1}{g_{ds}}$$

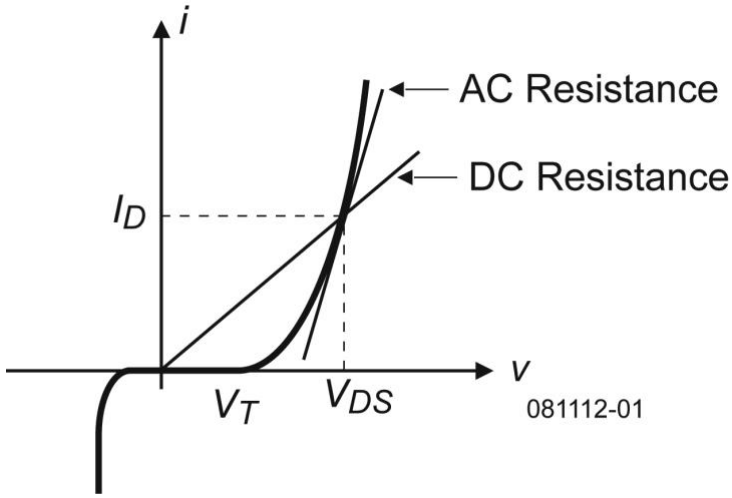
where

$$g_{ds} \approx \frac{\beta}{2}(V_{GS}\text{-}V_T)^2\lambda = I_D\lambda$$

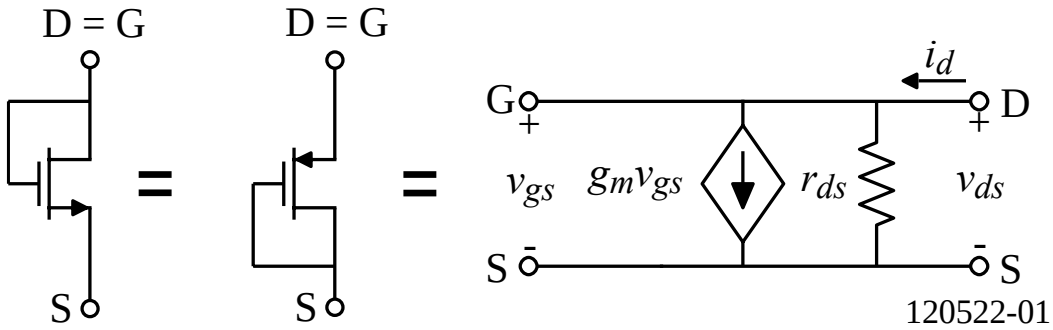
MOS Diode as a Resistor

AC and DC resistance:

$$\text{DC resistance} = \frac{V_{DS}}{I_D} = \frac{V_T}{I_D} + \sqrt{\frac{2}{\beta I_D}}$$



Small-Signal Load (AC resistance):



$$\text{AC resistance} = \frac{v_{ds}}{i_d} = \frac{1}{g_m + g_{ds}} \approx \frac{1}{g_m}$$

where

$$g_m = \beta(V_{GS}\text{-}V_T) = \sqrt{2\beta I_D}$$

Use of the MOSFET to Implement a Floating Resistor

In many applications, it is useful to implement a resistance using a MOSFET. First, consider the simple, single MOSFET implementation.

Fig. 4.2-9

$$R_{AB} = \frac{L}{K'W(V_{GS} - V_T)}$$

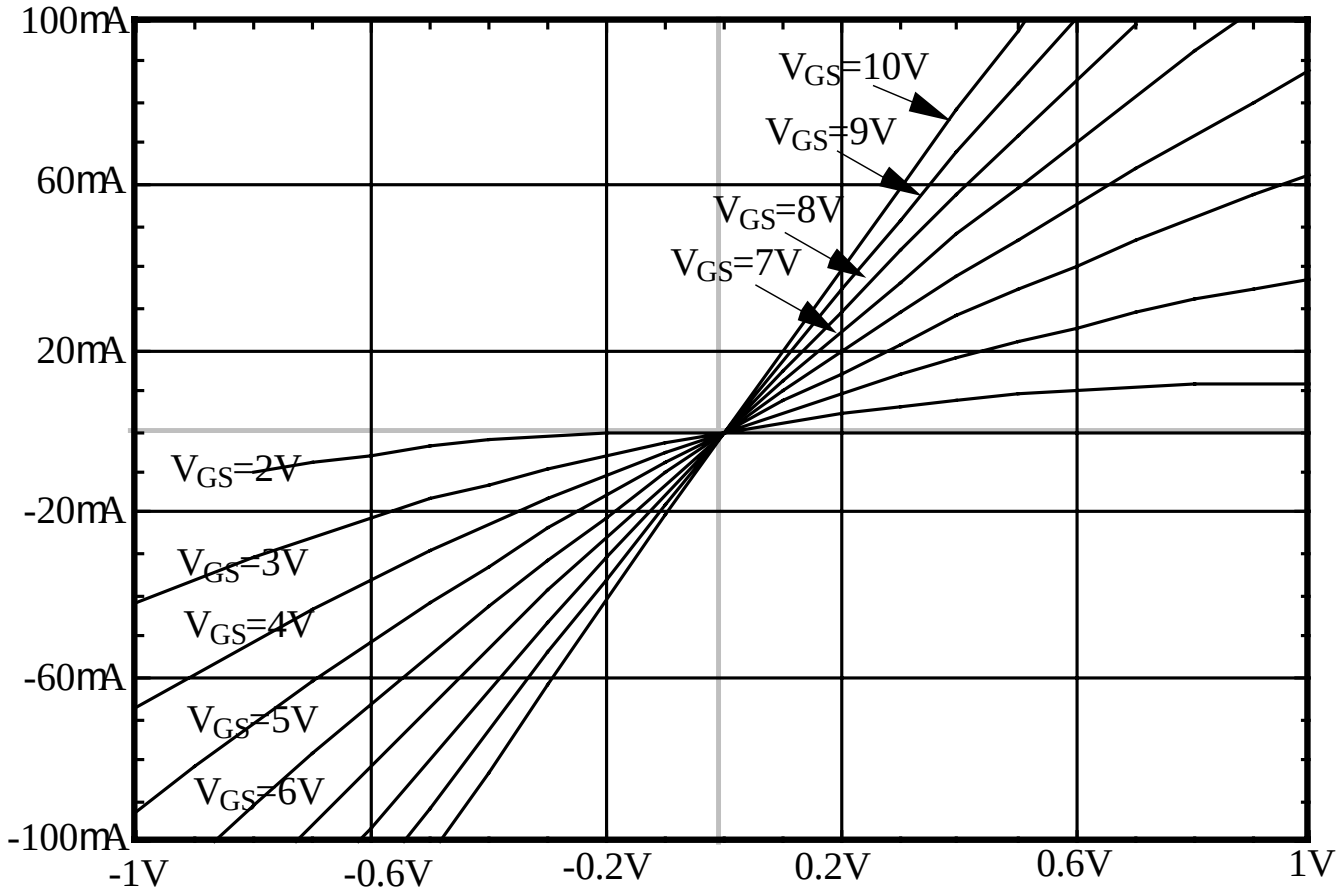
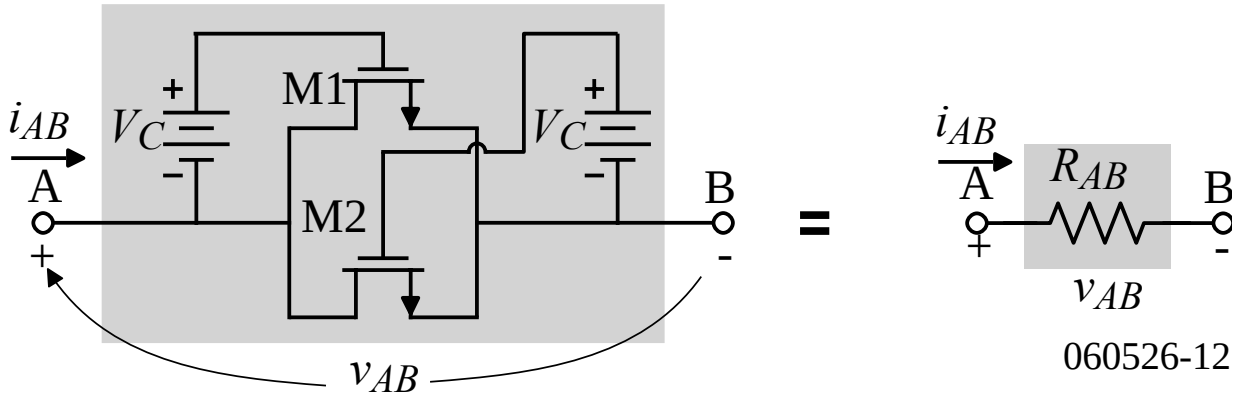


Fig. 4.2-95

Cancellation of Second-Order Voltage Dependence – Parallel MOSFETs

Circuit:



Assume both devices are non-saturated

$$i_{D1} = ß_1\left[(v_{AB} + V_C - V_T)v_{AB} - \frac{v_{AB}^2}{2}\right]$$

$$i_{D2} = ß_2\left[(V_C - V_T)v_{AB} - \frac{v_{AB}^2}{2}\right]$$

$$i_{AB} = i_{D1} + i_{D2} = ß\left[v_{AB}^2 + (V_C - V_T)v_{AB} - \frac{v_{AB}^2}{2} + (V_C - V_T)v_{AB} - \frac{v_{AB}^2}{2}\right]$$

$$i_{AB} = 2ß(V_C - V_T)v_{AB} \quad \Rightarrow \quad \boxed{R_{AB} = \frac{1}{2ß(V_C - V_T)}}$$

Parallel MOSFET Performance

Voltage-Current Characteristic:

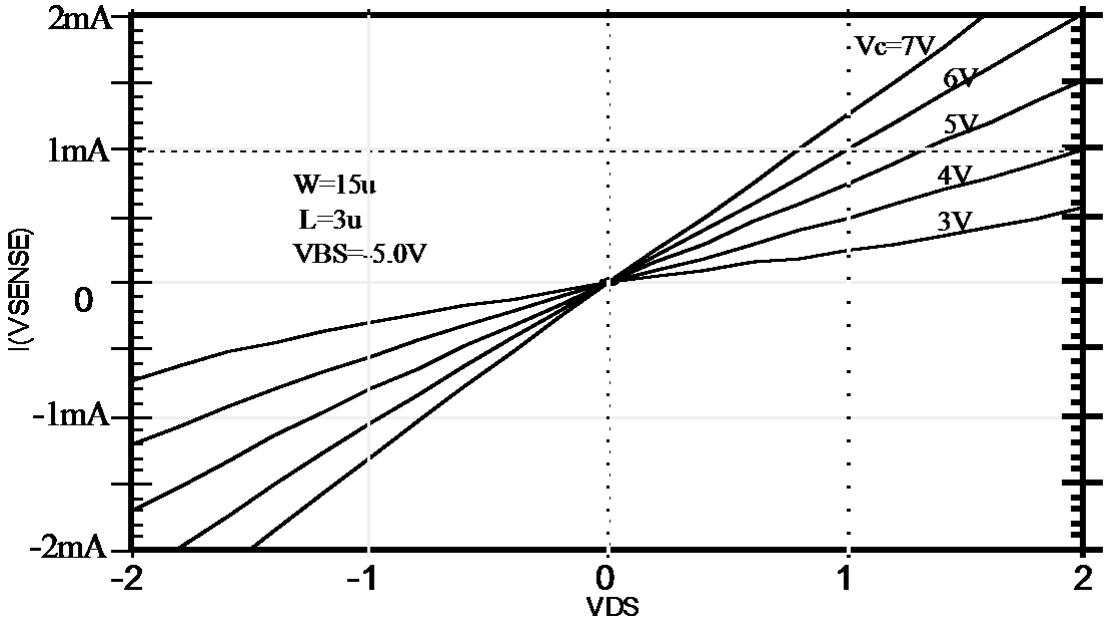


Fig. 4.1-11

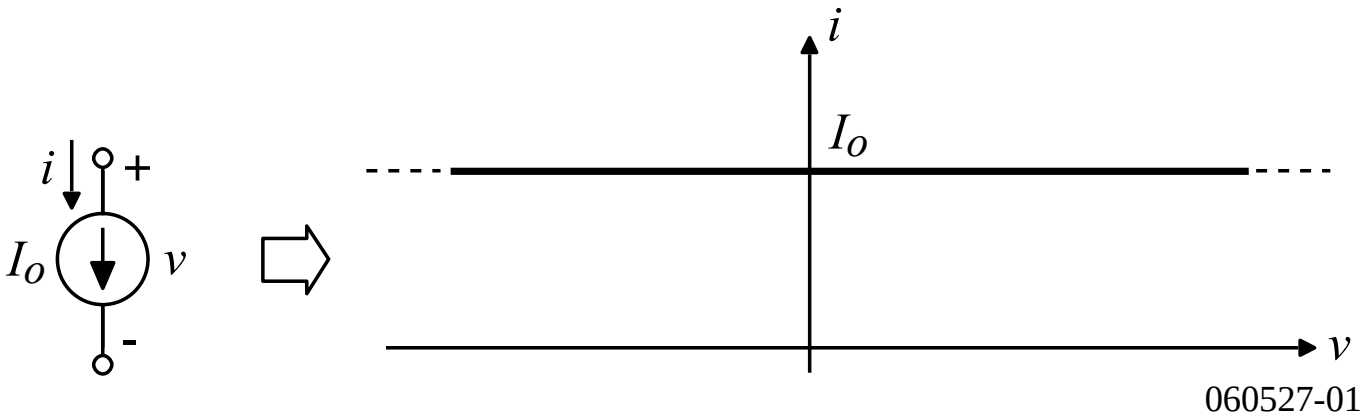
SPICE Input File:

```
NMOS parallel transistor realization
M1 2 1 0 5 MNMOS W=15U L=3U
M2 2 4 0 5 MNMOS W=15U L=3U
.MODEL MNMOS NMOS VTO=0.75, KP=25U, +LAMBDA=0.01,
GAMMA=0.8 PHI=0.6
VC 1 2
E1 4 0 1 2 1.0
VSENSE 10 2 DC 0
VDS 10 0
VSS 5 0 DC -5
.DC VDS -2.0 2.0 .2 VC 3 7 1
.PRINT DC I(VSENSE)
.PROBE
.END
```

SIMPLE CURRENT SINKS AND SOURCES

Ideal Current Sinks and Sources

What is an ideal current sink or source?



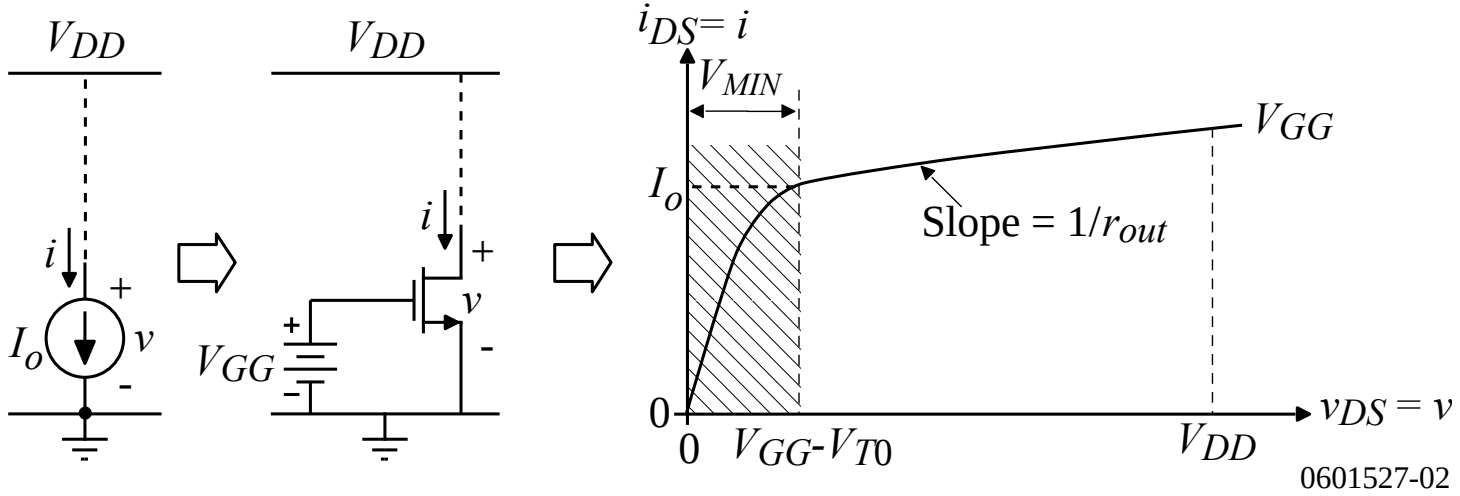
- Current is fixed at a value of I_O
- Voltage can be any value from +∞ to -∞
- Be careful when using a current sink or source to replace a MOSFET sink/source in simulation

Characterization of MOSFET Sinks and Sources

A sink/source is characterized by two quantities:

- r_{out} - a measure of the "flatness" of the current sink/source (its independence of voltage)
- V_{MIN} - the min. across the sink or source for which the current is no longer constant

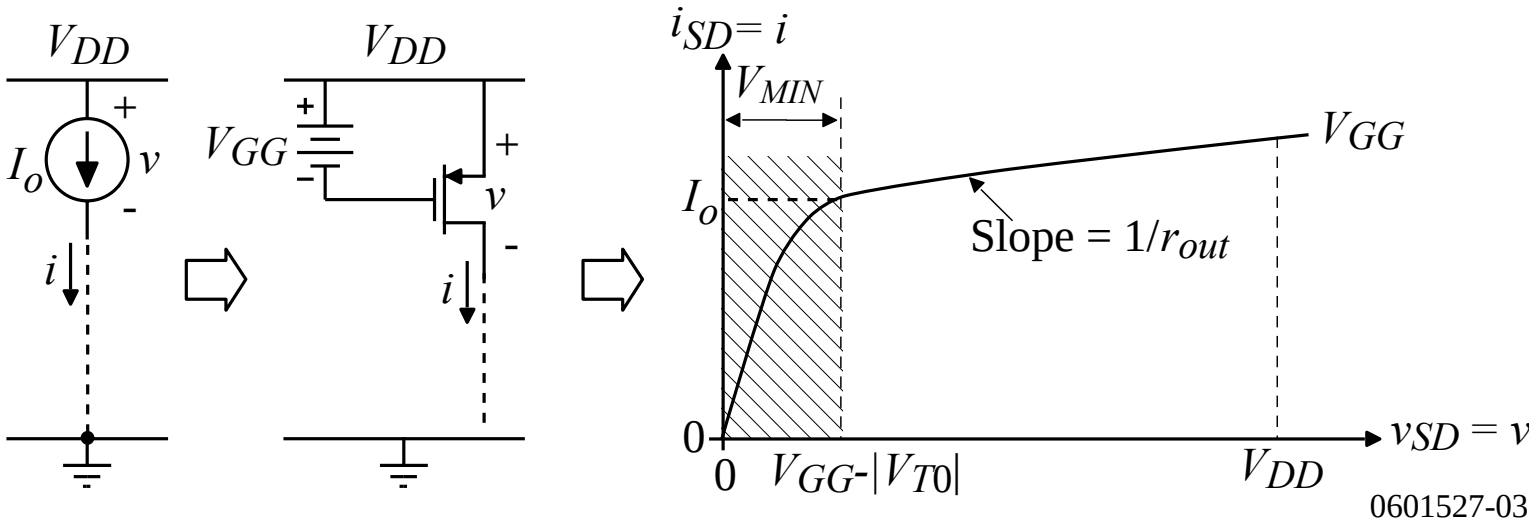
NMOS Current Sink:



$$r_{out} = \frac{1}{di_D/dv_{DS}} = \frac{1+\lambda V_{DS}}{\lambda I_D} \approx \frac{1}{\lambda I_D} \quad \text{and} \quad V_{MIN} = V_{DS}(\text{sat}) = V_{GS} - V_{T0} = V_{GG} - V_{T0}$$

Note: The NMOS current sink can only have positive values of v.

PMOS Current Source



Gate-Source Voltage Components

It is important to note that the gate-source voltage consists of two parts as illustrated below:

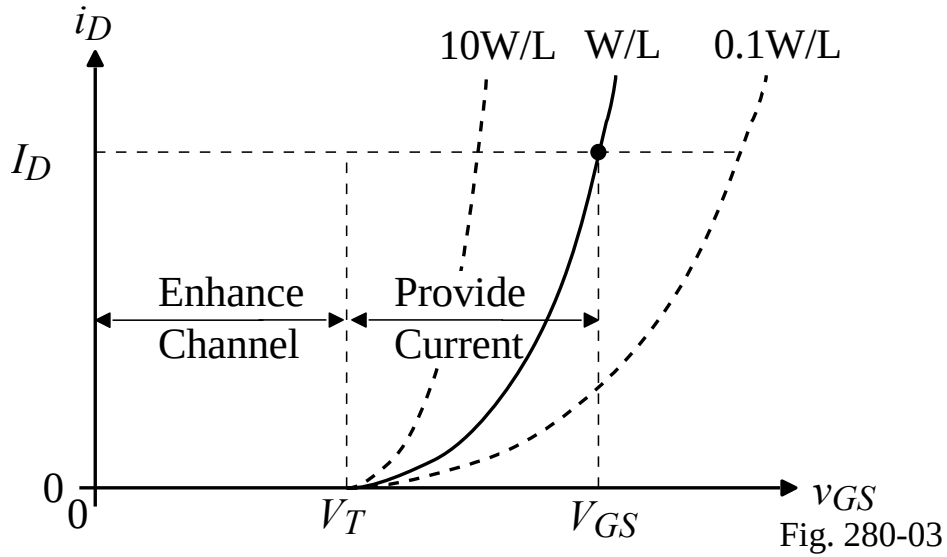


Fig. 280-03

$V_{GS} = V_{T0} + V_{ON}$ = Part to enhance the channel + Part to cause current flow

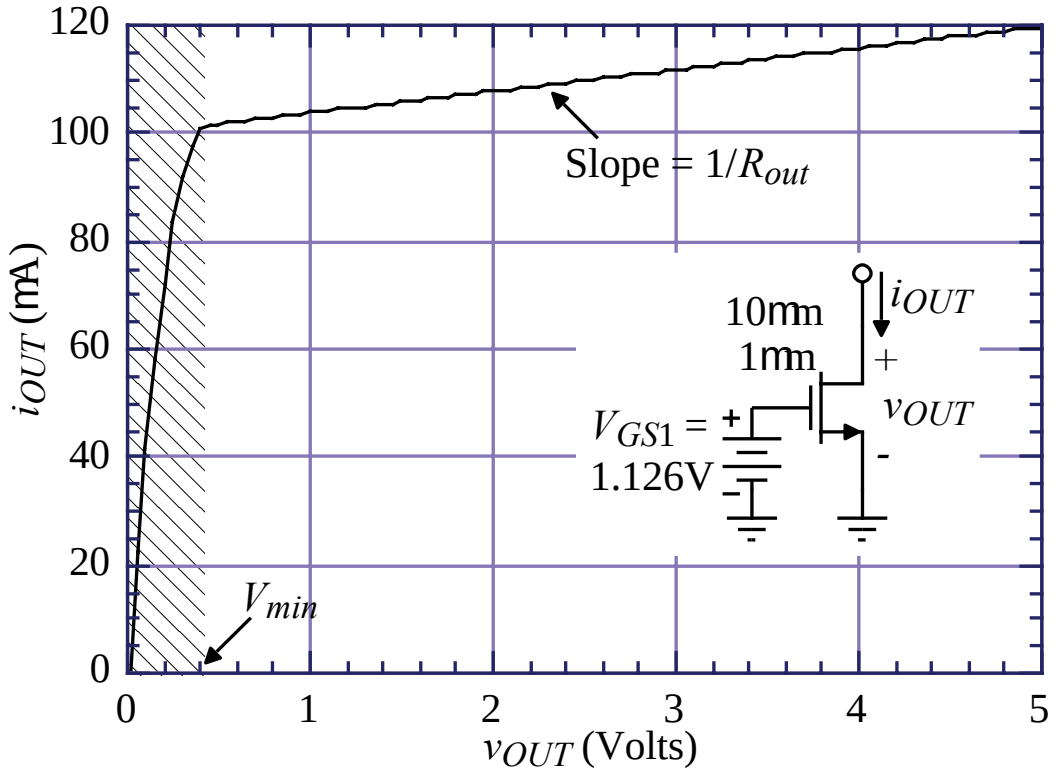
where

$V_{ON} = V_{DS}(\text{sat}) = V_{GS} - V_{T0}$

$\therefore$ $\boxed{V_{MIN} = V_{ON} = V_{DS}(\text{sat}) = \sqrt{\dfrac{2I_D}{K'(W/L)}}}$ for the simple current sink.

Note that V_{MIN} can be reduced by using large values of W/L.

Simulation of a Simple MOS Current Sink



Comments:

V_{MIN} is too large - desire V_{MIN} to approach zero, at least approach V_{CE}(sat)

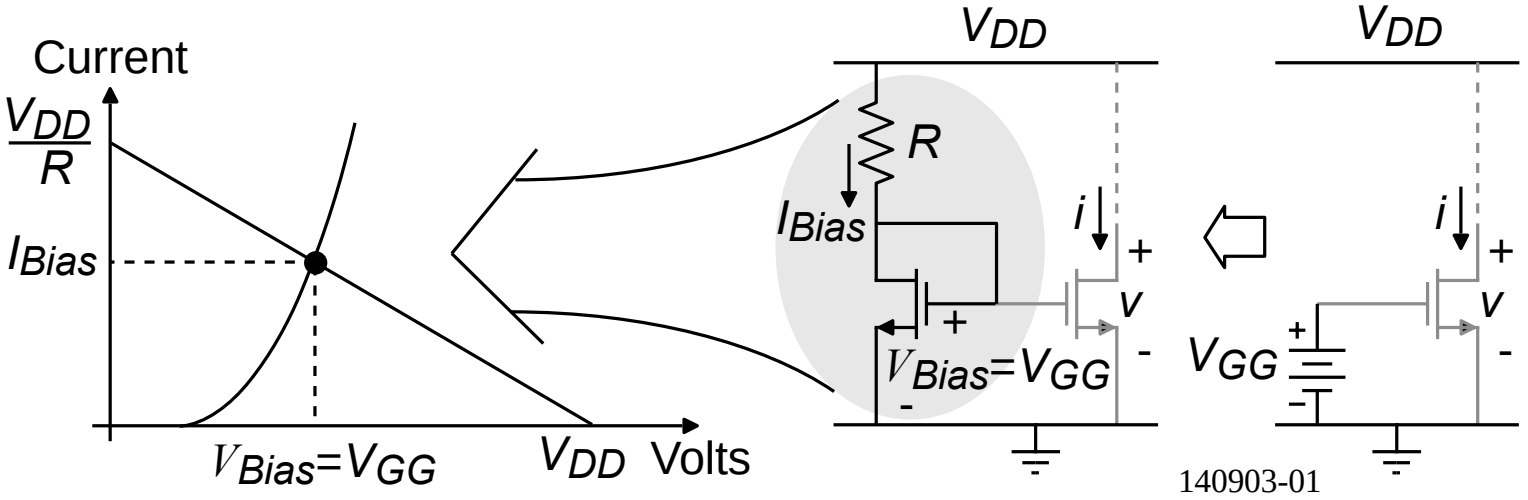
Slope too high - desire the characteristic to be flat implying very large output resistance

(K_N' = 110μA/V^2, V_T = 0.7Vand λ = 0.04V^{-1}) $\Rightarrow$ r_{ds} = 250kΩ

How is V_{GG} Implemented?

The only voltage source assumed available is V_{DD}.

Therefore, V_{GG}, can be implemented in many ways with the example below being one way.



Better and more stable implementations of V_{GG} will be shown later.

IMPROVED PERFORMANCE CURRENT SINKS

Improving the Performance of the Simple NMOS Current Sink

The simple NMOS current sink shown previously had two problems.

1.) The value of V_{MIN} may be too large.

2.) The output resistance (250kΩ) was too small.

How can the designer solve these problems?

1.) The first problem can be solved by increasing the *W/L* value of the NMOS transistor.

$$V_{MIN} = V_{ON} = V_{DS}(\text{sat}) = \sqrt{\frac{2I_D}{K'(W/L)}}$$

In the simulation shown previously,

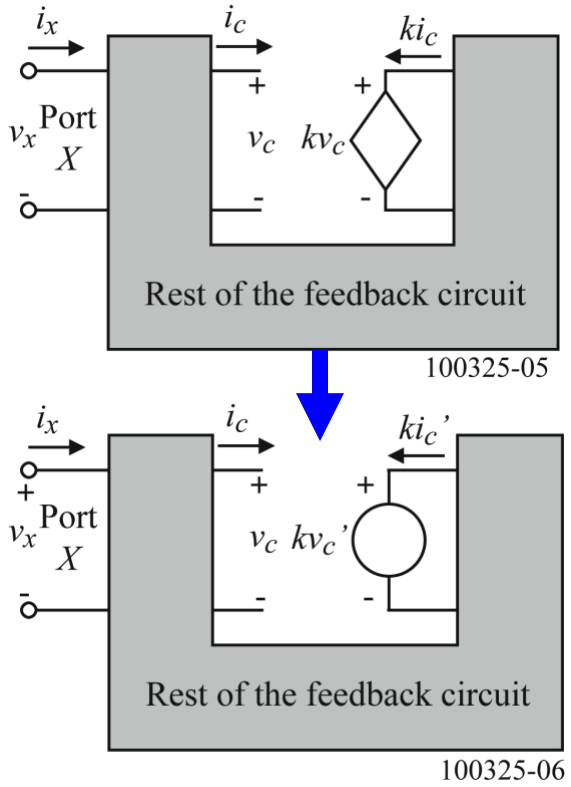
$$V_{MIN} = \sqrt{\frac{2 \cdot 100\mu A}{110\mu A/V^2 \cdot 10}} = 0.426V$$

We could decrease this to 0.1V with a *W/L* = 182.

2.) How can the small output resistance be increased? Answer is feedback.

Blackman's Formula for Finding the Resistance at a Port with Feedback†

Blackman's formula to find the resistance at a port *X*, is based on the following circuit:



The resistance seen looking into port *X* is given as,

$$R_X = R_X(k=0)\left[\frac{1 + RR(\text{port shorted})}{1 + RR(\text{port opened})}\right]$$

The return ratio, *RR*, is found by changing the dependent source to an independent source as shown:

Therefore, the return ratio is defined as,

$$RR = -\frac{v_c}{v_c'} = -\frac{i_c}{i_c'}$$

The key is to find a feedback circuit that when we calculate the RR, it is non-zero when port X is shorted and zero when port X is opened. In this case, the resistance at port *X* is

$$R_X = R_X(k=0)[1 + RR(\text{port shorted})]$$

† R.B. Blackman, "Effect of Feedback on Impedance," *Bell Sys. Tech.J.*, Vol. 23, pp. 269-277, October 1943.

How to find the Proper Type of Feedback

For the port *X*, the circuit variables associated with the input port should be able to be expressed as,

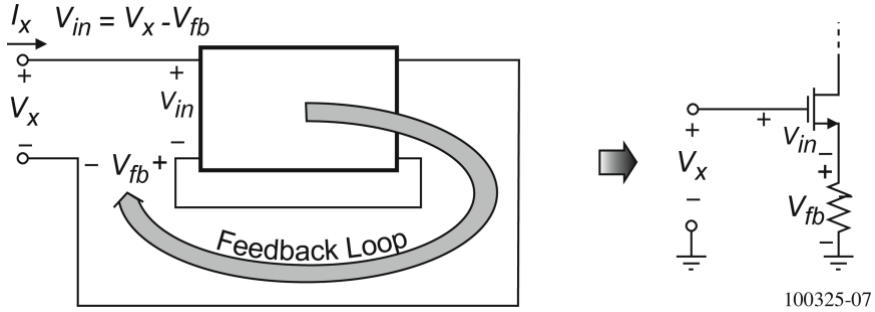
Input Variable to Port *X* = Signal variable to the circuit – Feedback variable

where the variables can be voltage or current.

1.) Series feedback (variables are voltage):

$RR(V_X = 0) \neq 0$

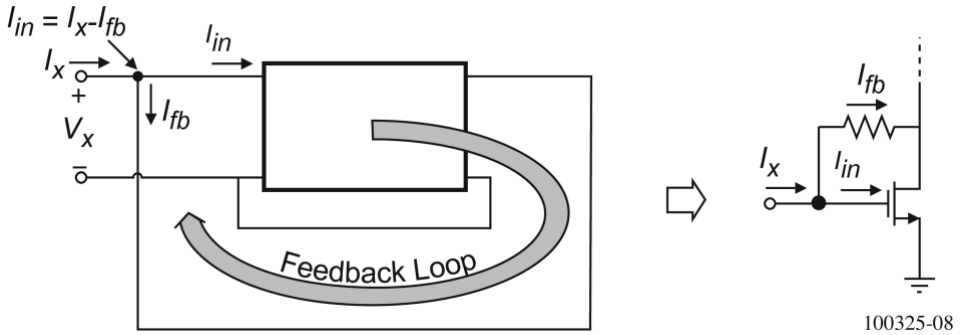
$\boldsymbol{RR(I_X = 0)} = 0$ (V_{in} is disconnected from V_{fb})



2.) Shunt feedback (variables are current):

$\boldsymbol{RR(V_X = 0)} = 0$($I_{in}$ is disconnected from I_{fb})

$RR(I_X = 0) \neq 0$

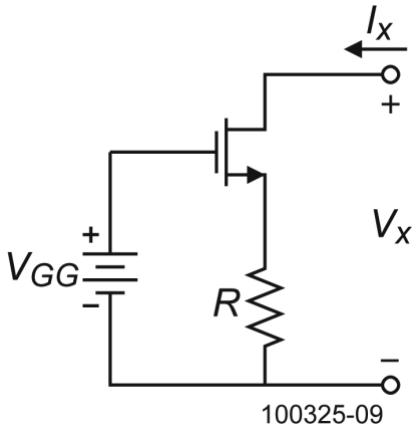


We see that for series feedback *RR*(port opened) will be zero and for shunt feedback that *RR*(port shorted) will be zero.

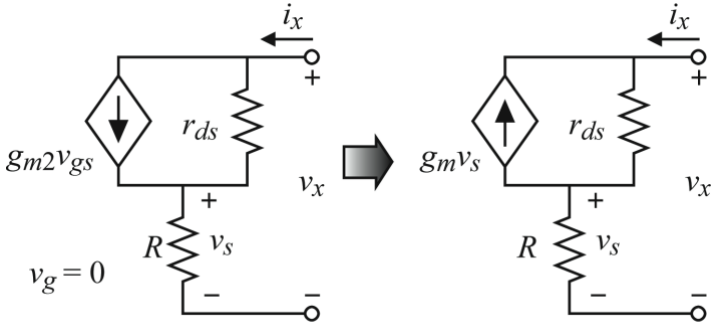
Therefore, to boost the resistance at port *X* select series feedback!

Increasing the Output Resistance of the Simple Current Sink

Choosing series feedback, we select the following circuit to boost the output resistance of the simple current sink:



Assume that we can neglect the bulk effect and find the input resistance by 1.) small-signal analysis and 2.) return ratio method.

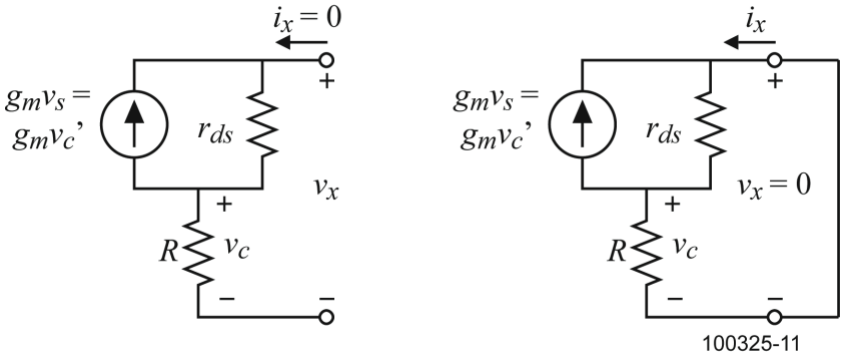


1.) Small-signal Analysis:

$$v_x = (i_x + g_m v_s) r_{ds} + i_x R$$

$$v_x = (i_x + g_m i_x R) r_{ds} + i_x R = i_x (r_{ds} + R + g_m r_{ds} R)$$

$$\therefore R_x = \frac{v_x}{i_x} = r_{ds} + R + g_m r_{ds} R \approx g_m r_{ds} R$$



2.) Return Ratio:

$$R_x(k=0) = R_x(g_m=0) = r_{ds} + R$$

$$RR(v_x = 0) = -\frac{v_c}{v_c'} = g_m \left(\frac{r_{ds} R}{r_{ds} + R} \right)$$

$$RR(i_x = 0) = 0$$

$$\therefore R_x = (r_{ds} + R)\left[1 + g_m \left(\frac{r_{ds} R}{r_{ds} + R} \right) \right] = r_{ds} + R + g_m r_{ds} R \approx g_m r_{ds} R$$

Cascode Current Sink

Replacing *R* with the simple current sink leads to a practical implementation shown as:

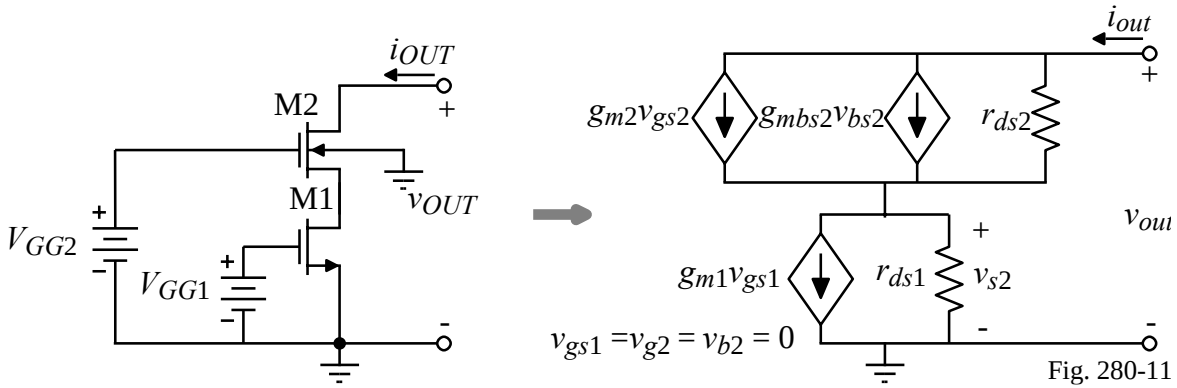


Fig. 280-11

Small signal output resistance:

Noting that $v_{gs1} = v_{g2} = v_{b2} = 0$ and writing a loop equation we get,

$$v_{out} = (i_{out} - g_{m2}v_{gs2} - g_{mbs2}v_{bs2})r_{ds2} + r_{ds1}i_{out}$$

However,

$$v_{gs2} = 0 - v_{s2} = -i_{out}r_{ds1} \quad \text{and} \quad v_{bs2} = 0 - v_{s2} = -i_{out}r_{ds1}$$

Therefore,

$$v_{out} = i_{out}[r_{ds1} + r_{ds2} + g_{m2}r_{ds1}r_{ds2} + g_{mbs2}r_{ds1}r_{ds2}]$$

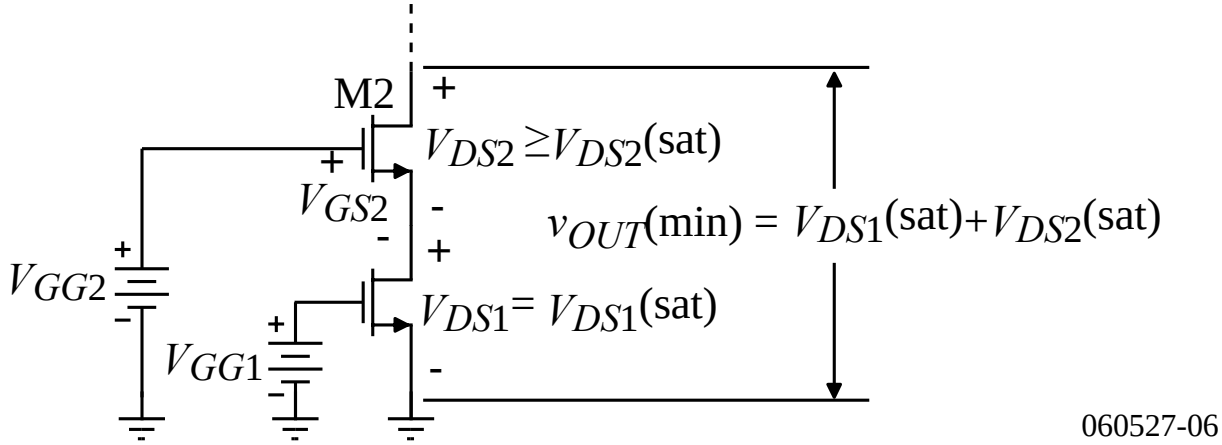
or

$$r_{out} = \frac{v_{out}}{i_{out}} = r_{ds1} + r_{ds2} + g_{m2}r_{ds1}r_{ds2} + g_{mbs2}r_{ds1}r_{ds2} \approx g_{m2}r_{ds1}r_{ds2}$$

A general principle is beginning to emerge:

The output resistance of a cascode circuit $\approx R$ x (*Common source voltage gain of the cascoding transistor*)

Design of V_{GG1} and V_{GG2}



1.) V_{GG1} is selected to provide the desired current. M1 is assumed to be in saturation.

2.) V_{GG2} is selected to keep V_{DS1} as small as possible and still be in saturation.

$$V_{GG2} = V_{DS1}(\text{sat}) + V_{GS2} = V_{DS1}(\text{sat}) + V_T + V_{DS2}(\text{sat})$$

If $W_1/L_1 = W_2/L_2$, then $V_{GG2} = 2V_{DS}(\text{sat}) + V_T = 2V_{ON} + V_T$

Thus, for the previous NMOS current sink, V_{GG2} would be equal to,

$$V_{GG2} = 2(0.426) + 0.7 = 1.552\text{V}$$

Simulation of the Cascode CMOS Current Sink

Example

Use the model parameters K_N'=110μA/V^2, V_T = 0.7 and λ_N = 0.04V^{-1} to calculate (a) the small-signal output resistance for the simple current sink if I_{OUT} = 100μA and (b) the small-signal output resistance for the cascode current sink with I_{OUT} = 100μA. Assume that all W/L values are 1.

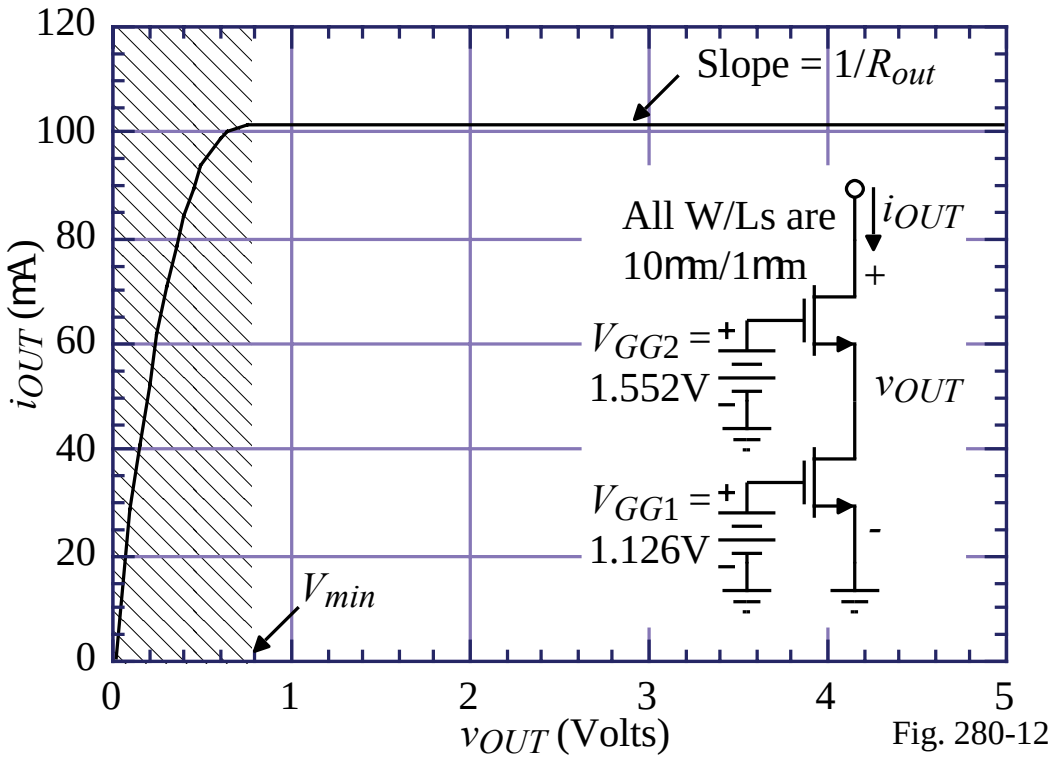


Fig. 280-12

Solution

(a) Using λ = 0.04 V^{-1} and I_{OUT} = 100μA gives r_{ds1} = 250kΩ = r_{ds2}. (b) Ignoring the bulk effect, we find that g_{m1} = g_{m2} = 469μS which gives r_{out} = (250kΩ)(469μS)(250kΩ) = 29.32MΩ.

High-Swing Cascode Current Sink

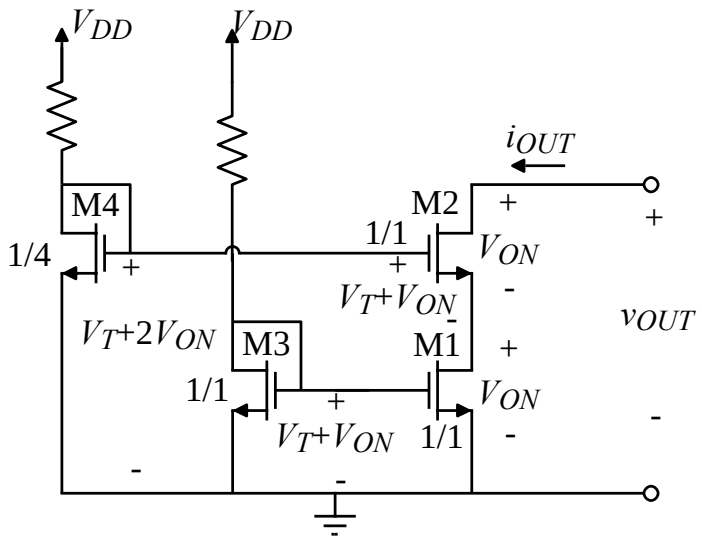
This current sink achieves the smallest possible V_{MIN}.

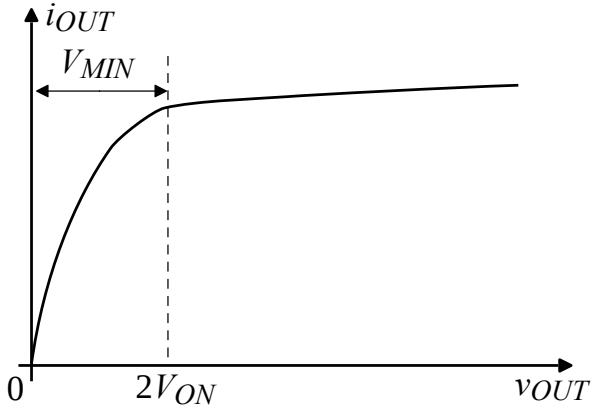
Since

$$V_{ON} = \sqrt{\frac{2I_D}{K'(W/L)}}$$

then if L/W of M4 is quadrupled, V_{ON} is doubled to get

$$V_{MIN} = 2V_{ON}.$$





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Example

Use the cascode current sink configuration above to design a current sink of 100µA and a V_{MIN} = 1V. Assume the device parameters of Table 3.1-2.

Solution

With V_{MIN} = 1V, choose V_{ON} = 0.5V. Assuming M1 and M2 are identical gives

$$\frac{W}{L} = \frac{2 \cdot I_{OUT}}{K' \cdot V_{ON}^2} = \frac{2 \cdot 100\text{x}10^{-6}}{110\text{x}10^{-6}\text{x}0.25} = 7.27 \quad \Rightarrow \quad \frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{W_3}{L_3} = \underline{\underline{7.27}} \text{ and } \frac{W_4}{L_4} = \underline{\underline{1.82}}$$

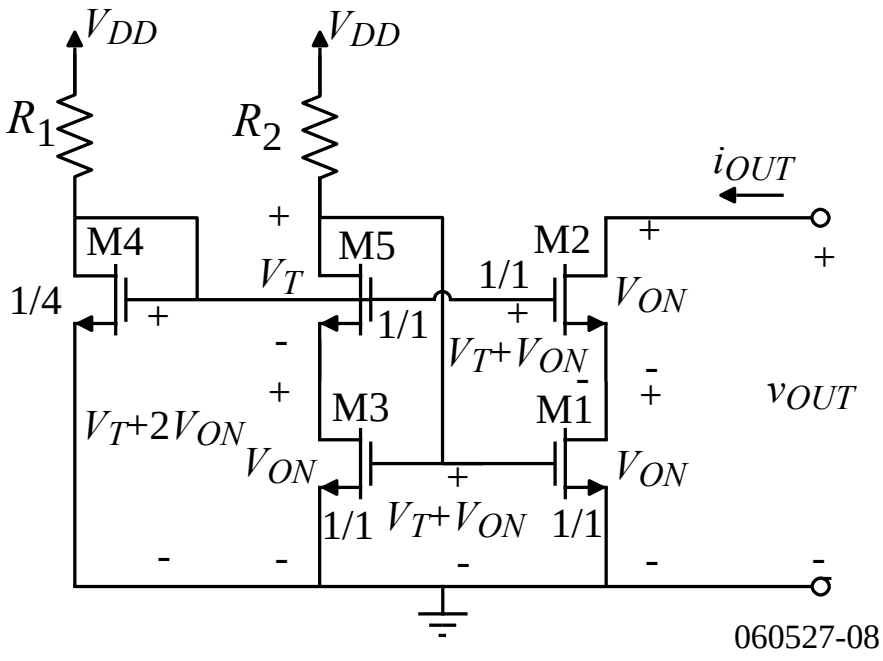
Unfortunately, the drain voltages of M1 and M3 are not matched.

Improved High-Swing Cascode Current Sink

Because the drain-source voltages of the matching transistors, M1 and M3 are not equal, $i_{OUT} \neq I_{REF}$.

To circumvent this problem the cascode current sink shown is utilized:

Note that the drain-source voltage of M1 and M3 are identical causing i_{OUT} to be a replication of I_{REF}.



Design Procedure

1.) Since $V_{MIN} = 2V_{ON} = 2V_{DS}(\text{sat})$, let $V_{ON} = 0.5V_{MIN}$.

2.) $$V_{ON} = \sqrt{\frac{2I_{REF}}{K'(W/L)}} \quad \Rightarrow \quad \frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{W_3}{L_3} = \frac{W_5}{L_5} = \frac{2I_{REF}}{K'V_{ON}^2} = \frac{8I_{REF}}{K'V_{MIN}^2}$$

3.) $$\frac{W_4}{L_4} = \frac{2I_{REF}}{K'(V_{GS4}-V_T)^2} = \frac{2I_{REF}}{K'(2V_{ON})^2} = \frac{I_{REF}}{2K'V_{ON}^2}$$

Signal Flow in Transistors

The last example brings up an interesting and important point. This point is illustrated by the following question, "How does I_{REF} flow into the M3-M5 combination of transistors since there is no path to the gate of M5?"

Consider how signals flow in transistors:

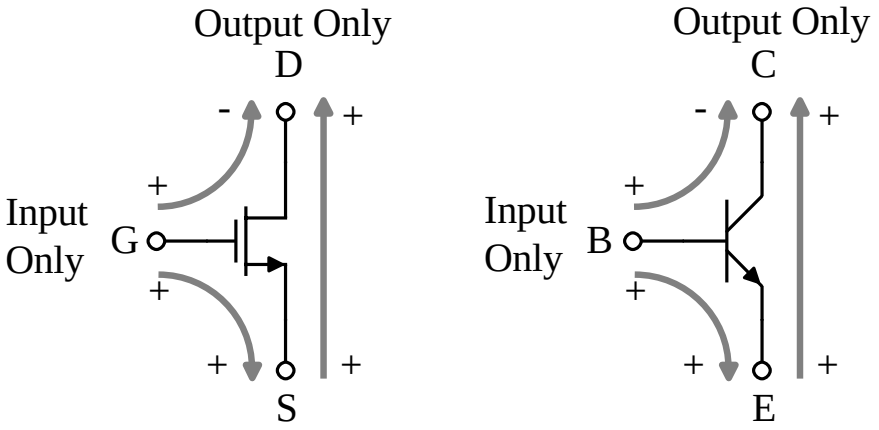


Fig. 4.3-12B

Answer to the above question:

As V_{DD} increases (i.e. the circuit begins to operate), I_{REF} cannot flow into the drain of M5, so it flows through the path indicated by the arrow to the gate of M3. It charges the stray capacitance and causes the gate-source voltage of M3 to increase to the exact value necessary to cause I_{REF} to flow through the M3-M5 combination.

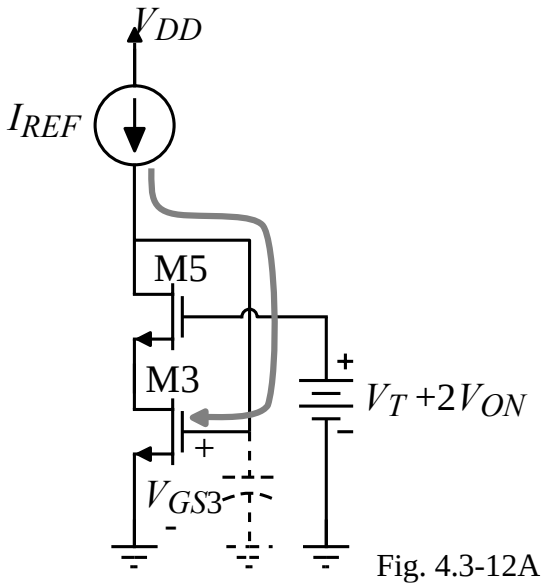


Fig. 4.3-12A

Example 15-1 - Design of a Minimum V_{MIN} Current Sink

Assume I_{REF} = 100µA and design a cascode current sink with a V_{MIN} = 0.3V using the following parameters: VTO=0.7, KP=110U, LAMBDA=0.04, GAMMA=0.4, PHI=0.7

Solution

From the previous equations, we get

$$\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{W_3}{L_3} = \frac{W_5}{L_5} = \frac{8I_{REF}}{K'V_{MIN}{}^2} = \frac{8\cdot 100}{110\cdot(0.3\text{V})^2} = 80.8 \text{ and}$$

$$\frac{W_4}{L_4} = \frac{I_{REF}}{2K'V_{ON}{}^2} = \frac{100}{2\cdot 110\cdot 0.15^2} = 20.2$$

Simulation Results:

```
Low Vmin Cascade Current Sink - Method No. 2
M1 5 1 0 0 MNMOS W=81U L=1U
M2 2 3 5 5 MNMOS W=81U L=1U
M3 4 1 0 0 MNMOS W=81U L=1U
M4 3 3 0 0 MNMOS W=20U L=1U
M5 1 3 4 4 MNMOS W=81U L=1U
.MODEL MNMOS NMOS VTO=0.7 KP=110U
+LAMBDA=0.04 GAMMA=0.4 PHI=0.7
VDD 6 0 DC 5V
IIN1 6 1 DC 100U
IIN2 6 3 DC 100U
VOUT 2 0 DC 5.0
.OP
.DC VOUT 5 0 0.05
.PRINT DC ID(M2)
.END
```

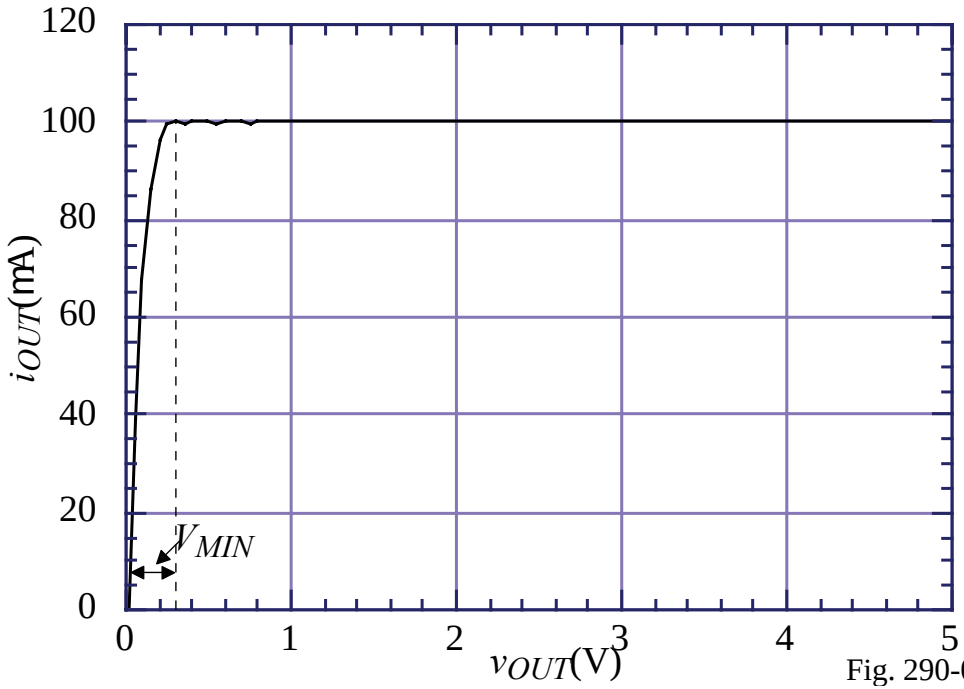


Fig. 290-06

Self-Biased Cascode Current Sink†

The $V_T + 2V_{ON}$ bias voltage is developed through a series resistor.

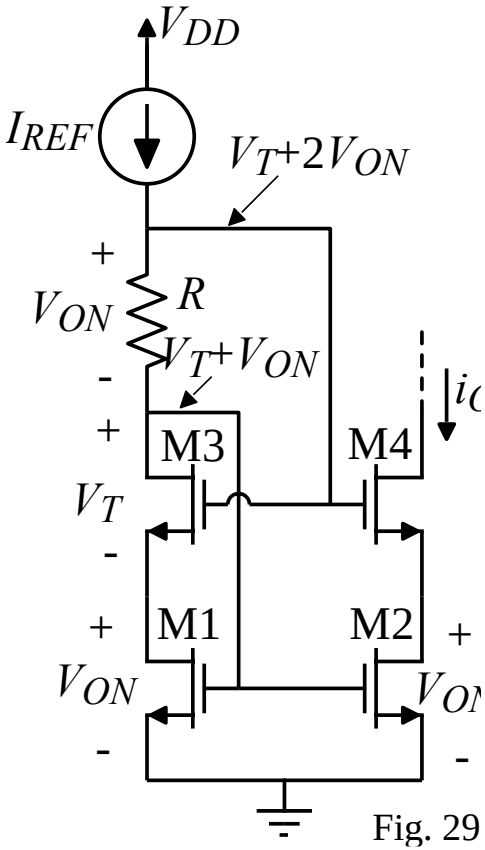


Fig. 29

Design procedure:

Same as the previous except

$$R = \frac{V_{ON}}{I_{REF}} = \frac{V_{MIN}}{2I_{REF}}$$

For the previous example,

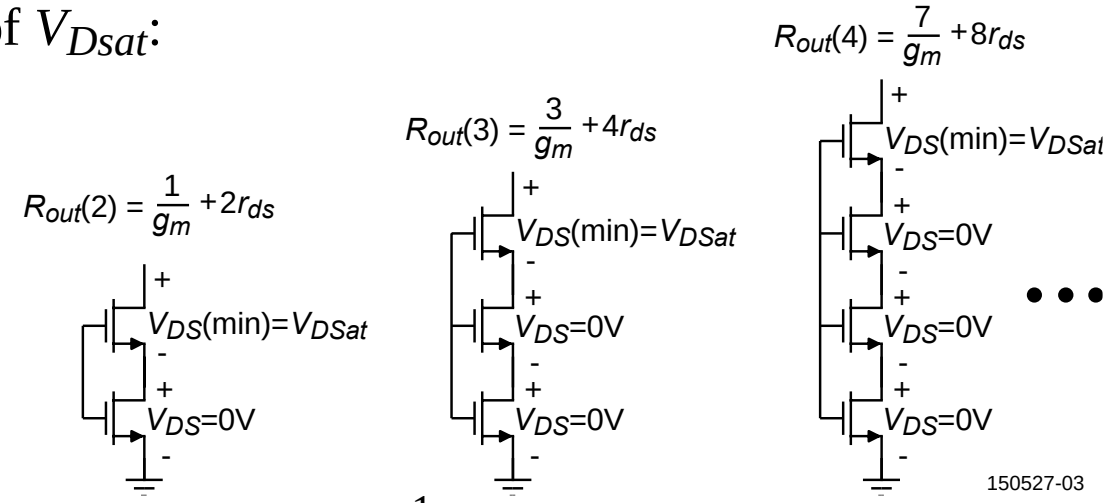
$$R = \frac{0.3\text{V}}{2 \cdot 100\mu\text{A}} = 1.5\text{k}\Omega$$

If the reference current is small, R can become large.

† T.L. Brooks and A.L. Westwick, "A Low-Power Differential CMOS Bandgap Reference," *Proc. of IEEE Inter. Solid-State Circuits Conf.*, Feb. 1994, pp. 248-249.

Minimum Voltage Cascode Sinks

The following configuration gives increased output resistance with a fixed minimum voltage drop of V_{Dsat}:



It can be shown that $R_{out}(n)$ is $\frac{2^{n-1}-1}{g_m} + 2^{n-1}r_{ds}$ if the gates are grounded. Therefore, the output resistance is increasing by a factor of 2^{n-1} for each cascade device and the minimum voltage across the sink remains constant at V_{DSat}.

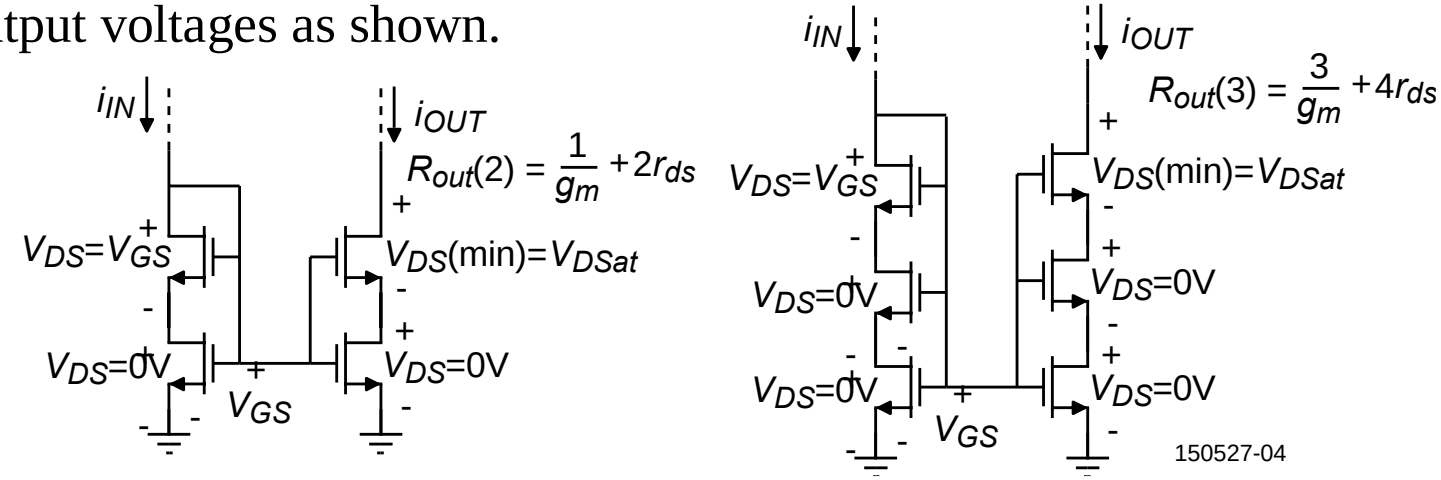
The upper transistor is in saturation while all the other transistors have $V_{DS} = 0$ which implies that $g_m = 0$ and $r_{ds} = 1/g_m(\text{sat})$.

This really only works well if the transistors are isolated and the bulk can be connected to the source.

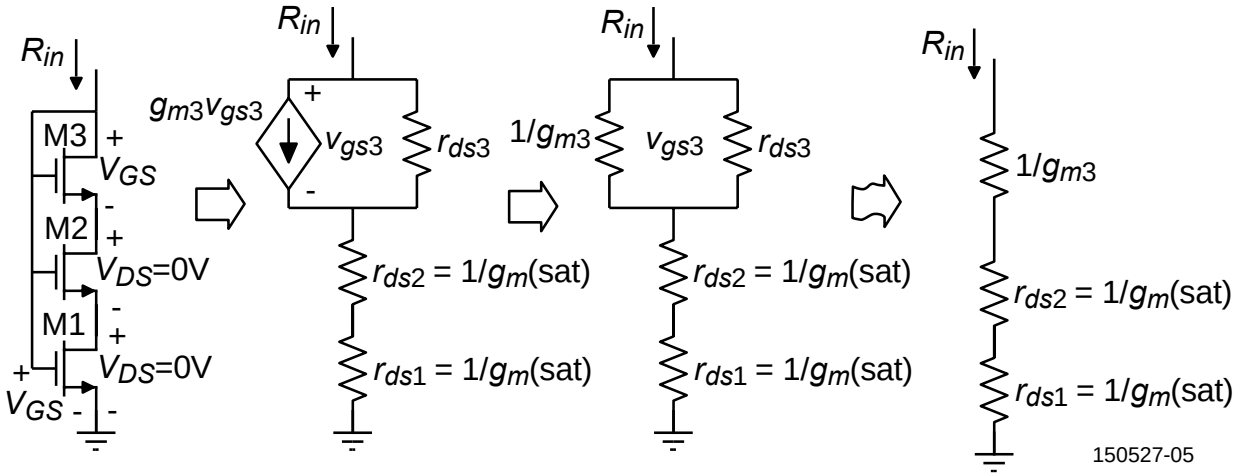
The area required for the sink will increase significantly because of the isolation.

Minimum Voltage Cascode Current Mirrors

The previous technique can be used to create current mirrors with low minimum input and output voltages as shown.



The input resistance to the current mirrors can be written as $R_{in} \approx \frac{n}{g_m}$. This is illustrated by the following small signal model (remember when $V_{DS} = 0$ that $g_m = 0$ and $r_{ds} = 1/g_m(\text{sat})$.



MOS Regulated Cascode Sink†

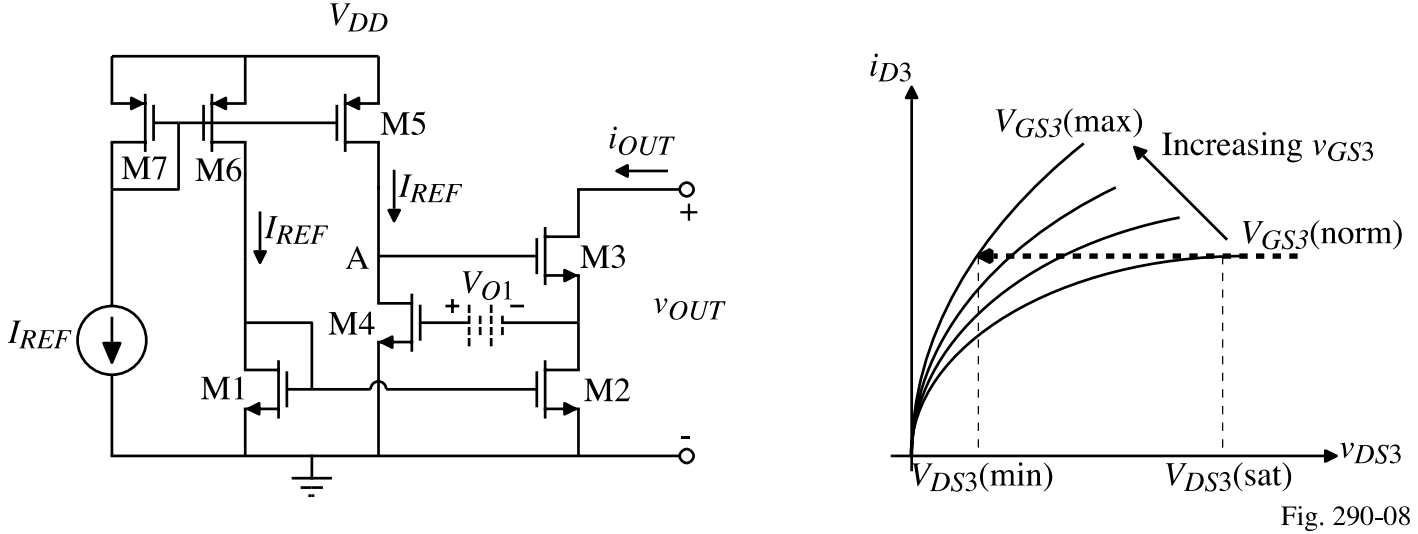


Fig. 290-08

Comments:

- Achieves very high output resistance by increasing the loop gain (return-ratio) due to the M4-M5 inverting amplifier.

$$\text{LG} = g_{m3}r_{ds2}\left(\frac{g_{m4}}{g_{ds4}+g_{ds5}}\right) \approx \frac{g_{m3}r_{ds2}g_{m4}r_{ds4}}{2}$$

If $r_{ds4} \approx r_{ds5}$, then $r_{out} \approx \dfrac{r_{ds3}g_{m3}r_{ds2}g_{m4}r_{ds4}}{2}$

- M3 maintains "constant" current even though it is no longer in the saturation region.

† E. Sackinger and W. Guggenbuhl, "A Versatile Building Block: The CMOS Differential Difference Amplifier," *IEEE J. of Solid-State Circuits*, vol. SC-22, no. 2, pp. 287-294, April 1987.

Regulated Cascode Current Sink - Continued

Small signal model:

Solving for the output resistance:

$$i_{out} = g_{m3}v_{gs3} + g_{ds3}(v_{out}-v_{gs4})$$

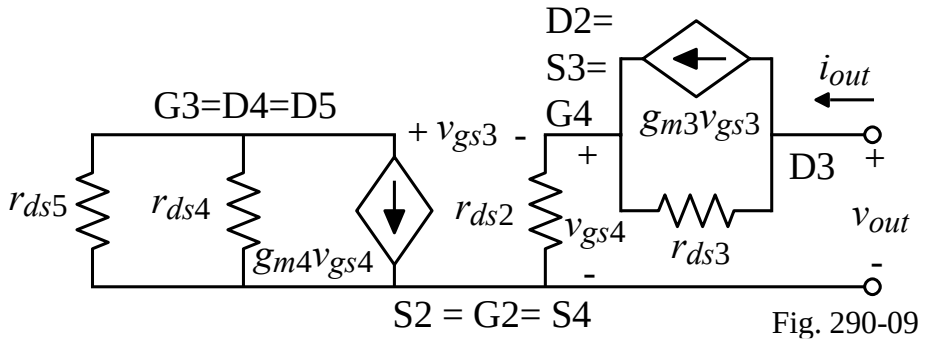


Fig. 290-09

But

$$v_{gs4} = i_{out}r_{ds2}$$

and

$$v_{gs3} = v_{g3} - v_{s3} = -g_{m4}(r_{ds4}\|r_{ds5})v_{gs4} - v_{gs4} = -r_{ds2}[1 + g_{m4}(r_{ds4}\|r_{ds5})]i_{out}$$

$$\therefore \quad i_{out} = -g_{m3}r_{ds2}[1 + g_{m4}(r_{ds4}\|r_{ds5})]i_{out} + g_{ds3}v_{out} - g_{ds3}r_{ds2}i_{out}$$

$$v_{out} = r_{ds3}[1 + g_{m3}r_{ds2} + g_{ds3}r_{ds2} + g_{m3}r_{ds2}g_{m4}(r_{ds4}\|r_{ds5})]i_{out}$$

$$\therefore r_{out} = \frac{v_{out}}{i_{out}} = r_{ds3}[1 + g_{m3}r_{ds2} + g_{ds3}r_{ds2} + g_{m3}r_{ds2}g_{m4}(r_{ds4}\|r_{ds5})]$$

$$\approx r_{ds3}g_{m3}r_{ds2}g_{m4}(r_{ds4}\|r_{ds5})$$

If I_{REF} = 100µA, all W/Ls are 10µm/1µm we get r_{ds} = 0.25MΩ and g_m = 469µS which gives

$$r_{out} \approx (0.25\text{M}\Omega)(469\mu\text{S})(0.25\text{M}\Omega)(469\mu\text{S})(0.125\text{M}\Omega) = 1.72\text{G}\Omega$$

Can 1GΩ Output Resistance Really be Achieved?

No, because of substrate currents.
Substrate currents are caused by impact ionization due to high electric fields cause an impact which generates a hole-electron pair. The electrons flow out the drain and the holes flow into the substrate causing a substrate current flow.

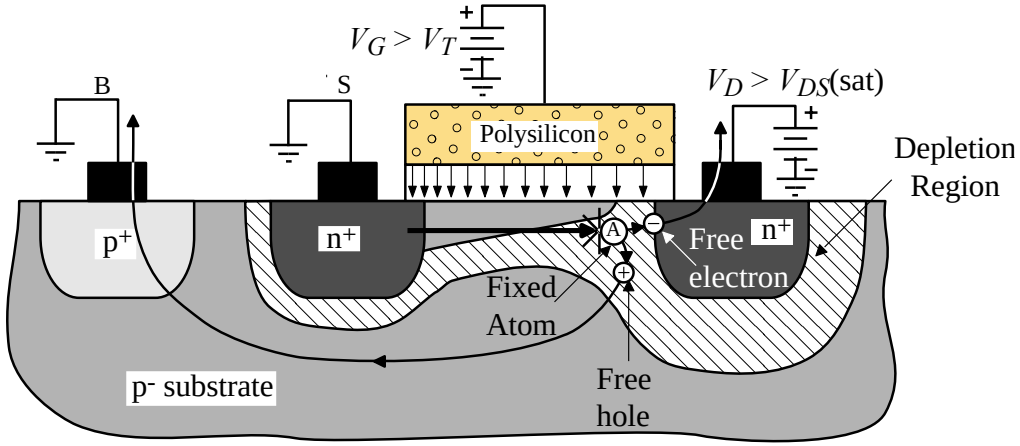


Fig130-7

Max. output resistance ≈ 500MΩ-1GΩ

Substrate current:

$$i_{DB} = K_1(v_{DS} - v_{DS}(\text{sat}))i_D e^{-[K_2/(v_{DS}-v_{DS}(\text{sat}))]}$$

where

K_1 and K_2 are process-dependent parameters

(typical values: $K_1 = 5\text{V}^{-1}$ and $K_2 = 30\text{V}$)

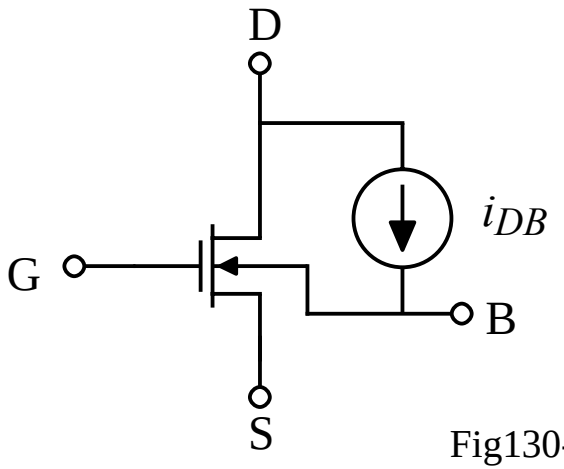


Fig130-8

Small-signal model:

$$g_{db} = \frac{i_{DB}}{v_{DB}} = K_2 \frac{I_{DB}}{V_{DS} - V_{DS}(\text{sat})} \approx 1\text{nS}$$

This conductance will prevent the realization of very high-output resistances.

Minimizing the V_{MIN} of the Regulated Cascode Current Sink

V_{MIN}:

Without the use of the V_{O1} battery shown, V_{MIN} is pretty bad. It is,

$V_{MIN} = V_{GS4} + V_{DS3}(\text{sat}) = V_T + 2V_{ON}$

Minimizing V_{MIN}:

If $V_{O1} = V_T$, then $V_{MIN} = 2V_{ON}$. This is accomplished by the following circuit:

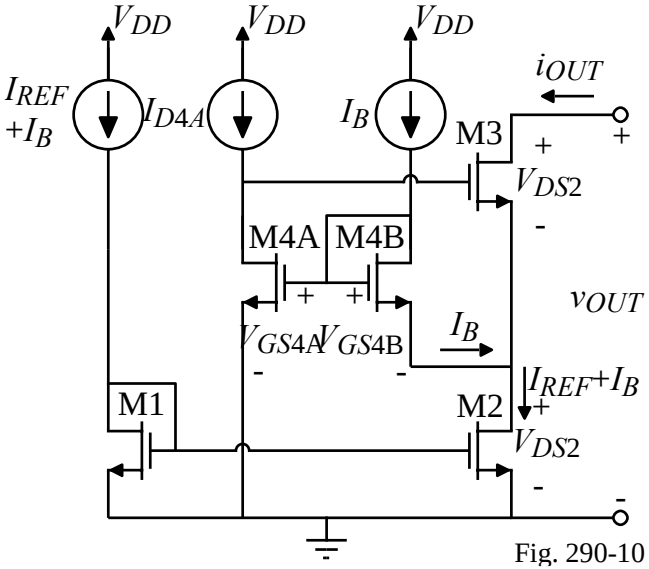


Fig. 290-10

If $V_{GS4A} - V_{GS4B} = V_{DS2}(\text{sat}) = V_{ON}$, then $V_{MIN} = 2V_{ON}$

$$\sqrt{\frac{2I_{D4}}{K_N'(W_{4A}/L_{4A})}} - \sqrt{\frac{2I_B}{K_N'(W_{4B}/L_{4B})}} = \sqrt{\frac{2I_B+2I_{REF}}{K_N'(W_2/L_2)}}$$

or

$$\sqrt{\frac{I_{D4}}{W_{4A}/L_{4A}}} - \sqrt{\frac{I_B}{W_{4B}/L_{4B}}} = \sqrt{\frac{I_B+I_{REF}}{W_2/L_2}}$$

A number of solutions exist. For example, let $I_B = I_{REF}$. This gives $I_{D4A} = 5.824I_{REF}$ assuming all W/L ratios are identical.

Example 15-2 - Design of a Minimum V_{MIN} Regulated Cascode Current Sink

Design a regulated cascode current sink for 100µA and minimum voltage of V_{MIN} = 0.3V.

Solution

Let the W/L ratios of M1 through M5 be equal and let I_B = 10µA. Therefore,

$$V_{MIN} = 0.3\text{V} = V_{ON3} + V_{ON2} = \sqrt{\frac{2\cdot 100\mu\text{A}}{110\mu\text{A/V}^2(W/L)}} + \sqrt{\frac{2\cdot 110\mu\text{A}}{110\mu\text{A/V}^2(W/L)}}$$

$$= \sqrt{\frac{2\cdot 100\mu\text{A}}{110\mu\text{A/V}^2(W/L)}}\left(\sqrt{1} + \sqrt{1.1}\right)$$

Therefore,

$$0.3\text{V} = \sqrt{\frac{2\cdot 100\mu\text{A}}{110\mu\text{A/V}^2(W/L)}}(2.049)$$

$$\frac{W}{L} = \frac{2\cdot 100\mu\text{A}\cdot 2.049^2}{110\mu\text{A/V}^2 0.3^2} = 84.8 \approx 85.$$

With I_B = 10µA, then I_{D4A} = $\left(\sqrt{10} + \sqrt{110}\right)^2$ = 186µA

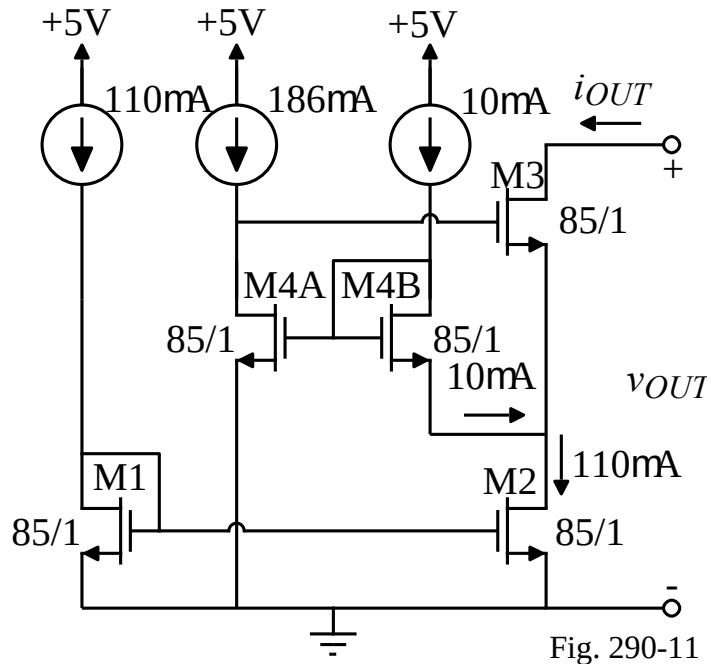


Fig. 290-11

Comparison of the MOS Cascode and Regulated Cascode Current Sink

Close examination in the knee area reveals interesting differences.

Simulation results:

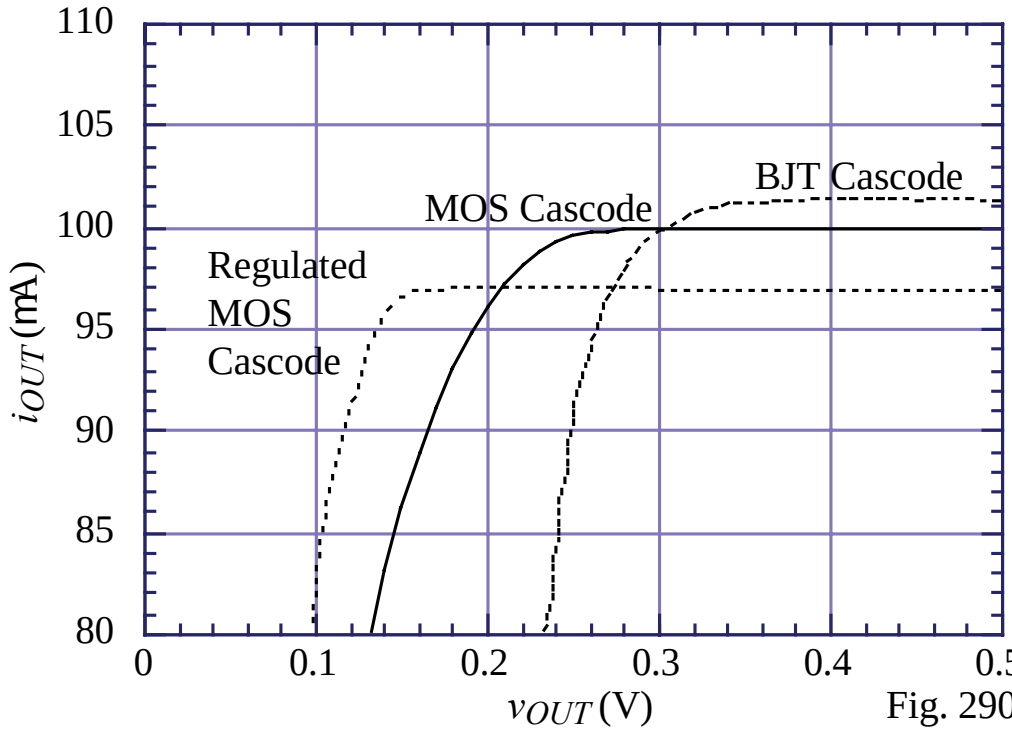


Fig. 290-12

Comments:

- The regulated cascode current is smaller than the cascode current because the drain-source voltages of M1 and M2 are not equal.
- The regulated cascode current sink has a smaller V_{MIN} due to the fact that M3 can have a drain-source voltage smaller than V_{DS}(sat)

SUMMARY

Summary of Both BJT and MOS Current Sinks/Sources

Current Sink/Source	r_{OUT}	V_{MIN}
Simple MOS Current Sink	$r_{ds} = \frac{1}{\lambda I_D}$	$V_{DS}(\text{sat}) = V_{ON}$
Simple BJT Current Sink	$r_o = \frac{V_A}{I_C}$	$V_{CE}(\text{sat}) \approx 0.2\text{V}$
Cascode MOS	$\approx g_{m2} r_{ds2} r_{ds1}$	$2V_{ON}$
Cascode BJT	$\approx \beta_F r_o$	$2V_{CE}(\text{sat})$
Regulated Cascode Current Sink	$\approx r_{ds3} g_{m3} r_{ds2} g_{m4} (r_{ds4} \| r_{ds5})$	$\approx V_T + V_{ON}$
Minimum V_{MIN} Regulated Cascode Current Sink	$\approx r_{ds3} g_{m3} r_{ds2} g_{m4} (r_{ds4} \| r_{ds5})$	$\approx V_{ON}$

Resistor Implementations

- MOSFET resistors may use less area than actual resistors
- Linearity is the primary issue for MOSFET resistor realizations