LECTURE 13 – COMPUTER MODELS AND EXTRACTION OF THE SIMPLE LARGE SIGNAL MODEL

LECTURE ORGANIZATION

Outline

- Computer Models
- Extraction of a large signal model for hand calculations
- Extraction of the simple model for short channel MOSFETs
- Summary

CMOS Analog Circuit Design, 3rd Edition Reference

Pages 90-96 and 662-685

COMPUTER MODELS

FET Model Generations

- First Generation – Physically based analytical model including all geometry dependence.
- Second Generation – Model equations became subject to mathematical conditioning for circuit simulation. Use of empirical relationships and parameter extraction.
- Third Generation – A return to simpler model structure with reduced number of parameters which are physically based rather than empirical. Uses better methods of mathematical conditioning for simulation including more specialized smoothing functions.

Performance Comparison of Models (from Cheng and Hu, *MOSFET Modeling & BSIM3 Users Guide*)

Model	Minimum L (µm)	Minimum Tox (nm)	Model Continuity	i_D Accuracy in Strong Inversion	i_D Accuracy in Subthreshold	Small signal parameter	Scalability
MOS1	5	50	Poor	Poor	Not Modeled	Poor	Poor
MOS2	2	25	Poor	Poor	Poor	Poor	Fair
MOS3	1	20	Poor	Fair	Poor	Poor	Poor
BSIM1	0.8	15	Fair	Good	Fair	Poor	Fair
BSIM2	0.35	7.5	Fair	Good	Good	Fair	Fair
BSIM3v2	0.25	5	Fair	Good	Good	Good	Good
BSIM3v3	0.15	4	Good	Good	Good	Good	Good

First Generation Models

Level 1 (MOS1)

- Basic square law model based on the gradual channel approximation and the square law for saturated drain current.
- Good for hand analysis.
- Needs improvement for deep-submicron technology (must incorporate the square law to linear shift)

Level 2 (MOS2)

- First attempt to include small geometry effects
- Inclusion of the channel-bulk depletion charge results in the familiar 3/2 power terms
- Introduced a simple subthreshold model which was not continuous with the strong inversion model.
- Model became quite complicated and probably is best known as a "developing ground" for better modeling techniques.

Level 3 (MOS3)

- Used to overcome the limitations of Level 2. Made use of a semi-empirical approach.
- Added DIBL and the reduction of mobility by the lateral field.
- Similar to Level 2 but considerably more efficient.
- Used binning but was poorly implemented.

Second Generation Models

BSIM (Berkeley Short-Channel IGFET Model)

- Emphasis is on mathematical conditioning for circuit simulation
- Short channel models are mostly empirical and shifts the modeling to the parameter extraction capability
- Introduced a more detailed subthreshold current model with good continuity
- Poor modeling of channel conductance

HSPICE Level 28

- Based on BSIM but has been extensively modified.
- More suitable for analog circuit design
- Uses model binning
- Model parameter set is almost entirely empirical
- User is locked into HSPICE
- Model is proprietary

BSIM2

- Closely based on BSIM
- Employs several expressions developed from two dimensional analysis
- Makes extensive modifications to the BSIM model for mobility and the drain current
- Uses a new subthreshold model
- Output conductance model makes the model very suitable for analog circuit design

Third Generation Models

BSIM2 – Continued

- The drain current model is more accurate and provides better convergence
- Becomes more complex with a large number of parameters
- No provisions for variations in the operating temperature

BSIM3

- This model has achieved stability and is being widely used in industry for deep submicron technology.
- Initial focus of simplicity was not realized.

MOS Model 9

- Developed at Philips Laboratory
- Has extensive heritage of industrial use
- Model equations are clean and simple – should be efficient

Other Candidates

- EKV (Enz-Krummenacher-Vittoz) – fresh approach well suited to the needs of analog circuit design

BSIM2 Model

Generic composite expression for the model parameters:

$$X = X_o + \frac{LX}{L_{eff}} + \frac{WX}{W_{eff}}$$

where

X_o = parameter for a given W and L

LX (WX) = first-order dependence of X on L (W)

Modeling features of BSIM2:

Mobility

- Mobility reduction by the vertical and the lateral field

Drain Current

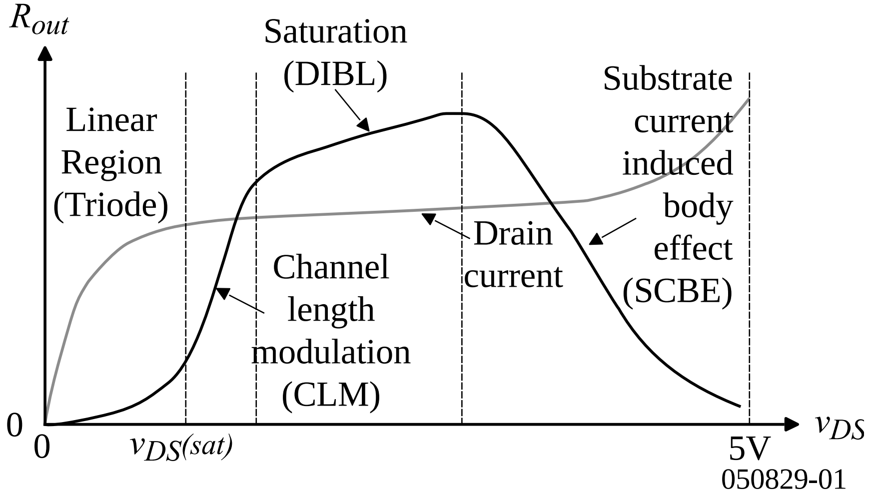
- Velocity saturation
- Linear region drain current
- Saturation region drain current
- Subthreshold current

$$i_{DS} = \frac{\mu_o C_{ox} W_{eff}}{L_{eff}} \cdot \left(\frac{kT}{q}\right) \frac{e^{v_{GS}-V_t-V_{off}}}{n} \cdot \left[1 - e^{qV_{DS}/kT}\right]$$

where

$$V_{off} = VOF + VOFB \cdot v_{BS} + VOFD \cdot v_{DS} \quad \text{and} \quad n = NO + \frac{NB}{\sqrt{PHI - v_{BS}}} + ND \cdot v_{DS}$$

BSIM2 Output Conductance Model



- Drain-Induced Barrier Lowering (DIBL) – Lowering of the potential barrier at the source-bulk junction allowing carriers to traverse the channel at a lower gate bias than would otherwise be expected.
- Substrate Current-Induced Body Effect (SCBE) – The high field near the drain accelerates carriers to high energies resulting in impact ionization which generates a hole-electron pair (hot carrier generation). The opposite carriers are swept into the substrate and have the effect of slightly forward-biasing the source-substrate junction. This reduces the threshold voltage and increases the drain current.

Charge Model

- Eliminates the partitioning choice (50%/50% is used)
- BSIM charge model better documented with more options

BSIM3 Model

The background for the BSIM3 model and the equations are given in detail in the text *MOSFET Modeling & BSIM3 User's Guide*, by Y. Cheng and C. Hu, Kluwer Academic Publishers, 1999.

The short channel effects included in the BSIM3 model are:

- Normal and reverse short-channel and narrow-width effects on the threshold.
- Channel length modulation (*CLM*).
- Drain induced barrier lowering (*DIBL*).
- Velocity saturation.
- Mobility degradation due to the vertical electric field.
- Impact ionization.
- Band-to-band tunneling.
- Velocity overshoot.
- Self-heating.

1.) Channel quantization.

2.) Polysilicon depletion.

BSIM3v3 Model Equations for Hand Calculations

In strong inversion, approximate hand equations are:

$$i_{DS} = \mu_{eff}C_{ox}\frac{W_{eff}}{L_{eff}}\frac{1}{1+\dfrac{v_{DS}}{E_{sat}L_{eff}}}\left(v_{GS} - V_{th} - \frac{A_{bulk}v_{DS}}{2}\right)v_{DS}\ , \qquad v_{DS} < V_{DS}(\mathrm{sat})$$

$$i_{DS} = W_{eff}v_{sat}C_{ox}[v_{GS} - V_{th} - A_{bulk}V_{DS}(\mathrm{sat})]\left(1+\frac{v_{DS} - V_{DS}(\mathrm{sat})}{V_A}\right), \qquad v_{DS} > V_{DS}(\mathrm{sat})$$

where

$$V_{DS}(\mathrm{sat}) = \frac{E_{sat}L_{eff}(v_{GS}-V_{th})}{A_{bulk}E_{sat}L_{eff} + (v_{GS}-V_{th})}$$

$L_{eff} = L_{drawn} - 2\Delta L$

$W_{eff} = W_{drawn} - 2\Delta W$

E_{sat} = Electric field where the drift velocity (v) saturates

v_{sat} = saturation velocity of carriers in the channel

$$\mu = \frac{\mu_{eff}}{1+(E_y/E_{sat})} \qquad \Rightarrow \qquad \mu_{eff} = \frac{2v_{sat}}{E_{sat}}$$

Note: Assume $A_{bulk} \approx 1$ and extract V_{th} and V_A.

MOSIS Parametric Test Results

http://www.mosis.org/

RUN: T02D VENDOR: TSMC
TECHNOLOGY: SCN025 FEATURE SIZE: 0.25 microns

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: TSMC 0251P5M.

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	0.36/0.24			
Vth		0.54	-0.50	volts
SHORT	20.0/0.24			
Idss		557	-256	uA/um
Vth		0.56	-0.56	volts
Vpt		7.6	-7.2	volts
WIDE	20.0/0.24			
Ids0		6.6	-1.5	pA/um
LARGE	50.0/50.0			
Vth		0.47	-0.60	volts
Vjbkd		5.8	-7.0	volts
Ijlk		-25.0	-1.1	pA
Gamma		0.44	0.61	$V^{0.5}$
K’ (Uo*Cox/2)		112.0	-23.0	uA/V^2

0.25µm BSIM3v3.1 NMOS Parameters

```
.MODEL CMOSN NMOS (                    LEVEL   = 49
+VERSION = 3.1         TNOM    = 27          TOX     = 5.7E-9
+XJ      = 1E-7        NCH     = 2.3549E17   VTH0    = 0.4273342
+K1      = 0.3922983   K2      = 0.0185825   K3      = 1E-3
+K3B     = 2.0947677   W0      = 2.171779E-7 NLX     = 1.919758E-7
+DVT0W   = 0           DVT1W   = 0           DVT2W   = 0
+DVT0    = 7.137212E-3 DVT1    = 6.066487E-3 DVT2    = -0.3025397
+U0      = 403.1776038 UA      = -3.60743E-12 UB     = 1.323051E-18
+UC      = 2.575123E-11 VSAT   = 1.616298E5  A0      = 1.4626549
+AGS     = 0.3136349   B0      = 3.080869E-8 B1      = -1E-7
+KETA    = 5.462411E-3 A1      = 4.653219E-4 A2      = 0.6191129
+RDSW    = 345.624986  PRWG    = 0.3183394   PRWB    = -0.1441065
+WR      = 1           WINT    = 8.107812E-9 LINT    = 3.375523E-9
+XL      = 3E-8        XW      = 0           DWG     = 6.420502E-10
+DWB     = 1.042094E-8 VOFF    = -0.1083577  NFACTOR = 1.1884386
+CIT     = 0           CDSC    = 2.4E-4      CDSCD   = 0
+CDSCB   = 0           ETA0    = 4.914545E-3 ETAB    = 4.215338E-4
+DSUB    = 0.0313287   PCLM    = 1.2088426   PDIBLC1 = 0.7240447
+PDIBLC2 = 5.120303E-3 PDIBLCB = -0.0443076  DROUT   = 0.7752992
+PSCBE1  = 4.451333E8  PSCBE2  = 5E-10       PVAG    = 0.2068286
+DELTA   = 0.01        MOBMOD  = 1           PRT     = 0
+UTE     = -1.5        KT1     = -0.11       KT1L    = 0
+KT2     = 0.022       UA1     = 4.31E-9     UB1     = -7.61E-18
+UC1     = -5.6E-11    AT      = 3.3E4       WL      = 0
+WLN     = 1           WW      = -1.22182E-16 WWN    = 1.2127
+WWL     = 0           LL      = 0           LLN     = 1
+LW      = 0           LWN     = 1           LWL     = 0
+CAPMOD  = 2           XPART   = 0.4         CGDO    = 6.33E-10
+CGSO    = 6.33E-10    CGBO    = 1E-11       CJ      = 1.766171E-3
+PB      = 0.9577677   MJ      = 0.4579102   CJSW    = 3.931544E-10
+PBSW    = 0.99        MJSW    = 0.2722644   CF      = 0
+PVTH0   = -2.126483E-3 PRDSW  = -24.2435379 PK2     = -4.788094E-4
+WKETA   = 1.430792E-3 LKETA   = -6.548592E-3   )
```

0.25μm BSIM3v3.1 PMOS Parameters

```
MODEL CMOSP PMOS (                        LEVEL   = 49
+VERSION = 3.1         TNOM    = 27          TOX     = 5.7E-9
+XJ      = 1E-7        NCH     = 4.1589E17   VTH0    = -0.6193382
+K1      = 0.5275326   K2      = 0.0281819   K3      = 0
+K3B     = 11.249555   W0      = 1E-6        NLX     = 1E-9
+DVT0W   = 0           DVT1W   = 0           DVT2W   = 0
+DVT0    = 3.1920483   DVT1    = 0.4901788   DVT2    = -0.0295257
+U0      = 185.1288894 UA      = 3.40616E-9  UB      = 3.640498E-20
+UC      = -6.35238E-11 VSAT   = 1.975064E5  A0      = 0.4156696
+AGS     = 0.0702036   B0      = 3.111154E-6 B1      = 5E-6
+KETA    = 0.0253118   A1      = 2.421043E-4 A2      = 0.6754231
+RDSW    = 866.896668  PRWG    = 0.0362726   PRWB    = -0.293946
+WR      = 1           WINT    = 6.519911E-9 LINT    = 2.210804E-8
+XL      = 3E-8        XW      = 0           DWG     = -2.423118E-8
+DWB     = 3.052612E-8 VOFF    = -0.1161062  NFACTOR = 1.2546896
+CIT     = 0           CDSC    = 2.4E-4      CDSCD   = 0
+CDSCB   = 0           ETA0    = 0.7241245   ETAB    = -0.3675267
+DSUB    = 1.1734643   PCLM    = 1.0837457   PDIBLC1 = 9.608442E-4
+PDIBLC2 = 0.0176785   PDIBLCB = -9.605935E-4 DROUT  = 0.0735541
+PSCBE1  = 1.579442E10 PSCBE2  = 6.707105E-9 PVAG    = 0.0409261
+DELTA   = 0.01        MOBMOD  = 1           PRT     = 0
+UTE     = -1.5        KT1     = -0.11       KT1L    = 0
+KT2     = 0.022       UA1     = 4.31E-9     UB1     = -7.61E-18
+UC1     = -5.6E-11    AT      = 3.3E4       WL      = 0
+WLN     = 1           WW      = 0           WWN     = 1
+WWL     = 0           LL      = 0           LLN     = 1
+LW      = 0           LWN     = 1           LWL     = 0
+CAPMOD  = 2           XPART   = 0.4         CGDO    = 5.11E-10
+CGSO    = 5.11E-10    CGBO    = 1E-11       CJ      = 1.882953E-3
+PB      = 0.99        MJ      = 0.4690946   CJSW    = 3.018356E-10
+PBSW    = 0.8137064   MJSW    = 0.3299497   CF      = 0
+PVTH0   = 5.268963E-3 PRDSW   = -2.2622317  PK2     = 3.952008E-3
+WKETA   = -7.69819E-3 LKETA   = -0.0119828    )
```

EXTRACTION OF A LARGE SIGNAL MODEL FOR HAND CALCULATIONS

Objective

Extract a simple model that is useful for design from the computer models such as BSIM3.

Extraction for Short Channel Models

Procedure for extracting short channel models:

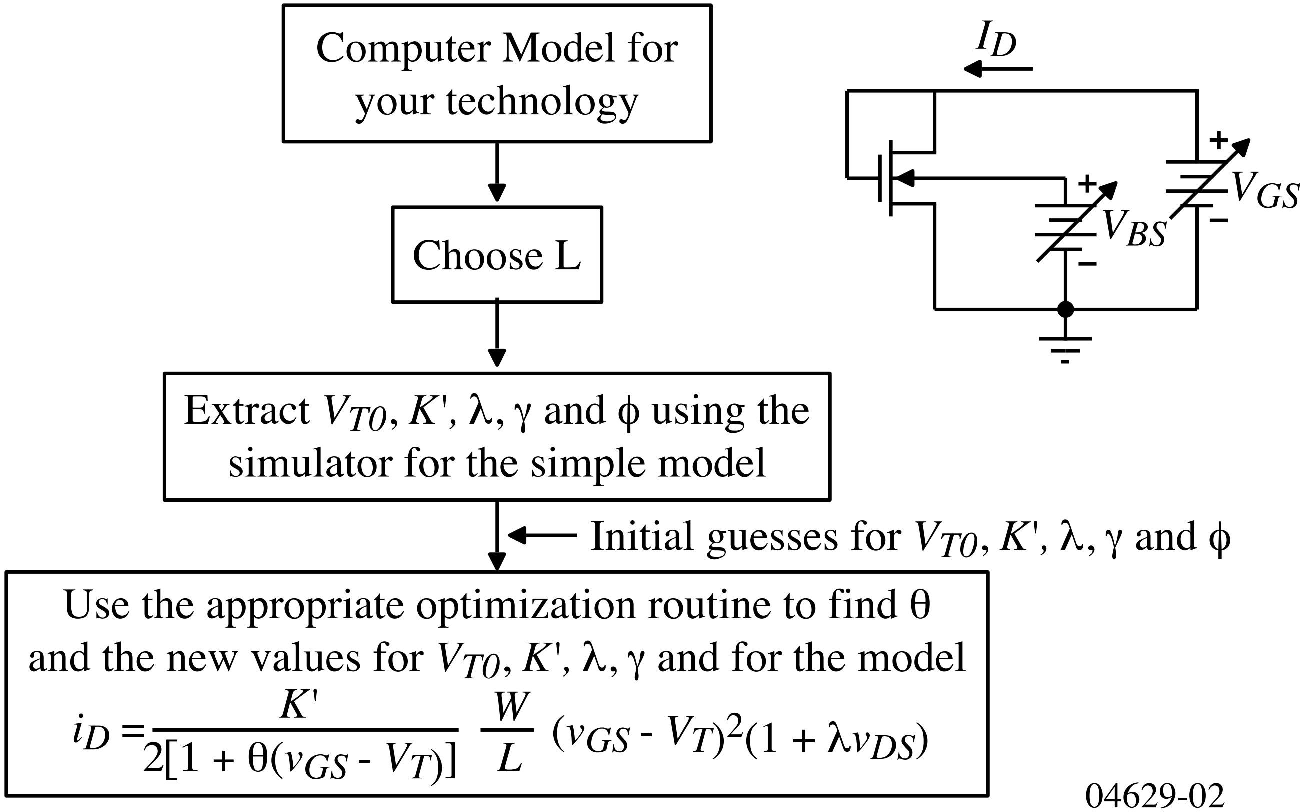
1.) Extract the square-law model parameters for a transistor with length at least 10 times L_{min}.

2.) Using the values of K', V_T, λ, and γ extract the model parameters for the following model:

$$i_D = \frac{K'}{2[1+\theta(v_{GS}-V_T)]}\frac{W}{L}[v_{GS}-V_T]^2(1+\lambda v_{DS})$$

Adjust the values of K', V_T, and λ as needed.

Illustration of the Extraction Procedure



Computer Model for your technology

Choose L

Extract V_{T0}, K', λ, γ and ϕ using the simulator for the simple model

Initial guesses for V_{T0}, K', λ, γ and ϕ

Use the appropriate optimization routine to find θ and the new values for V_{T0}, K', λ, γ and for the model

$$i_D = \frac{K'}{2[1 + \theta(v_{GS} - V_T)]}\,\frac{W}{L}\,(v_{GS} - V_T)^2(1 + \lambda v_{DS})$$

04629-02

EXTRACTION OF THE SIMPLE, SQUARE-LAW MODEL

Characterization of the Simple Square-Law Model

Equations for the MOSFET in strong inversion:

$$i_D = K'\left(\frac{W_{\text{eff}}}{2L_{\text{eff}}}\right)(v_{GS} - V_T)^2(1 + \lambda v_{DS}) \qquad (1)$$

$$i_D = K'\left(\frac{W_{\text{eff}}}{L_{\text{eff}}}\right)\left[(v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2}\right](1 + \lambda v_{DS}) \qquad (2)$$

where

$$V_T = V_{T0} + \gamma\left[\sqrt{2|\phi_{\text{F}}| + v_{SB}} - \sqrt{2|\phi_{\text{F}}|}\,\right] \qquad (3)$$

Extraction of Model Parameters:

First assume that v_{DS} is chosen such that the λv_{DS} term in Eq. (1) is much less than one and v_{SB} is zero, so that $V_T = V_{T0}$.

Therefore, Eq. (1) simplifies to

$$i_D = K'\left(\frac{W_{\text{eff}}}{2L_{\text{eff}}}\right)(v_{GS} - V_{T0})^2 \qquad (4)$$

This equation can be manipulated algebraically to obtain the following

$$i_D^{1/2} = \left(\frac{K'\,W_{\text{eff}}}{2L_{\text{eff}}}\right)^{1/2} v_{GS} - \left(\frac{K'\,W_{\text{eff}}}{2L_{\text{eff}}}\right)^{1/2} V_{T0} \qquad (5)$$

which has the form

$$y = mx + b \qquad (6)$$

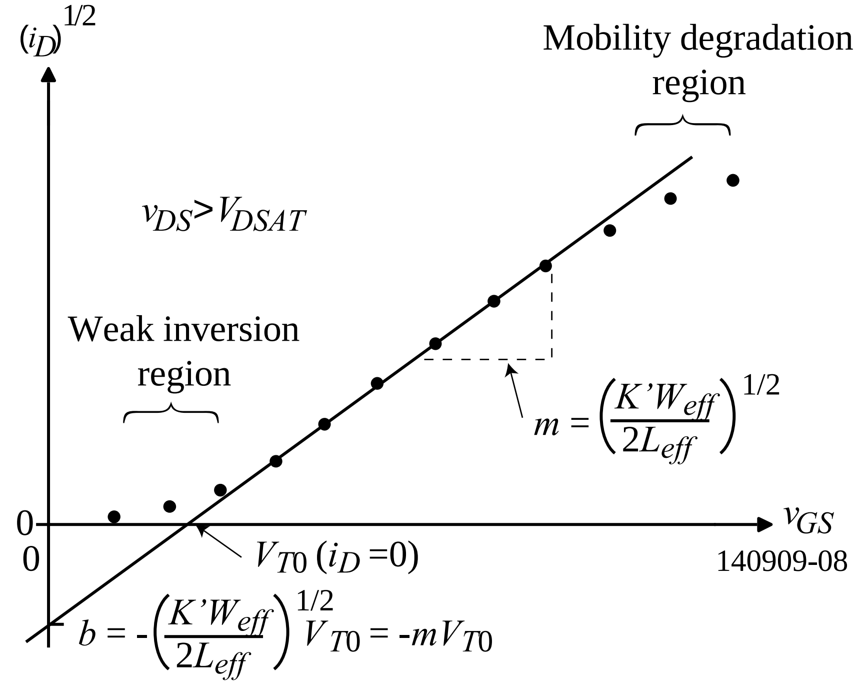
This equation is easily recognized as the equation for a straight line with m as the slope and b as the y-intercept. Comparing Eq. (5) to Eq. (6) gives

$$y = i_{\text{D}}^{1/2} \qquad (7)$$

$$x = v_{GS} \qquad (8)$$

$$m = \left(\frac{K'\,W_{\text{eff}}}{2L_{\text{eff}}}\right)^{1/2} \quad \text{and} \quad b = -\left(\frac{K'\,W_{\text{eff}}}{2L_{\text{eff}}}\right)^{1/2} V_{T0}$$

Illustration of *K'* and V_T Extraction



Comments:

- Stay away from the extreme regions of mobility degradation and weak inversion
- Use channel lengths greater than L_{min}

Example 13-1 – Extraction of *K’* and V_T Using Linear Regression

Given the following transistor data shown in Table 1 and linear regression formulas based on the form,

$$y = mx + b \tag{11}$$

and

$$m = \frac{\Re x_i\, y_i - (\Re\, x_i \Re\, y_i)/n}{\Re x_i^2 - (\Re x_i)^2/n} \tag{12}$$

determine V_{T0} and $K'W/2L$. The data in Table 1 also give $I_D^{1/2}$ as a function of V_{GS}.

Table 1 Data for Example 13-1

V_{GS} (V)	I_D (μA)	$\sqrt{I_D}$ (μA)$^{1/2}$	V_{SB} (V)
1.000	0.700	0.837	0.000
1.200	2.00	1.414	0.000
1.500	8.00	2.828	0.000
1.700	13.95	3.735	0.000
1.900	22.1	4.701	0.000

Example 13-1 – Continued

Solution

The data must be checked for linearity before linear regression is applied. Checking slopes between data points is a simple numerical technique for determining linearity. Using the formula that

$$\text{Slope} = m = \frac{\Delta y}{\Delta x} = \frac{\sqrt{I_{D2}} - \sqrt{I_{D1}}}{V_{GS2} - V_{GS1}}$$

Gives

$$m_1 = \frac{1.414 - 0.837}{0.2} = 2.885 \qquad m_2 = \frac{2.828 - 1.414}{0.3} = 4.713$$

$$m_3 = \frac{3.735 - 2.828}{0.2} = 4.535 \qquad m_4 = \frac{4.701 - 3.735}{0.2} = 4.830$$

These results indicate that the first (lowest value of V_{GS}) data point is either bad, or at a point where the transistor is in weak inversion. This data point will not be included in subsequent analysis. Performing the linear regression yields the following results.

$$V_{T0} = 0.898 \text{ V} \qquad \text{and} \qquad \frac{K'W_{\text{eff}}}{2L_{\text{eff}}} = 21.92\ \mu\text{A/V}^2$$

Extraction of the Bulk-Threshold Parameter γ

Using the same techniques as before, the following equation

$$V_T = V_{T0} + \gamma\left[\sqrt{2|\phi_F| + v_{SB}} - \sqrt{2|\phi_F|}\,\right]$$

is written in the linear form where

$$y = V_T$$

$$x = \sqrt{2|\phi_F| + v_{SB}} - \sqrt{2|\phi_F|} \tag{13}$$

$$m = \gamma$$

$$b = V_{T0}$$

The term $2|\phi_F|$ is unknown but is normally in the range of 0.6 to 0.7 volts.

Procedure:

1.) Pick a value for $2|\phi_F|$.

2.) Extract a value for γ.

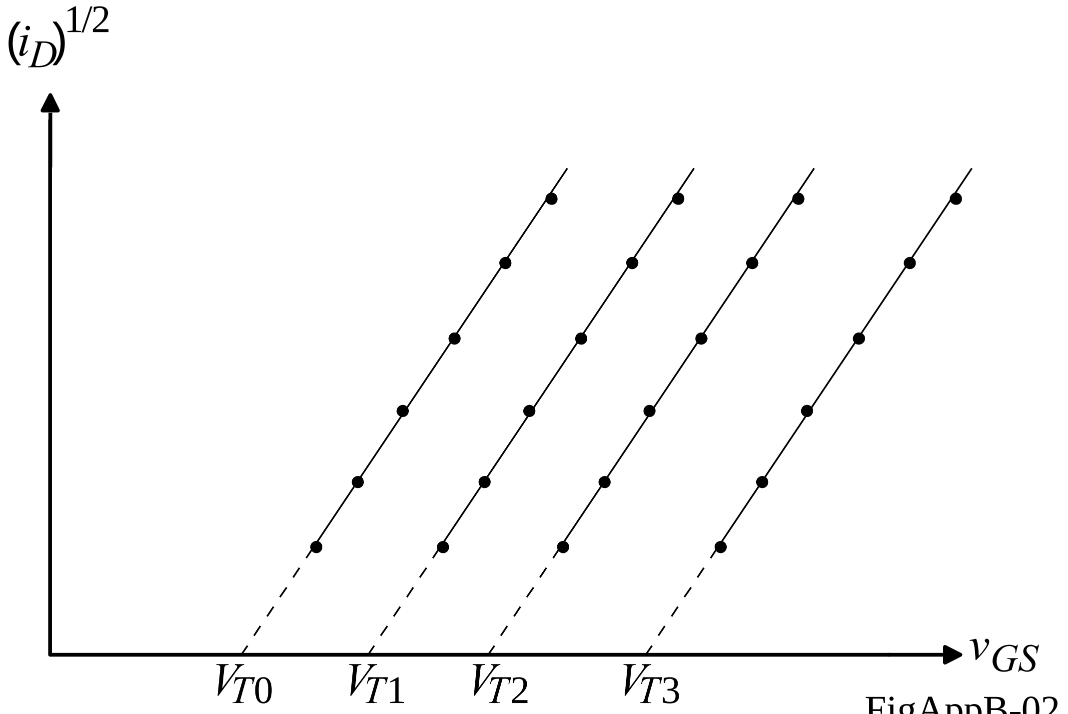
3.) Calculate N_{SUB} using the relationship, $\gamma = \dfrac{\sqrt{2\varepsilon_{si}\, q\, N_{SUB}}}{C_{ox}}$

4.) Calculate ϕ_F using the relationship, $\phi_F = -\dfrac{kT}{q}\ln\left(\dfrac{N_{SUB}}{n_i}\right)$

5.) Iterative procedures can be used to achieve the desired accuracy of γ and $2|\phi_F|$. Generally, an approximate value for $2|\phi_F|$ gives adequate results.

Illustration of the Procedure for Extracting γ

A plot of $\sqrt{i_D}$ versus v_{GS} for different values of v_{SB} used to determine γ is shown below.

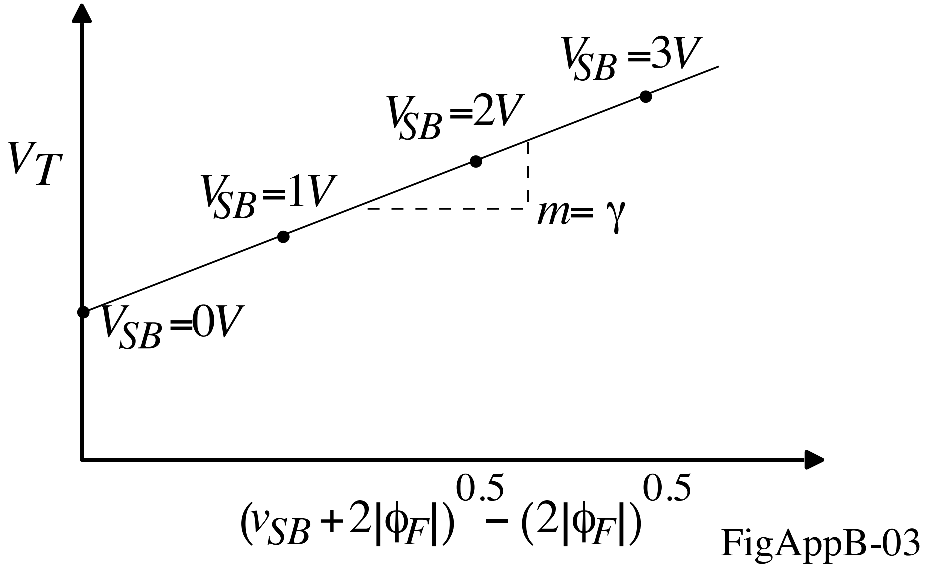


FigAppB-02

By plotting V_T versus x of Eq. (13) one can measure the slope of the best fit line from which the parameter γ can be extracted. In order to do this, V_T must be determined at various values of v_{SB} using the technique previously described.

Illustration of the Procedure for Extracting γ - Continued

Each V_T determined above must be plotted against the v_{SB} term. The result is shown below. The slope m, measured from the best fit line, is the parameter γ.



FigAppB-03

Example 13-2 – Extraction of the Bulk Threshold Parameter

Using the results from Ex. 13-1 and the following transistor data, determine the value of γ using linear regression techniques. Assume that $2|\phi_F|$ is 0.6 volts.

Table 2 Data for Example 13-2.

V_{SB} (V)	V_{GS} (V)	I_D (μA)
1.000	1.400	1.431
1.000	1.600	4.55
1.000	1.800	9.44
1.000	2.000	15.95
2.000	1.700	3.15
2.000	1.900	7.43
2.000	2.10	13.41
2.000	2.30	21.2

Solution

Table 2 shows data for V_{SB} = 1 volt and V_{SB} = 2 volts. A quick check of the data in this table reveals that $\sqrt{I_D}$ versus V_{GS} is linear and thus may be used in the linear regression analysis. Using the same procedure as in Ex. 1, the following thresholds are determined: V_{T0} = 0.898 volts (from Ex. 1), V_T = 1.143 volts (@V_{SB} = 1 V), and V_T = 1.322 V (@V_{SB} = 2V). Table 3 gives the value of V_T as a function of $\left[\sqrt{2|\phi_F| + V_{SB}} - \sqrt{2|\phi_F|}\right]$ for the three values of V_{SB}.

Example 13-2 - Continued

Table 3 Data for Example 13-2.

V_{SB} (V)	V_T (V)	$[\sqrt{2\|\phi_F\| + V_{SB}} - \sqrt{2\|\phi_F\|}]$ ($V^{1/2}$)
0.000	0.898	0.000
1.000	1.143	0.490
2.000	1.322	0.838

With these data, linear regression must be performed on the data of V_T versus $[(2|\phi_F| + V_{SB})^{0.5} - (2|\phi_F|)^{0.5}]$. The regression parameters of Eq. (12) are

$\Sigma x_i y_i = 1.668$

$\Sigma x_i \Sigma y_i = 4.466$

$\Sigma x_i^2 = 0.9423$

$(\Sigma x_i)^2 = 1.764$

These values give $m = 0.506 = \gamma$.

Extraction of the Channel Length Modulation Parameter, λ

The channel length modulation parameter λ should be determined for all device lengths that might be used. For the sake of simplicity, Eq. (1) is rewritten as

$$i_D = i'_D = \lambda' v_{DS} + i'_D$$

which is in the familiar linear form where

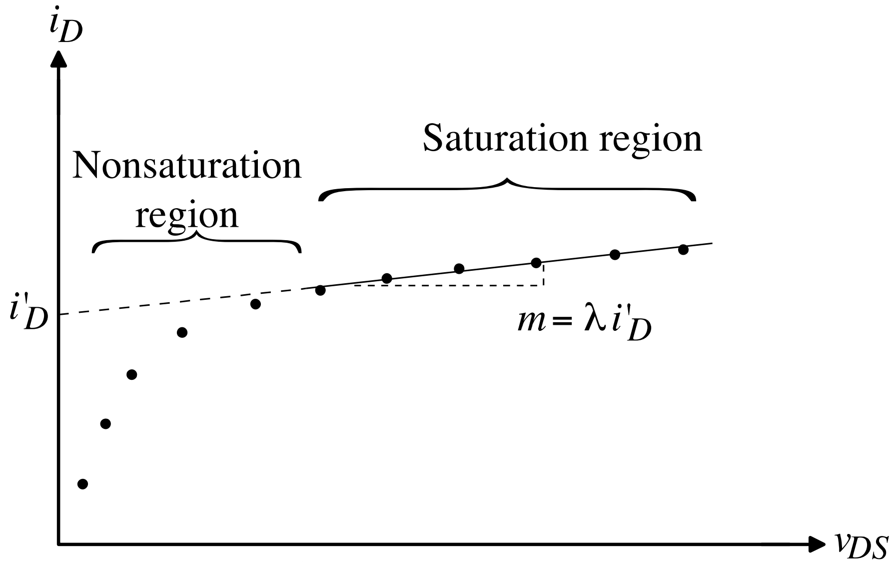
$y = \mathrm{i}_D$ (Eq. (1))

$x = v_{DS}$

$m = \lambda i'_D$

$b = i'_D$ (Eq. (1) with $\lambda = 0$)

By plotting i_D versus v_{DS}, measuring the slope of the data in the saturation region, and dividing that value by the y-intercept, λ can be determined. The procedure is illustrated in the figure shown.



AppB-03

EXTRACTION OF THE SIMPLE MODEL FOR SHORT CHANNEL MOSFETS

Extraction for Short Channel MOSFETS

The model proposed is the following one which is the square-law model modified by the velocity saturation influence.

$$i_D = \frac{K'}{2[1 + \theta(v_{GS}-V_T)]}\frac{W}{L}[\, v_{GS} - V_T]^2(1+\lambda v_{DS})$$

Using the values of K', V_T, λ, and γ extracted previously, use an appropriate extraction procedure to find the value of θ adjusting the values of K', V_T, and λ as needed.

Comments:

- We will assume that the bulk will be connected to the source or the standard relationship between V_T and V_{BS} can be used.
- The saturation voltage is still given by

$$V_{DS}(\text{ sat}) = V_{GS} - V_T$$

Example of a Genetic Algorithm[†]

1.) To use this algorithm or any other, use the simulator and an appropriate short-channel model (BSIM3) to generate a set of data for the transconductance (i_D vs. v_{GS}) and output characteristics (i_D vs. v_{DS}) of the transistor with the desired W and L values.

2.) The best fit to the data is found using a genetic algorithm. The constraints on the parameters are obtained from experience with prior transistor parameters and are:

$10E\text{-}6 < \beta < 610E\text{-}6$, $1 < \theta < 5$, $0 < V_T < 1$, and $0 < \lambda < 0.5$

3,) The details of the genetic algorithm are:

Gene structure is $A = [\beta, \theta, V_T,$ fitness]. A mutation was done by varying all four parameters. A weighted sum of the least square errors of the data curves was used as the error function. The fitness of a gene was chosen as 1/error.

4.) The results for an extraction run of 8000 iterations for an NMOS transistor is shown below.

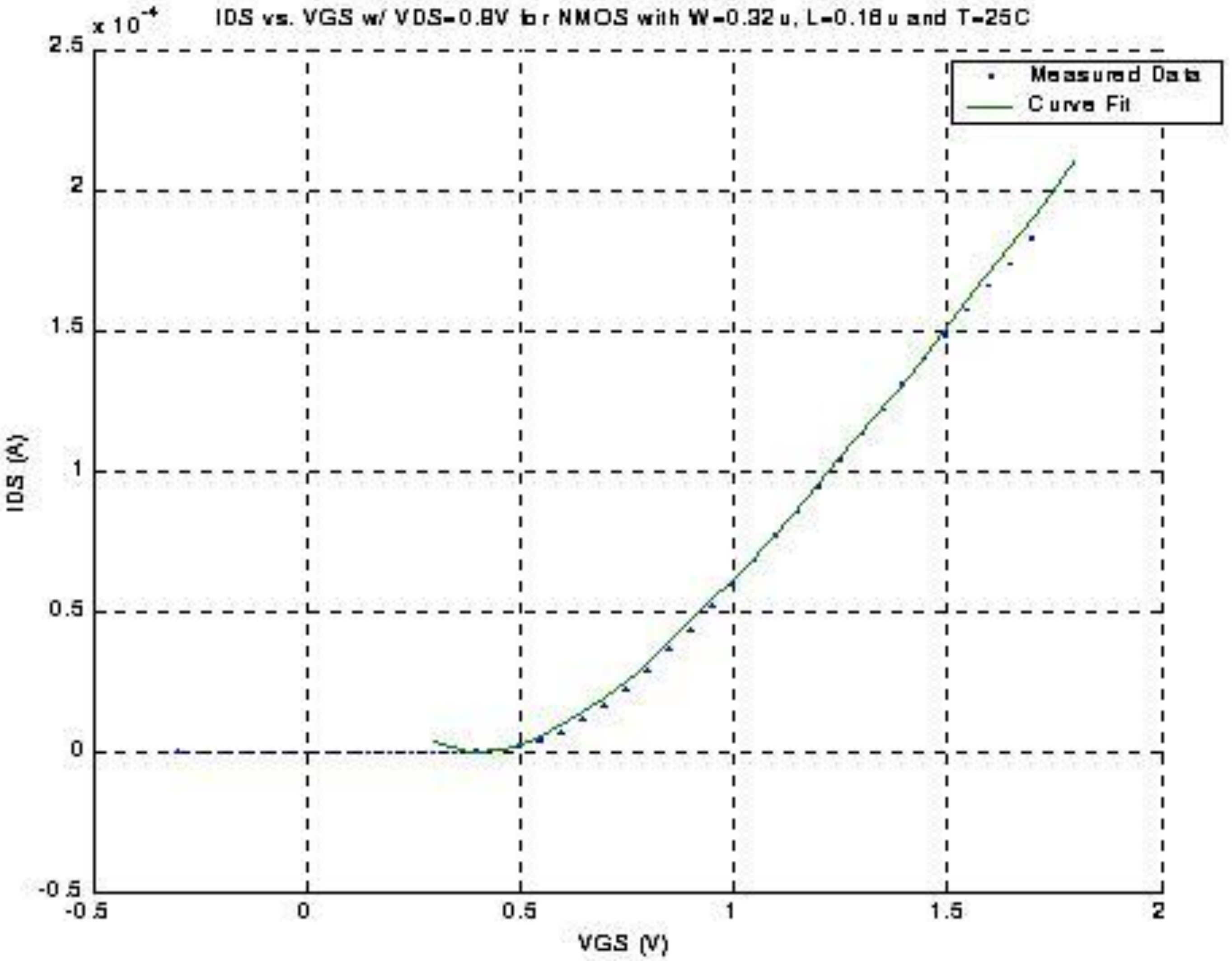
β(A/V^2)	θ	V_T(V)	λ(V^{-1})
$294.1\text{x}10^{-6}$	1.4564	0.4190	0.1437

5.) The results for a NMOS and PMOS transistor are shown on the following pages.

[†] Anurag Kaplish, "Parameter Optimization of Deep Submicron MOSFETS Using a Genetic Algorithm," May 4, 2000, Special Project Report, School of ECE, Georgia Tech.

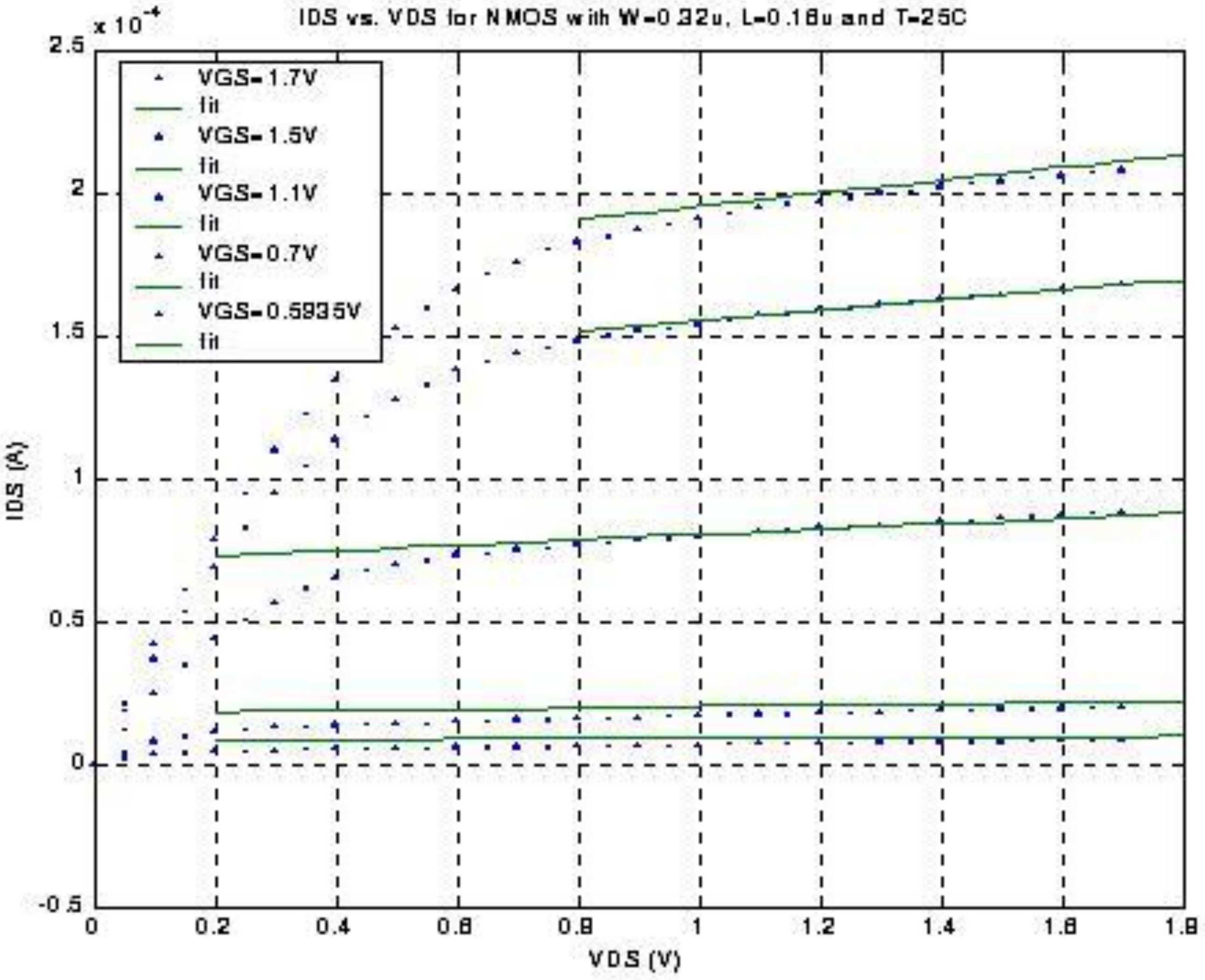
Extraction Results for an NMOS Transistor with *W* = 0.32µm and *L* = 0.18µm

Transconductance:



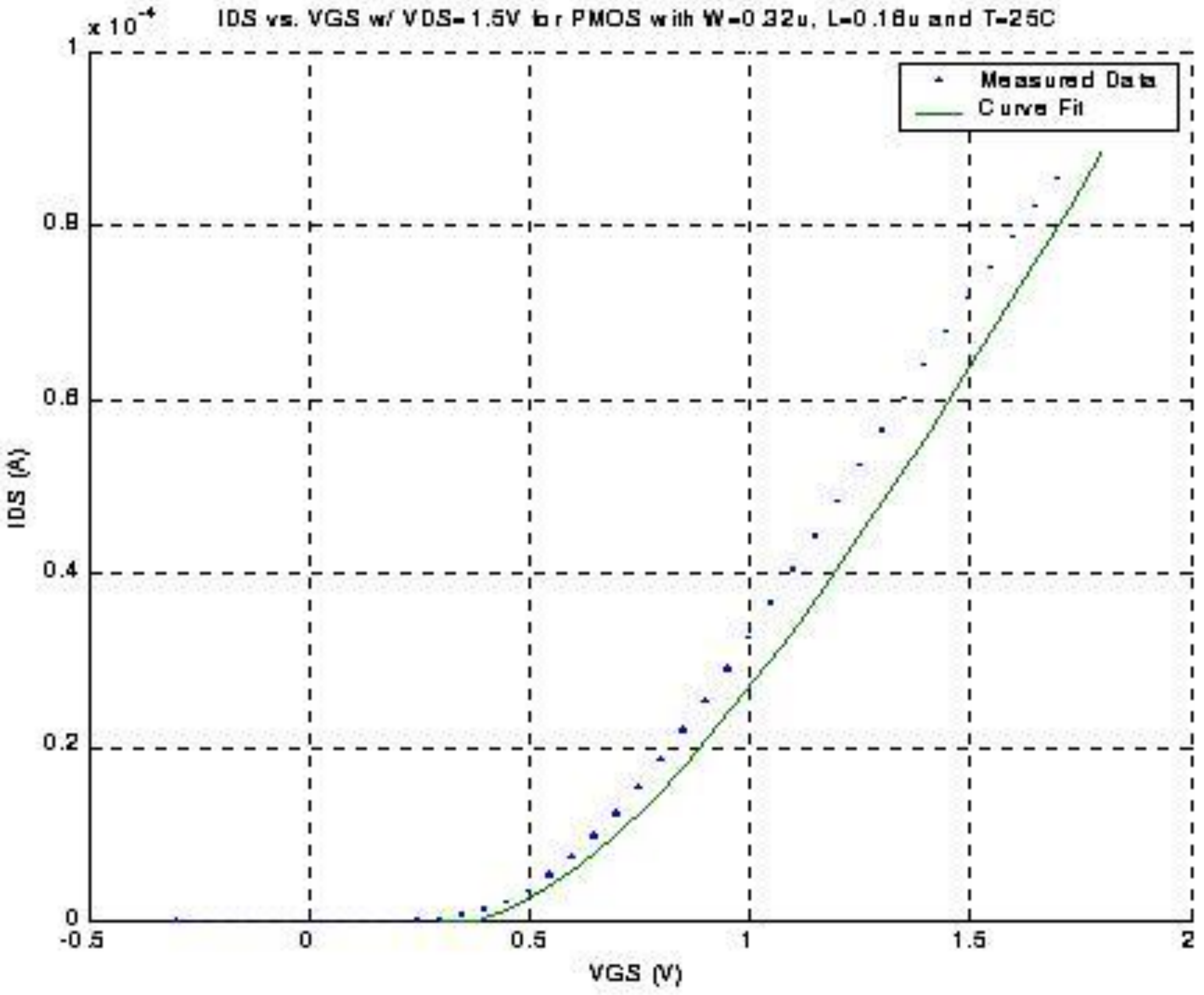
Extraction Results for an NMOS Transistor with W = 0.32µm and L = 0.18µm

Output:



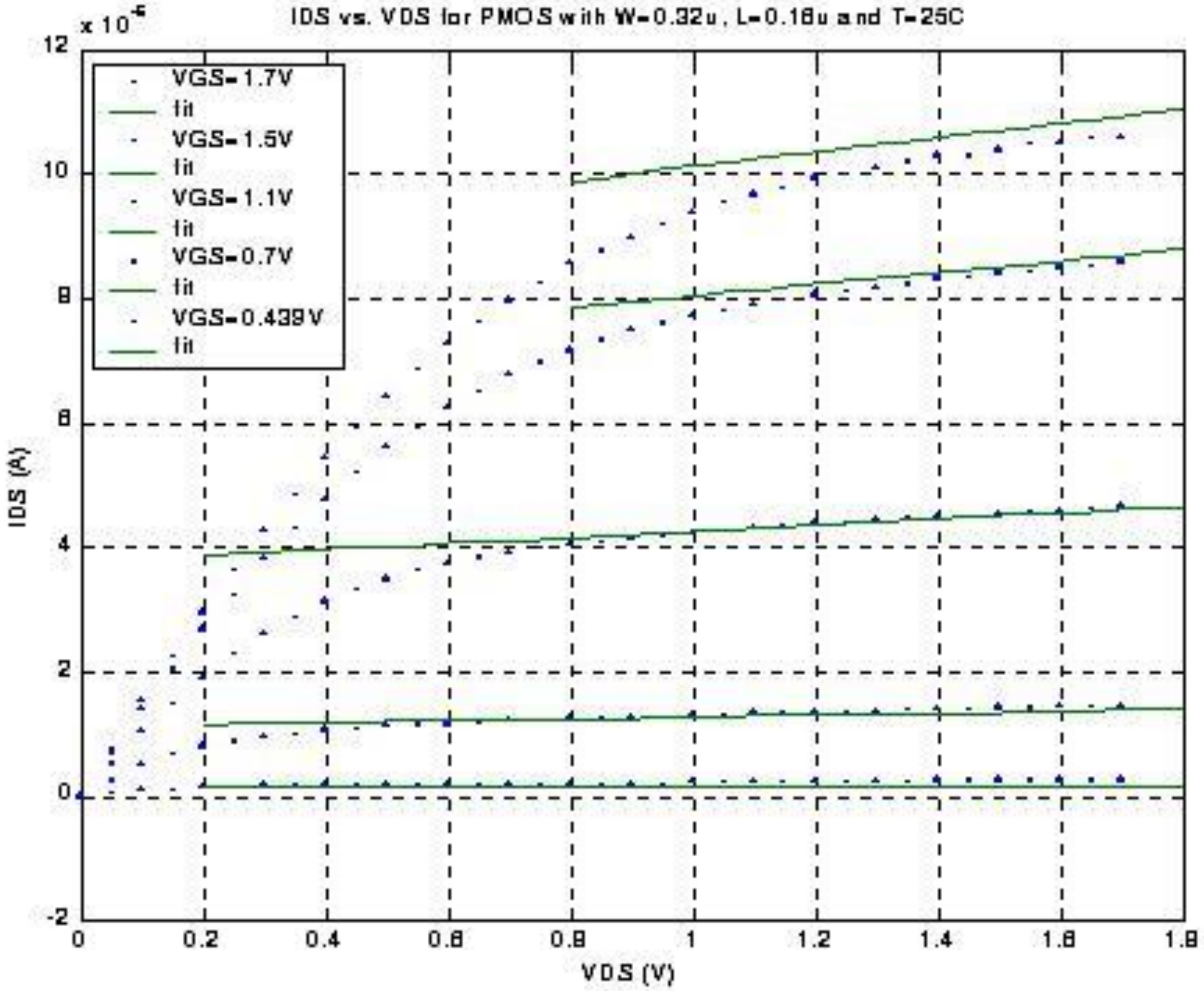
Extraction Results for an PMOS Transistor with *W* = 0.32µm and *L* = 0.18µm

Transconductance:



Extraction Results for an PMOS Transistor with *W* = 0.32μm and *L* = 0.18μm

Output:



SUMMARY

- Models have greatly improved over time resulting in efficient computer simulation
- Output conductance model is greatly improved
- Narrow channel transistors have difficulty with modeling
- Can have discontinuities at bin boundaries
- The BSIM model is a complex model, widely used and difficult to understand in detail
- The simple large signal model can be extracted from any computer model
- Extract the model at the desired channel length for the design
- Short channel technology can be modeled by finding the θ by any optimization routine