LECTURE 12 – COMPONENT MATCHING

LECTURE ORGANIZATION

Outline

- Introduction
- Electrical matching
- Physical matching
- Summary

***CMOS Analog Circuit Design*, 3rd Edition Reference**

Pages 640-652 and new material

INTRODUCTION

What is Accuracy and Matching?

The *accuracy* of a quantity specifies the difference between the actual value of the quantity and the ideal or true value of the quantity.

The *mismatch* between two quantities is the difference between the actual ratio of the quantities and the desired ratio of the two quantities.

Example:

x_1 = actual value of one quantity

x_2 = actual value of a second quantity

X_1 = desired value of the first quantity

X_2 = desired value of the second quantity

The accuracy of a quantity can be expressed as,

$$\text{Accuracy} = \frac{x - X}{X} = \frac{\Delta X}{X}$$

The mismatch, δ, can be expressed as,

$$\delta = \frac{\frac{x_2}{x_1} - \frac{X_2}{X_1}}{\frac{X_2}{X_1}} = \frac{X_1 x_2}{X_2 x_1} - 1$$

Relationship between Accuracy and Matching

Let:

$$\Delta X_1 = |x_1 - X_1| \quad \rightarrow \quad x_1 = X_1 \pm \Delta X_1$$

and

$$\Delta X_2 = |x_2 - X_2| \quad \rightarrow \quad x_2 = X_2 \pm \Delta X_2$$

Therefore, the mismatch can be expressed as,

$$\delta = \frac{X_1(X_2 \pm \Delta X_2)}{X_2(X_1 \pm \Delta X_1)} - 1 = \frac{1 \pm \dfrac{\Delta X_2}{X_2}}{1 \pm \dfrac{\Delta X_1}{X_1}} - 1 \approx \left(1 \pm \frac{\Delta X_2}{X_2}\right)\left(1 \mp \frac{\Delta X_1}{X_1}\right) - 1$$

$$\delta \approx 1 \pm \frac{\Delta X_2}{X_2} \mp \frac{\Delta X_1}{X_1} - 1 = \pm \frac{\Delta X_2}{X_2} \mp \frac{\Delta X_1}{X_1}$$

Thus, the mismatch is approximately equal to the difference in the accuracies of x_1 and x_2 assuming the deviations (ΔX) are small with respect to X.

Characterization of the Mismatch

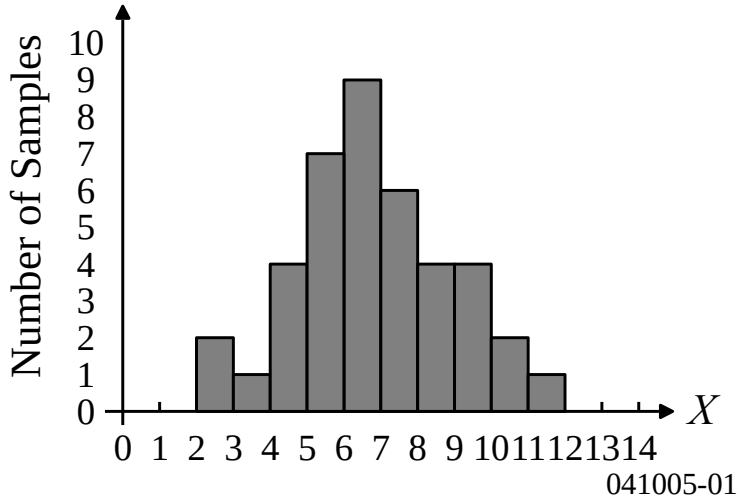
Mean of the mismatch for N samples-

$$m_\delta = \frac{1}{N}\sum_{i=1}^{N}\delta_i$$

Standard deviation of the mismatch for N samples-

$$s_\delta = \sigma = \sqrt{\frac{1}{N\text{-}1}\sum_{i=1}^{N}(\delta_i - m_\delta)^2}$$

Example:



$$m_\delta = \frac{253}{40} = 6.325 \qquad s_\delta = 2.115$$

Motivation for Matching of Components

The accuracy of analog signal processing is determined by the accuracy of gains and time constants. These accuracies are dependent upon:

Gain $\propto$ Ratios of components or areas

Time constants $\propto$ Products of components or areas

Ratio Accuracy?

$$\text{Actual Ratio} = \frac{X_1 \pm \Delta X_1}{X_2 \pm \Delta X_2} = \frac{X_1}{X_2}\left(\frac{1 \pm \dfrac{\Delta X_1}{X_1}}{1 \pm \dfrac{\Delta X_2}{X_2}}\right) \approx \frac{X_1}{X_2}\left(1 \pm \frac{\Delta X_1}{X_1}\right)\left(1 \mp \frac{\Delta X_2}{X_2}\right) \approx \frac{X_1}{X_2}\left(1 \pm \frac{\Delta X_1}{X_1} \mp \frac{\Delta X_2}{X_2}\right)$$

If X_1 and X_2 match ($\Delta X_1/X_1 \approx \Delta X_2/X_2$), then the actual ratio becomes the ideal ratio.

Product Accuracy?

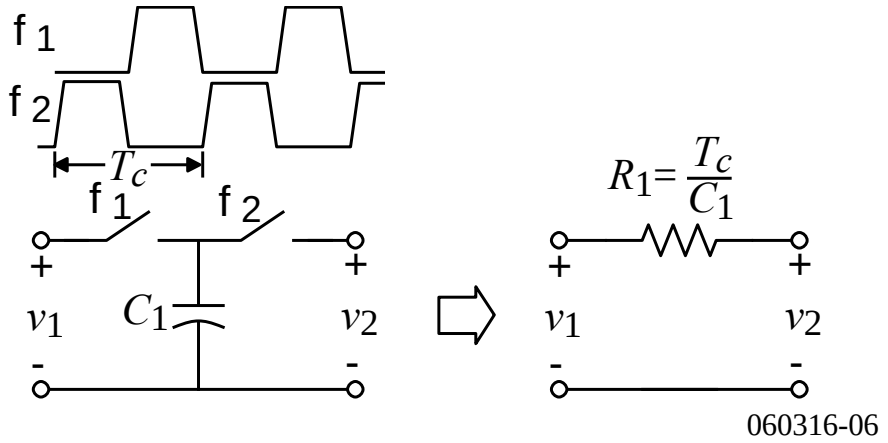
$$\text{Product accuracy} = (X_1 \pm \Delta X_1)(X_2 \pm \Delta X_2) = X_1 X_2\left(1 \pm \frac{\Delta X_1}{X_1}\right)\left(1 \pm \frac{\Delta X_2}{X_2}\right) \approx X_1 X_2\left(1 \pm \frac{\Delta X_1}{X_1} \pm \frac{\Delta X_2}{X_2}\right)$$

Unfortunately, the product cannot be accurately maintained in integrated circuits.

Switched Capacitor Circuits

Switched capacitor circuits offer a solution to the product accuracy problem.

A switched capacitor replacement of a resistor:



The product of a resistor, R_1, and a capacitor, C_2, now become,

$$R_1C_2 = \left(\frac{T_c}{C_1}\right)C_2 = \left(\frac{1}{f_cC_1}\right)C_2 = \frac{C_2}{f_cC_1}$$

The accuracy of the time constant (product) now becomes,

$$\frac{C_2}{f_cC_1}\left(1 \pm \frac{\Delta C_2}{C_2} \mp \frac{\Delta C_1}{C_1} \mp \frac{\Delta f_c}{f_c}\right)$$

Assuming the clock frequency is accurate and larger than the signal bandwidth, then time constants in analog signal processing can be accurately matched by ratios of elements.

Types of Mismatches

1.) Those controlled or influenced by electrical design

- Transistor operation
- Circuit techniques
- Correction/calibration techniques

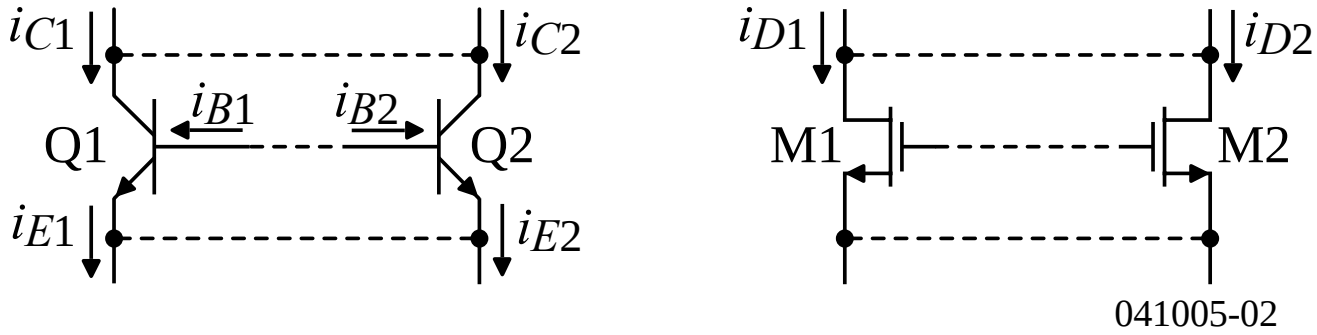
2.) Those controlled or influenced by physical design

- Random statistical fluctuations (microscopic fluctuations and irregularities)
- Process bias (geometric variations)
- Pattern shift (misalignment)
- Diffusion interactions
- Stress gradients and package shifts
- Temperature gradients and thermoelectrics
- Electrostatic interactions

ELECTRICAL MATCHING

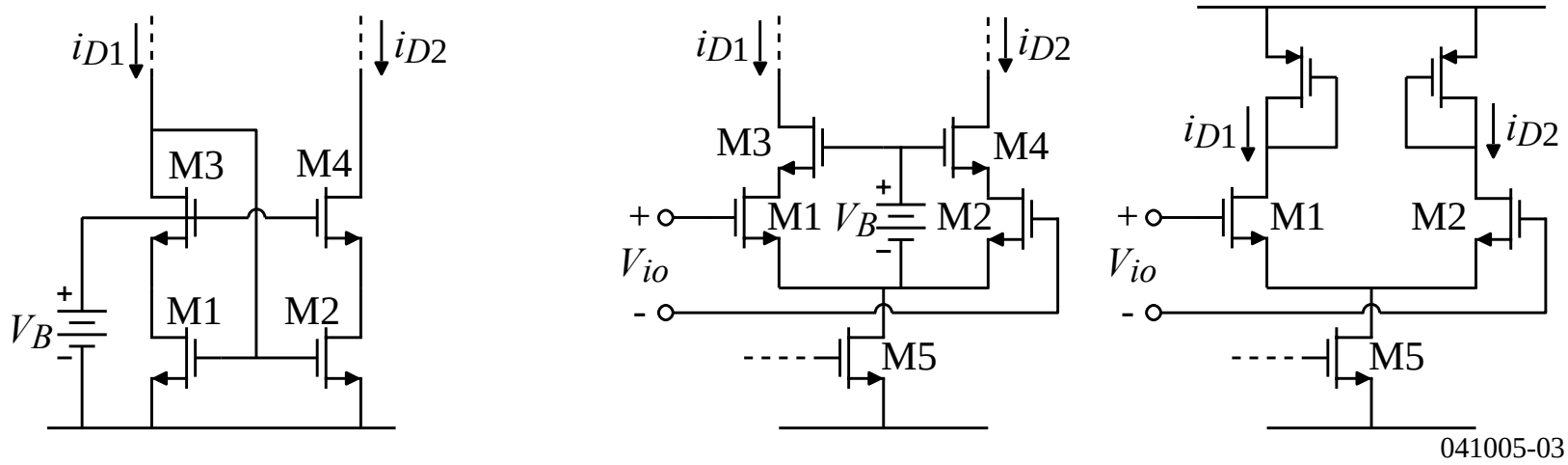
Matching Principle

Assume that two transistors are matched (large signal model parameters are equal). Then if all terminal voltages of one transistor are equal to the terminal voltages of the other transistor, then the terminal currents will be matched.



Note that the terminals may be physically connected together or at the same potential but not physically connected together.

Examples of the Matching Principle



Cascode current mirror:

The key transistors are M1 and M2. The gates and sources are physically connected and the drains are equal due to M3 and M4 gate-source drops. As a result, i_{D1} will be very close to i_{D2}.

Differential amplifier:

When i_{D1} and i_{D2} are equal, the fact that the drains of M1 and M2 are equal should give the smallest value of the input offset voltage, V_{io}.

Note: Since the drain voltages of M3 and M4 in both circuits are not necessarily equal, the gate-source voltages of M3 and M4 are not exactly equal which cause the drain voltages of M1 and M2 to not be exactly equal.

Gate-Source Matching

Not as precise as the previous principle but useful for biasing applications.

A. If the gate-source voltages of two or more FETs are equal and the FETs are matched and operating in the saturation region, then the currents are related by the W/L ratios of the individual FETs. The gate-source voltages may be directly or indirectly connected.

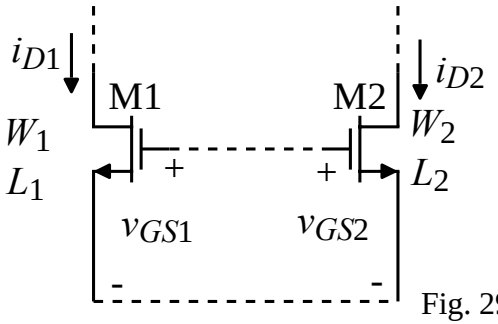


Fig. 290-02

$$i_{D1} = \frac{K'W_1}{2L_1}(v_{GS1}-V_{T1})^2 \rightarrow (v_{GS1}-V_{T1})^2 = \frac{2K'i_{D1}}{(W_1/L_1)}$$

$$i_{D2} = \frac{K'W_2}{2L_2}(v_{GS2}-V_{T2})^2 \rightarrow (v_{GS2}-V_{T2})^2 = \frac{2K'i_{D2}}{(W_2/L_2)}$$

If $v_{GS1} = v_{GS2}$, then $\boxed{\left(\frac{W_2}{L_2}\right) i_{D1} = \left(\frac{W_1}{L_1}\right) i_{D2}}$ or $\boxed{i_{D1} = \left(\frac{W_1/L_1}{W_2/L_2}\right) i_{D2}}$

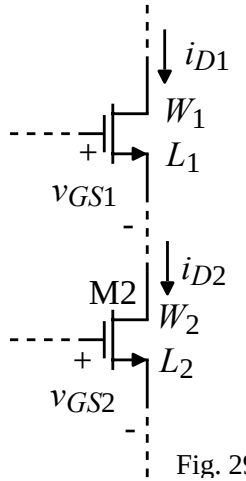


Fig. 290-03

B. If the drain currents of two or more transistors are equal and the transistors are matched and operating in the saturation region, then the gate-source voltages are related by the W/L ratios (ignoring bulk effects).

If $i_{D1}=i_{D2}$, then

$$\boxed{v_{GS1} = V_{T1} + \sqrt{\frac{W_2/L_2}{W_1/L_1}}(v_{GS2}-V_{T2}) \text{ or } v_{GS1} = v_{GS2} \text{ if } \frac{W_2}{L_2} = \frac{W_1}{L_1}}$$

Process Independent Biasing - MOSFET

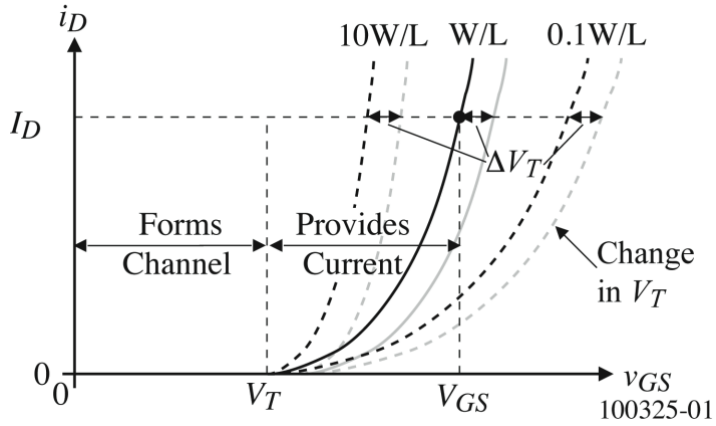
The sensitivity of the bias points of all transistors depend on both the variation of the technological parameters and the accuracy of the biasing circuits.

Gate-source voltage decomposition:

The gate-source voltage of the MOSFET can be divided into two parts:

1.) The part necessary to form or enhance the channel, V_T

2.) The part necessary to cause current to flow, $V_{GS} - V_T = V_{ON}$, called the overdrive.



This overdrive can be expressed,

$$V_{ON} = V_{DS}(\text{sat}) = \sqrt{\frac{2I_D}{K'(W/L)}}$$

The dependence of the bias point on the technology, V_T, can be reduced by making $V_{ON} = V_{DS}(\text{sat}) >> V_T$.

This implies that small values of W/L are preferable. Unfortunately, this causes the transconductance to become small if the current remains the same.

Doubly Correlated Sampling

Illustration of the use of chopper stabilization to remove the undesired signal, v_u, from the desired signal, v_{in}. In this case, the undesired signal is the gate leakage current.

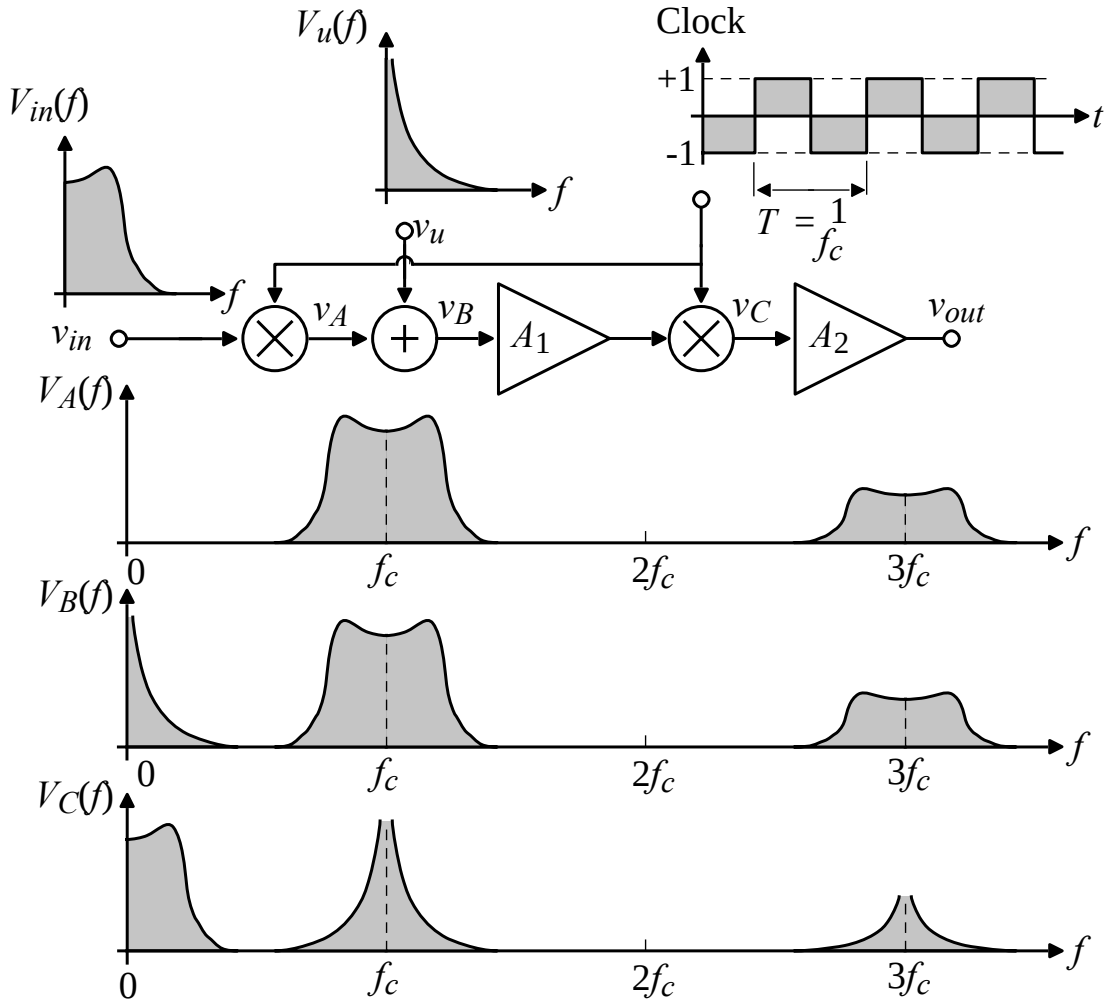
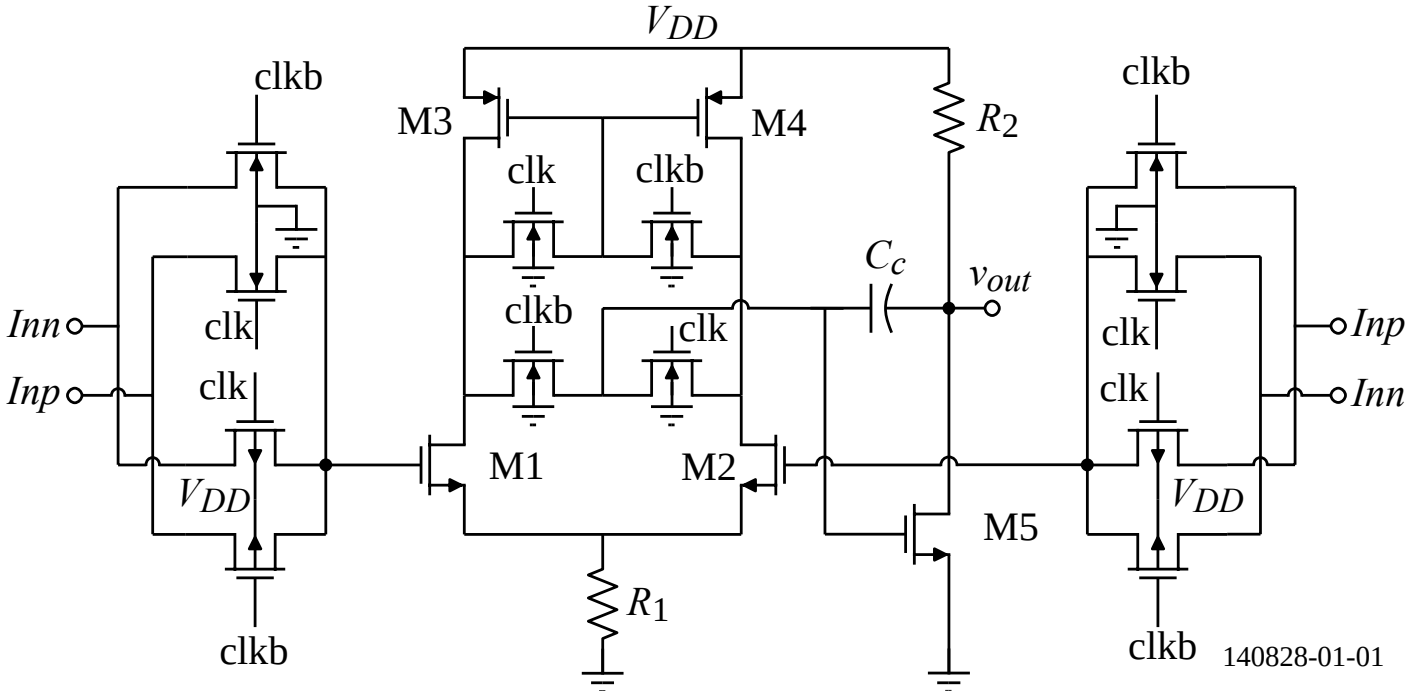


Fig. 7.5-8

An Op Amp Using Doubly Correlated Sampling to Remove DC Offsets

Problem: M1 and M2 are thin gate oxide which have dc current at gate.



- Chopping with 50% duty cycle
- All switches use thick oxide devices to reduce gate leakage
- Gain $\approx g_{m1}(r_{ds2}\|r_{ds4})g_{m5}R_2$

Will examine further in low noise op amps.

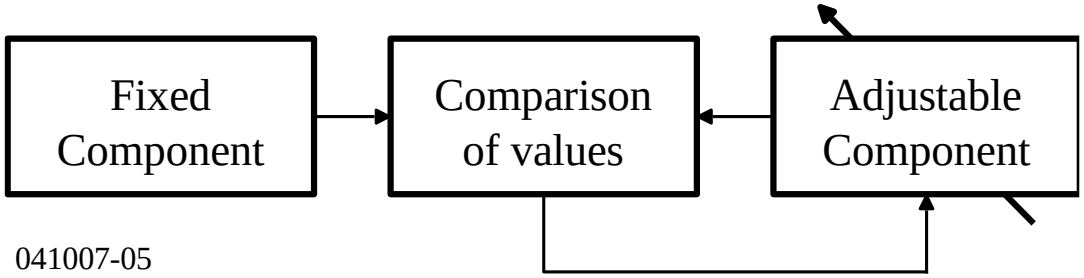
Self-Calibration Techniques

The objective of self-calibration is to increase the matching between two or more components (generally passive).

The requirements for self-calibration:

1.) A time interval in which to perform the calibration

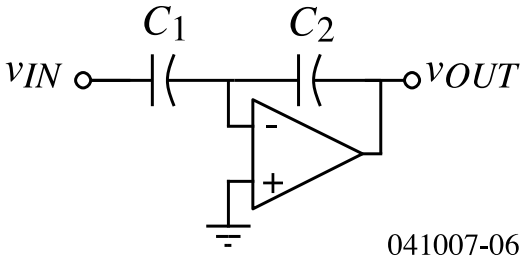
2.) A means of adjusting the value of one or more of the components.



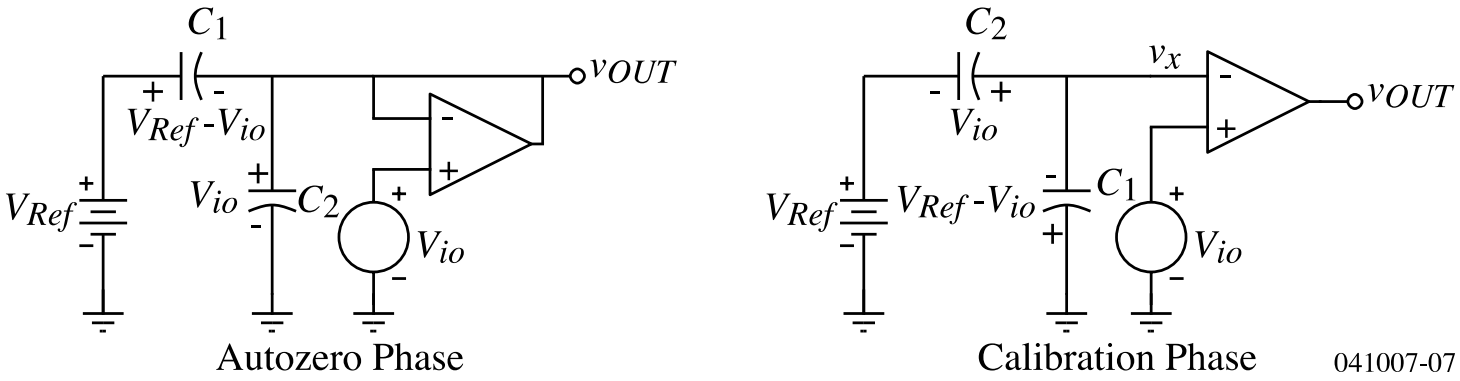
Self-calibration can typically improve the matching by a factor of 2-3 bits (4-8).

Example of Capacitor Self-Calibration

Consider the charge amplifier below that should have a gain of unity.



Assume the amplifier has a DC input offset voltage of V_{io}. The following shows how to calibrate one (or both) of the capacitors.



In the calibration phase, v_x, is:

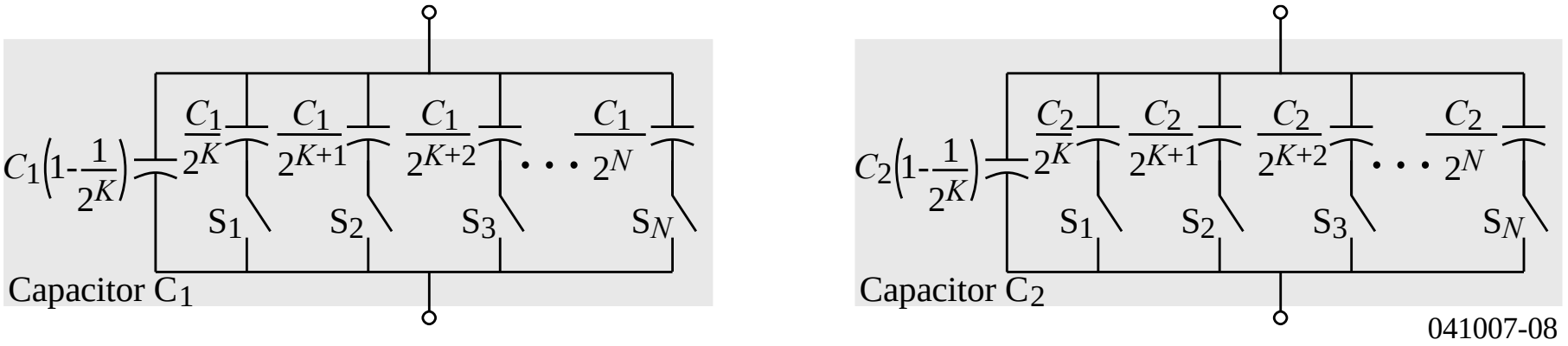
$$v_x = (V_{REF}\text{-}V_{io})\left(\frac{C_2}{C_1+C_2}\right) - (V_{REF}\text{-}V_{io})\left(\frac{C_1}{C_1+C_2}\right) = (V_{REF}\text{-}V_{io})\left(\frac{C_2\text{-}C_1}{C_1+C_2}\right)$$

The correction circuitry varies C_1 or C_2 until $v_x = 0$ as observed by v_{OUT}.

Variable Components

The correction circuitry should be controlled by logic circuits so that the correction can be placed into memory to maintain the calibration of the circuit during application.

Implementation for C_1 and C_2 of the previous example:



K is selected to achieve the desired tolerance or variation

N is selected to achieve the desired resolution ($N > K$)

Additional circuitry:

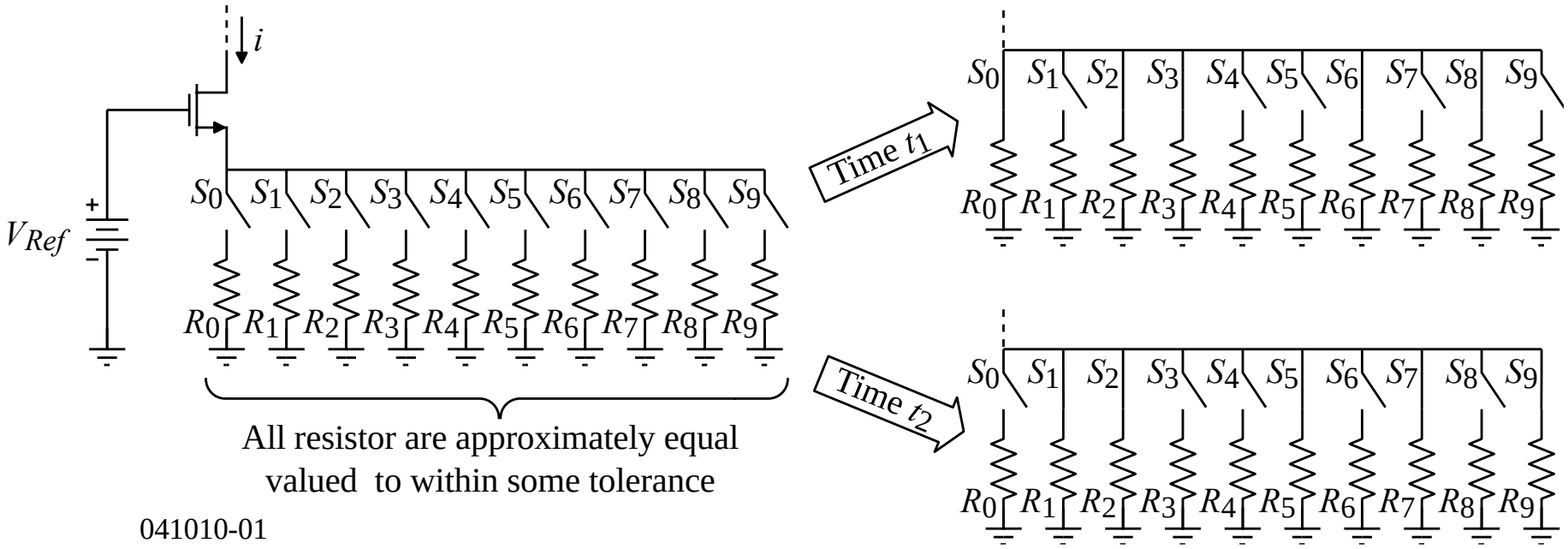
Every self-calibration system will need additional logic circuits to sense when the value of v_x changes from positive to negative (or vice versa) and to store the switch settings in memory to maintain the calibration.

Basics of Dynamic Element Matching†

Dynamic element matching chooses different, approximately equal-valued elements to represent a more precise value of a component as a function of time.

Goal of dynamic element matching:

Convert the error due to element mismatch from a dc offset into an ac signal of equivalent power which can be removed by the appropriate means (doubly-correlated sampling, highpass filtering of a sigma-delta modulator, etc.)



† L. R. Carley, "A Noise-Shaping Coder Topology for 15+ Bit Converters, *IEEE J. of Solid-State Circuits*, vol. 24, no. 2, April 1989, pp. 267-273.

How Dynamic Element Matching Works

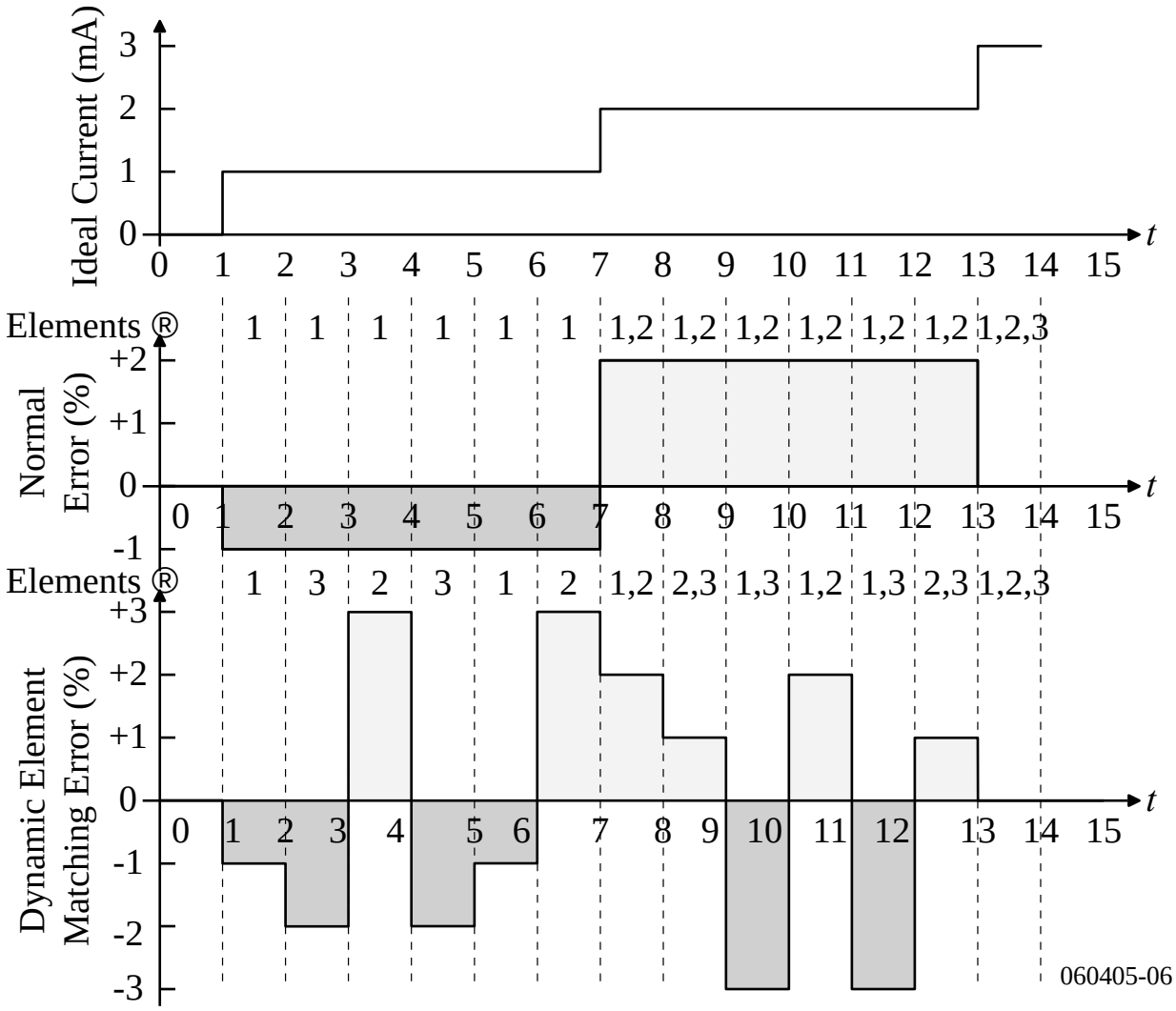
Assume that we have three approximately equal elements with the following currents:

Element 1 = 0.99mA Element 2 = 1.03mA Element 3 = 0.98mA

Ideal current output level →

Error when dynamic element matching is not → used

Error when dynamic element matching is used →

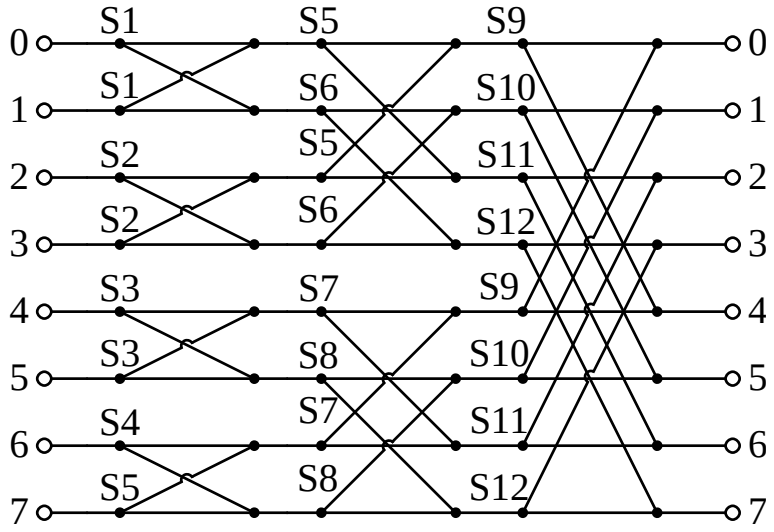


Issues of Dynamic Element Matching

- The selection of the elements must be truly random for the maximum benefit to occur.
- If the number of elements is large this can be an overwhelming task to implement. An approximation to random selection is the butterfly-type randomizer below:

Three-stage, eight-line butterfly randomizer. Each pair of switches marked with the same label is controlled to either exchange the two signal lines or pass them directly to the next stage.

041010-03



- When using the dynamic element technique, one needs to be careful that the averaging activity of the dynamic element matching process does not interfere with other averaging processes that might be occurring simultaneously (i.e. ΣΔ modulators).
- Other references:

1.) B.H. Leung and s. Sutarja, "Multibit Σ-Δ A/D Converter Incorporating A Novel Class of Dynamic Element Matching Techniques," *IEEE Trans. on Circuits and Systems*-II, vol. 39, no. 1, Jan. 1992, pp. 35-51.

2.) R. Baird and T. Fiez, "Linearity Enhancement of Multibit Δ-Σ A/D and D/A Converters Using Data Weighted Averaging," *IEEE Trans. on Circuits and Systems*-II, vol. 42, no. 12, Dec. 1995, pp. 753-762.

PHYSICAL MATCHING

Review of Physical Matching

We have examined these topics in previous lectures. To summarize, the sources of physical mismatch are:

- Random statistical fluctuations (microscopic fluctuations and irregularities)
- Process bias (geometric variations)
- Pattern shift (misalignment)
- Diffusion interactions
- Stress gradients and package shifts
- Temperature gradients and thermoelectrics
- Electrostatic interactions

Rules for Resistor Matching†

1.) Construct matched resistors from the same material.
2.) Make matched resistors the same width.
3.) Make matched resistors sufficiently wide.
4.) Where practical, use identical geometries for resistors (replication principle)
5.) Orient resistors in the same direction.
6.) Place matched resistors in close physical proximity.
7.) Interdigitate arrayed resistors.
8.) Place dummy resistors on either end of a resistor array.
9.) Avoid short resistor segments.
10.) Connect matched resistors in order to cancel thermoelectrics.
11.) If possible place matched resistors in a low stress area (minimize pieozoresistance).
12.) Place matched resistors well away from power devices.
13.) Place precisely matched resistors on the axes of symmetry of the die.

† Alan Hastings, *Art of Analog Layout*, 2nd ed, 2006, Pearson Prentice Hall, New Jersey

Rules for Resistor Matching – Continued

14.) Consider the influence of tank modulation for HSR resistors (the voltage modulation of the reverse-biased depletion region changes the sheet resistivity).

15.) Sectioned resistors are superior to serpentine resistors.

16.) Use poly resistors in preference to diffused resistors.

17.) Do not allow the buried layer shadow to intersect matched diffused resistors.

18.) Use electrostatic shielding where necessary.

19.) Do not route unconnected metal over matched resistors.

20.) Avoid excessive power dissipation in matched resistors.

Rules for Capacitor Matching†

1.) Use identical geometries for matched capacitors (replication principle).
2.) Use square or octogonal geometries for precisely matched capacitors.
3.) Make matched capacitors as large as possible.
4.) Place matched capacitors adjacent to one another.
5.) Place matched capacitors over field oxide.
6.) Connect the upper electrode of a matched capacitor to the higher-impedance node.
7.) Place dummy capacitors around the outer edge of the array.
8.) Electrostatically shield matched capacitors.
9.) Cross-couple arrayed matched capacitors.
10.) Account for the influence of the leads connecting to matched capacitors.
11.) Do not run leads over matched capacitors unless they are electrostatically shielded.
12.) Use thick-oxide dielectrics in preference to thin-oxide or composite dielectrics.
13.) If possible, place matched capacitors in areas of low stress gradients.
14.) Place matched capacitors well away from power devices.
15.) Place precisely matched capacitors on the axes of symmetry for the die.

† Alan Hastings, *Art of Analog Layout*, 2nd ed, 2006, Pearson Prentice Hall, New Jersey

Mismatched Transistors

Assume two transistors have $v_{DS1} = v_{DS2}$, $K_1' \neq K_2'$ and $V_{T1} \neq V_{T2}$. Therefore we have

$$\frac{i_O}{i_I} = \frac{K_2'(v_{GS} - V_{T2})^2}{K_1'(v_{GS} - V_{T1})^2}$$

How do you analyze the mismatch? Use plus and minus worst case approach. Define

$\Delta K' = K'_2 - K'_1$ and $K' = 0.5(K_2' + K_1') \Rightarrow K_1' = K' - 0.5\Delta K'$ and $K_2' = K' + 0.5\Delta K'$

$\Delta V_T = V_{T2} - V_{T1}$ and $V_T = 0.5(V_{T1} + V_{T2}) \Rightarrow V_{T1} = V_T - 0.5\Delta V_T$ and $V_{T2} = V_T + 0.5\Delta V_T$

Substituting these terms into the above equation gives,

$$\frac{i_O}{i_I} = \frac{(K' + 0.5\Delta K')(v_{GS} - V_T - 0.5\Delta V_T)^2}{(K' - 0.5\Delta K')(v_{GS} - V_T + 0.5\Delta V_T)^2} = \frac{\left(1 + \frac{\Delta K'}{2K'}\right)\left(1 - \frac{\Delta V_T}{2(v_{GS} - V_T)}\right)^2}{\left(1 - \frac{\Delta K'}{2K'}\right)\left(1 + \frac{\Delta V_T}{2(v_{GS} - V_T)}\right)^2}$$

Assuming that the terms added to or subtracted from "1" are smaller than unity gives

$$\frac{i_O}{i_I} \approx \left(1 + \frac{\Delta K'}{2K'}\right)\left(1 + \frac{\Delta K'}{2K'}\right)\left(1 - \frac{\Delta V_T}{2(v_{GS} - V_T)}\right)^2\left(1 - \frac{\Delta V_T}{2(v_{GS} - V_T)}\right)^2 \approx 1 + \frac{\Delta K'}{K'} - \frac{2\Delta V_T}{(v_{GS} - V_T)}$$

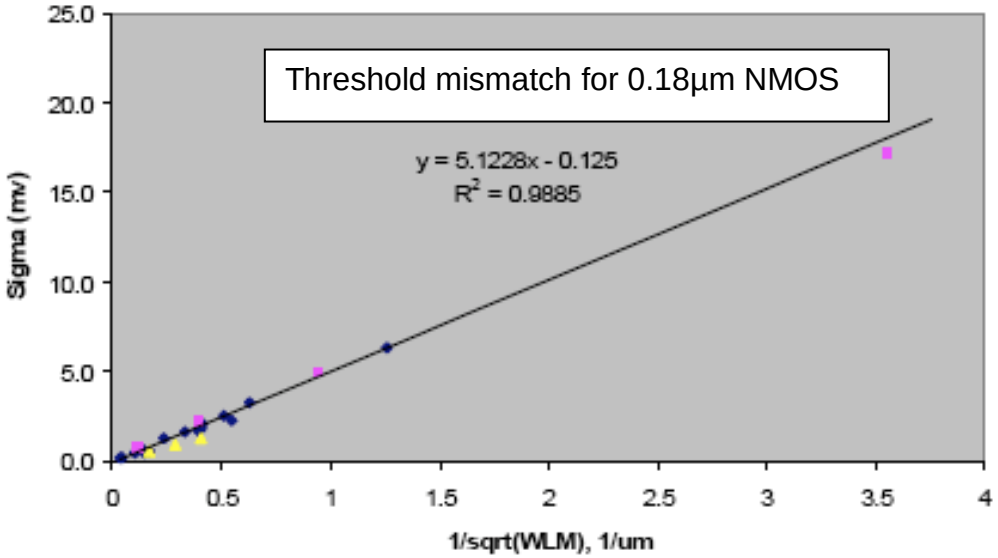
If $\Delta K'/K' = \pm 5\%$ and $\Delta V_T/(v_{GS} - V_T) = \pm 10\%$, then $i_O/i_I \approx 1 \pm 0.05 \pm (-0.20) = 1 \pm (0.25)$

Pelgrom's Law

Spatial Averaging: Local and random variations decrease as the device size increases, since the parameters "average out" over a greater area.

Pelgrom's Law:

$$\sigma^2(\Delta P) = \frac{A_p^2}{WL} + S_p^2 D_x^2$$



where,

ΔP = mismatch in a parameter, P

WL = width times the length of the device (effective Pelgrom area)

A_p = proportionality constant between the standard deviation of ΔP and the area of the device

D_x = distance between the matched devices

S_p = proportionality constant between the standard deviation of ΔP and D_x

As D_x becomes large, the standard deviation tends to infinity which is not realistic.

Geometric Effects

How does the size and shape of the transistor effect its matching?

Gate Area:

$$\sigma_{Vth} = \frac{C_{Vth}}{\sqrt{W_{eff}L_{eff}}} \qquad \sigma_{Kp} = K' \frac{C_{Kp}}{\sqrt{W_{eff}L_{eff}}} \qquad \sigma_{\Delta W/W} = \frac{C_{\Delta W/W}}{\sqrt{W_{eff}L_{eff}}}$$

where C_{Vth}, C_{Kp} and $C_{\Delta W/W}$ are constants determined by measurement.

Values from a 0.35µm CMOS technology:

$$\sigma_{V_{th},\text{NMOS}} = \frac{10.6\text{mV}\cdot\mu\text{m}}{\sqrt{W_{eff}L_{eff}}} \qquad \sigma_{V_{th},\text{PMOS}} = \frac{8.25\text{mV}\cdot\mu\text{m}}{\sqrt{W_{eff}L_{eff}}}$$

and

$$\sigma\left(\frac{\Delta W}{W}\right)_{\text{NMOS}} = \frac{0.0056\cdot\mu\text{m}}{\sqrt{W_{eff}L_{eff}}} \qquad \sigma\left(\frac{\Delta W}{W}\right)_{\text{PMOS}} = \frac{0.0011\cdot\mu\text{m}}{\sqrt{W_{eff}L_{eff}}}$$

The above results suggest that PMOS devices would be better matched than NMOS devices in this technology.

Rules for Transistor Matching†

1.) Use identical finger geometries.
2.) Use large active areas.
3.) For voltage matching, keep V_{GS}-V_T, small (i.e. 0.1V).
4.) For current matching, keep V_{GS}-V_T, large (i.e. 0.5V).
5.) Orient the transistors in the same direction.
6.) Place the transistors in close proximity to each other.
7.) Keep the layout of the matched transistors as compact as possible.
8.) Where practical use common centroid geometry layouts.
9.) Place dummy segments on the ends of arrayed transistors.
10.) Avoid using very short or narrow transistors.
11.) Place transistors in areas of low stress gradients.
12.) Do not place contacts on top of active gate area.
13.) Keep junctions of deep diffusions as far away from the active gate area as possible.
14.) Do not route metal across the active gate region.
15.) Place precisely matched transistors on the axes of symmetry of the die.
16.) Do not allow the buried layer shadow to intersect the active gate area.
17.) Connect gate fingers using metal connections.

† Alan Hastings, *Art of Analog Layout*, 2nd ed, 2006, Pearson Prentice Hall, New Jersey

SUMMARY

- IC technology offers poor absolute values but good relative values or matching
- In analog circuits, gains are determined by ratios (good matching) and time constants are determined by products (poor matching)
- Electrical matching is determined in the electrical design phase
  - Matching due to equal terminal voltages
  - Matching due to process independent biasing
  - Doubly correlated sampling
  - Self-calibration techniques
  - Dynamic element matching
- Physical matching is determined in the physical design phase
  - Random statistical fluctuations (microscopic fluctuations and irregularities)
  - Process bias (geometric variations)
  - Pattern shift (misalignment)
  - Diffusion interactions
  - Stress gradients and package shifts
  - Temperature gradients and thermoelectrics
  - Electrostatic interactions