LECTURE 09 – LARGE SIGNAL MOSFET MODEL

LECTURE ORGANIZATION

Outline

- Introduction to modeling
- Operation of the MOS transistor
- Simple large signal model (SAH model)
- Subthreshold model
- Short channel, strong inversion model
- Summary

***CMOS Analog Circuit Design*, 3rd Edition Reference**

Pages 68-76 and 96-98

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INTRODUCTION TO MODELING

Models Suitable for Understanding Analog Design

The model required for analog design with CMOS technology is one that leads to understanding and insight as distinguished from accuracy.

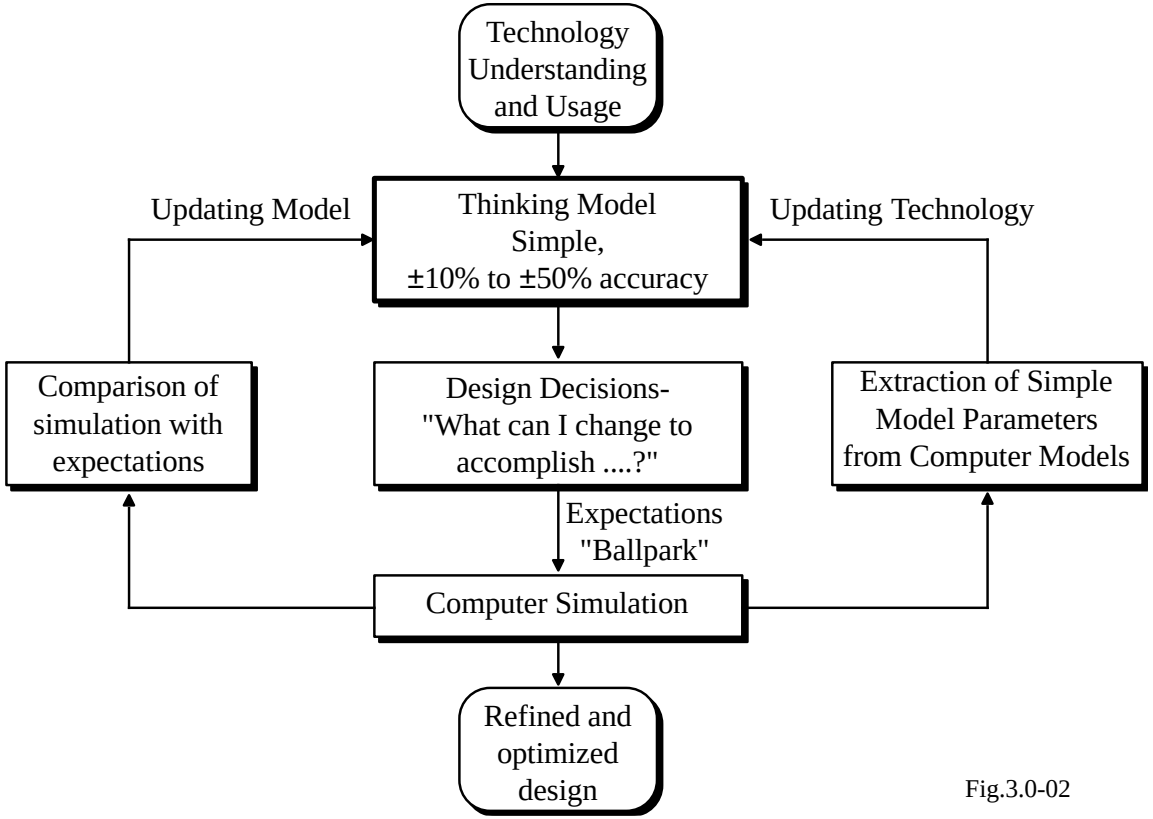

Fig.3.0-02

This lecture is devoted to the simple model suitable for design *not* using simulation.

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Categorization of Electrical Models

		Time Dependence	
		Time Independent	Time Dependent
Linearity	Linear	Small-signal, midband R_{in}, A_v, R_{out} (.TF)	Small-signal frequency response-poles and zeros (.AC)
	Nonlinear	DC operating point $i_D = f(v_D, v_G, v_S, v_B)$ (.OP)	Large-signal transient response - Slew rate (.TRAN)

Based on the simulation capabilities of SPICE.

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OPERATION OF THE MOS TRANSISTOR

Formation of the Channel for an Enhancement MOS Transistor

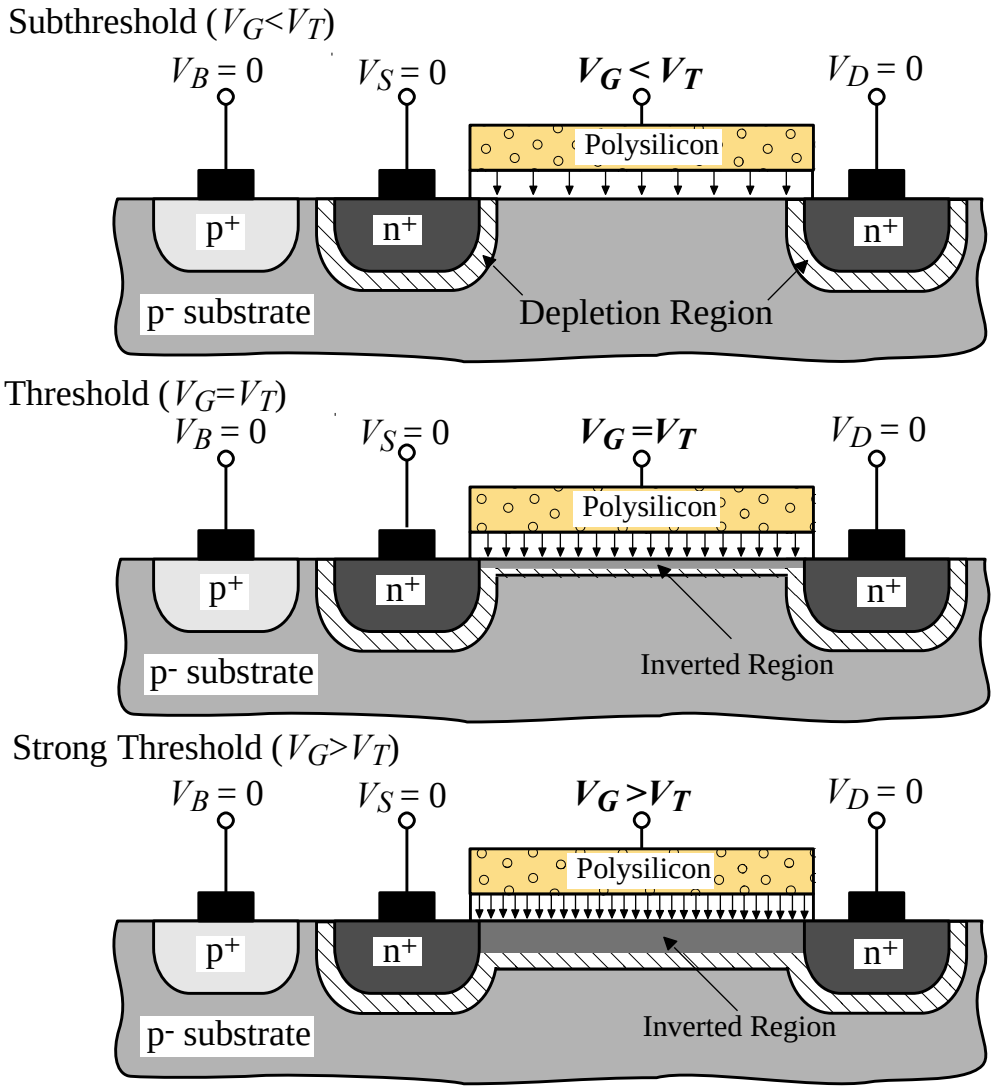

Fig.3.1-02

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Transconductance Characteristics of an Enhancement NMOS when V_{DS} = 0.1V

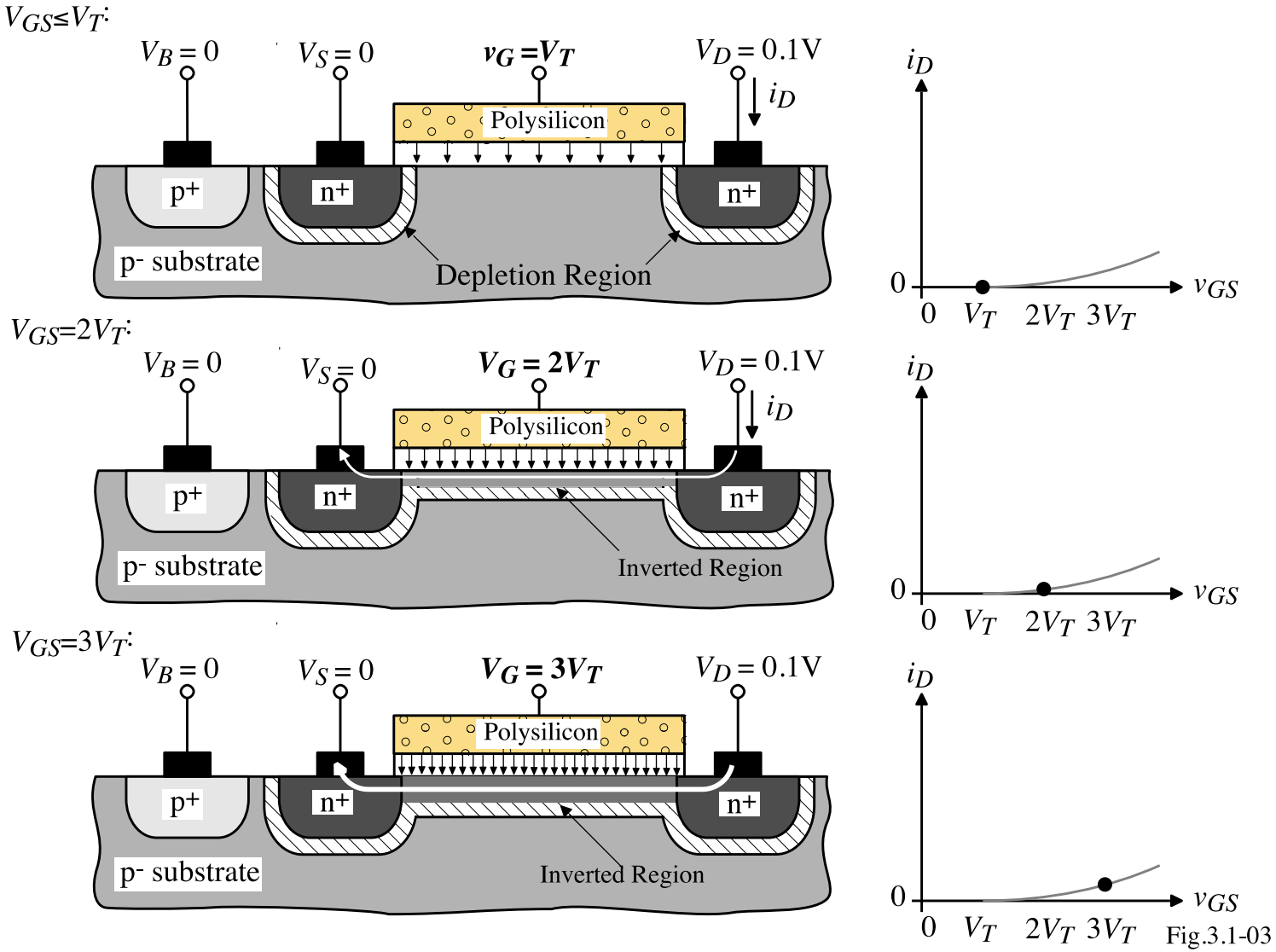

Fig.3.1-03

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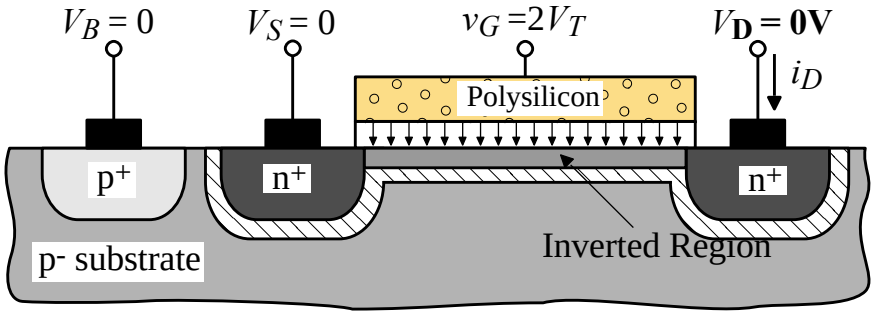
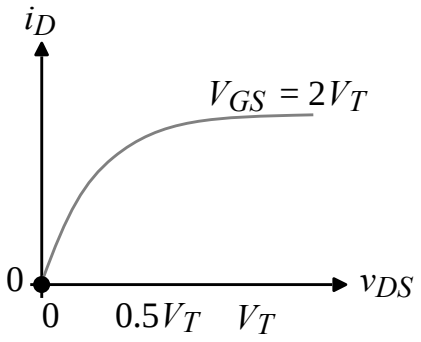
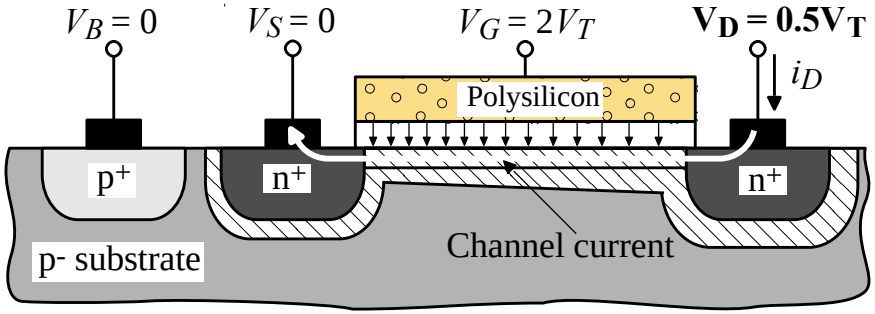
Output Characteristics of an Enhancement NMOS Transistor for $V_{GS} = 2V_T$

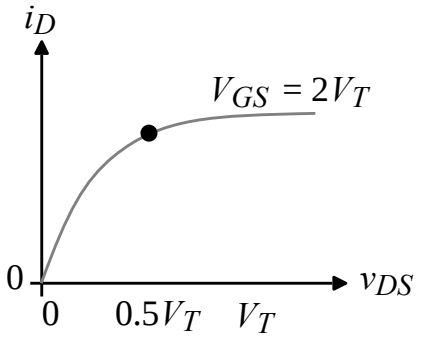
V_{DS}=0:



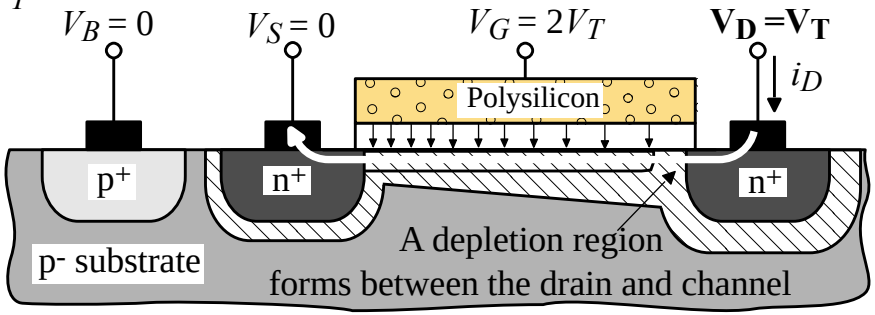


V_{DS}=$0.5V_T$:





V_{DS}=V_T:



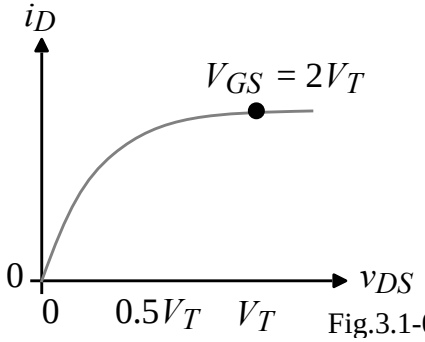


Fig.3.1-04

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Output Characteristics of an Enhancement NMOS when $v_{DS} = 2V_T$

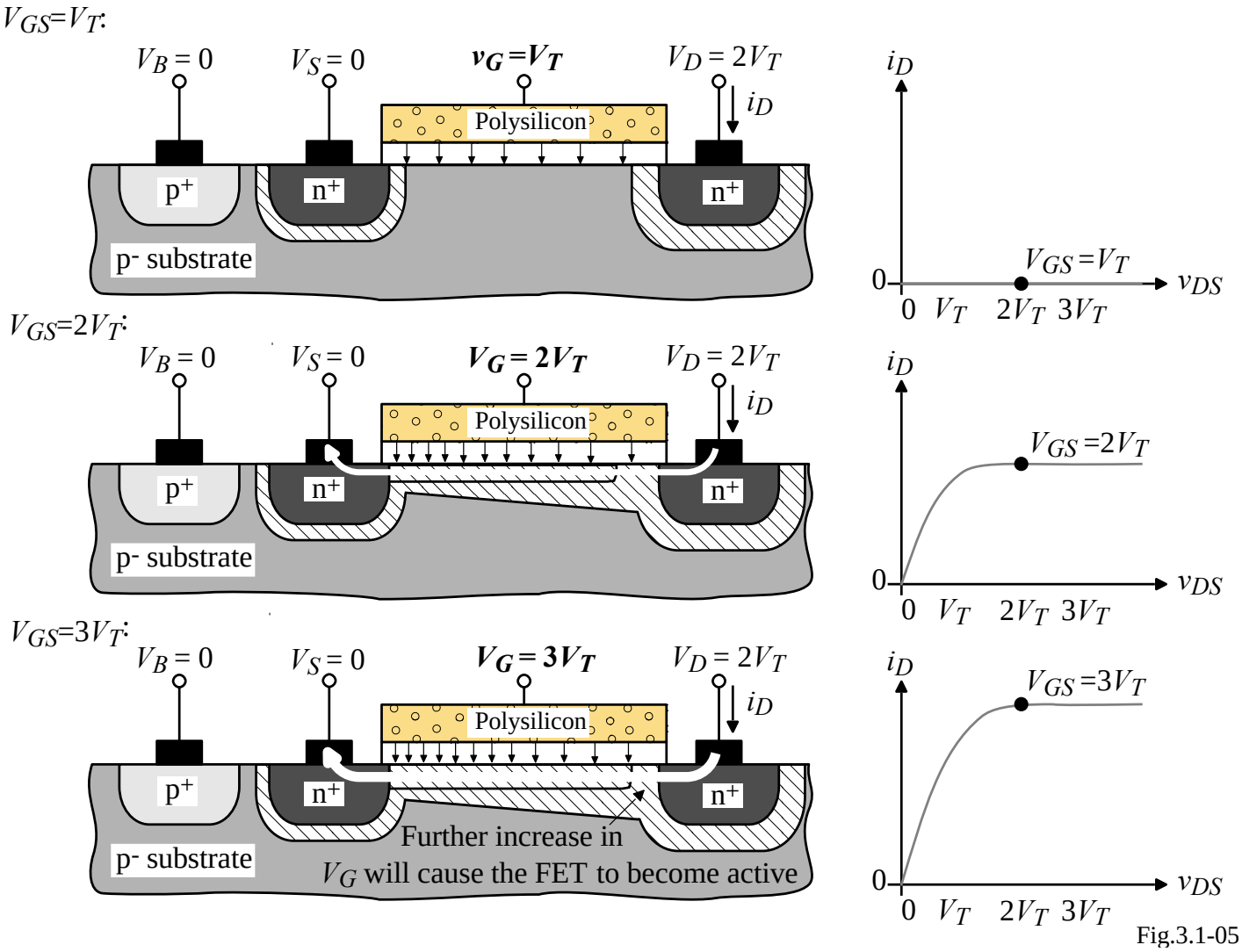

Fig.3.1-05

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Output Characteristics of an Enhancement NMOS Transistor

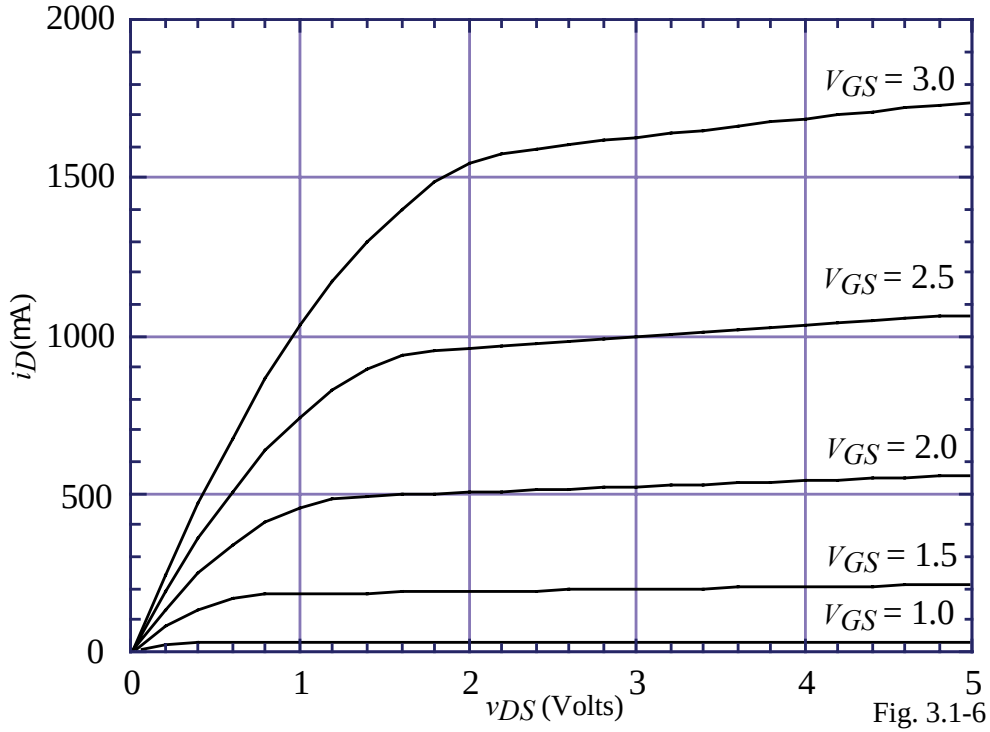

Fig. 3.1-6

SPICE Input File:

```
Output Characteristics for NMOS
M1 6 1 0 0 MOS1 w=5u l=1.0u
VGS1 1 0 1.0
M2 6 2 0 0 MOS1 w=5u l=1.0u
VGS2 2 0 1.5
M3 6 3 0 0 MOS1 w=5u l=1.0u
VGS3 3 0 2.0
M4 6 4 0 0 MOS1 w=5u l=1.0u
VGS4 4 0 2.5
M5 6 5 0 0 MOS1 w=5u l=1.0u
VGS5 5 0 3.0
VDS 6 0 5
.model mos1 nmos (vto=0.7 kp=110u
+gamma=0.4 lambda=.04 phi=.7)
.dc vds 0 5 .2
.print dc ID(M1), ID(M2), ID(M3), ID(M4),
ID(M5)
.end
```


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Transconductance Characteristics of an Enhancement NMOS Transistor

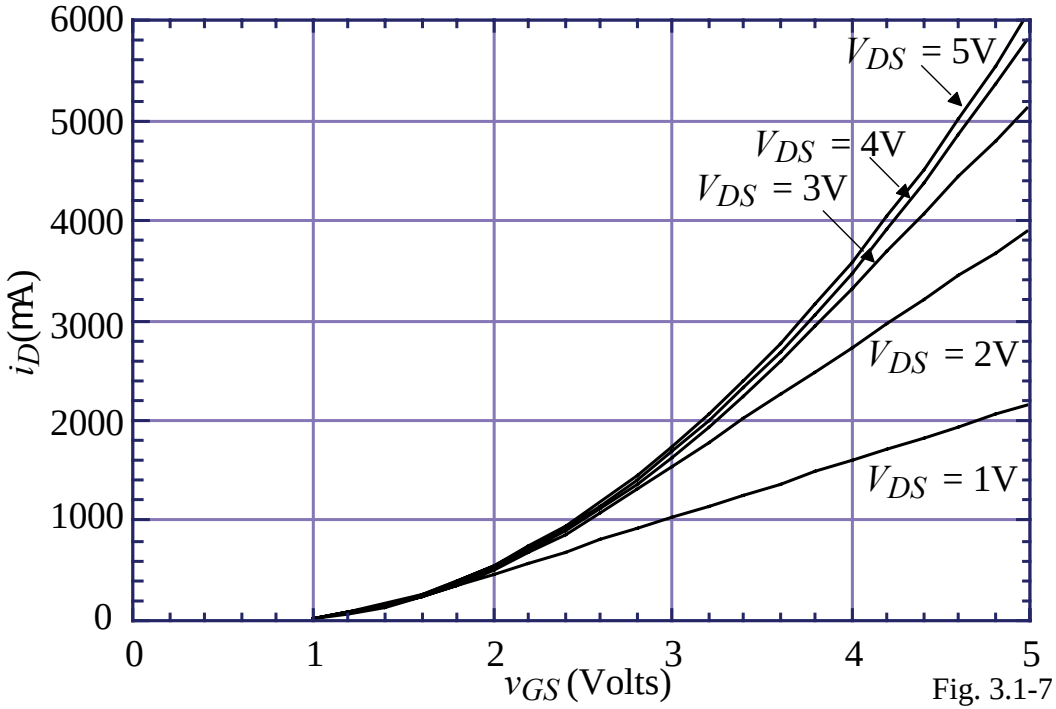

Fig. 3.1-7

SPICE Input File:

```
Transconductance Characteristics for NMOS
M1 1 6 0 0 MOS1 w=5u l=1.0u
VDS1 1 0 1.0
M2 2 6 0 0 MOS1 w=5u l=1.0u
VDS2 2 0 2.0
M3 3 6 0 0 MOS1 w=5u l=1.0u
VDS3 3 0 3.0
M4 4 6 0 0 MOS1 w=5u l=1.0u
VDS4 4 0 4.0
M5 5 6 0 0 MOS1 w=5u l=1.0u
VDS5 5 0 5.0
VGS 6 0 5
.model mos1 nmos (vto=0.7 kp=110u
+gamma=0.4 lambda=.04 phi=.7)
.dc vgs 0 5 .2
.print dc ID(M1), ID(M2), ID(M3), ID(M4),
ID(M5)
.probe
.end
```


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SIMPLE LARGE SIGNAL MODEL (SAH MODEL)

Large Signal Model Derivation

1.) Let the charge per unit area in the channel inversion layer be

$$Q_I(y) = -C_{ox}[v_{GS}-v(y)-V_T] \quad (\text{coul./cm}^2)$$

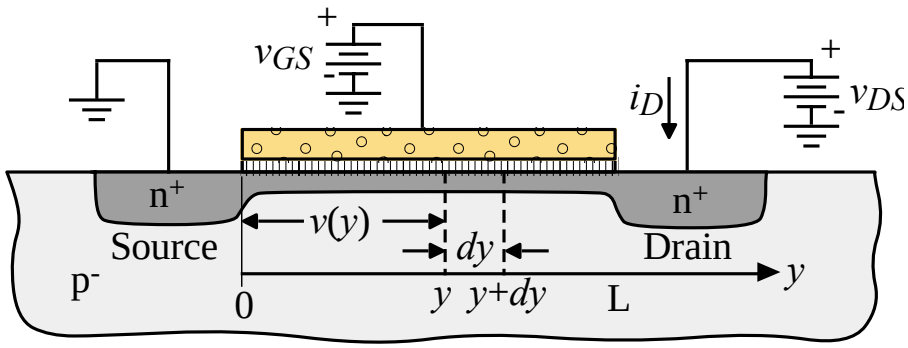

Fig.110-03

2.) Define sheet conductivity of the inversion layer per square as

$$\sigma_S = \mu_o Q_I(y)\left(\frac{\text{cm}^2}{\text{v}\cdot\text{s}}\right)\left(\frac{\text{coulombs}}{\text{cm}^2}\right) = \frac{\text{amps}}{\text{volt}} = \frac{1}{\Omega/\text{sq.}}$$

3.) Ohm's Law for current in a sheet is

$$J_S = \frac{i_D}{W} = -\sigma_S E_y = -\sigma_S \frac{dv}{dy} \rightarrow dv = \frac{-i_D}{\sigma_S W}\,dy = \frac{-i_D dy}{\mu_o Q_I(y) W} \rightarrow i_D\,dy = -W\mu_o Q_I(y)dv$$

4.) Integrating along the channel for 0 to L gives

$$\int_0^L i_D dy = -\int_0^{v_{DS}} W\mu_o Q_I(y)dv = \int_0^{v_{DS}} W\mu_o C_{ox}[v_{GS}-v(y)-V_T]\,dv$$

5.) Evaluating the limits gives

$$i_D = \frac{W\mu_o C_{ox}}{L}\left[(v_{GS}-V_T)v(y) - \frac{v^2(y)}{2}\right]_0^{v_{DS}} \rightarrow \boxed{i_D = \frac{W\mu_o C_{ox}}{L}\left[(v_{GS}-V_T)v_{DS} - \frac{v_{DS}^2}{2}\right]}$$

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Saturation Voltage - V_{DS}(sat)

Interpretation of the large signal model:

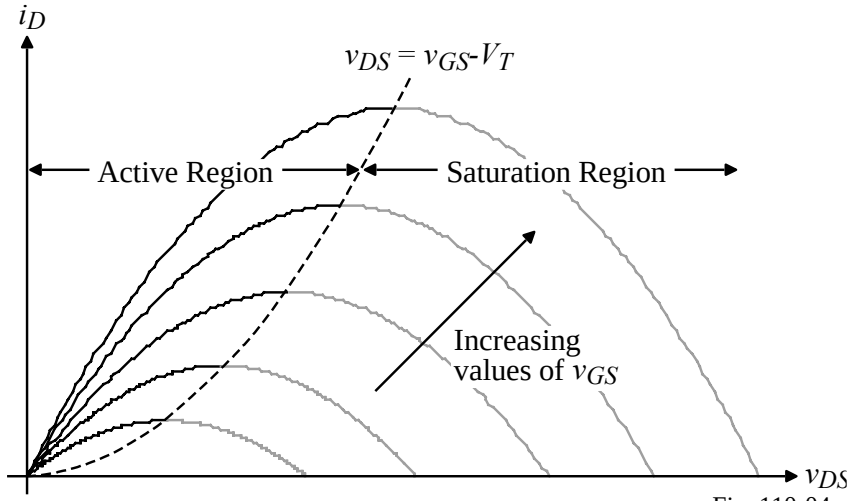

Fig. 110-04

The saturation voltage for MOSFETs is the value of drain-source voltage at the peak of the inverted parabolas.

$$\frac{di_D}{dv_{DS}} = \frac{\mu_o C_{ox} W}{L}\left[(v_{GS}\text{-}V_T) - v_{DS}\right] = 0$$

$$\boxed{v_{DS}(\text{sat}) = v_{GS} - V_T}$$

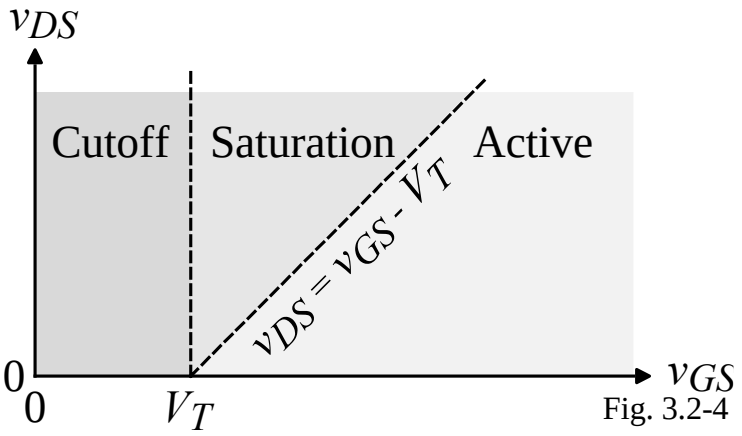

Fig. 3.2-4

Useful definitions:

$$\frac{\mu_o C_{ox} W}{L} = \frac{K'W}{L} = \beta$$

Note that newest editions of *Analysis and Design of Analog ICs*, P.R. Gray et.al, switches the definition for the active and saturation regions.

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The Simple Large Signal MOSFET Model

Regions of Operation of the MOS Transistor:

1.) Cutoff Region:

$v_{GS} - V_T < 0$

$i_D = 0$

(Ignores subthreshold currents)

2.) Active Region

$0 < v_{DS} < v_{GS} - V_T$

$$i_D = \frac{\mu_o C_{ox} W}{2L}\left[2(v_{GS} - V_T) - v_{DS}\right] v_{DS}$$

3.) Saturation Region

$0 < v_{GS} - V_T < v_{DS}$

$$i_D = \frac{\mu_o C_{ox} W}{2L}\left(v_{GS} - V_T\right)^2$$

Output Characteristics of the MOSFET:

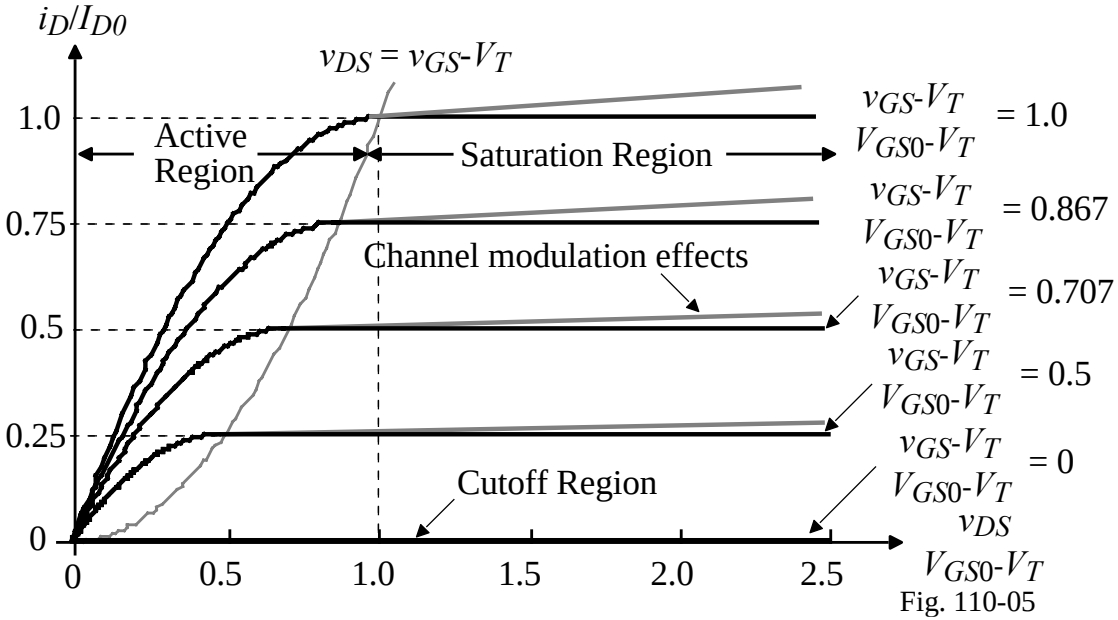

Fig. 110-05

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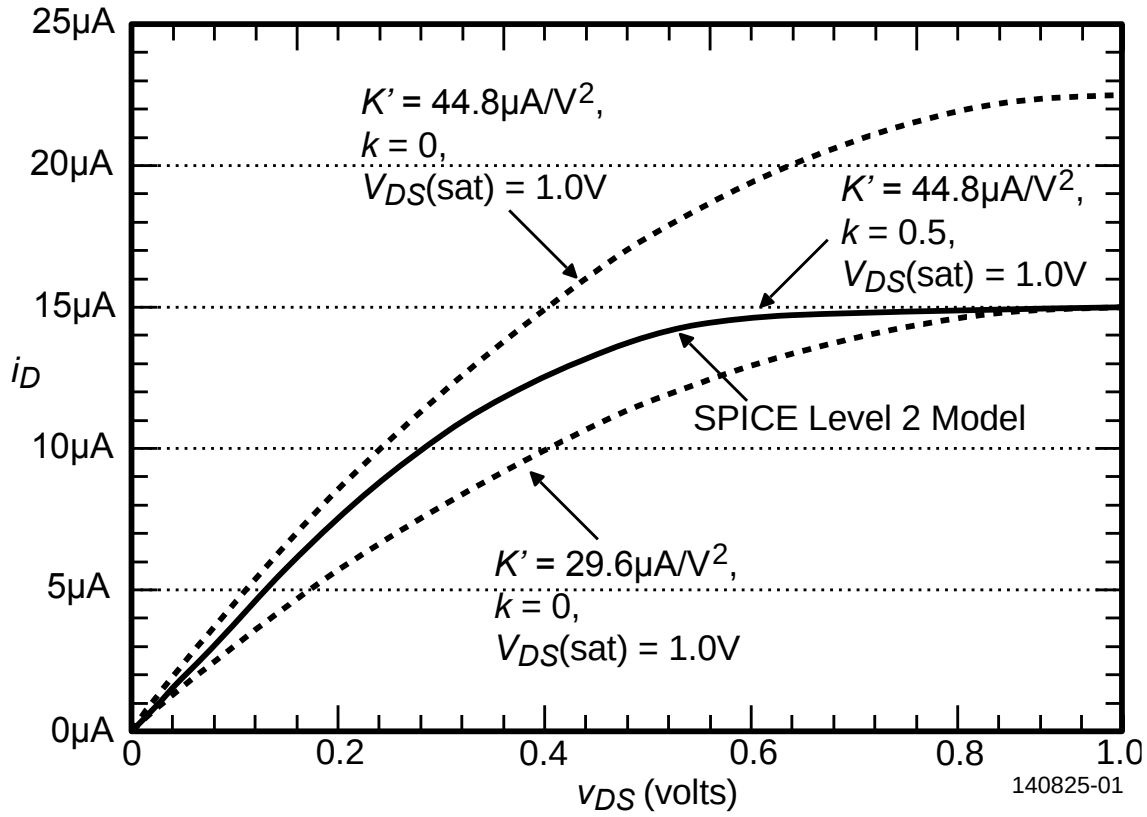
Performance Limitations of the Simple Sah

It turns out, that if we compare the Sah model to a more precise model (SPICE level 2) that the Sah model has issues with the "knee" area as shown.



V_{GS} = 2.0V, W/L = 100μm/100μm

This discrepancy is due to the fact that we assumed that the threshold, V_T, was constant over the channel.

If we let $V_T(y) = V_T + kv(y)$ then the Sah model is exactly the same as the SPICE model.

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Modification of the Previous Model to Include the Effects of v_{DS} on V_T

From the previous derivation:

$$\int_0^L i_D\,dy = -\int_0^{v_{DS}} W\mu_o Q_I(y)dv = \int_0^{v_{DS}} W\mu_o C_{ox}[v_{GS} - v(y) - V_T]dv$$

Assume that the threshold voltage varies across the channel in the following way:

$$V_T(y) = V_T + kv(y)$$

where V_T is the value of V_T the at the source end of the channel and k is a constant.

Integrating the above gives,

$$i_D = \frac{W\mu_o C_{ox}}{L}\left[(v_{GS}-V_T)v(y) - (1+k)\frac{v(y)^2}{2}\right]_0^{v_{DS}} \rightarrow i_D = \frac{W\mu_o C_{ox}}{L}\left[(v_{GS}-V_T)v_{DS} - (1+k)\frac{v_{DS}^2}{2}\right]$$

To find v_{DS}(sat), set the di_D/dv_{DS} equal to zero and solve for $v_{DS} = v_{DS}$(sat),

$$v_{DS}(\text{sat}) = \frac{v_{GS} - V_T}{1 + k}$$

Therefore, in the saturation region, the drain current is

$$i_D = \frac{W\mu_o C_{ox}}{2(1+k)L}(v_{GS} - V_T)^2$$

For $k = 0.5$ and $K' = 44.8\mu A/V^2$, excellent correlation is achieved with SPICE 2 as seen on the previous slide.

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Influence of v_{DS} on the Output Characteristics

Channel modulation effect:

As the value of v_{DS} increases, the effective L decreases causing the current to increase.

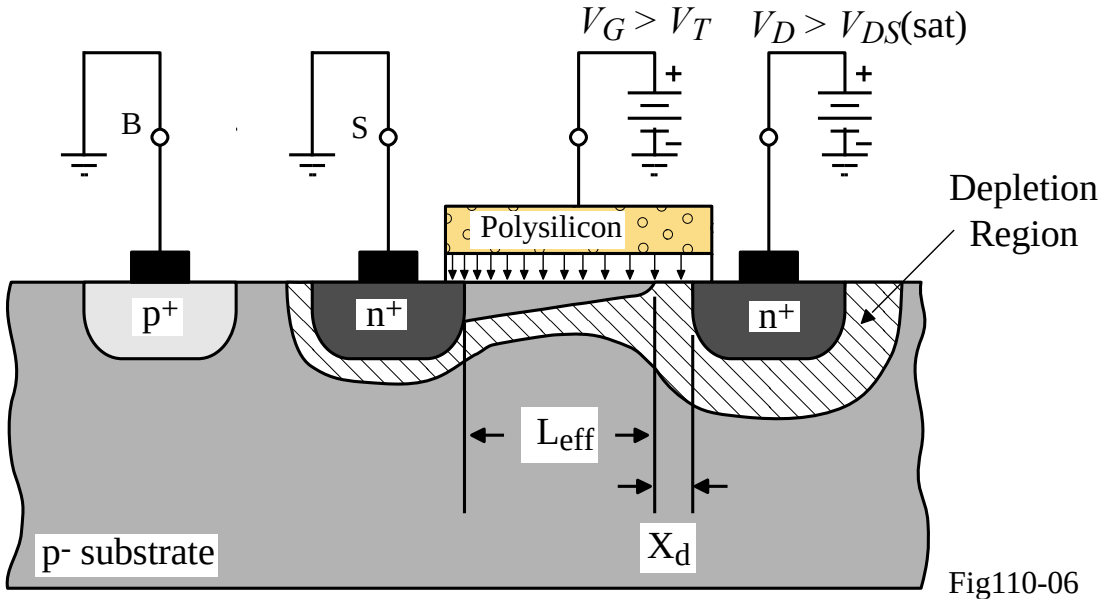

Fig110-06

Illustration:

Note that $L_{\text{eff}} = L - X_d$

Therefore the model in saturation becomes,

$$i_D = \frac{K'W}{2L_{\text{eff}}}(v_{GS}-V_T)^2 \rightarrow \frac{di_D}{dv_{DS}} = -\frac{K'W}{2L_{\text{eff}}^2}(v_{GS}-V_T)^2\frac{dL_{\text{eff}}}{dv_{DS}} = \frac{i_D}{L_{\text{eff}}}\frac{dX_d}{dv_{DS}} \equiv \lambda i_D$$

Therefore, a good approximation to the influence of v_{DS} on i_D is

$$i_D \approx i_D(\lambda = 0) + \frac{di_D}{dv_{DS}}v_{DS} = i_D(\lambda = 0)(1 + \lambda v_{DS}) = \frac{K'W}{2L}(v_{GS}-V_T)^2(1+\lambda v_{DS})$$

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Channel Length Modulation Parameter, λ

Assume the MOS is transistor is saturated-

$$\therefore \quad i_D = \frac{\mu C_{ox} W}{2L} (v_{GS} - V_T)^2 (1 + \lambda v_{DS})$$

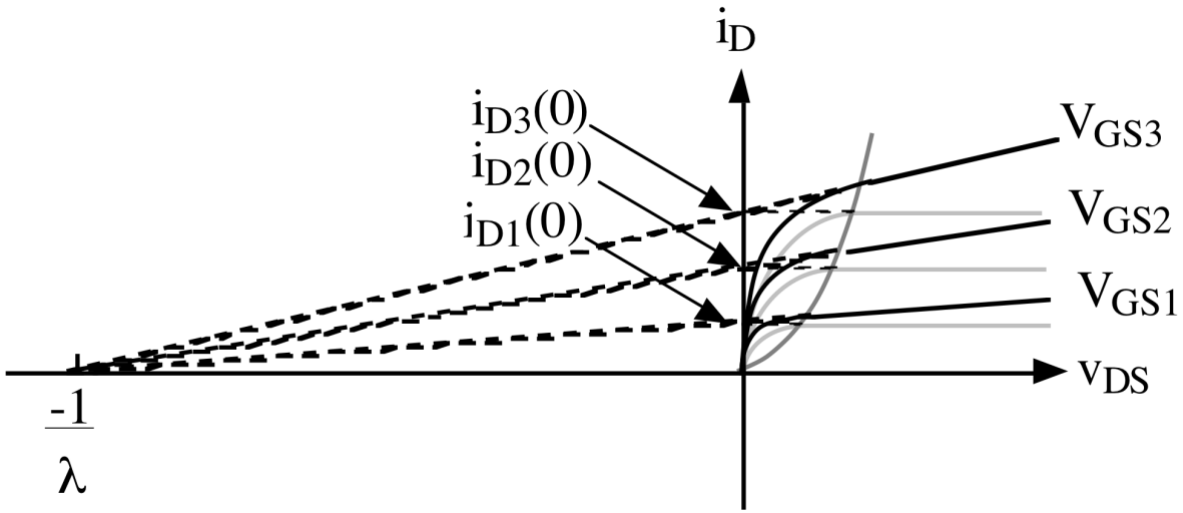
Define $i_D(0) = i_D$ when $v_{DS} = 0$V.

$$\therefore \quad i_D(0) = \frac{\mu C_{ox} W}{2L} (v_{GS} - V_T)^2$$

Now,

$$i_D = i_D(0)[1 + \lambda v_{DS}] = i_D(0) + \lambda i_D(0)\, v_{DS}$$

Matching with $y = mx + b$ gives the value of λ



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Influence of Channel Length on λ

Note that the value of λ varies with channel length, L. The data below is from a 0.25μm CMOS technology.

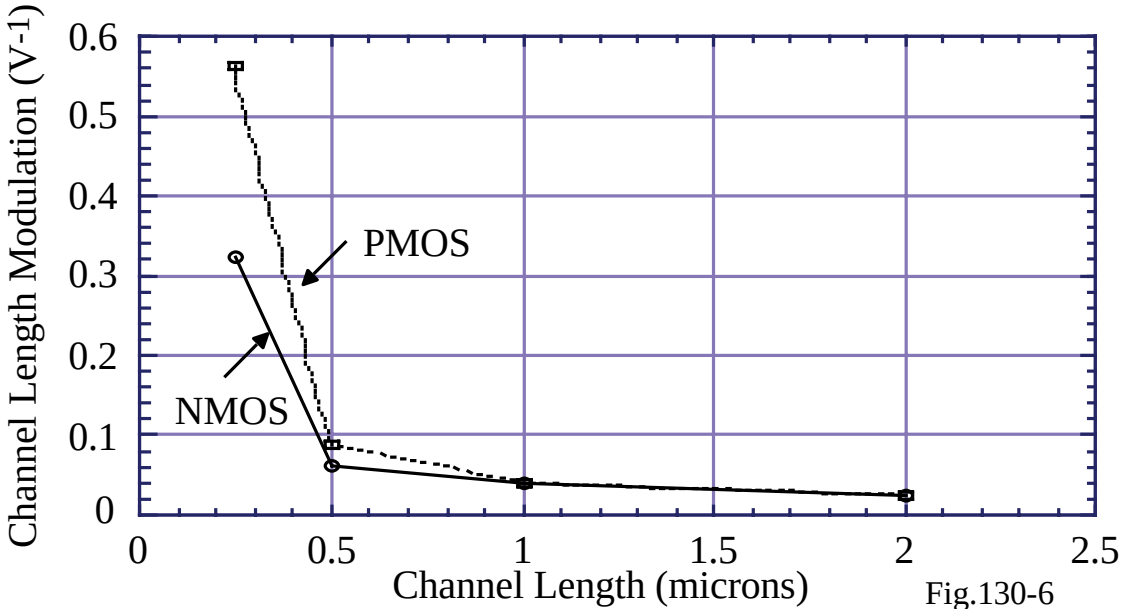

Fig.130-6

Most analog designers stay away from minimum channel length to get better gains and matching at the sacrifice of speed.

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Influence of the Bulk Voltage on the Large Signal MOSFET Model

The components of the threshold voltage are:

$V_{SB0} = 0$:

V_T = Gate-bulk work function (ϕ_{MS})

+ voltage to change the surface potential ($-2\phi_F$)

+ voltage to offset the channel-bulk depletion charge ($-Q_b/C_{ox}$)

$V_{SB1} > 0$:

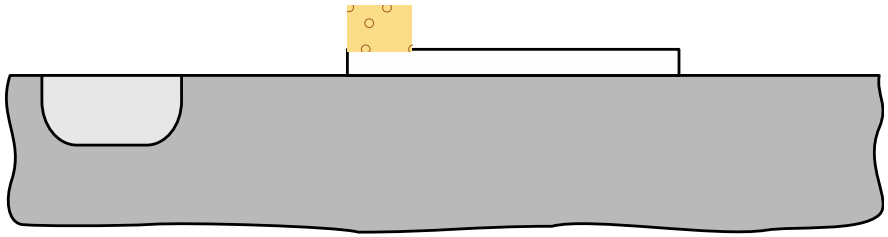
$V_D > 0$

+ voltage to compensate the undesired interface charge ($-Q_{ss}/C_{ox}$)

We know that

$$Q_b = \gamma\sqrt{2|\phi_F| - v_{BS}}$$

$V_{SB2} > V_{SB1}$:



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Therefore, as the bulk becomes more reverse biased with respect to the source, the threshold voltage must increase to offset the increased channel-bulk depletion charge.

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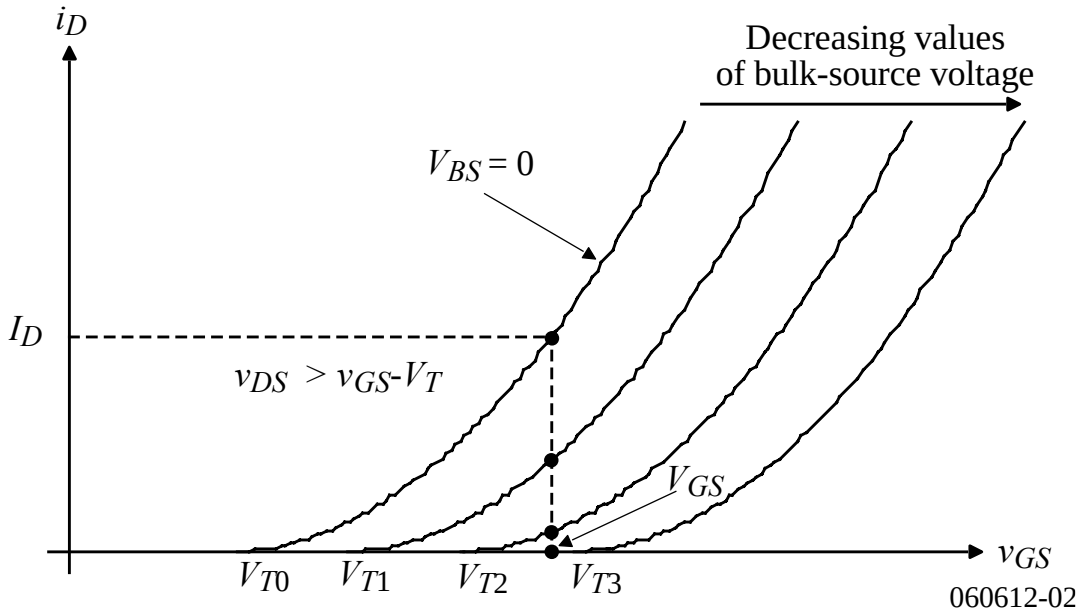
Influence of the Bulk Voltage on the Large Signal MOSFET Model - Continued

Bulk-Source (v_{BS}) influence on the transconductance characteristics-



In general, the simple model incorporates the bulk effect into V_T by the previously developed relationship:

$$V_T(v_{BS}) = V_{T0} + \gamma\sqrt{2|\phi_f| - v_{BS}} - \gamma\sqrt{2|\phi_f|}$$

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Summary of the Simple Large Signal MOSFET Model

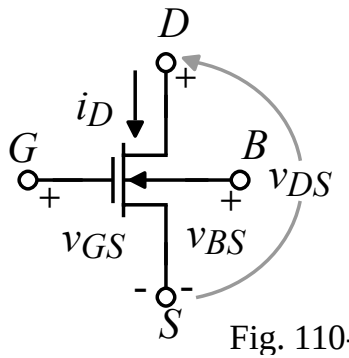

Fig. 110-10

N-channel reference convention:

Non-saturation-

$$i_D = \frac{W\mu_o C_{ox}}{L}\left[(v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2}\right](1 + \lambda v_{DS})$$

Saturation-

$$i_D = \frac{W\mu_o C_{ox}}{L}\left[(v_{GS}-V_T)v_{DS}(\text{sat})-\frac{v_{DS}(\text{sat})^2}{2}\right](1+\lambda v_{DS}) = \frac{W\mu_o C_{ox}}{2L}(v_{GS}-V_T)^2(1+\lambda v_{DS})$$

where:

μ_o = zero field mobility ($cm^2/volt\cdot sec$)

C_{ox} = gate oxide capacitance per unit area (F/cm^2)

λ = channel-length modulation parameter ($volts^{-1}$)

$V_T = V_{T0} + \gamma\left(\sqrt{2|\phi_f| - v_{BS}} - \sqrt{2|\phi_f|}\right)$

V_{T0} = zero bias threshold voltage

γ = bulk threshold parameter ($volts^{0.5}$)

$2|\phi_f|$ = strong inversion surface potential (volts)

Terms in red are model parameters

For p-channel MOSFETs, use n-channel equations with p-channel parameters and invert the current.

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Silicon Constants

Constant Symbol	Constant Description	Value	Units
V_G	Silicon bandgap (27°C)	1.205	V
k	Boltzmann's constant	1.381×10^{-23}	J/K
n_i	Intrinsic carrier concentration (27°C)	1.45×10^{10}	cm^{-3}
ε_o	Permittivity of free space	8.854×10^{-14}	F/cm
ε_{Si}	Permittivity of silicon	$11.7\ \varepsilon_o$	F/cm
ε_{OX}	Permittivity of SiO_2	$3.9\ \varepsilon_o$	F/cm

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MOSFET Parameters

Model Parameters for a Typical CMOS Bulk Process (0.25µm CMOS *n*-well):

Parameter Symbol	Parameter Description	Typical Parameter Value		Units
		N-Channel	P-Channel	
V_{T0}	Threshold Voltage ($V_{BS} = 0$)	0.5± 0.15	-0.5 ± 0.15	V
K'	Transconductance Parameter (in saturation)	120.0 ± 10%	25.0 ± 10%	$\mu A/V^2$
γ	Bulk threshold parameter	0.4	0.6	$(V)^{1/2}$
λ	Channel length modulation parameter	0.32 ($L=L_{min}$) 0.06 ($L \geq 2L_{min}$)	0.56 ($L=L_{min}$) 0.08 ($L \geq 2L_{min}$)	$(V)^{-1}$
$2\lvert\phi_F\rvert$	Surface potential at strong inversion	0.7	0.8	V

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SUBTHRESHOLD MODEL

Large-Signal Model for Weak Inversion

The electrons in the substrate at the source side can be expressed as,

$$n_p(0) = n_{po}\exp\left(\frac{\phi_s}{V_t}\right)$$

The electrons in the substrate at the drain side can be expressed as,

$$n_p(L) = n_{po}\exp\left(\frac{\phi_s - v_{DS}}{V_t}\right)$$

Therefore, the drain current due to diffusion is,

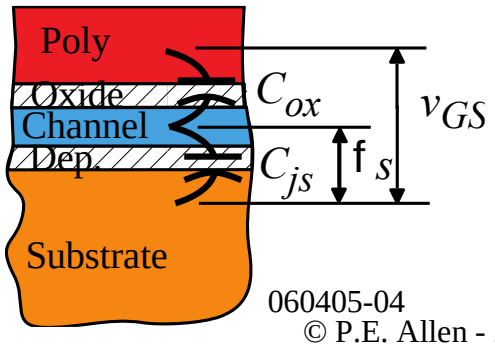
$$i_D = qAD_n\left(\frac{n_p(L) - n_p(0)}{L}\right) = \frac{W}{L}qXD_n n_{po}\exp\left(\frac{\phi_s}{V_t}\right)\left[1 - \exp\left(-\frac{v_{DS}}{V_t}\right)\right]$$

where X is the thickness of the region in which i_D flows.

In weak inversion, the changes in the surface potential, $\Delta\phi_s$ are controlled by changes in the gate-source voltage, Δv_{GS}, through a voltage divider consisting of C_{ox} and C_{js}, the depletion region capacitance.

$$\therefore \quad \frac{d\phi_s}{dv_{GS}} = \frac{C_{ox}}{C_{ox} + C_{js}} = \frac{1}{n} \quad \rightarrow \quad \phi_s = \frac{v_{GS}}{n} + k_1 = \frac{v_{GS} - V_T}{n} + k_2$$

where $k_2 = k_1 + \frac{V_T}{n}$



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Large-Signal Model for Weak Inversion – Continued

Substituting the above relationships back into the expression for i_D gives,

$$i_D = \frac{W}{L} qXD_n n_{po} \exp\left(\frac{k_2}{V_t}\right)\exp\left(\frac{v_{GS}-V_T}{nV_t}\right)\left[1 - \exp\left(-\frac{v_{DS}}{V_t}\right)\right]$$

Define I_t as

$$I_t = qXD_n n_{po} \exp\left(\frac{k_2}{V_t}\right)$$

to get,

$$i_D = \frac{W}{L} I_t \exp\left(\frac{v_{GS}-V_T}{nV_t}\right)\left[1 - \exp\left(-\frac{v_{DS}}{V_t}\right)\right]$$

where $n \approx 1.5 - 3$

If $v_{DS} > 0$, then

$$i_D = I_t \frac{W}{L} \exp\left(\frac{v_{GS}-V_T}{nV_t}\right)\left(1 + \frac{v_{DS}}{V_A}\right)$$

The boundary between nonsaturated and saturated is found as,

$$V_{ov} = V_{DS}(\text{sat}) = V_{ON} = V_{GS} - V_T = 2nV_t$$

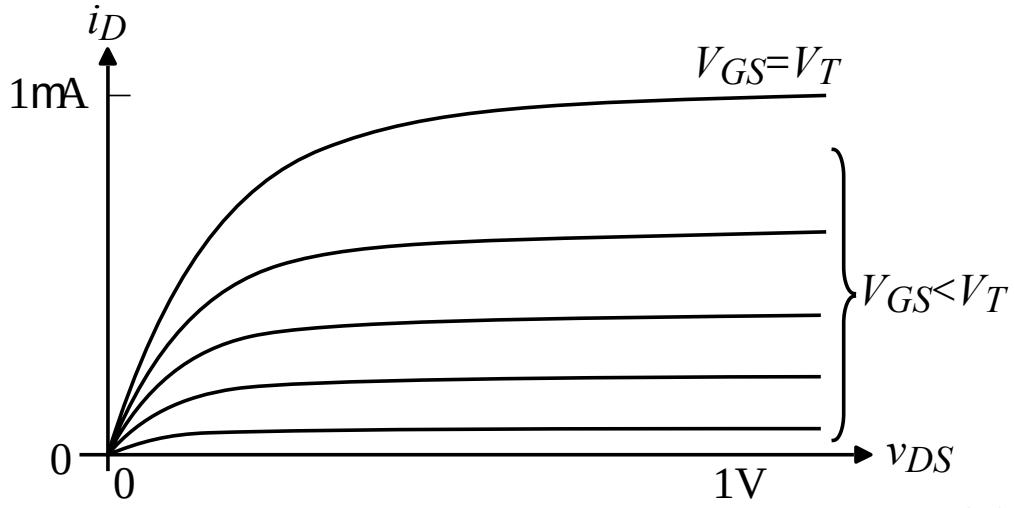

Fig. 140-03

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SHORT CHANNEL, STRONG INVERSION MODEL

What is Velocity Saturation?

The most important short-channel effect in MOSFETs is the velocity saturation of carriers in the channel. A plot of electron drift velocity versus electric field is shown below.

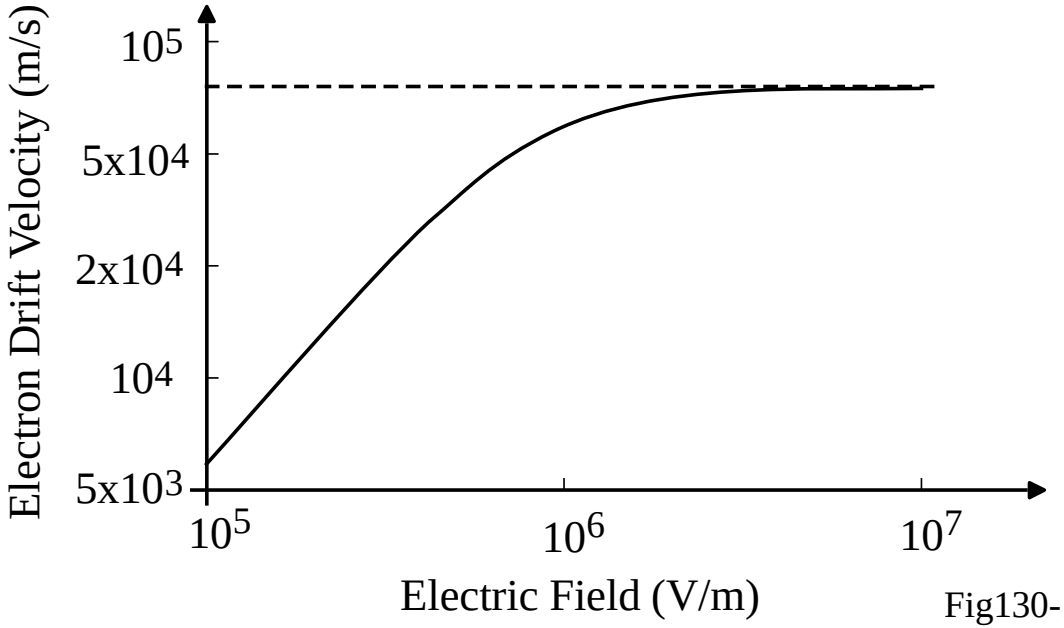

Fig130-1

An expression for the electron drift velocity as a function of the electric field is,

$$v_d \approx \frac{\mu_n E}{1 + E/E_c}$$

where

v_d = electron drift velocity (m/s)

μ_n = low-field mobility ($\approx 0.07 m^2/V \cdot s$)

E_c = critical electrical field at which velocity saturation occurs

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Short-Channel Model Derivation

As before,

$$J_D = J_S = \frac{i_D}{W} = Q_I(y)v_d(y) \rightarrow i_D = WQ_I(y)v_d(y) = \frac{WQ_I(y)\mu_n E}{1 + E/E_c} \rightarrow i_D\left(1+ \frac{E}{E_c}\right) = WQ_I(y)\mu_n E$$

Replacing E by dv/dy gives,

$$i_D\left(1 + \frac{1}{E_c}\frac{dv}{dy}\right) = WQ_I(y)\mu_n\frac{dv}{dy}$$

Integrating along the channel gives,

$$\int_0^L i_D\left(1 + \frac{1}{E_c}\frac{dv}{dy}\right)dy = \int_0^{v_{DS}} WQ_I(y)\mu_n dv$$

The result of this integration is,

$$i_D = \frac{\mu_n C_{ox}}{2\left(1 + \frac{1}{E_c}\frac{v_{DS}}{L}\right)}\frac{W}{L}[2(v_{GS}\text{-}V_T)v_{DS}\text{-}v_{DS}^2] = \frac{\mu_n C_{ox}}{2(1 + \theta v_{DS})}\frac{W}{L}\ [2(v_{GS}\text{-}V_T)v_{DS}\text{-}v_{DS}^2]$$

where $\theta = 1/(E_c L)$ with dimensions of V^{-1}.

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Saturation Voltage

Differentiating i_D with respect to v_{DS} and setting equal to zero gives,

$$V'_{DS}(\text{sat}) = \frac{1}{\theta}\left(\sqrt{1 + 2\theta(V_{GS}-V_T}\,-1\right) \approx (V_{GS}-V_T)\left(1 - \frac{\theta(V_{GS}-V_T)}{2} + \cdots\right)$$

if

$$\frac{\theta(V_{GS}-V_T)}{2} < 1$$

Therefore,

$$V'_{DS}(\text{sat}) \approx V_{DS}(\text{sat})\left(1 - \frac{\theta(V_{GS}-V_T)}{2} + \cdots\right)$$

Note that the transistor will enter the saturation region for $v_{DS} < v_{GS} - V_T$ in the presence of velocity saturation.

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Large Signal Model for the Saturation Region

To develop the large signal model, we will assume that

$$\frac{\theta(V_{GS}-V_T)}{2} < 1$$

so that we can substitute the less complex expression of

$$V'_{DS}(\text{sat}) \approx (V_{GS}-V_T)$$

into the active region version of the model to get,

$$i_D = \frac{K'}{2\left(1 + \theta(v_{GS} - V_T)\right)}\frac{W}{L}\ [2(v_{GS}-V_T)(v_{GS}-V_T)- (v_{GS}-V_T)^2]$$

$$= \frac{K'}{2[1 + \theta(v_{GS}-V_T)]}\frac{W}{L}[\ v_{GS} - V_T]^2$$

However, we continue to use the following to define when the MOSFET is in the saturation region,

$$v_{DS} \geq (V_{GS}-V_T)\left(1 - \frac{\theta(V_{GS}-V_T)}{2} + \cdots\right)$$

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The Influence of Velocity Saturation on the Transconductance Characteristics

The following plot was made for K' = 110μA/V^2 and W/L = 1:

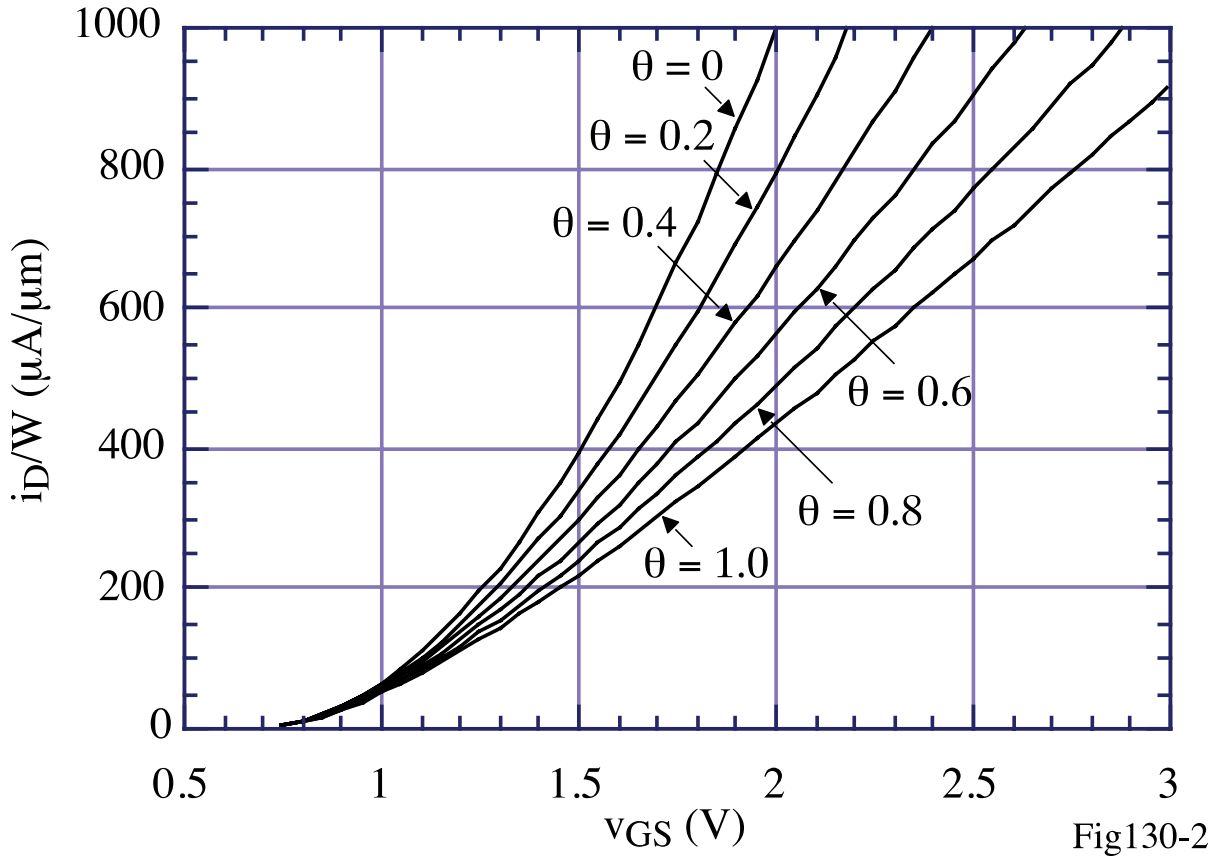

Fig130-2

Note as the velocity saturation effect becomes stronger, that the drain current-gate voltage relationship becomes linear.

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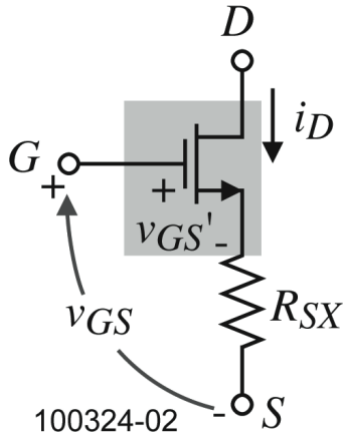
Circuit Model for Velocity Saturation

A simple circuit model to include the influence of velocity saturation is is shown:



We know that

$$i_D = \frac{K'W}{2L}(v_{GS}' - V_T)^2 \quad \text{and} \qquad v_{GS} = v_{GS}' + i_D R_{SX}$$

or

$$v_{GS}' = v_{GS} - i_D R_{XS}$$

Substituting v_{GS}' into the current relationship gives,

$$i_D = \frac{K'W}{2L}(v_{GS} - i_D R_{SX} - V_T)^2$$

Solving for i_D results in,

$$i_D = \frac{K'}{2\left[1 + K'\frac{W}{L}R_{SX}(v_{GS} - V_T)\right]}\frac{W}{L}(v_{GS} - V_T)^2$$

Comparing with the previous result, we see that

$$\theta = K'\frac{W}{L}R_{SX} \qquad \rightarrow \quad R_{SX} = \frac{\theta L}{K'W} = \frac{1}{E_c K'W}$$

Therefore for $K' = 110\mu A/V^2$, $W = 1\mu m$ and $E_c = 1.5 \times 10^6 V/m$, we get $R_{SX} = 6.06k\Omega$.

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SUMMARY

- The modeling of this lecture is devoted to understanding how the circuit works
- The two primary current-voltage characteristics of the MOSFET are the transconductance characteristic and the output characteristic
- The simple Sah large signal model is good enough for most applications and technology
- The Sah model can be improved in the region of the knee and for the weak dependence of drain current on drain-source voltage in the saturation region
- Most designers do not work at minimum channel length because of the channel length modulation effect and because worse matching occurs for small areas
- The threshold voltage is increased as the bulk-source is reverse biased
- The subthreshold model accounts for very small currents that flow in the channel when the gate-source voltage is smaller than the threshold voltage
- The subthreshold current is exponentially related to the gate-source voltage
- Velocity saturation occurs at minimum channel length and can be modeled by including a source degeneration resistor with the simple large signal model

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