LECTURE 08 – LATCHUP AND ESD

LECTURE ORGANIZATION

Outline

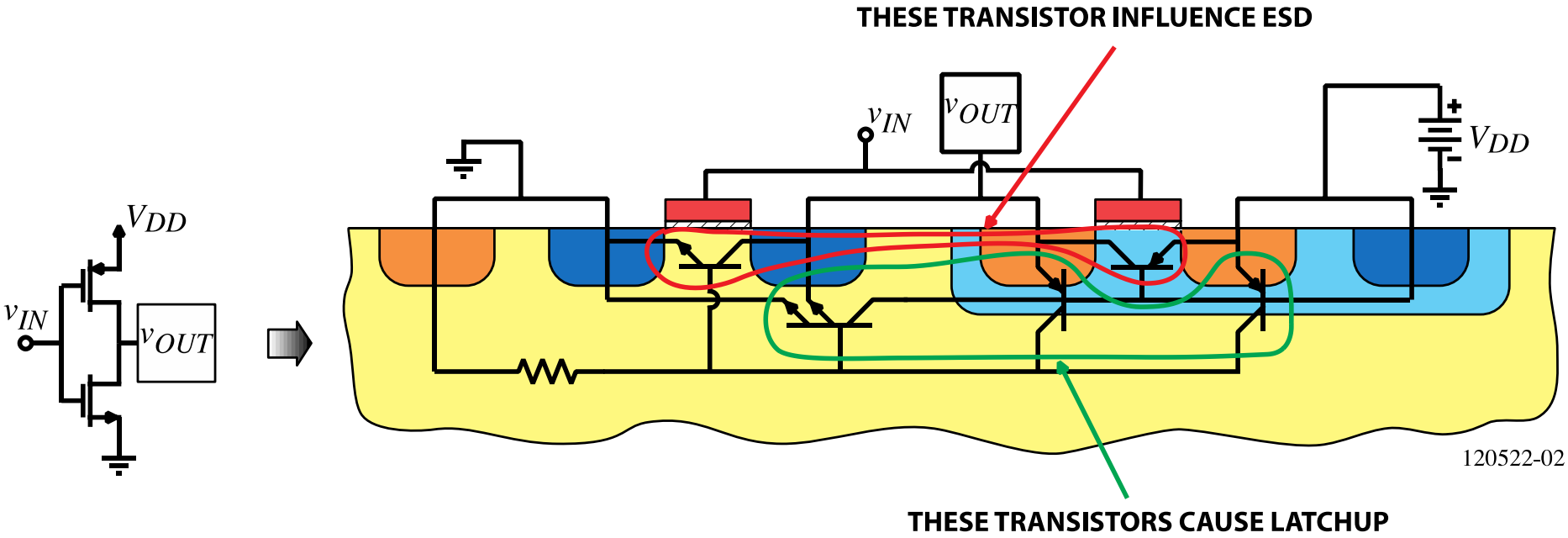
- MOSFET parasitic BJTs
- Latchup
- ESD
- Summary

***CMOS Analog Circuit Design*, 3rd Edition Reference**

Pages 53 - 60 and new material

MOSFET PARASITIC BJTS

Parasitic BJTs of a MOSFET

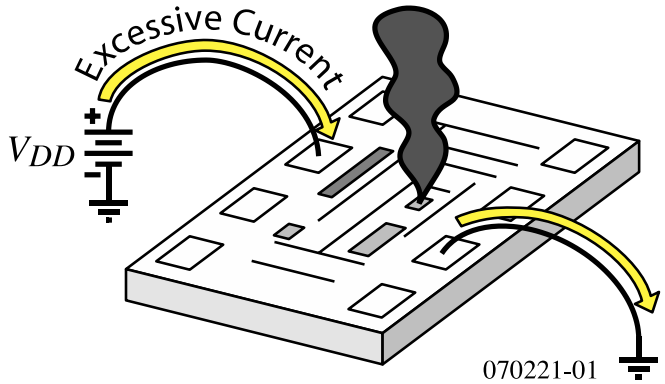


Furthermore, the resistance from the bases of the NPN transistors and collectors of the PNP transistor greatly influences both latchup and ESD. Thus, both latchup and ESD are influenced by layout.

LATCHUP

What is Latchup?

- Latchup is the creation of a low impedance path between the power supply rails.
- Latchup is caused by the triggering of parasitic bipolar structures within an integrated circuit when applying a current or voltage stimulus on an input, output, or I/O pin or by an over-voltage on the power supply pin.



- Temporary versus true latchup:

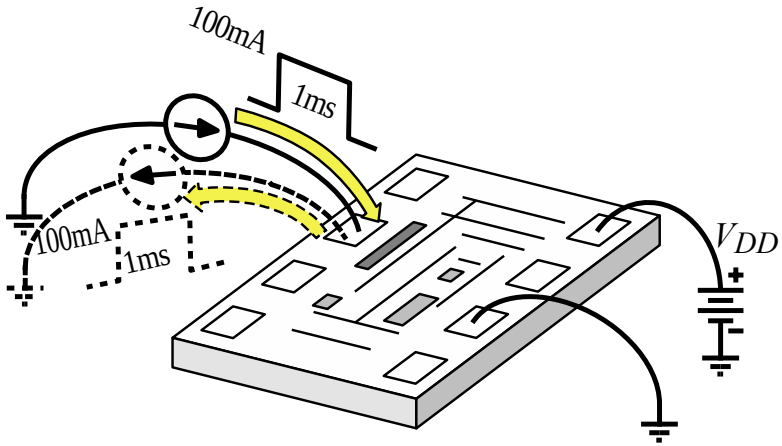
  A temporary or transient latchup occurs only while the pulse stimulus is connected to the integrated circuit and returns to normal levels once the stimulus is removed.

  A true latchup remains after the stimulus has been removed and requires a power supply shut down to remove the low impedance path between the power supply rails.

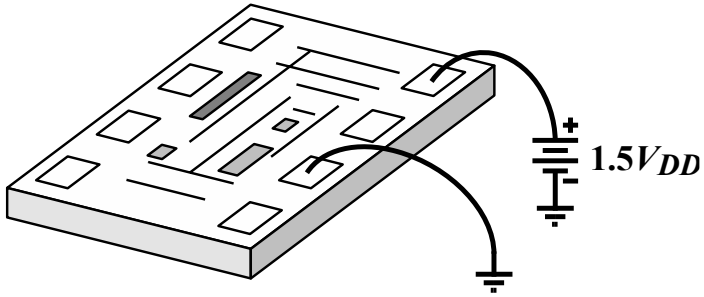
Latchup Testing

The test for latchup defines how the designer must think about latchup.

- For latchup prevention, you must consider where a current limited (≥100mA), 10ms pulse is going to go when applied to a pad when the voltage compliance of the pad is constrained to 50% above maximum power supply and to 2V below ground. (Higher temperatures, 85C°and 125°C, are more demanding, since V_{BE} is lower.)
- V_{DD} is increased by 150% (must be careful for low voltage ICs)



CURRENT INJECTION

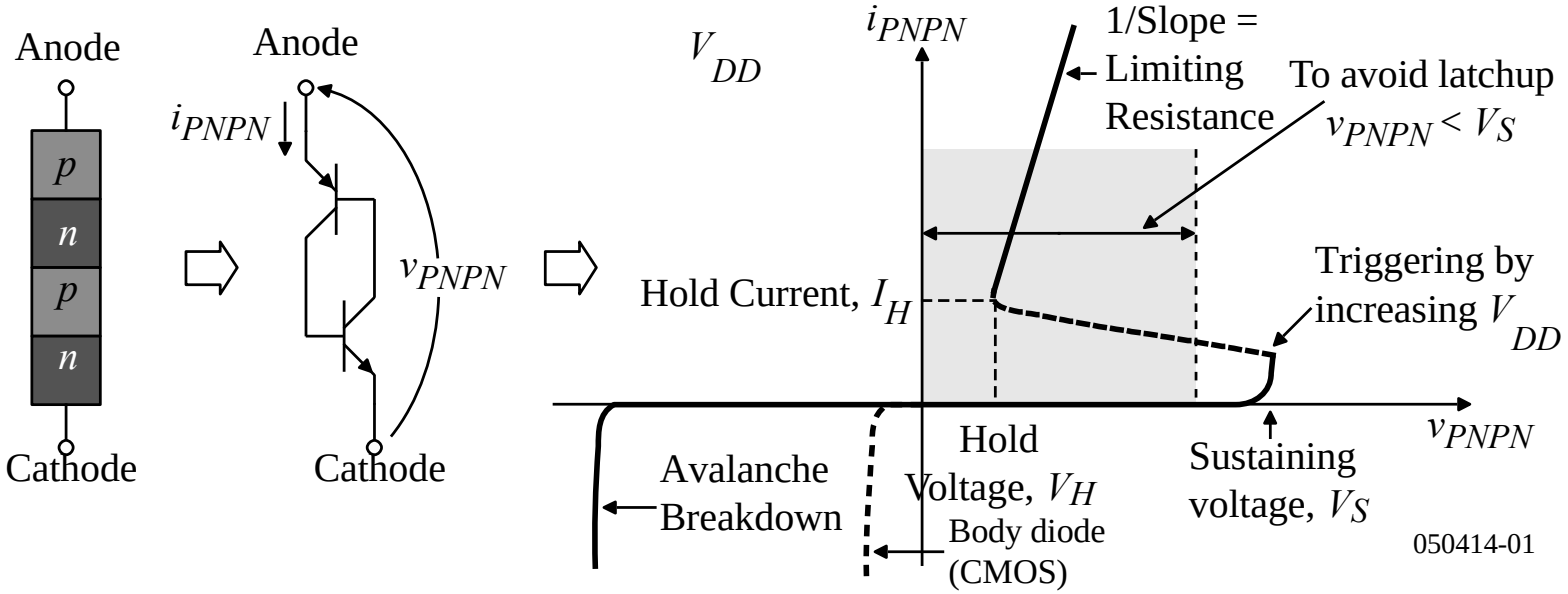


150% OVERVOLTAGE 130620-01

- Latchup is sensitive to layout and is most often solved at the physical layout level.

How Does Latchup Occur?

Latchup is the regenerative process that can occur in a *pnpn* structure (SCR-silicon controlled rectifier) formed by a parasitic *npn* and a parasitic *pnp* transistor.



Important concepts:

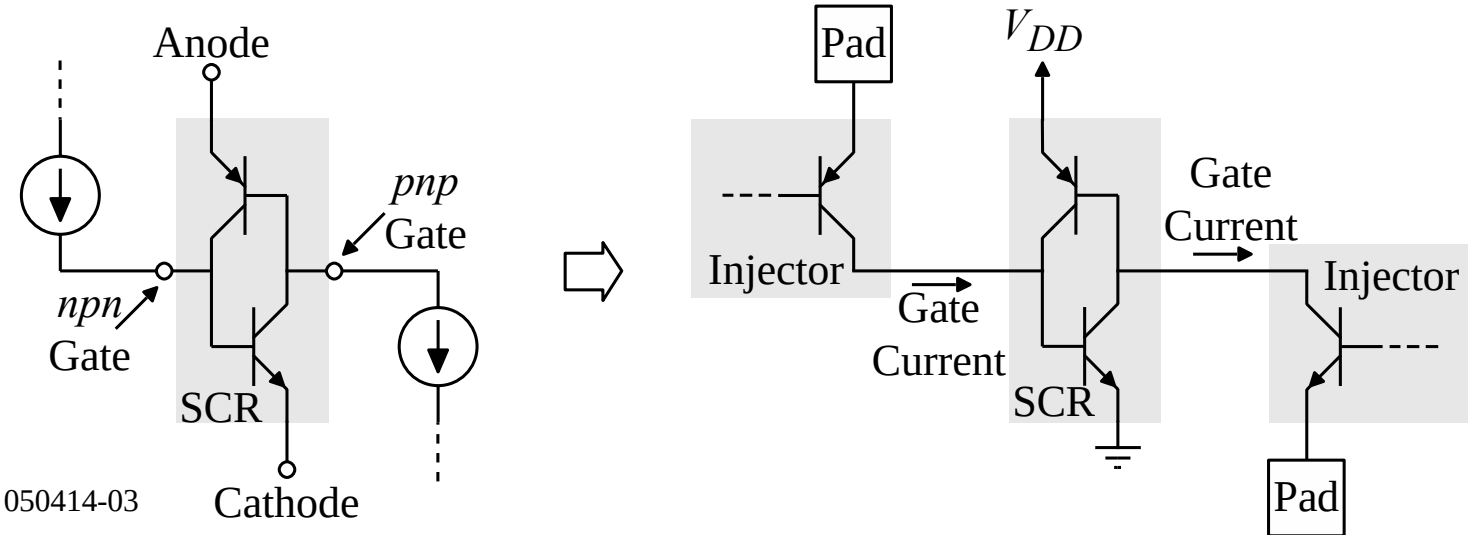
- To avoid latchup, $v_{PNPN} \leq V_S$
- Once the *pnpn* structure has latched up, the large current required by the above *i-v* characteristics must be provided externally to sustain latchup
- To remove latchup, the current must be reduced below the holding current

Latchup Triggering

Latchup of the SCR can be triggered by two different mechanisms.

1.) Allowing v_{PNPN} to exceed the sustaining voltage, V_S.

2.) Injection of current by a triggering device (gate triggered)



Note: The gates mentioned above are SCR junction gates, not MOSFET gates.

From the above considerations, latchup requires the following components:

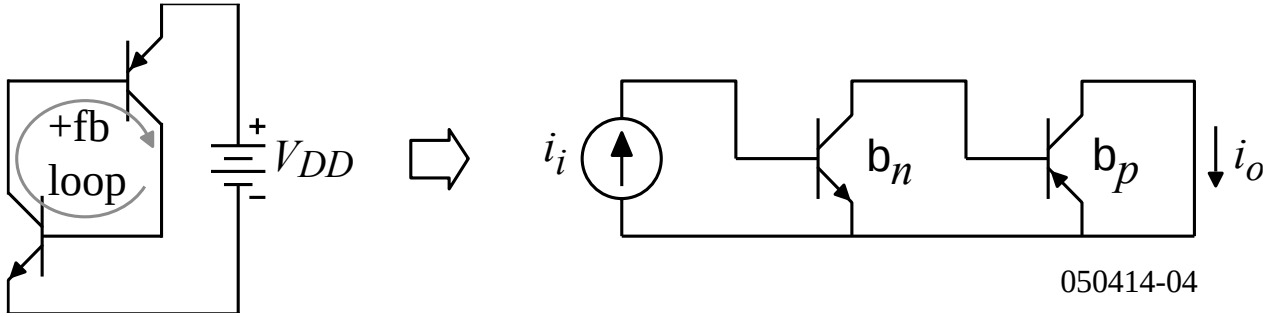
1.) A four-layer structure (SCR) connected between V_{DD} and ground.

2.) An injector.

3.) A stimulus.

Necessary Conditions for Latchup

1.) The loop gain of the relevant BJT configuration must exceed unity.



Loop gain:

$$\frac{i_o}{i_i} \approx \beta_p \beta_n$$

2.) A bias condition must exist such that both bipolars are turned on long enough for current through the "SCR" to exceed its switching current.

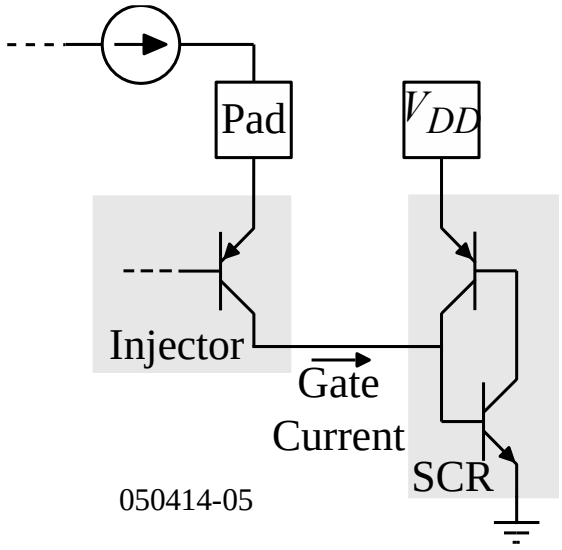
3.) The bias supply and associated circuits must be capable of supplying the current at least equal to the switching current and at least equal to the holding current to maintain the latched state.

Latchup Trigger Modes

Current mode (Positive Injection Example):

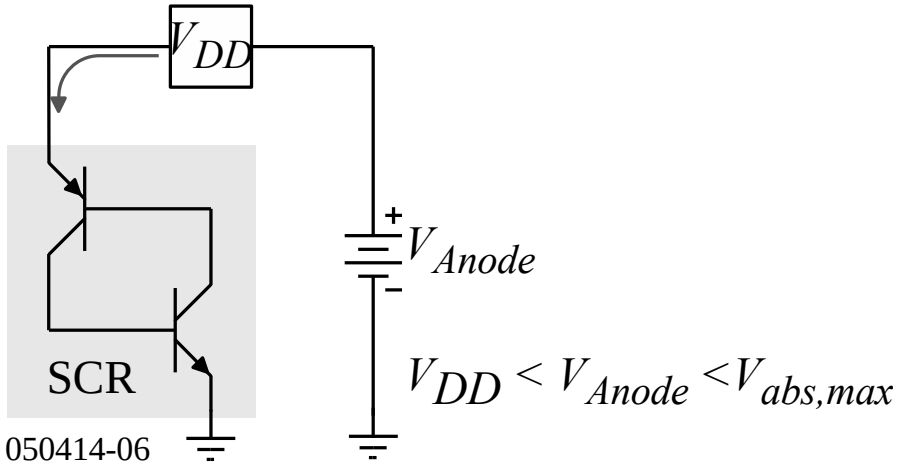
When a current is applied to a pad, it can flow through an injector and trigger latchup of an SCR formed from parasitic bipolar transistors.

SCR gate current injection parasitic can occur in *p*-well or *n*-well technology.



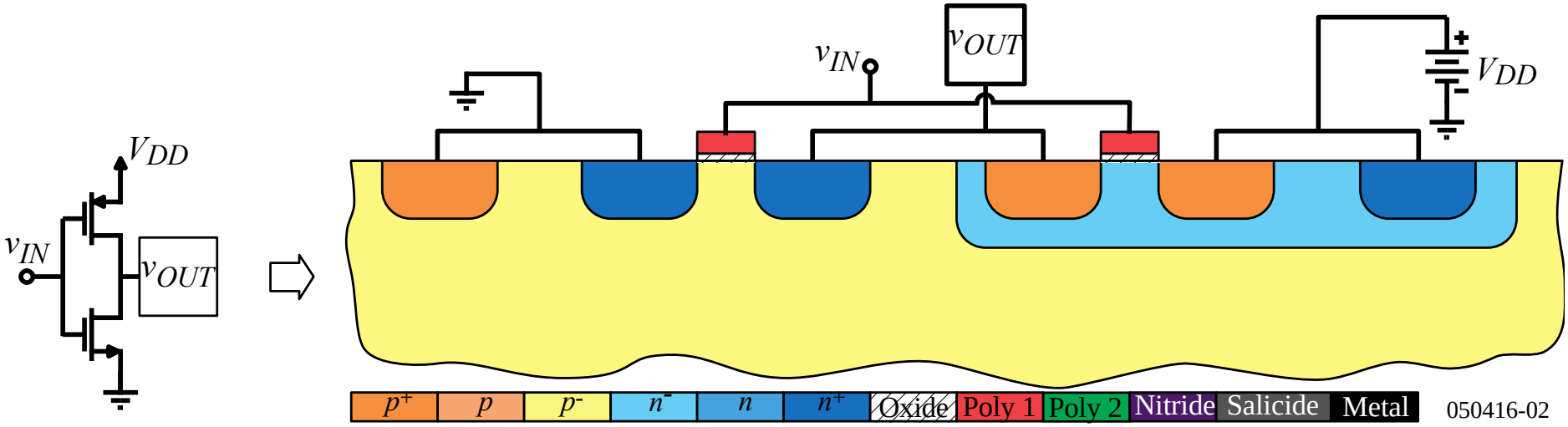
Voltage mode:

When the power supply is increased above the nominal value, the SCR formed from parasitic bipolar transistors can be triggered.



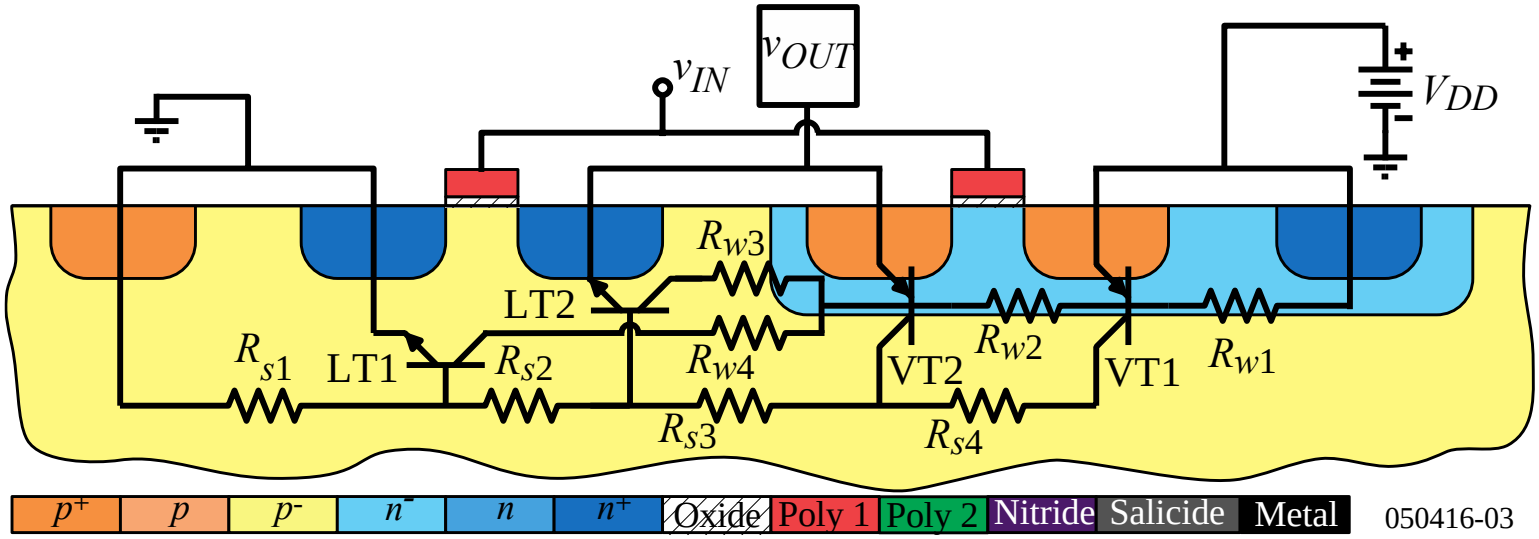
How does Latchup Occur in an IC?

Consider an output driver in CMOS technology:



Assume that the output is connected to a pad.

Parasitic Bipolar Transistors for the n-well CMOS Inverter

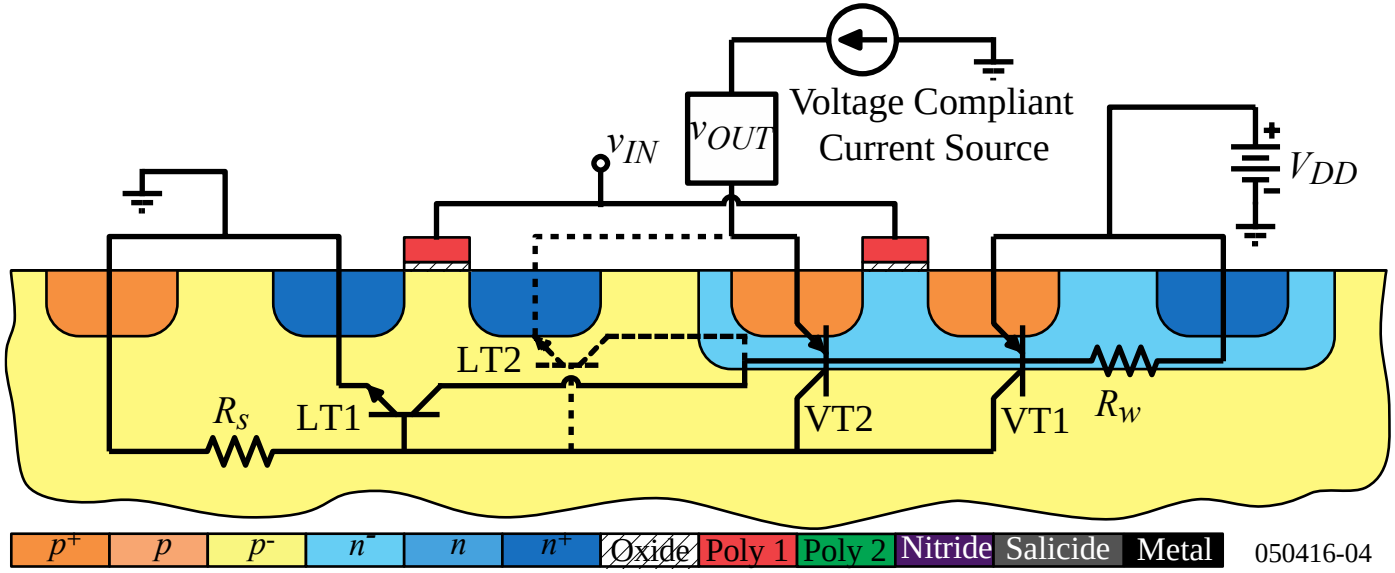


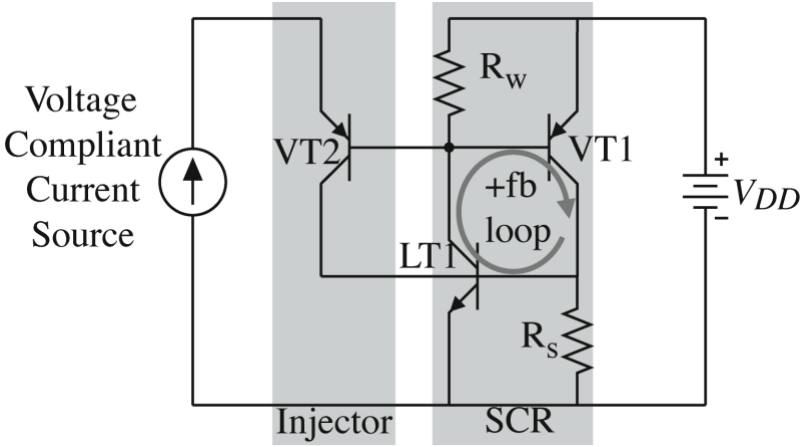
Parasitic components:

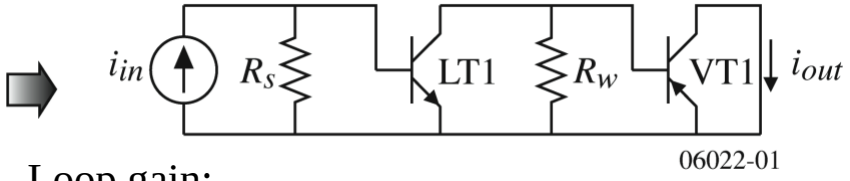
- Lateral BJTs LT1 and LT2
- Vertical BJTs VT1 and VT2
- Bulk substrate resistances R_{s1}, R_{s2}, R_{s3}, and R_{s4}
- Bulk well resistances R_{w1}, R_{w2}, R_{w3}, and R_{w4}

Current Source Injection

Apply a voltage compliant current source to the output pad ($v_{OUT} > V_{DD}$).







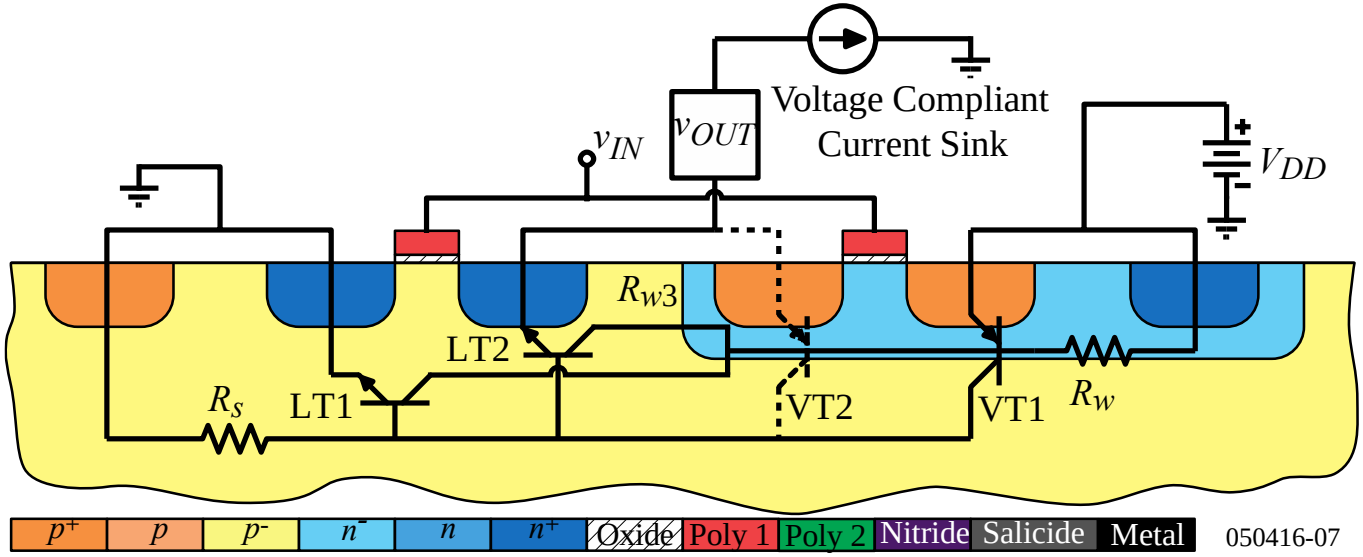
Loop gain:

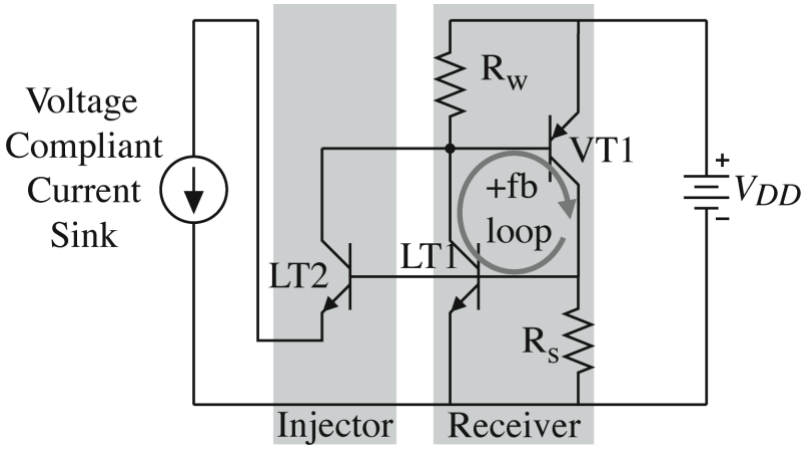
$$\frac{i_{out}}{i_{in}} = \beta_{P1}\left(\frac{R_W}{R_W + r_{\pi P1}}\right)\beta_{N1}\left(\frac{R_S}{R_S + r_{\pi N1}}\right)$$

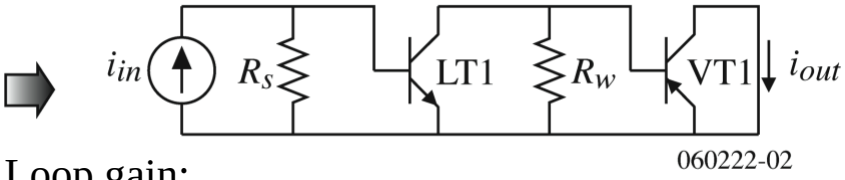
$$= \beta_{P1}\beta_{N1}\left(\frac{R_W}{R_W + \frac{\beta_{P1}V_t}{I_{P1}}}\right)\left(\frac{R_S}{R_S + \frac{\beta_{N1}V_t}{I_{P2}}}\right)$$

Current Sink Injection

Apply a voltage compliant current sink to the output pad ($v_{OUT} < 0$).







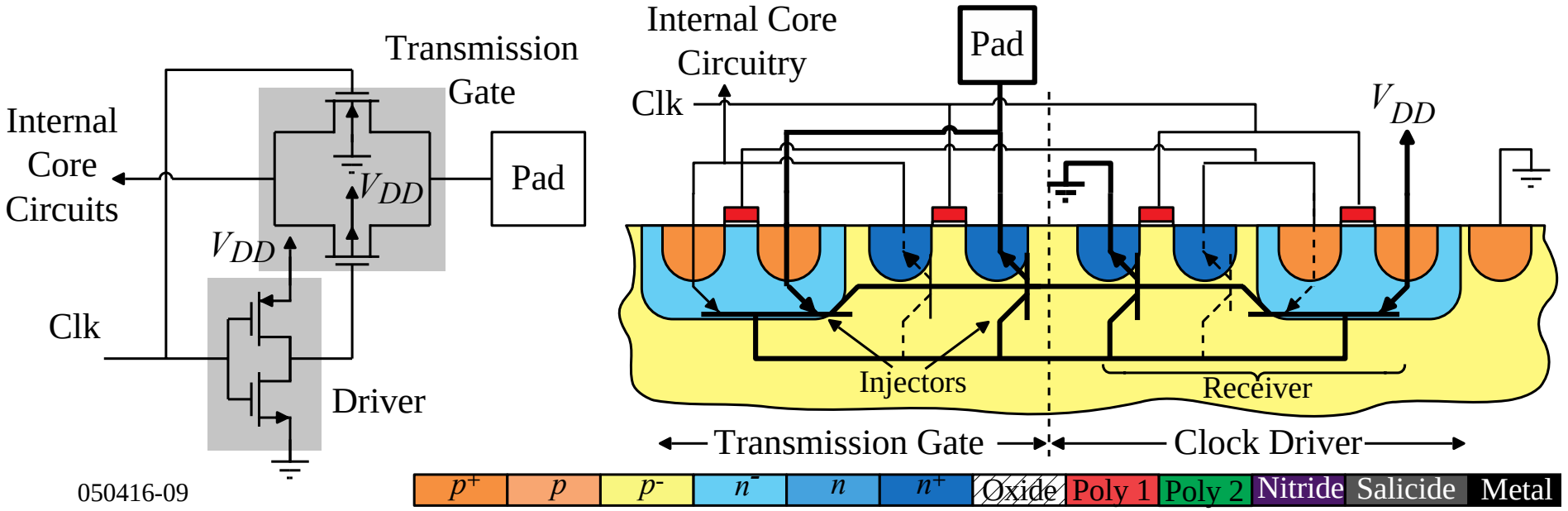
Loop gain:

$$\frac{i_{out}}{i_{in}} = \beta_{P1}\left(\frac{R_w}{R_w + r_{\pi P1}}\right)\beta_{N1}\left(\frac{R_s}{R_s + r_{\pi N1}}\right)$$

$$= \beta_{P1}\beta_{N1}\left(\frac{R_w}{R_w + \frac{\beta_{P1}V_t}{I_{P1}}}\right)\left(\frac{R_s}{R_s + \frac{\beta_{N1}V_t}{I_{P2}}}\right)$$

Latchup from a Transmission Gate

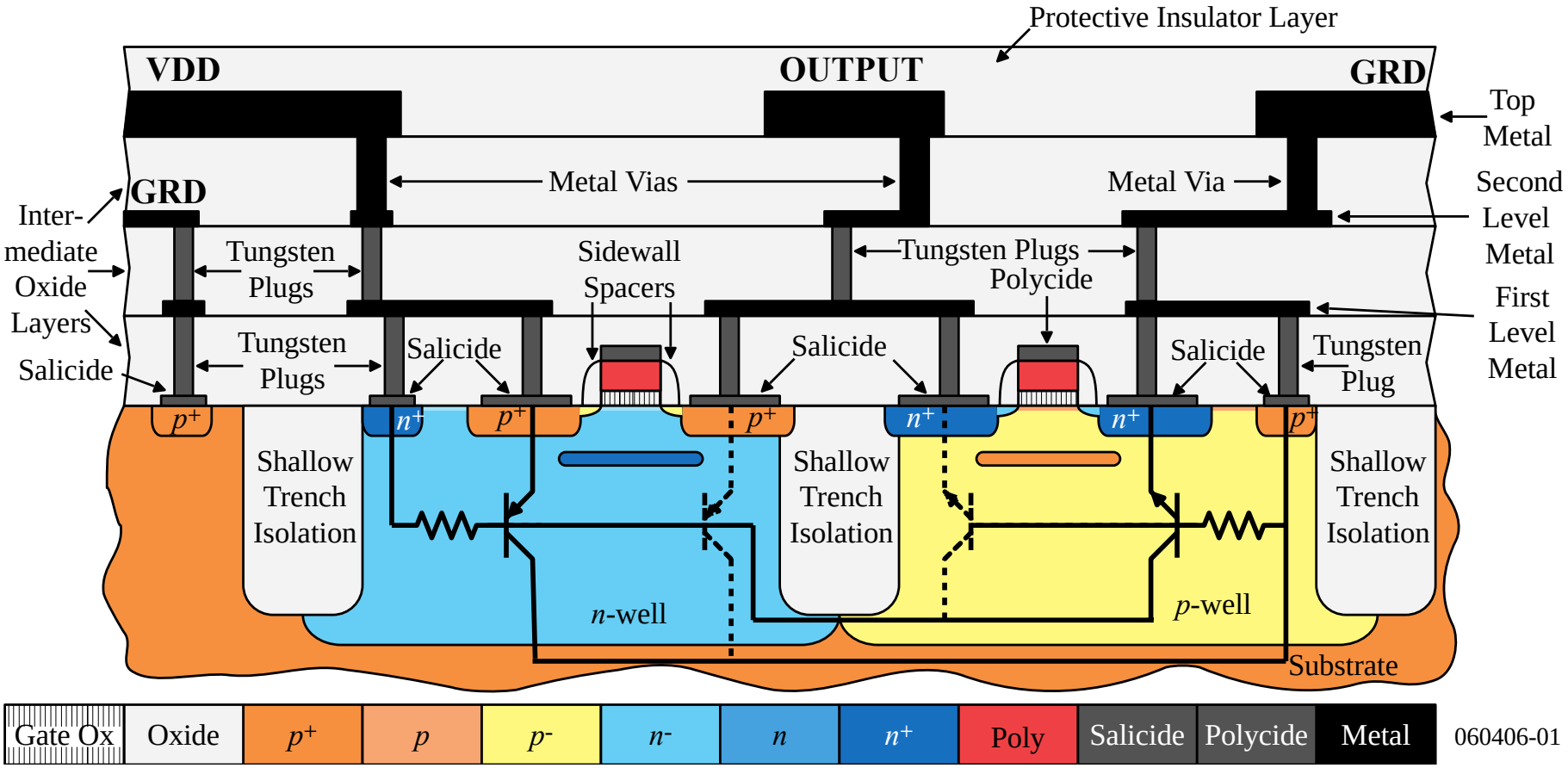
The classical push-pull output stage is only one of the many configurations that can lead to latchup. Here is another configuration:



The two bold solid bipolar transistors in the transmission gate act as injectors to the *npn-pnp* parasitic bipolars of the clock driver and cause these transistors to latchup. The injector sites are the diffusions connected to the pad.

The Influence of Shallow Trench Isolation on Latchup

As seen below, the STI causes the parasitic betas to be smaller and slightly reduces the sensitivity to latchup.

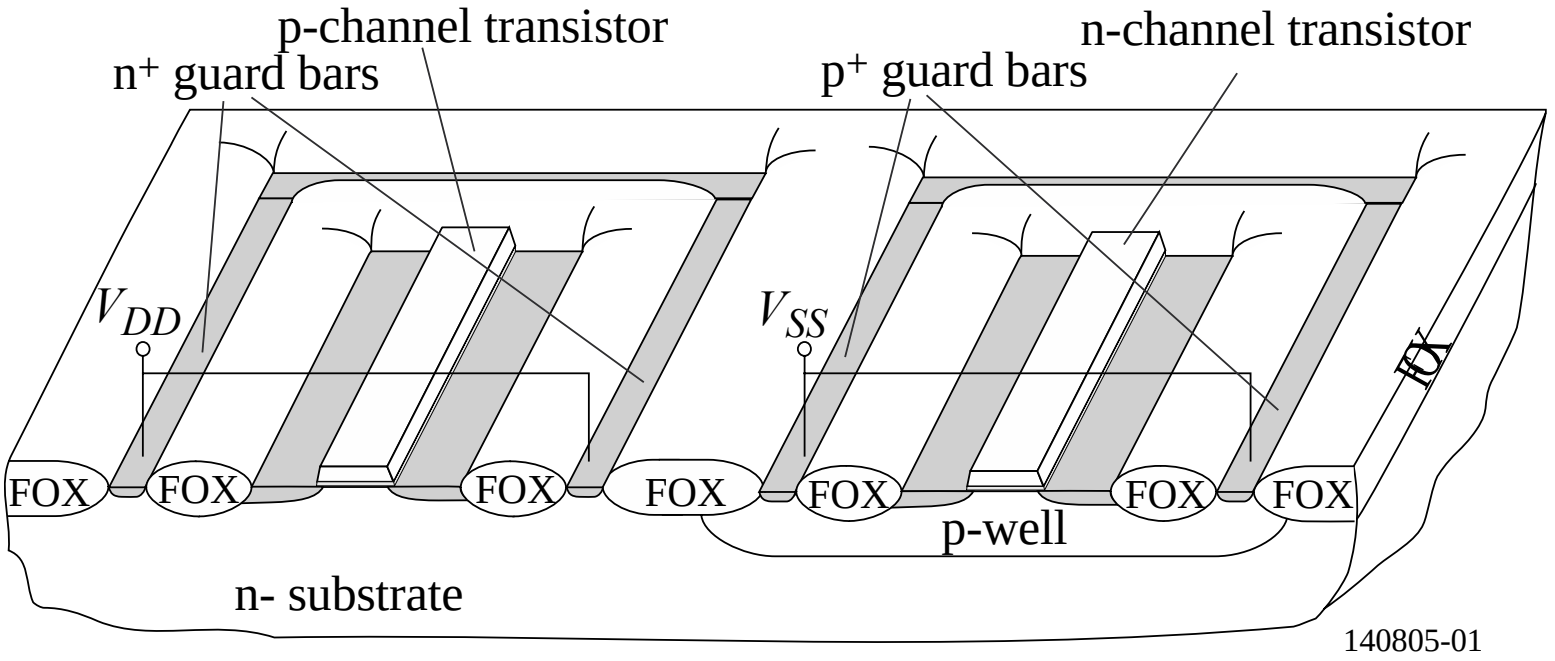


Preventing Latch-Up

1.) Keep the source/drain of the MOS device not in the well as far away from the well as possible. This will lower the value of the BJT betas.

2.) Reduce the values of $R_{N\text{-}}$ and $R_{P\text{-}}$. This requires more current before latch-up can occur.

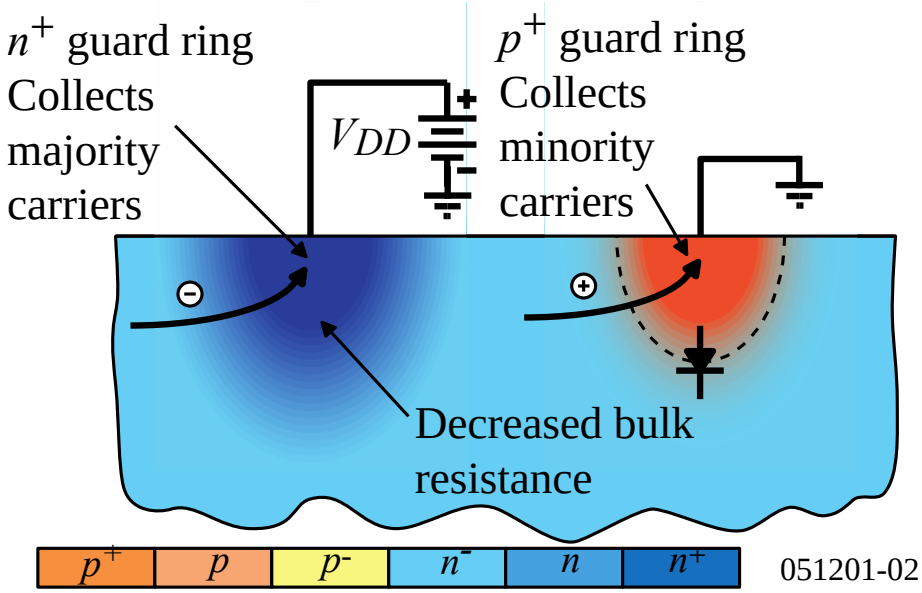
3.) Surround the transistors with guard rings. Guard rings reduce transistor betas and divert collector current from the base of SCR transistors.



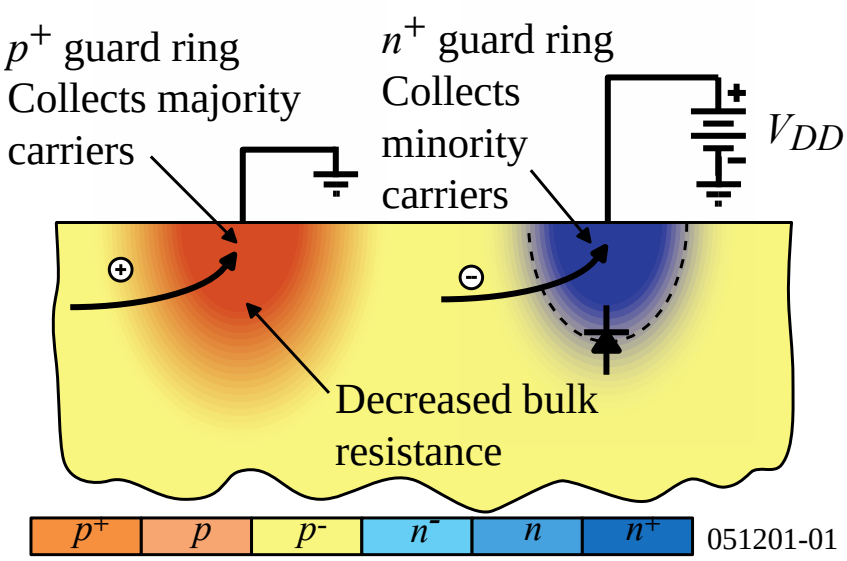
What are Guard Rings?

Guard rings are used to collect carriers flowing in the silicon. They can be designed to collect either majority or minority carriers.

Guard rings in *n*-material:



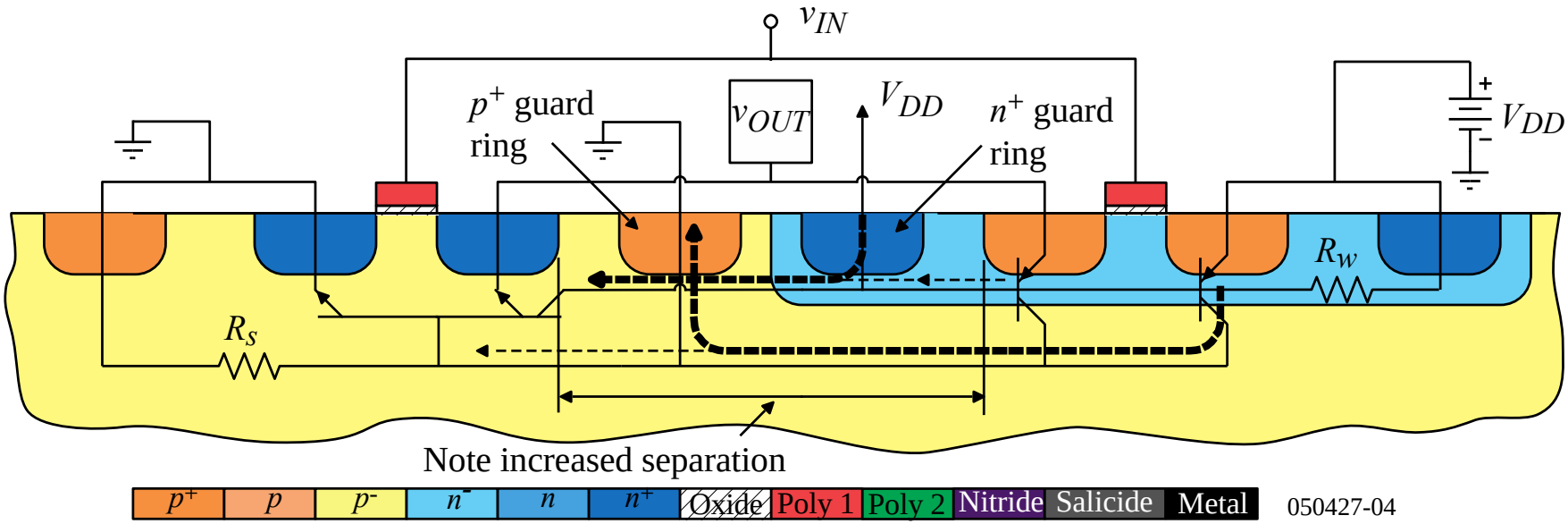
Guard rings in *p*-material:



Also, the increased doping level of the n^+ (p^+)guard ring in n (p) material decreases the resistance in the area of the guard ring.

Example of Reducing the Sensitivity to Latchup by using Guard Rings

Start with placing guard rings around the NMOS and PMOS transistors (both I/O and logic) to collect most of the parasitic NPN and PNP currents locally and prevent turn-on of adjacent devices.

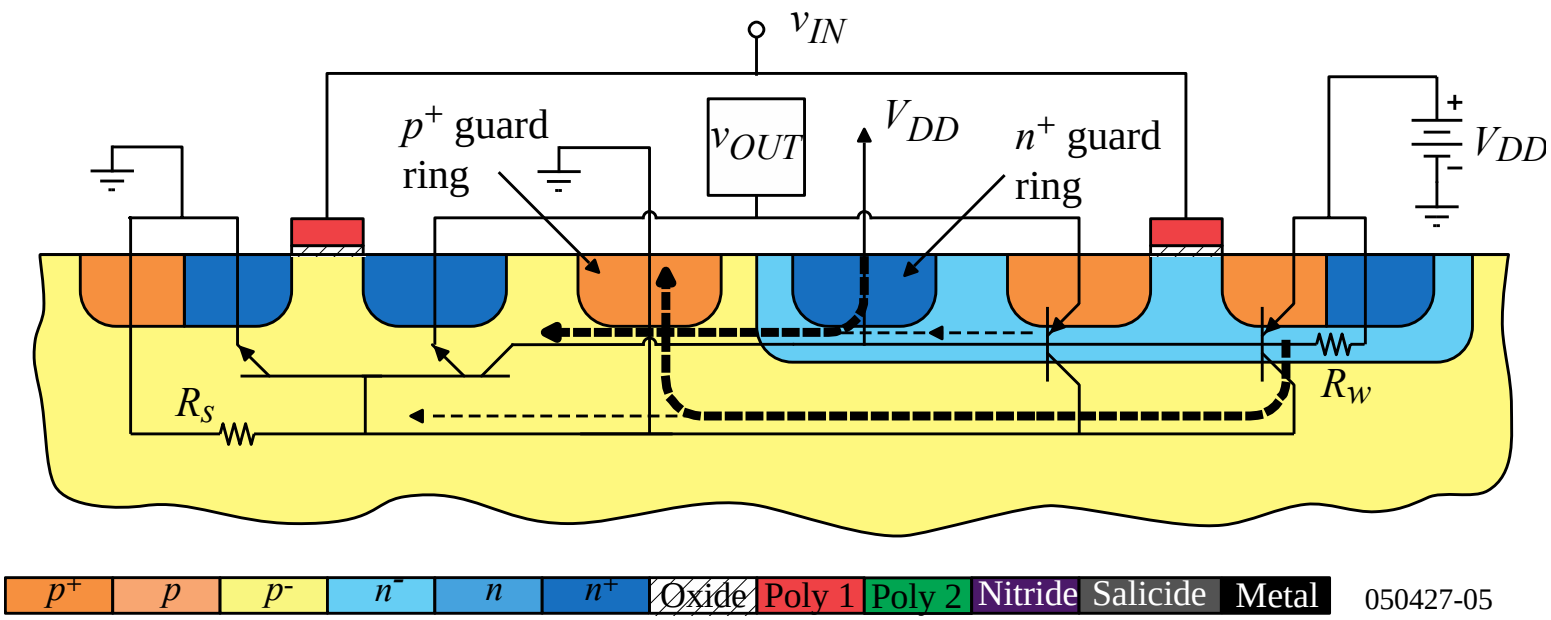


- The guard rings also help to reduce the effective well and substrate resistance.
- The guard rings reduce the lateral beta

Key: The guard rings should act like collectors

Example of Reducing the Sensitivity to Latchup by using Butted Contacts

Finally, use butted source contacts to further reduce the well resistance and reduce the substrate resistance.



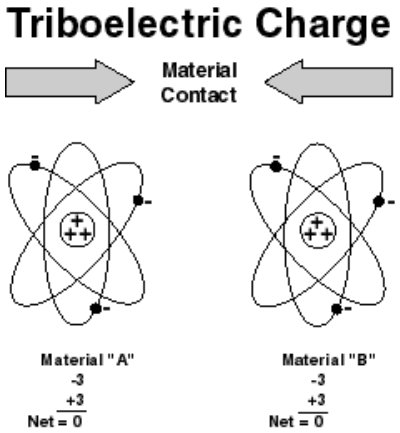
Guidelines for Guard Rings

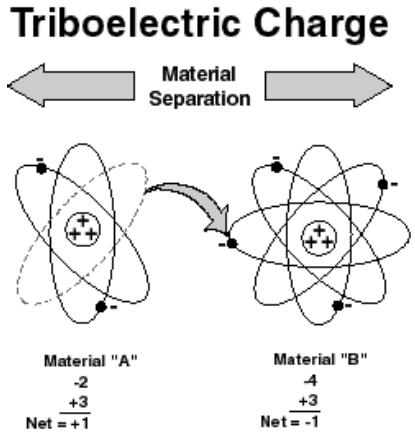
- Guard rings should be low resistance paths.
- Guard rings should utilize continuous diffusion areas.
- More than one transistor of the same type can be placed inside the same well inside the same guard ring as long as the design rules for spacing are followed.
- Only 2 guard rings are required between adjacent PMOS and NMOS transistors
- The well taps and/or the guard ring should be laid out as close to the MOSFET source as possible.
- I/O output NMOSFET should use butted composite for source to bulk connections when the source is electrically connected to the *p*-well tap. If separate well tap and source connections are required due to substrate noise injection problems, minimize the source-well tap spacing. This will minimize latch up and early snapback of the output MOSFETs with the drain diffusion tied directly (in metal) to the bond pad.

ESD IN CMOS TECHNOLOGY

What is Electrostatic Discharge?

Triboelectric charging happens when 2 materials come in contact and then are separated.

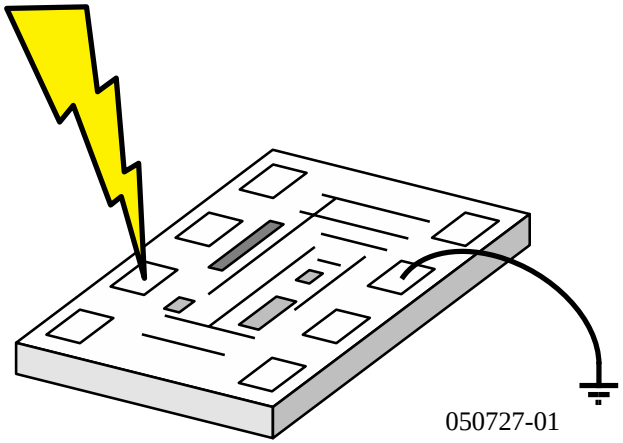




An ESD event occurs when the stored charge is discharged.

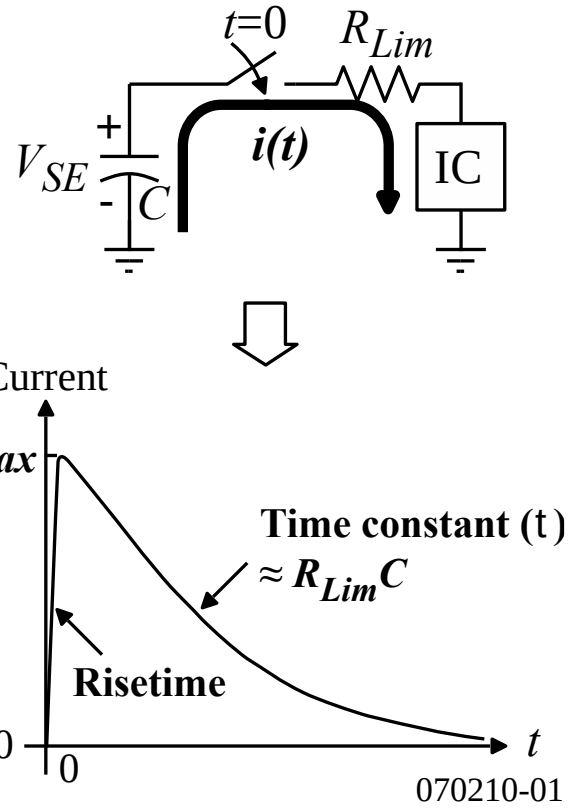
ESD and Integrated Circuits

- ICs consist of components that are very sensitive to excess current and voltage above the nominal power supply.
- Any path to the outside world is susceptible to ESD
- ESD damage can occur at any point in the IC assembly and packaging, the packaged part handling or the system assembly process.
- Note that power is normally not on during an ESD event



ESD Models and Standards

- Standard tests give an indication of the ICs robustness to withstand ESD stress.
- Increased robustness:
  - Reduces field failures due to ESD
  - Demanded by customers
- Simple ESD model:
  - V_{SE} = Charging Voltage
  - Key parameters of the model:
    - Maximum current flow
    - Time constant or how fast the ESD event discharges
    - Risetime of the pulse

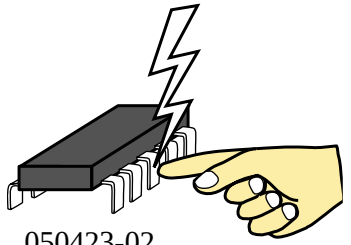


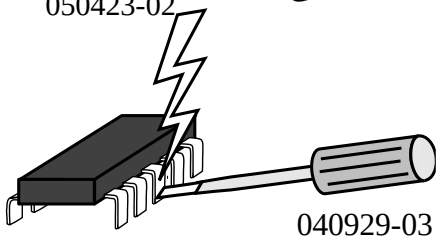
ESD Models

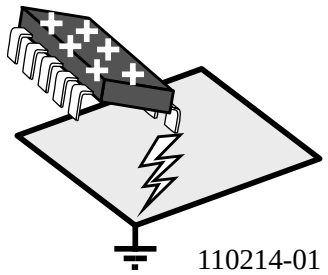
- Human body model (HBM): Representative of an ESD event between a human and an electronic component.

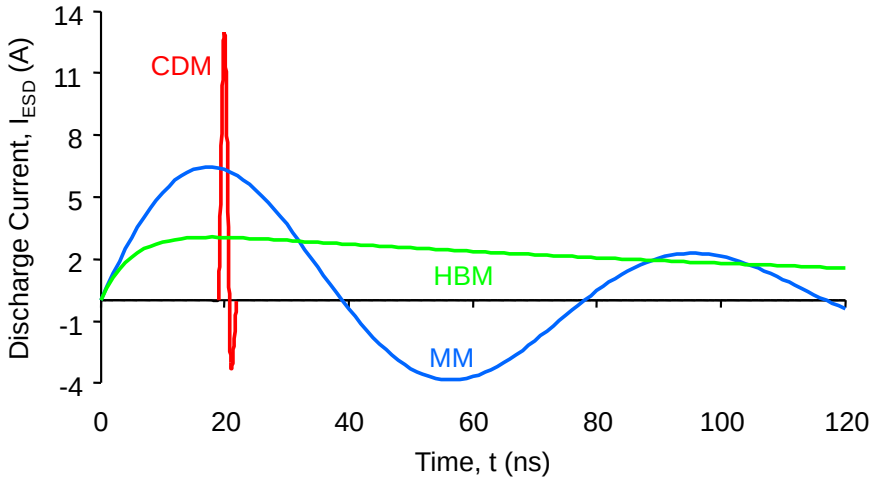
- Machine model (MM): Simulates the ESD event when a charged "machine" discharges through a component.

- Charge device model (CDM): Simulates the ESD event when the component is charged and then discharges through a pin. The substrate of the chip becomes charged and discharges through a pin.









ESD Influence on Components

An ESD event typically creates very high values of current (1-10A) for very short periods of time (150 ns) with very rapid rise times (1ns).

Therefore, components experience extremely high values of current with very little power dissipation or thermal effects.

Resistors – become nonlinear at high currents and will breakdown

Capacitors – become shorts and can breakdown from overvoltage (pad to substrate)

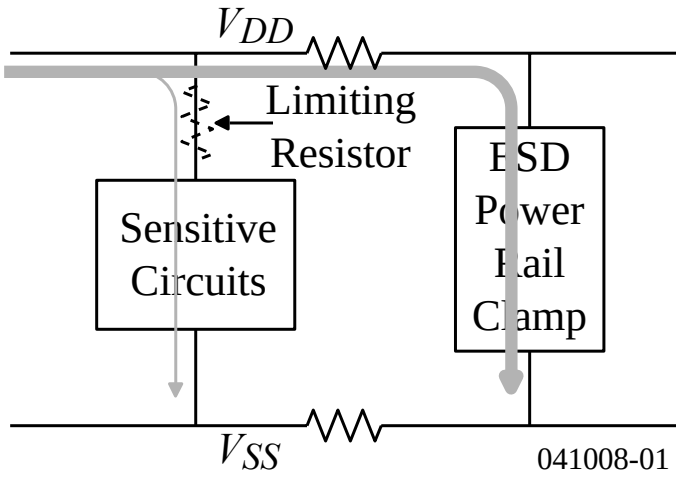
Diodes – current no longer flows uniformly (the connections to the diodes represent the ohmic resistance limit)

Transistors – ESD event is only a two terminal event, the third terminal is influenced by parasitics and many of the transistor parameters are poorly controlled.

- MOSFETs – the parasitic bipolar experiences snapback under an ESD event
- BJTs – will experience snapback under ESD event

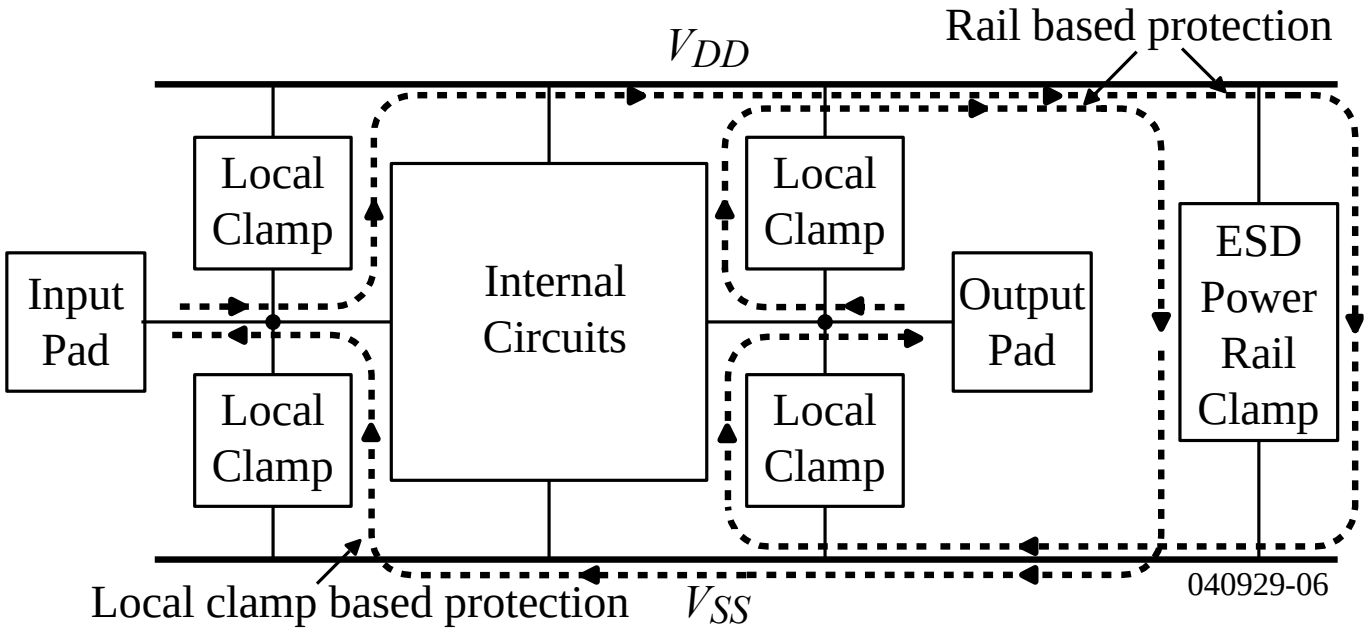
Objective of ESD Protection

- There must be a safe low impedance path between every combination of pins to sink the ESD current (i.e. 1.5A for 2kV HBM)
- The ESD device should clamp the voltage below the breakdown voltage of the internal circuitry
- The metal busses must be designed to survive 1.5A (fast transient) without building up excessive voltage drop
- ESD current must be steered away from sensitive circuits



- ESD protection will require area on the chip (busses and timing components)

ESD Protection Architecture



Local clamps – Conducts ESD current without loading the internal (core) circuits

ESD power rail clamps – Conducts a large amount of current with a small voltage drop

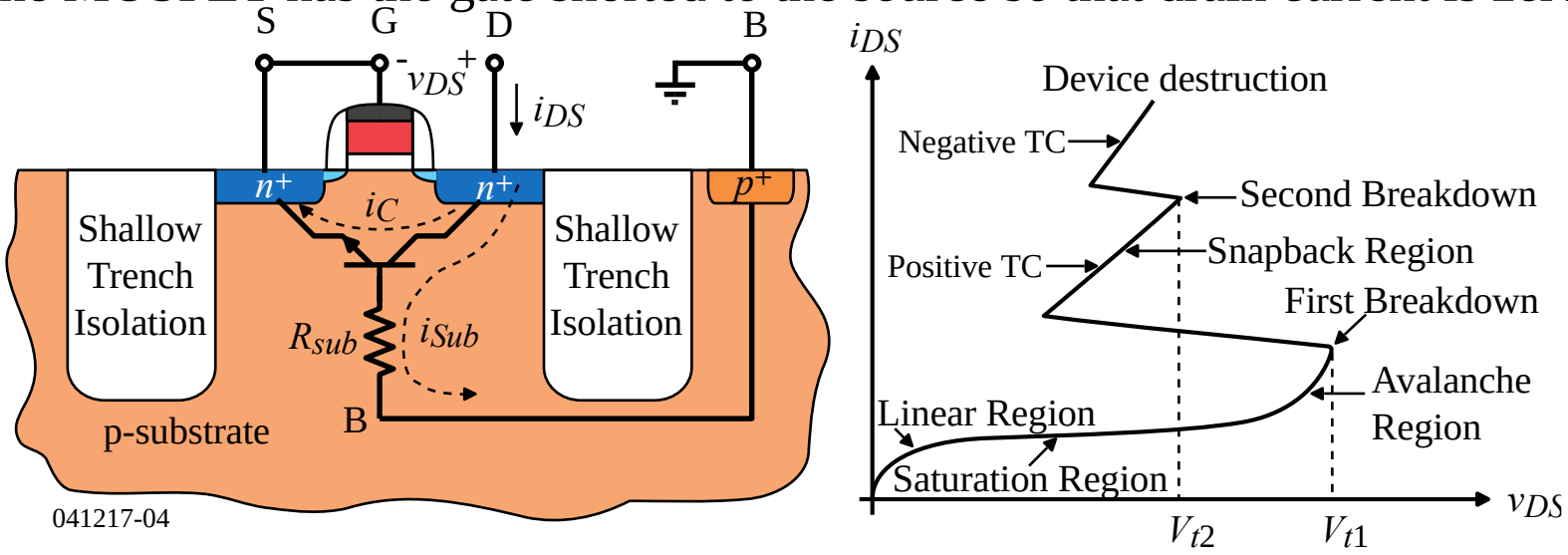
ESD Events:

Pad-to-rail (uses local clamps only)

Pad-to-pad (uses either local or local and ESD power rail clamps)

Example of an ESD Breakdown Clamp

A normal MOSFET that uses the parasitic lateral BJT to achieve a snapback clamp. Normally, the MOSFET has the gate shorted to the source so that drain current is zero.



Operation:

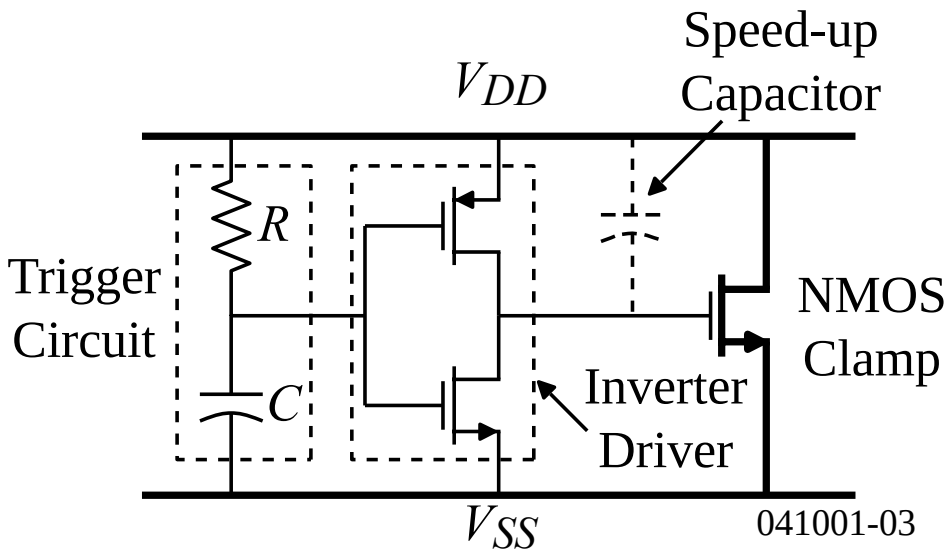
- Impact ionization at drain edge generates a substrate current
- Substrate current causes the transistor to turn on creating current from the emitter and "snapping back" from a BV_{CES} to BV_{CER} characteristic

Issues:

- If the drain voltage becomes too large, the gate oxide may breakdown
- The current should be distributed evenly among multiple fingers
- The SCR discussed previously makes an excellent breakdown clamp

Example of a Non-Breakdown Clamp

NMOS Clamp:



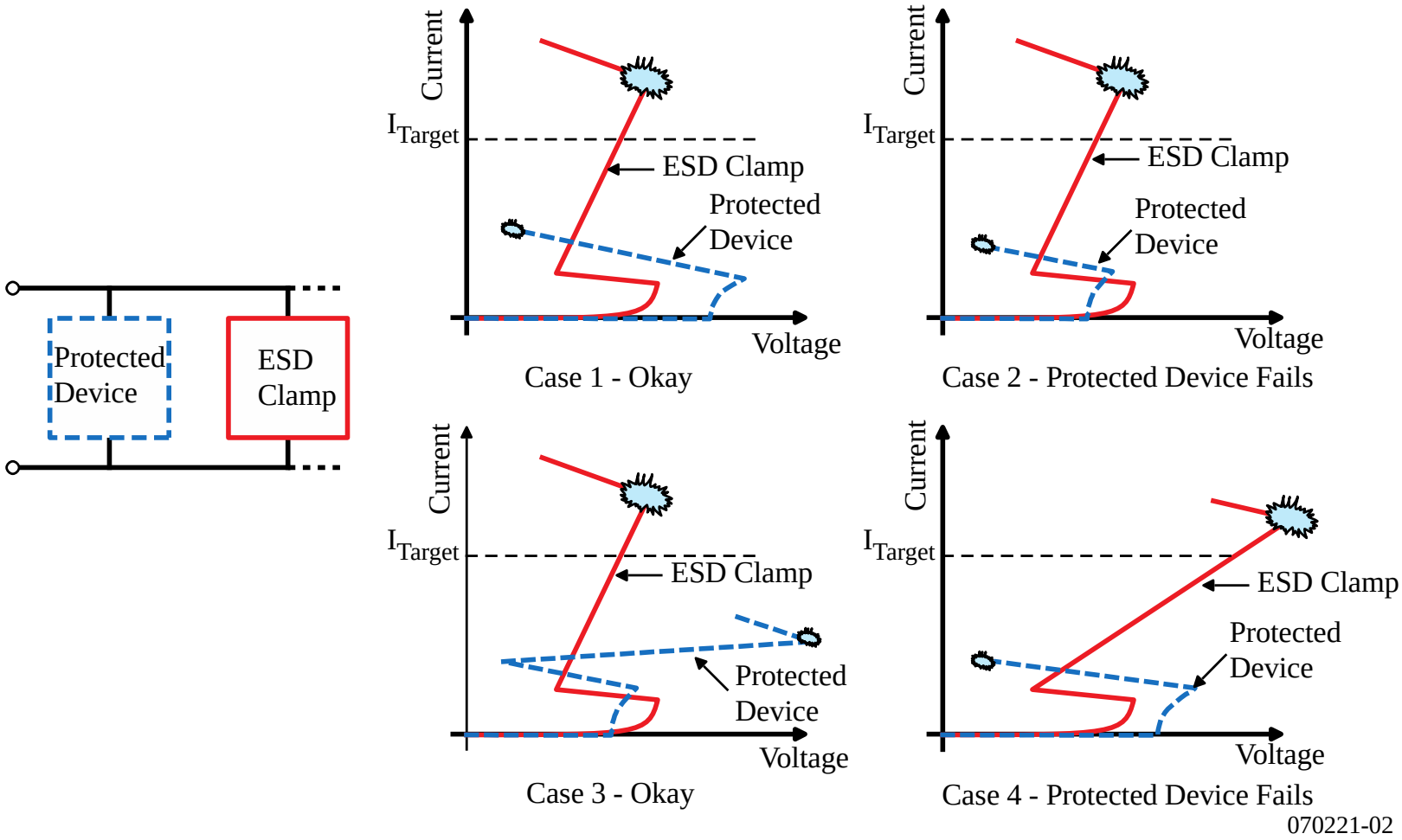
Operation:

- Normally, the input to the driver is high, the output low and the NMOS clamp off
- For a positive ESD event, the voltage increases across *R* causing the inverter to turn on the NMOS clamp providing a low impedance path between the rails
- Cannot be used for pads that go above power supply or are active when powered up
- For power supply turn-on, the circuit should not trigger (*C* holds the clamp off during turn-on)

Also, forward biased diodes serve as non-breakdown clamps.

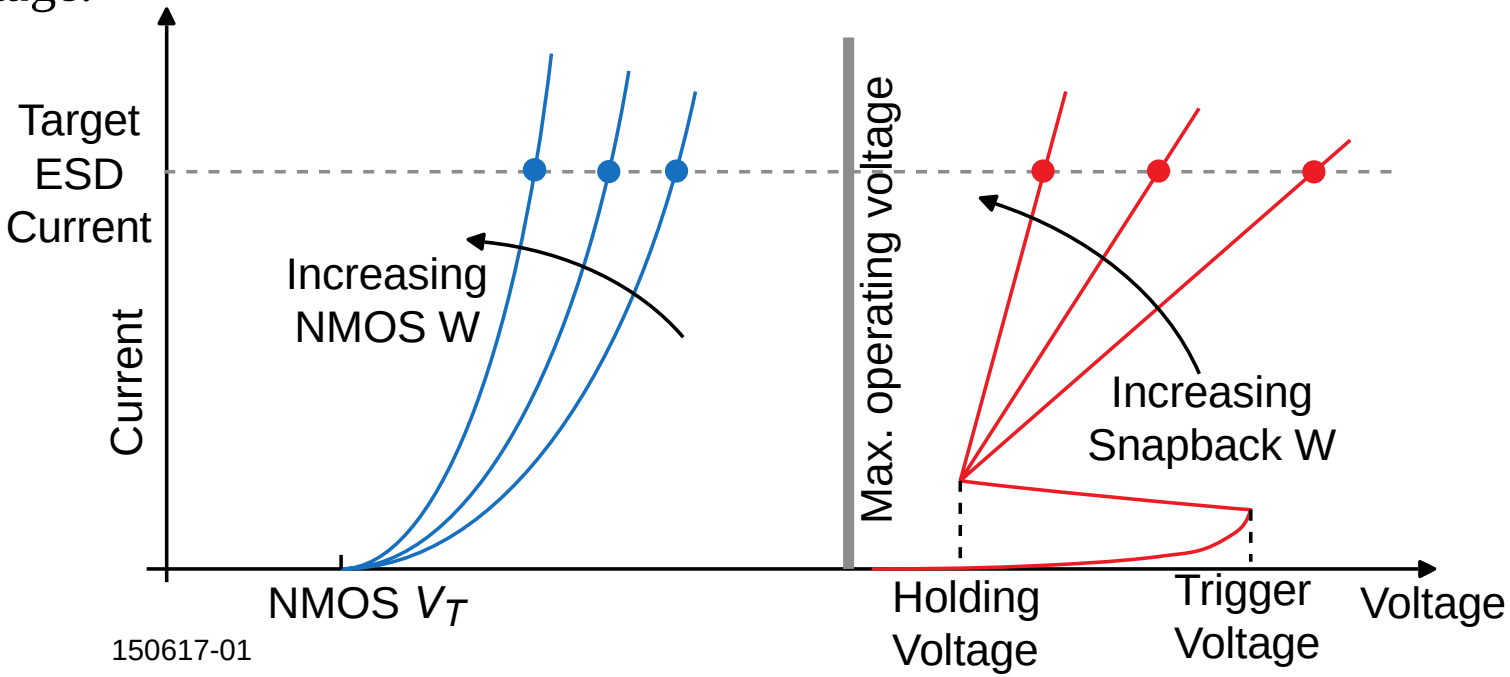
IV Characteristics of Good ESD Protection

Goal: Sink the ESD current and clamp the voltage.



Comparison Between the NMOS Clamp and the Snapback Clamp

Increasing the width of either the active or snapback NMOS clamp will reduce the clamp voltage.



Note that the NMOS clamp does not normally exceed the absolute maximum voltage. NMOS clamps should be used with EPROMs to avoid reprogramming during an ESD event.

ESD Practice

General Guidelines:

- Understand the current flow requirements for an ESD event
- Make sure the current flows where desired and is uniformly distributed
- Series resistance is used to limit the current in the protected devices
- Minimize the resistance in protecting devices
- Use distributed (smaller) active clamps to minimize the effect of bus resistance
- Understand the influence of packaging on ESD
- Use guard rings to prevent latchup

Check list:

- Check the ESD path between every pair of pads
- Check for ESD protection between the pad and internal circuitry
- Check for low bus resistance
  - Current: Minimum metal for ESD ≈ 40 x Electromigration limit
  - Voltage: 1.5A in a metal bus of 0.03Ω/square of 1000μm long and 30μm wide gives a voltage drop of 1.5V
- Check for sufficient contacts and vias in the ESD path (uniform current distribution)

SUMMARY

- Latchup is a low impedance path between V_{DD} and ground causing excessive current.
- The conditions for latchup are:
  - A four-layer, *pnpn* structure connected between power supply rails
  - An injector (any diffusion connected to a pad)
  - A stimulus
- Latchup is prevented by:
  - Keeping the NMOS and PMOS transistors separated
  - Reducing the well resistance with appropriate well ties
  - Surrounding the transistors with guard rings
- ESD is caused by triboelectric charging which discharges through the IC
- The current produced by an ESD event must be controlled – uniform current flow, minimum voltage drop, and must not flow through sensitive circuitry
- An ESD event turns on very quickly (<1ns), has a high peak current (1A), and lasts for approximately 100 ns.
- ESD clamps consist of breakdown clamps (snapback) and non-breakdown clamps.
- A 16-lecture, on-line course on the Analog Design viewpoint of ESD can be found at

  http://www.udemy.com/esd-an-analog-design-viewpoint