LECTURE 07 – RESISTORS AND INDUCTORS

LECTURE ORGANIZATION

Outline
• Resistors
• Inductors
• Summary

CMOS Analog Circuit Design, 3rd Edition Reference
Pages 50-52, 652-654 and new material
RESISTORS

Types of Resistors Compatible with CMOS Technology

1.) Diffused and/or implanted resistors.
2.) Well resistors.
3.) Polysilicon resistors.
4.) Metal resistors.
Characterization of Resistors

1.) Value

\[ R = \frac{\rho L}{A} \]

AC and DC resistance

2.) Linearity

Does \( V = IR \)?

Velocity saturation of carriers

3.) Power

\[ P = VI = I^2R \]

4.) Current

Electromigration

5.) Parasitics
CMOS Resistors - Source/Drain Resistor

Diffusion:
10-100 ohms/square
Absolute accuracy = ±35%
Relative accuracy=2% (5µm), 0.2% (50µm)
Temperature coefficient = +1500 ppm/°C
Voltage coefficient ≈ 200 ppm/V

Ion Implanted:
500-2000 ohms/square
Absolute accuracy = ±15%
Relative accuracy=2% (5µm), 0.15% (50µm)
Temperature coefficient = +400 ppm/°C
Voltage coefficient ≈ 800 ppm/V

Comments:
• Parasitic capacitance to substrate is voltage dependent.
• Piezoresistance effects occur due to chip strain from mounting.
Polysilicon Resistor

100-500 ohms/square (shielded)
Absolute accuracy = ±3 0%
Relative accuracy = 2% (5 µm)
Temperature coefficient = 500-1000 ppm/°C
Voltage coefficient ≈ 100 ppm/V
Comments:
• Used for fuzzes and laser trimming
• Good general resistor with low parasitics
N-well Resistor

1000-5000 ohms/square
Absolute accuracy = ±40%
Relative accuracy ≈ 5%
Temperature coefficient = 4000 ppm/°C
Voltage coefficient is large ≈ 8000 ppm/V
Comments:
• Good when large values of resistance are needed.
• Parasitics are large and resistance is voltage dependent
• Could put a $p^+$ diffusion into the well to form a pinched resistor
Metal as a Resistor

Illustration:

Resistance from A to B = Resistance of segments $L_1$, $L_2$, $L_3$, $L_4$, and $L_5$ with some correction subtracted because of corners.

Sheet resistance:

- $50-70 \text{ m\Omega/\square} \pm 30\%$ for lower or middle levels of metal
- $30-40 \text{ m\Omega/\square} \pm 15\%$ for top level metal

Watch out for the current limit for metal resistors.

Contact resistance varies from $5\Omega$ to $10\Omega$.

Tempco $\approx +4000 \text{ ppm/\degree C}$

Need to derate the current at higher temperatures:

$$I_{DC}(T_j) = D_t \cdot I_{DC}(T_r)$$

<table>
<thead>
<tr>
<th>$T_j$ ($\degree C$)</th>
<th>$T_r$ ($\degree C$)</th>
<th>$D_t$</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;85</td>
<td>85</td>
<td>1</td>
</tr>
<tr>
<td>100</td>
<td>85</td>
<td>0.63</td>
</tr>
<tr>
<td>110</td>
<td>85</td>
<td>0.48</td>
</tr>
<tr>
<td>125</td>
<td>85</td>
<td>0.32</td>
</tr>
<tr>
<td>150</td>
<td>85</td>
<td>0.18</td>
</tr>
</tbody>
</table>
**Thin Film Resistors**

A high-quality resistor fabricated from a thin nickel-chromium alloy or a silicon-chromium mixture.

Uppermost metal layer:

![Diagram of Thin Film Resistor](image)

Performance:

- Sheet resistivity is approximately 5-10 ohms/square
- Temperature coefficients of less than 100 ppm/°C
- Absolute tolerance of better than ±0.1% using laser trimming
- Selectivity of the metal etch must be sufficient to ensure the integrity of the thin-film resistor beneath the areas where metal is etched away.
Resistor Layout Techniques

End structure calculations:

\[ \Delta R_1 = \frac{R_{\text{cont}}}{N_{\text{cont}}} + R_{\text{sh(sil)}} \left( \frac{X_{c-r} + 0.75 \cdot L_{\text{con}}}{W - 2 \cdot \Delta W_{\text{sil}}} \right) \]

\[ (L_{\text{con}} = \text{width of the contact}) \]

\[ \Delta R_2 = \frac{R_{\text{cont}}}{N_{\text{cont}}} + R_{\text{sh(sil)}} \left( \frac{X_{c-r} + X_{\text{con}} + 1.75 \cdot L_{\text{con}}}{W - 2 \cdot \Delta W_{\text{sil}}} \right) \]

\[ \Delta R_{\text{total}} = \left( \frac{1}{\Delta R_1} + \frac{1}{\Delta R_2} + \cdots \right)^{-1} \]
Extending the Length of Resistors

Snaked Resistors:

These resistors typically have model problems because of non-uniform current flow at the corners.

Corner corrections:

Fig. 2.6-16B
Extending the Length of Resistors

Link Resistors:

For good matching between link resistors, keep the link length, $L_1$, identical.

Resistor Ending Influence:

Avoid “dogbone” resistors to minimize model errors.
**Process Bias Influence on Resistors**

Process bias is where the dimensions of the fabricated geometries are not the same as the layout data base dimensions.

Process biases introduce systematic errors.

Consider the effect of over-etching-

Assume that etching introduces a process bias of 0.1μm. Two resistors designed to have a ratio of 2:1 have equal lengths but the widths are different by a factor of two.

\[
\frac{R_2}{R_1} = \frac{W_1}{W_2} = \frac{4-0.2}{2-0.2} = \frac{3.8}{1.8} = 2.11 \quad \rightarrow \quad 5.6\% \text{ error in matching}
\]

Use the replication principle to eliminate this error.
**Etch Rate Variations – Polysilicon Resistors**

The size of the area to be etched determines the etch rate. Smaller areas allow less access to the etchant while larger areas allow more access to the etchant. This is illustrated below:

The objective is to make \( A = B = C \). In the left-hand case, \( B \) is larger due to the slower etch rates on *both* sides of \( B \). In the right-hand case, the dummy strips have caused the etch rates on both sides of \( A, B \) and \( C \) to be identical leading to better matching.

It may be advisable to connect the dummy strips to ground or some other low impedance node to avoid static electrical charge buildup.
**Diffusion Interaction – Diffused Resistors**

Problem:
Consider three adjacent $p^+$ diffusions into a $n$ epitaxial region,

If A, B, and C are resistors that are to be matched, we see that the effective concentration of B is larger than A or C because of diffusion interaction. This would cause the B resistor to be smaller even though the geometry is identical.

Solution: Place identical dummy resistors to the left of A and right of C. Connect the dummy resistors to a low impedance to prevent the formation of floating diffusions that might increase the sensitivity to latchup.
**Thermoelectric Effects**

The thermoelectric effect, also called the Seebeck effect, is a potential difference that is developed between two dissimilar materials that are at different temperatures. The potential developed is given as,

$$V_\gamma = S \cdot \Delta T$$

where,

- $S =$ Seebeck coefficient ($\approx 0.4\text{mV}/\text{°C}$)
- $\Delta T =$ temperature difference between the two metals

Thus, a temperature difference between the contacts to a resistor and the resistor of 1°C can generate a voltage of 0.4mV causing problems in certain circuits (bandgap).

Two possible resistor layouts with regard to the thermoelectric effect:
**High Sheet Resistivity Resistor Layout**

High sheet resistivity resistors must use p⁺ or n⁺ in order to make contacts to metal. Thus, there is plenty of opportunity for the thermoelectric effect to cause problems if care is not taken. Below are three high sheet resistor layouts with differing thermoelectric performance.

- **n** diffused resistor
- **n⁺** resistor head

**Sensitivity to Thermoelectric Effects**

- **Cold**
- **Hot**

**Vertical misalignment causes resistor errors**

- **Resistor layout that minimizes thermoelectric effect and misalignment**

Sensitive to thermoelectric effects. Sensitive to misalignment.
### MOS Passive RC Component Typical Performance Summary

<table>
<thead>
<tr>
<th>Component Type</th>
<th>Range of Values</th>
<th>Absolute Accuracy</th>
<th>Relative Accuracy</th>
<th>Temperature Coefficient</th>
<th>Voltage Coefficient</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOSFET gate Cap.</td>
<td>6-7 fF/µm²</td>
<td>10%</td>
<td>0.1%</td>
<td>20 ppm/°C</td>
<td>±20 ppm/V</td>
</tr>
<tr>
<td>Poly-Poly Capacitor</td>
<td>0.3-0.4 fF/µm²</td>
<td>20%</td>
<td>0.1%</td>
<td>25 ppm/°C</td>
<td>±50 ppm/V</td>
</tr>
<tr>
<td>Metal-Metal Capacitor</td>
<td>0.1-1 fF/µm²</td>
<td>10%</td>
<td>0.6%</td>
<td>-40 ppm/°C</td>
<td>±1 ppm/V</td>
</tr>
<tr>
<td>Diffused Resistor</td>
<td>10-100 Ω/sq.</td>
<td>35%</td>
<td>2%</td>
<td>1500 ppm/°C</td>
<td>200 ppm/V</td>
</tr>
<tr>
<td>Ion Implanted Resistor</td>
<td>0.5-2 kΩ/sq.</td>
<td>15%</td>
<td>2%</td>
<td>400 ppm/°C</td>
<td>800 ppm/V</td>
</tr>
<tr>
<td>Poly Resistor</td>
<td>30-200 Ω/sq.</td>
<td>30%</td>
<td>2%</td>
<td>1500 ppm/°C</td>
<td>100 ppm/V</td>
</tr>
<tr>
<td>n-well Resistor</td>
<td>1-10 kΩ/sq.</td>
<td>40%</td>
<td>5%</td>
<td>8000 ppm/°C</td>
<td>10 kppm/V</td>
</tr>
<tr>
<td>Top Metal Resistor</td>
<td>30 mΩ/sq.</td>
<td>15%</td>
<td>2%</td>
<td>4000 ppm/°C</td>
<td>-</td>
</tr>
<tr>
<td>Lower Metal Resistor</td>
<td>70 mΩ/sq.</td>
<td>28%</td>
<td>3%</td>
<td>4000 ppm/°C</td>
<td>-</td>
</tr>
</tbody>
</table>
INDUCTORS

Characterization of Inductors

1.) Value of the inductor

   Spiral inductor†:
   \[ L \approx \mu_0 n^2 r = 4\pi \times 10^{-7} n^2 r \approx 1.2 \times 10^{-6} n^2 r \]

2.) Quality factor, \( Q = \frac{\omega L}{R} \)

3.) Self-resonant frequency: \( f_{\text{self}} = \frac{1}{\sqrt{LC}} \)

4.) Parasitic and inter-winding capacitances


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IC Inductors

What is the range of values for on-chip inductors?

Consider an inductor used to resonate with 5pF at 1000MHz.

\[
L = \frac{1}{4\pi^2 f_o^2 C} = \frac{1}{(2\pi \cdot 10^9)^2 \cdot 5 \times 10^{-12}} = 5\text{nH}
\]

Note: Off-chip connections (bond-wires) will result in inductance as well.
Candidates for inductors in CMOS technology are:

1.) Bond wires
2.) Spiral inductors
3.) Multi-level spiral
4.) Solenoid

Bond wire Inductors:

- Function of the pad distance $d$ and the bond angle $\beta$
- Typical value is 1nH/mm which gives 2nH to 5nH in typical packages
- Series loss is 0.2 $\Omega$/mm for 1 mil diameter aluminum wire
- $Q \approx 60$ at 2 GHz
Planar Spiral Inductors in CMOS Technology

Typically: $3 < N_{\text{turns}} < 5$ and $S = S_{\text{min}}$ for the given current

Select the OD, $N_{\text{turns}}$, and $W$ so that $ID$ allows sufficient magnetic flux to flow through the center.

Loss Mechanisms:
- Skin effect
- Capacitive substrate losses
- Eddy currents in the silicon
Planar Spiral Inductors on a Lossy Substrate

- Spiral inductor is implemented using metal layers in CMOS technology
- Topmost metal is preferred because of its lower resistivity
- More than one metal layer can be connected together to reduce resistance or area
- Accurate analysis of a spiral inductor requires complex electromagnetic simulation
- Optimize the values of $W$, $S$, and $N$ to get the desired $L$, a high $Q$, and a high self-resonant frequency
- Typical values are $L = 1-8$ nH and $Q = 3-6$ at 2GHz
Inductor Modeling

Model:

\[
L \approx \frac{37.5 \mu_0 N^2 a^2}{11 D - 14 a} \\
C_{ox} = W L \frac{\varepsilon_{ox}}{t_{ox}} \\
R_s \approx \frac{L}{W \sigma \delta (1 - e^{-t/\delta})} \quad \text{(low freq. resistive loss)} \\
R_1 \approx \frac{W L C_{sub}}{2} \quad \text{(eddy current substrate loss)} \\
C_p = N W^2 L \frac{\varepsilon_{ox}}{t_{ox}} \quad \text{(overlap and coupling)} \\
C_1 \approx \frac{2}{W L C_{sub}} \quad \text{(substrate capacitance)}
\]

where

\[
\mu_0 = 4 \pi x 10^{-7} \text{ H/m (vacuum permeability)} \\
\sigma = \text{conductivity of the metal} \\
a = \text{distance from the center of the inductor to the middle of the windings} \\
L = \text{total length of the spiral} \\
t = \text{thickness of the metal} \\
\delta = \text{skin depth given by } \delta = \sqrt{\frac{2}{W \mu_0 \sigma}} \\
G_{sub}(C_{sub}) \text{ is a process-dependent parameter}
\]
**Reduction of Capacitance to Ground**

Comments concerning implementation:

1.) Put a metal ground shield between the inductor and the silicon to reduce the capacitance.
   - Should be patterned so flux goes through but electric field is grounded
   - Metal strips should be orthogonal to the spiral to avoid induced loop current
   - The resistance of the shield should be low to terminate the electric field

2.) Avoid contact resistance wherever possible to keep the series resistance low.

3.) Use the metal with the lowest resistance and farthest away from the substrate.

4.) Parallel metal strips if other metal levels are available to reduce the resistance.

Example → Fig. 2.5-12
**Inductor Improvements**

Symmetrical Layout:
- Good for differential circuits
- Higher Q
- Can achieve a center tap

**Q Improvement:**
- Substrate replaced with trenched silicon islands†

† M. Raieszadeh, Integrated Inductors on Trenched Silicon Islands, MS Thesis, School of Electrical and Computer Engineering, Georgia Institute of Technology, April 2005

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Multi-Level Spiral Inductors
Use of more than one level of metal to make the inductor.
• Can get more inductance per area
• Can increase the interwire capacitance so the different levels are often offset to get minimum overlap.
• Multi-level spiral inductors suffer from contact resistance (must have many parallel contacts to reduce the contact resistance).
• Metal especially designed for inductors is top level approximately 4µm thick.

\[ Q = 5-6, \quad f_{SR} = 30-40\text{GHz}. \quad Q = 10-11, \quad f_{SR} = 15-30\text{GHz}^{1}. \]  Good for high \( L \) in small area.

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1 The skin effect and substrate loss appear to be the limiting factor at higher frequencies of self-resonance.

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**Inductors - Continued**

Self-resonance as a function of inductance. Outer dimension of inductors.
Transformers
Transformer structures are easily obtained using stacked inductors as shown below for a 1:2 transformer.

Method of reducing the inter-winding capacitances.

Measured 1:2 transformer voltage gains:
Transformers – Continued

A 1:4 transformer:

Structure -

Measured voltage gain -

(C_L = 0, 50fF, 100fF, 500fF and 1pF. C_L is the capacitive loading on the secondary.)
Summary of Inductors

Scaling? To reduce the size of the inductor would require increasing the flux density which is determined by the material the flux flows through. Since this material will not change much with scaling, the inductor size will remain constant.

Increase in the number of metal layers will offer more flexibility for inductor and transformer implementation.

Performance:

- Inductors
  - Limited to nanohenrys
  - Very low $Q$ (3-5)

- Transformers
  - Reasonably easy to build and work well using stacked inductors

ASITIC† – A CAD tool that aids the RF circuit designer to optimize and model spiral inductors, transformers, capacitors, and substrate coupling. ASITIC calculations include the electrically induced losses and coupling as well as the magnetically induced eddy current losses. Skin effect and proximity effects, or eddy currents in the metallization, are also included.

† http://rfic.eecs.berkeley.edu/~niknejad/asitic.html

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SUMMARY

• Types of resistors include diffused, well, polysilicon and metal

• Resistors are characterized by:
  - Value
  - Linearity
  - Power
  - Parasitics

• Technology effects on resistors includes:
  - Process bias
  - Diffusion interaction
  - Thermoelectric effects
  - Piezoresistive effects

• Inductors are made by horizontal metal spirals, typically in top metal

• Inductors are characterized by:
  - Value
  - Losses
  - Self-resonant frequency
  - Parasitics

• RF transformers are reasonably easy to build and work well using stacked inductors