LECTURE 07 – RESISTORS AND INDUCTORS

LECTURE ORGANIZATION

Outline

- Resistors
- Inductors
- Summary

***CMOS Analog Circuit Design*, 3rd Edition Reference**

Pages 50-52, 652-654 and new material

RESISTORS

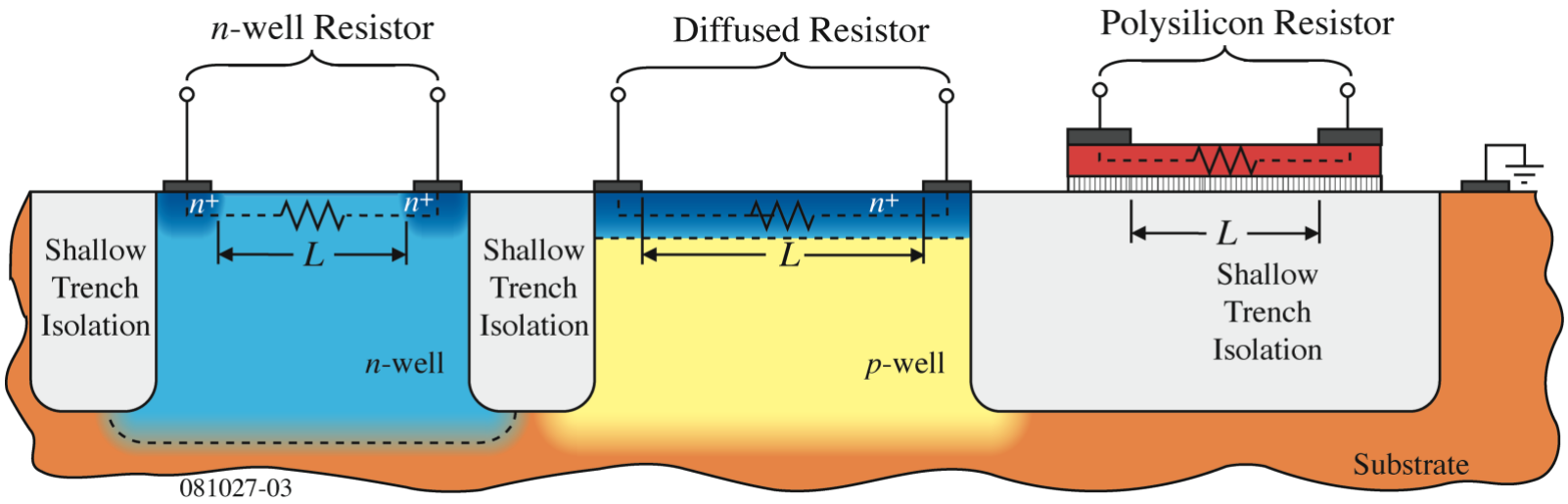
Types of Resistors Compatible with CMOS Technology

1.) Diffused and/or implanted resistors.

2.) Well resistors.

3.) Polysilicon resistors.

4.) Metal resistors.

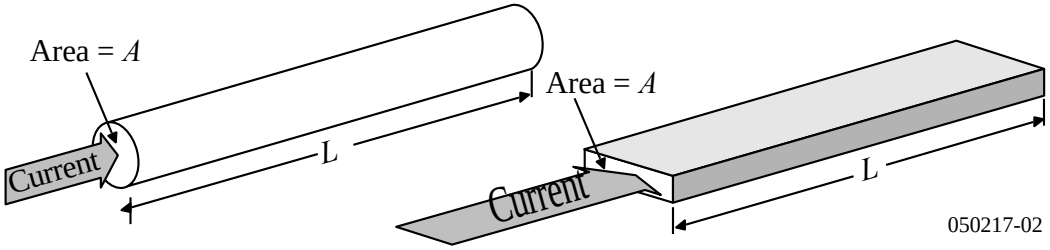


Characterization of Resistors

1.) Value

$$R = \frac{\rho L}{A}$$

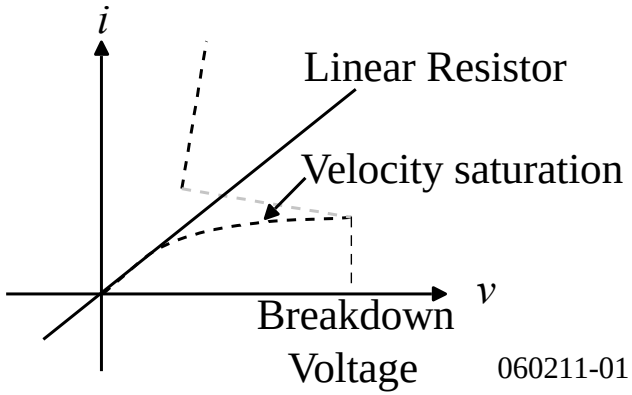
AC and DC resistance



2.) Linearity

Does $V = IR$?

Velocity saturation of carriers

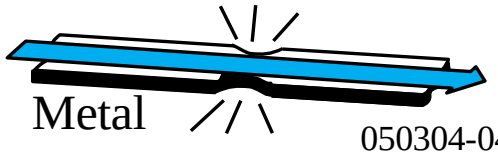


3.) Power

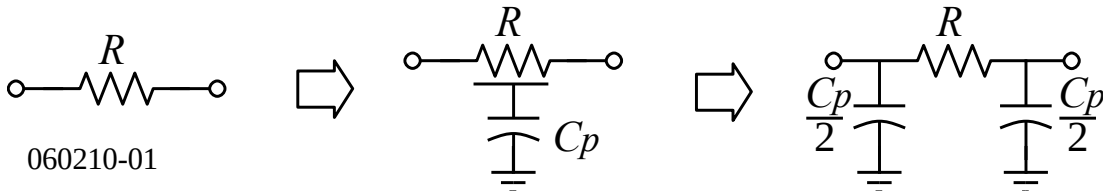
$P = VI = I^2R$

4.) Current

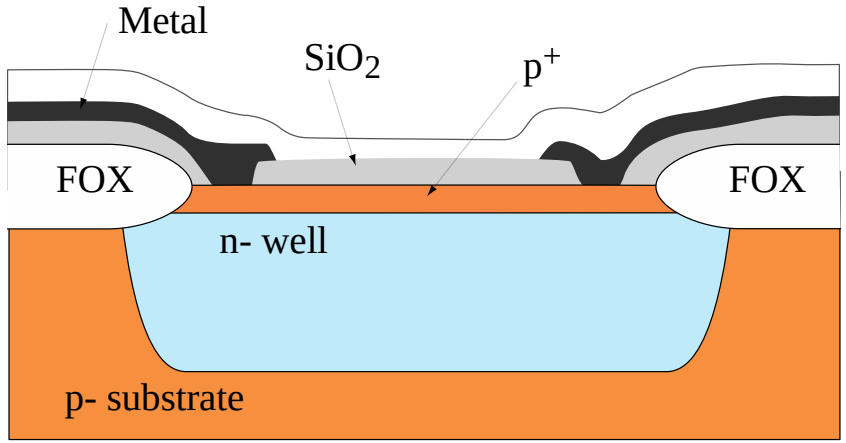
Electromigration



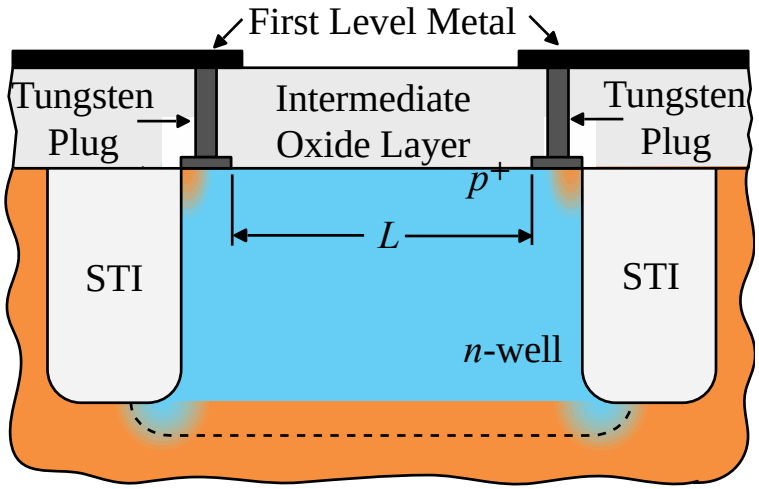
5.) Parasitics



MOS Resistors - Source/Drain Resistor



060214-02 Older LOCOS Technology



Diffusion:

10-100 ohms/square
Absolute accuracy = ±35%
Relative accuracy=2% (5µm), 0.2% (50µm)
Temperature coefficient = +1500 ppm/°C
Voltage coefficient ≈ 200 ppm/V

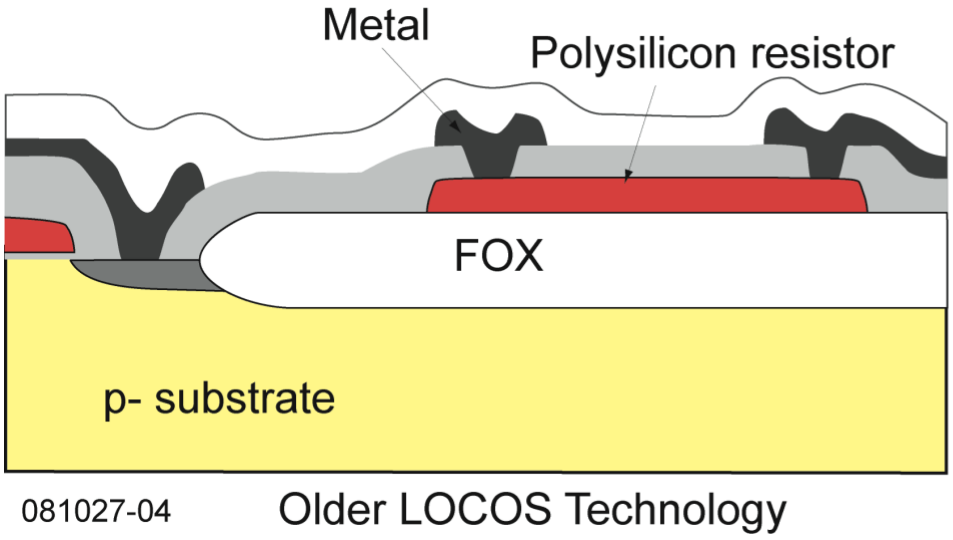
Ion Implanted:

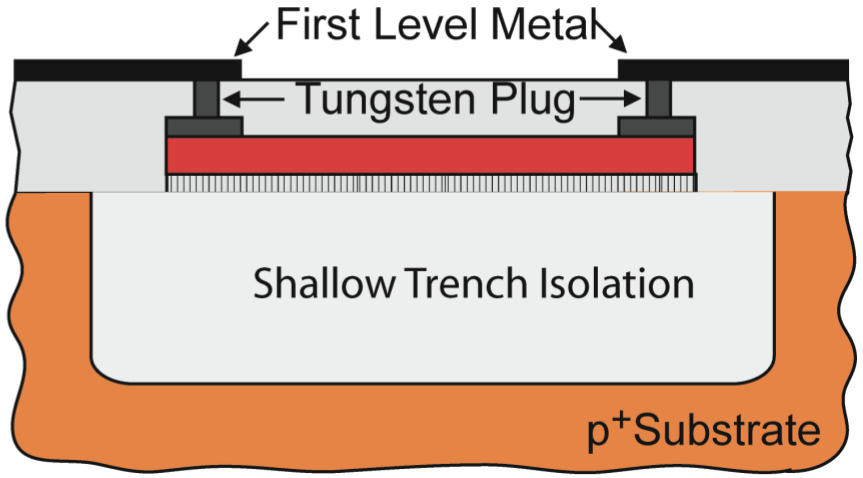
500-2000 ohms/square
Absolute accuracy = ±15%
Relative accuracy=2% (5µm), 0.15% (50µm)
Temperature coefficient = +400 ppm/°C
Voltage coefficient ≈ 800 ppm/V

Comments:

- Parasitic capacitance to substrate is voltage dependent.
- Piezoresistance effects occur due to chip strain from mounting.

Polysilicon Resistor



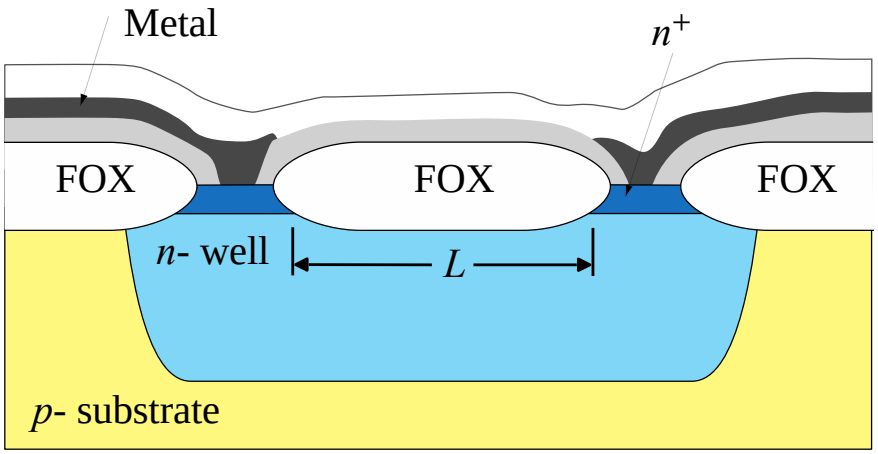


100-500 ohms/square (shielded)
Absolute accuracy = ±3 0%
Relative accuracy = 2% (5 µm)
Temperature coefficient = 500-1000 ppm/°C
Voltage coefficient ≈ 100 ppm/V

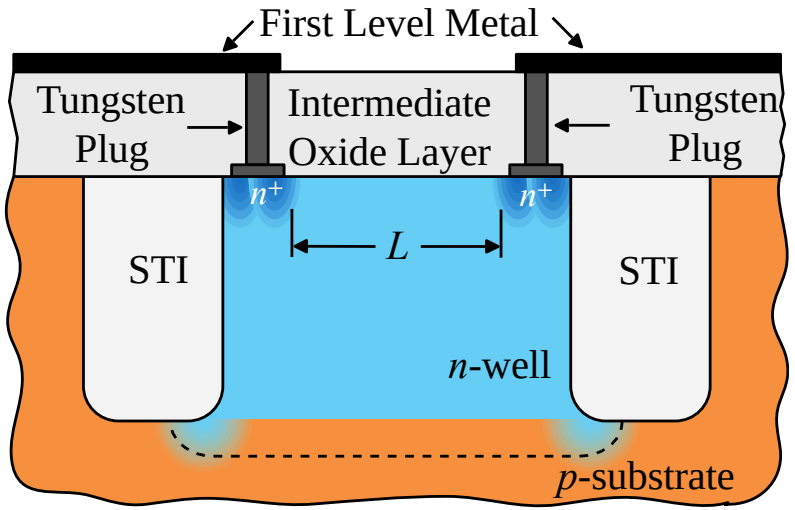
Comments:

- Used for fuzzes and laser trimming
- Good general resistor with low parasitics

N-well Resistor



LOCOS Technology



1000-5000 ohms/square

Absolute accuracy = ±40%

Relative accuracy ≈ 5%

Temperature coefficient = 4000 ppm/°C

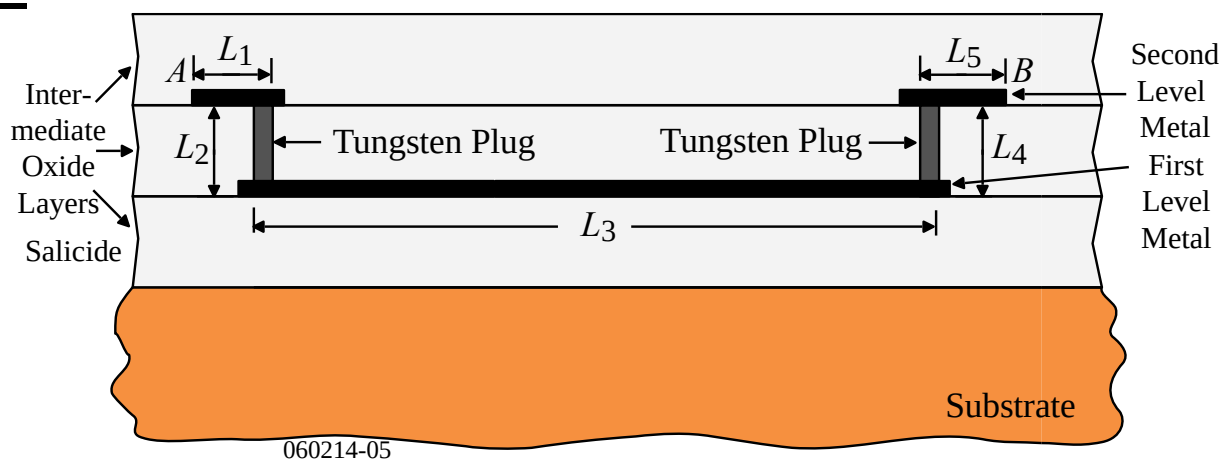
Voltage coefficient is large ≈ 8000 ppm/V

Comments:

- Good when large values of resistance are needed.
- Parasitics are large and resistance is voltage dependent
- Could put a p^+ diffusion into the well to form a pinched resistor

Metal as a Resistor

Illustration:



Resistance from A to B = Resistance of segments L_1, L_2, L_3, L_4, and L_5 with some correction subtracted because of corners.

Sheet resistance:

50-70 mΩ/☐ ± 30% for lower or middle levels of metal

30-40 mΩ/☐ ± 15% for top level metal

Watch out for the current limit for metal resistors.

Contact resistance varies from 5Ω to 10Ω.

Tempco ≈ +4000 ppm/°C

Need to derate the current at higher temperatures:

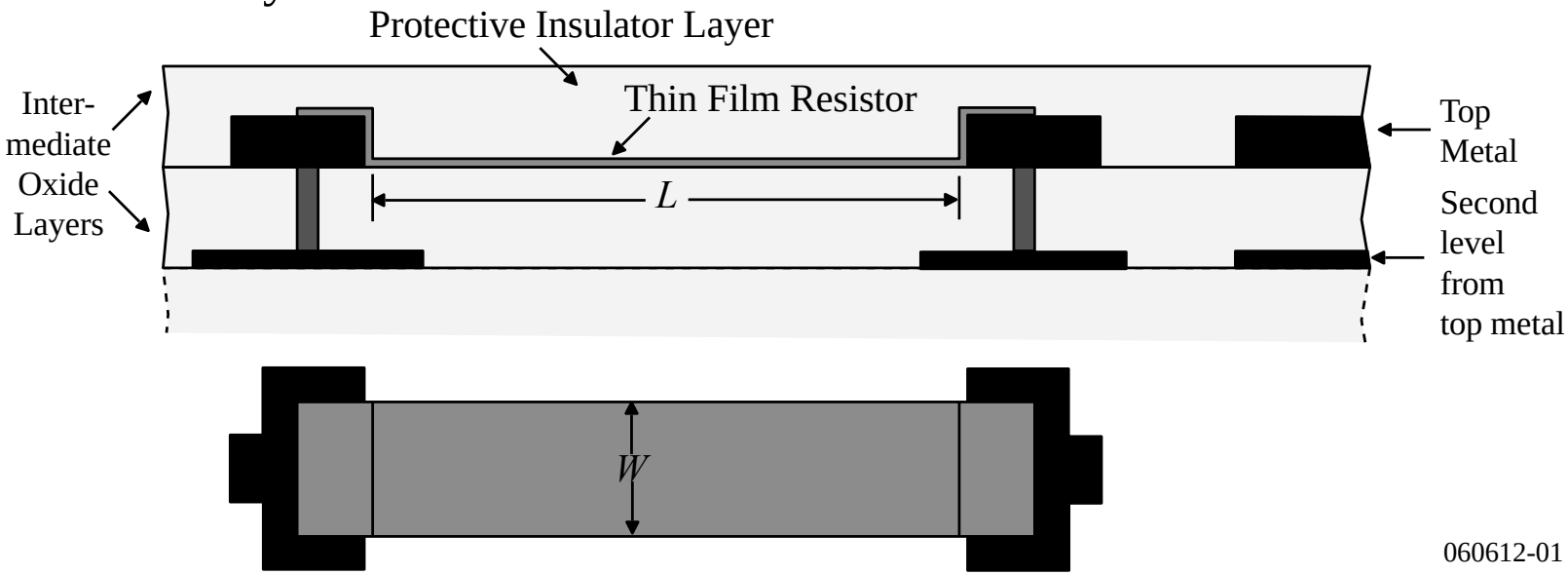
$$I_{DC}(T_j) = D_t \cdot I_{DC}(T_r)$$

T_j(°C)	T_r(°C)	D_t
<85	85	1
100	85	0.63
110	85	0.48
125	85	0.32
150	85	0.18

Thin Film Resistors

A high-quality resistor fabricated from a thin nickel-chromium alloy or a silicon-chromium mixture.

Uppermost metal layer:



Performance:

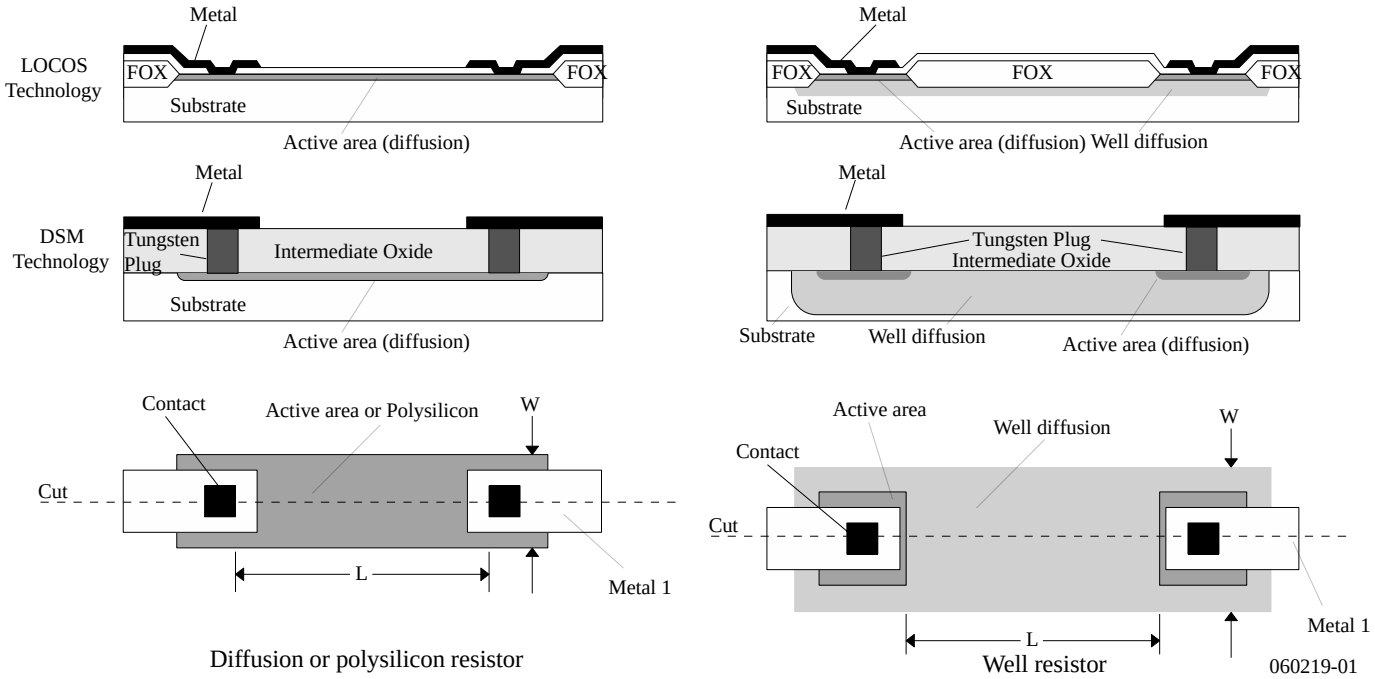
Sheet resistivity is approximately 5-10 ohms/square

Temperature coefficients of less than 100 ppm/°C

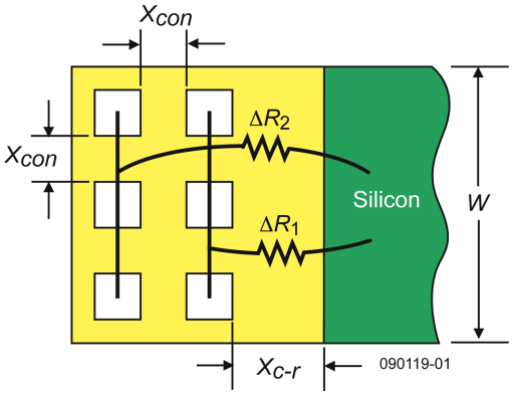
Absolute tolerance of better than ±0.1% using laser trimming

Selectivity of the metal etch must be sufficient to ensure the integrity of the thin-film resistor beneath the areas where metal is etched away.

Resistor Layout Techniques



End structure calculations:



$$\Delta R_1 = \frac{R_{\text{cont}}}{N_{\text{cont}}} + R_{\text{sh}}(\text{sil})\left(\frac{X_{\text{c-r}} + 0.75\cdot L_{\text{con}}}{W - 2\cdot \Delta W_{\text{sil}}}\right)$$

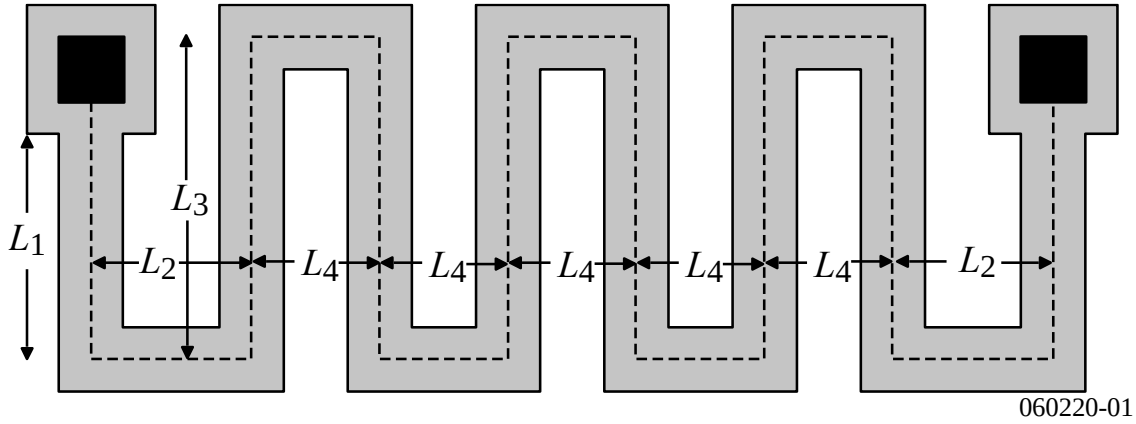
(L_{con} = width of the contact)

$$\Delta R_2 = \frac{R_{\text{cont}}}{N_{\text{cont}}} + R_{\text{sh}}(\text{sil})\left(\frac{X_{\text{c-r}} + X_{\text{con}} + 1.75\cdot L_{\text{con}}}{W - 2\cdot \Delta W_{\text{sil}}}\right)$$

$$\Delta R_{total} = \left(\frac{1}{\Delta R_1} + \frac{1}{\Delta R_2} + \cdots\right)^{-1}$$

Extending the Length of Resistors

Snaked Resistors:



These resistors typically have model problems because of non-uniform current flow at the corners.

Corner corrections:

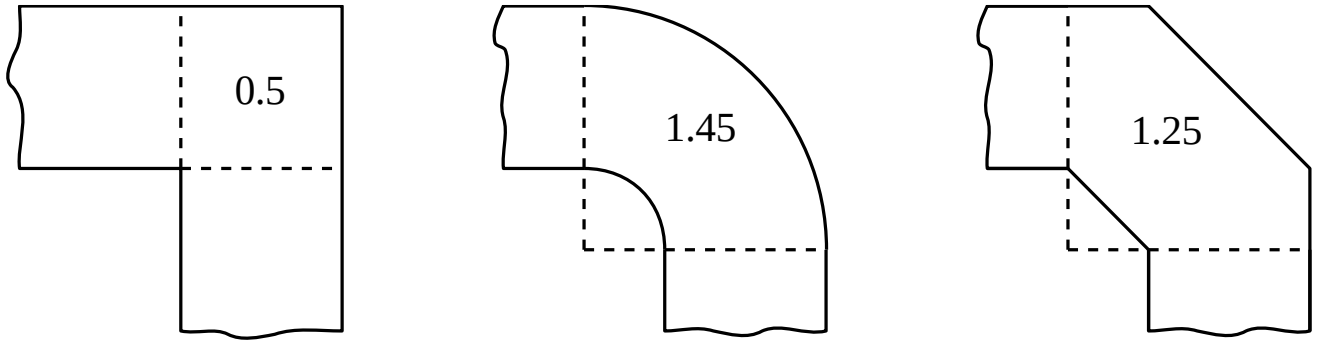
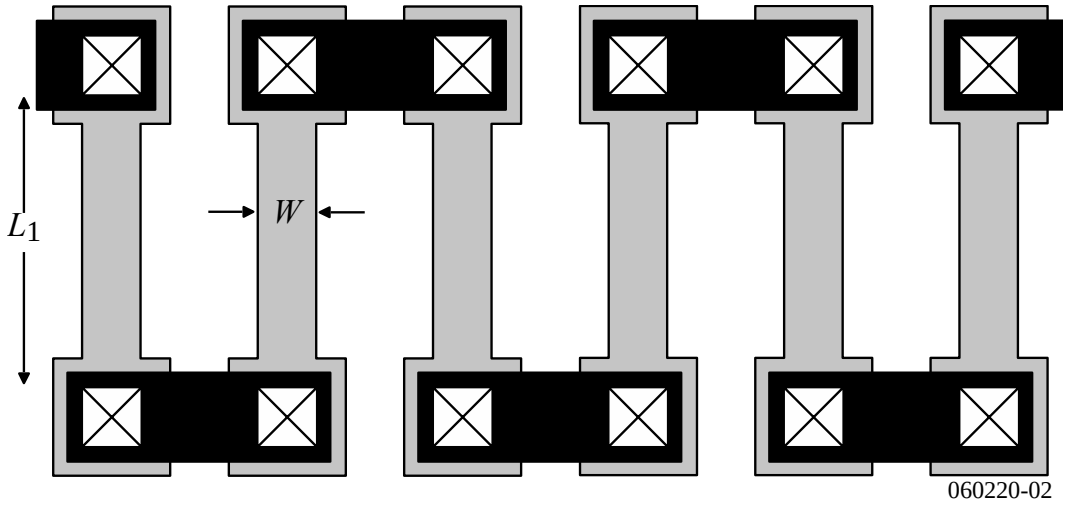


Fig. 2.6-16B

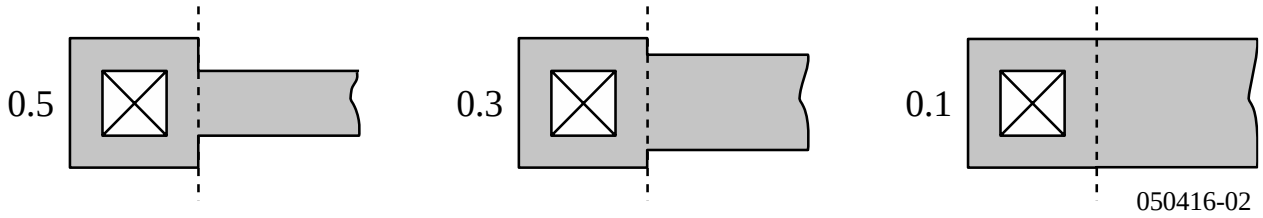
Extending the Length of Resistors

Link Resistors:



For good matching between link resistors, keep the link length, L_1, identical.

Resistor Ending Influence:



Avoid “dogbone” resistors to minimize model errors.

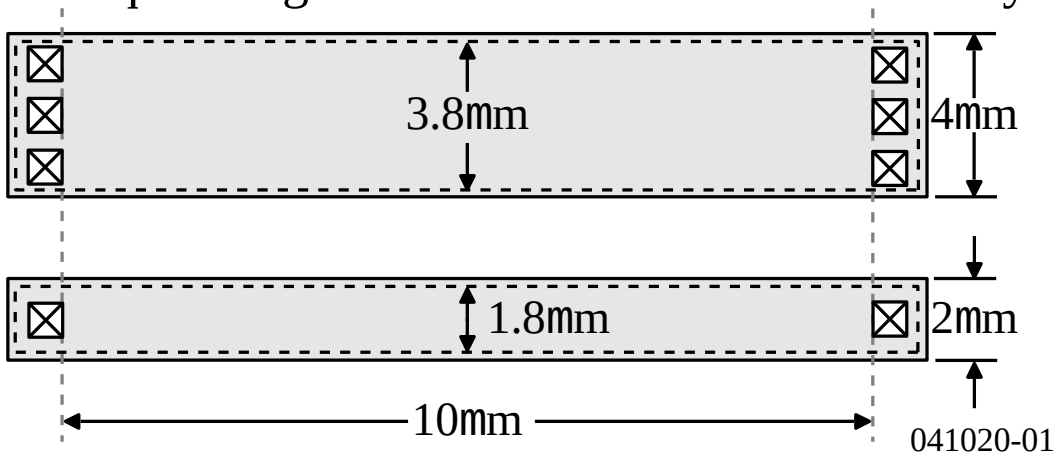
Process Bias Influence on Resistors

Process bias is where the dimensions of the fabricated geometries are not the same as the layout data base dimensions.

Process biases introduce systematic errors.

Consider the effect of over-etching-

Assume that etching introduces a process bias of 0.1μm. Two resistors designed to have a ratio of 2:1 have equal lengths but the widths are different by a factor of two.



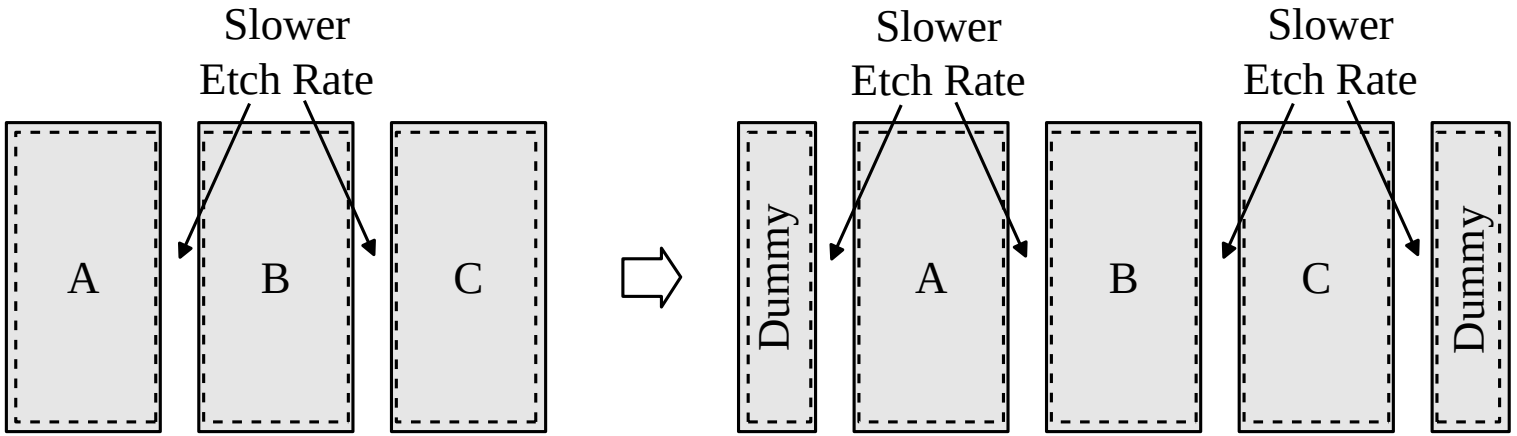
The actual matching ratio due to the etching bias is,

$$\frac{R_2}{R_1} = \frac{W_1}{W_2} = \frac{4\text{-}0.2}{2\text{-}0.2} = \frac{3.8}{1.8} = 2.11 \quad \rightarrow \quad 5.6\% \text{ error in matching}$$

Use the replication principle to eliminate this error.

Etch Rate Variations – Polysilicon Resistors

The size of the area to be etched determines the etch rate. Smaller areas allow less access to the etchant while larger areas allow more access to the etchant. This is illustrated below:



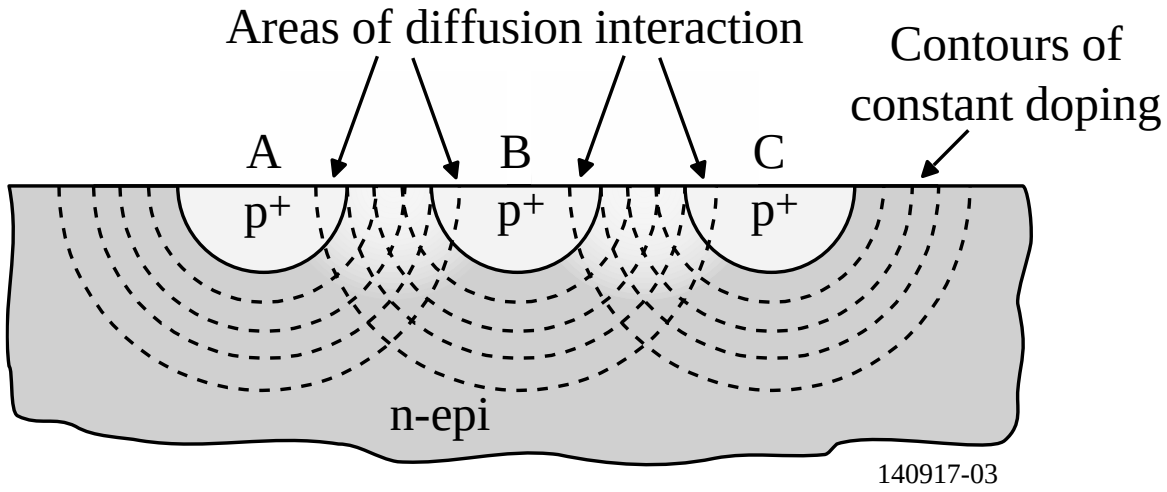
The objective is to make A = B = C. In the left-hand case, B is larger due to the slower etch rates on *both* sides of B. In the right-hand case, the dummy strips have caused the etch rates on both sides of A, B and C to be identical leading to better matching.

It may be advisable to connect the dummy strips to ground or some other low impedance node to avoid static electrical charge buildup.

Diffusion Interaction – Diffused Resistors

Problem:

Consider three adjacent p^+ diffusions into a *n* epitaxial region,



If A, B, and C are resistors that are to be matched, we see that the effective concentration of B is larger than A or C because of diffusion interaction. This would cause the B resistor to be smaller even though the geometry is identical.

Solution: Place identical dummy resistors to the left of A and right of C. Connect the dummy resistors to a low impedance to prevent the formation of floating diffusions that might increase the sensitivity to latchup.

Thermoelectric Effects

The thermoelectric effect, also called the Seebeck effect, is a potential difference that is developed between two dissimilar materials that are at different temperatures. The potential developed is given as,

$$V_\gamma = S \cdot \Delta T$$

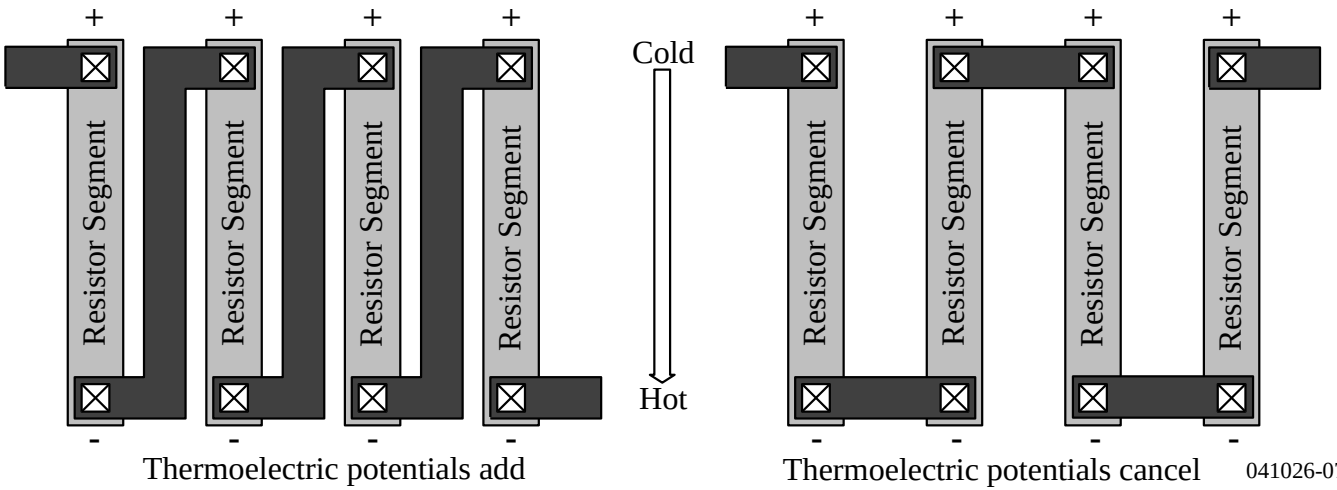
where,

S = Seebeck coefficient (≈ 0.4mV/°C)

ΔT = temperature difference between the two metals

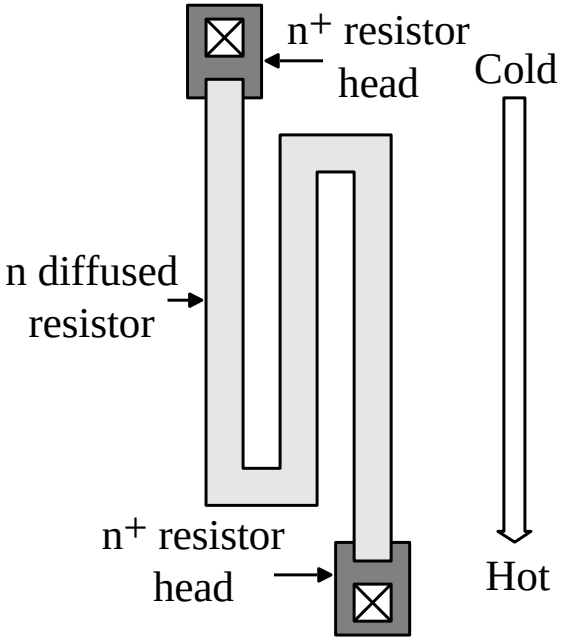
Thus, a temperature difference between the contacts to a resistor and the resistor of 1°C can generate a voltage of 0.4mV causing problems in certain circuits (bandgap).

Two possible resistor layouts with regard to the thermoelectric effect:

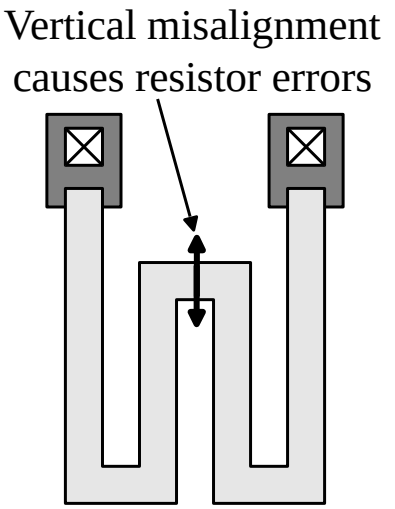


High Sheet Resistivity Resistor Layout

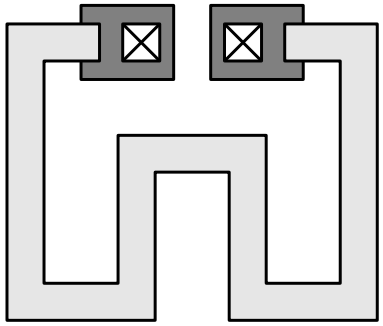
High sheet resistivity resistors must use p^+ or n^+ in order to make contacts to metal. Thus, there is plenty of opportunity for the thermoelectric effect to cause problems if care is not taken. Below are three high sheet resistor layouts with differing thermoelectric performance.



Sensitive to thermoelectric effects.



Sensitive to misalignment.



Resistor layout that minimizes thermoelectric effect and misalignment

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MOS Passive RC Component Typical Performance Summary

Component Type	Range of Values	Absolute Accuracy	Relative Accuracy	Temperature Coefficient	Voltage Coefficient
MOSFET gate Cap.	6-7 fF/μm^2	10%	0.1%	20ppm/°C	±20ppm/V
Poly-Poly Capacitor	0.3-0.4 fF/μm^2	20%	0.1%	25ppm/°C	±50ppm/V
Metal-Metal Capacitor	0.1-1fF/μm^2	10%	0.6%	-40ppm/°C	±1ppm/V
Diffused Resistor	10-100 Ω/sq.	35%	2%	1500ppm/°C	200ppm/V
Ion Implanted Resistor	0.5-2 kΩ/sq.	15%	2%	400ppm/°C	800ppm/V
Poly Resistor	30-200 Ω/sq.	30%	2%	1500ppm/°C	100ppm/V
n-well Resistor	1-10 kΩ/sq.	40%	5%	8000ppm/°C	10kppm/V
Top Metal Resistor	30 mΩ/sq.	15%	2%	4000ppm/°C	-
Lower Metal Resistor	70 mΩ/sq.	28%	3%	4000ppm/°C	-

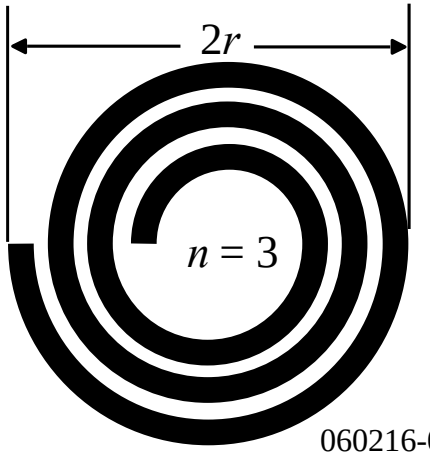
INDUCTORS

Characterization of Inductors

1.) Value of the inductor

Spiral inductor†:

$$L \approx \mu_0 n^2 r = 4\pi \text{x} 10^{-7} n^2 r \approx 1.2\text{x}10^{-6} n^2 r$$



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2.) Quality factor, $Q = \dfrac{\omega L}{R}$

3.) Self-resonant frequency: $f_{self} = \dfrac{1}{\sqrt{LC}}$

4.) Parasitic and inter-winding capacitances

† H.M Greenhouse, "Design of Planar Rectangular Microelectronic Inductors," *IEEE Trans. Parts, Hybrids, and Packaging*, vol. 10, no. 2, June 1974, pp. 101-109.

IC Inductors

What is the range of values for on-chip inductors?

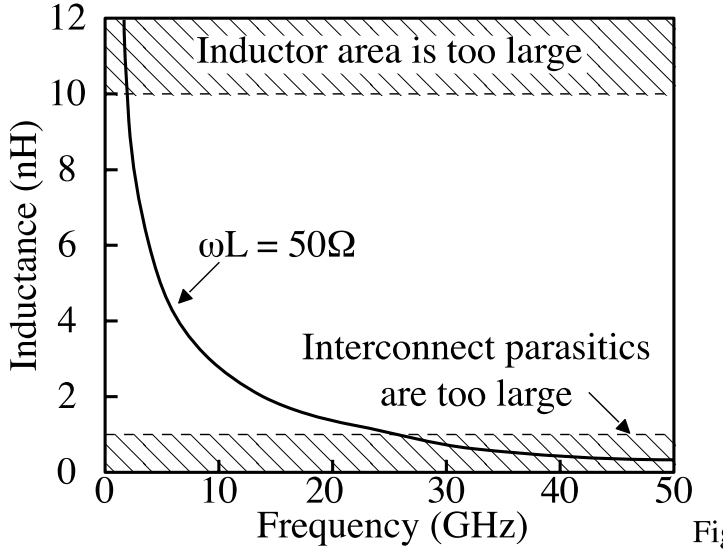


Fig. 6-5

Consider an inductor used to resonate with 5pF at 1000MHz.

$$L = \frac{1}{4\pi^2 f_o^2 C} = \frac{1}{(2\pi \cdot 10^9)^2 \cdot 5\text{x}10^{-12}} = 5\text{nH}$$

Note: Off-chip connections (bond-wires) will result in inductance as well.

Candidates for inductors in CMOS technology are:

1.) Bond wires

2.) Spiral inductors

3.) Multi-level spiral

4.) Solenoid

Bond wire Inductors:

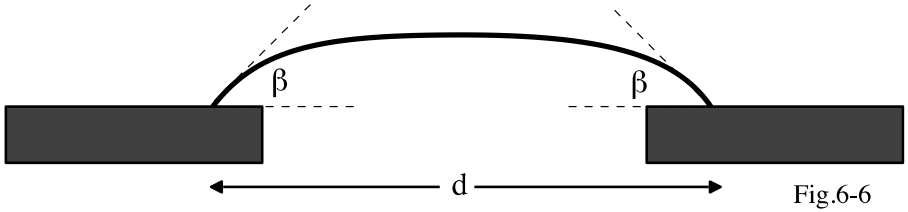
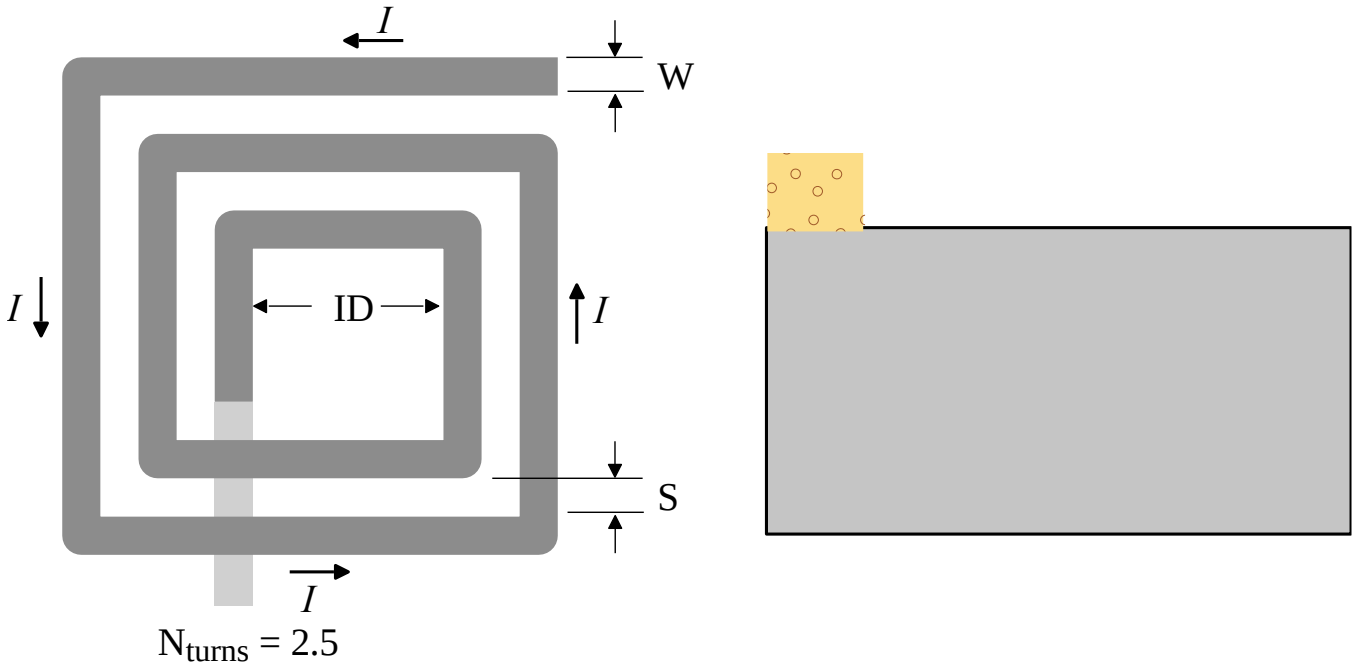


Fig.6-6

- Function of the pad distance d and the bond angle β
- Typical value is 1nH/mm which gives 2nH to 5nH in typical packages
- Series loss is 0.2 Ω/mm for 1 mil diameter aluminum wire
- $Q \approx 60$ at 2 GHz

Planar Spiral Inductors in CMOS Technology



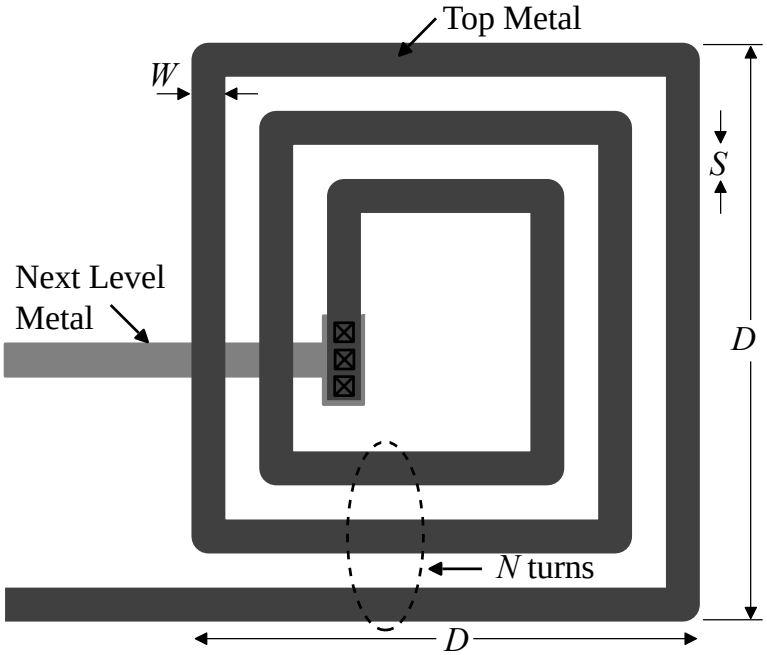
Typically: $3 < N_{turns} < 5$ and $S = S_{min}$ for the given current

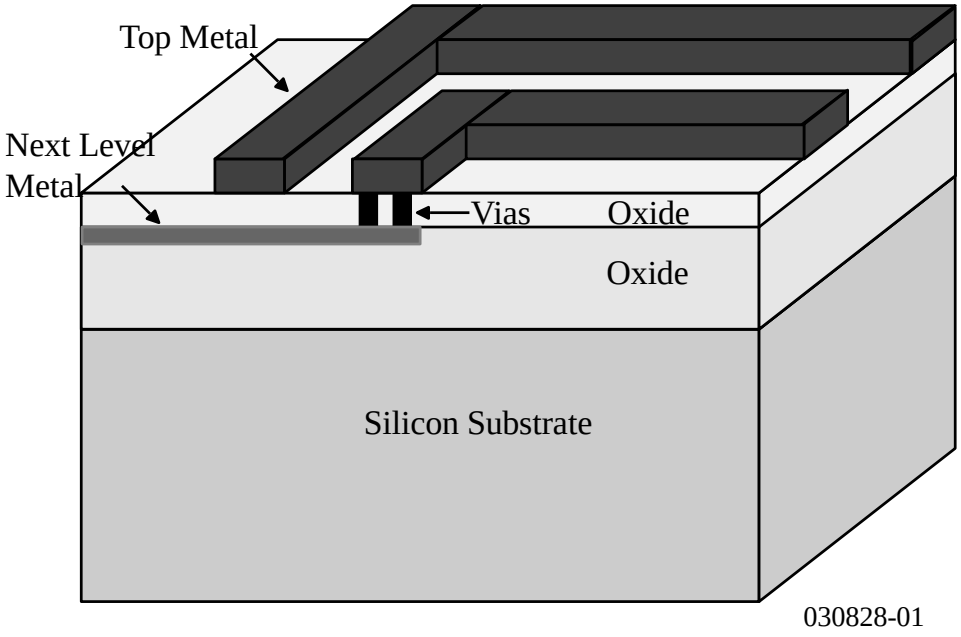
Select the OD, N_{turns}, and W so that ID allows sufficient magnetic flux to flow through the center.

Loss Mechanisms:

- Skin effect
- Capacitive substrate losses
- Eddy currents in the silicon

Planar Spiral Inductors on a Lossy Substrate

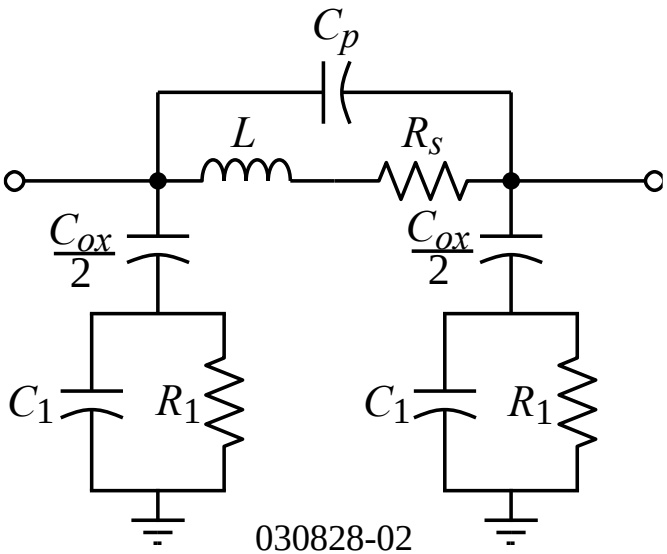




- Spiral inductor is implemented using metal layers in CMOS technology
- Topmost metal is preferred because of its lower resistivity
- More than one metal layer can be connected together to reduce resistance or area
- Accurate analysis of a spiral inductor requires complex electromagnetic simulation
- Optimize the values of *W*, *S*, and *N* to get the desired *L*, a high *Q*, and a high self-resonant frequency
- Typical values are *L* = 1-8nH and *Q* = 3-6 at 2GHz

Inductor Modeling

Model:



$$L \approx \frac{37.5\mu_0 N^2 a^2}{11D\text{-}14a} \qquad C_{ox} = W \cdot L \cdot \frac{\varepsilon_{ox}}{t_{ox}}$$

$$R_s \approx \frac{L}{W\sigma\delta(1\text{-}e^{-t/\delta})} \text{ (low freq. resistive loss)}$$

$$R_1 \approx \frac{WLC_{sub}}{2} \text{ (eddy current substrate loss)}$$

$$C_p = NW^2 L \cdot \frac{\varepsilon_{ox}}{t_{ox}} \text{ (overlap and coupling)}$$

$$C_1 \approx \frac{2}{WLC_{sub}} \text{ (substrate capacitance)}$$

where

$\mu_0 = 4\pi x10^{-7}$ H/m (vacuum permeability)

σ = conductivity of the metal

a = distance from the center of the inductor to the middle of the windings

L = total length of the spiral

t = thickness of the metal

δ = skin depth given by $\delta = \sqrt{2/W\mu_0\sigma}$

$G_{sub}(C_{sub})$ is a process-dependent parameter

Reduction of Capacitance to Ground

Comments concerning implementation:

1.) Put a metal ground shield between the inductor and the silicon to reduce the capacitance.
   - Should be patterned so flux goes through but electric field is grounded
   - Metal strips should be orthogonal to the spiral to avoid induced loop current
   - The resistance of the shield should be low to terminate the electric field

2.) Avoid contact resistance wherever possible to keep the series resistance low.

3.) Use the metal with the lowest resistance and farthest away from the substrate.

4.) Parallel metal strips if other metal levels are available to reduce the resistance.

Example →

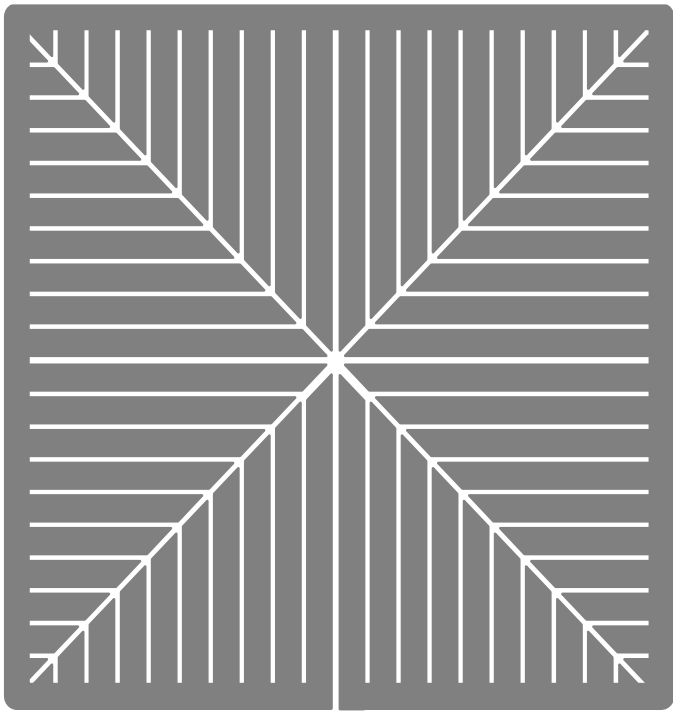
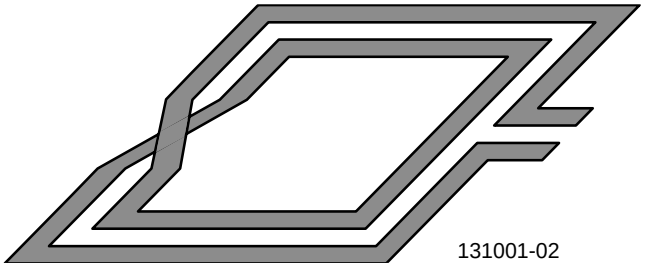


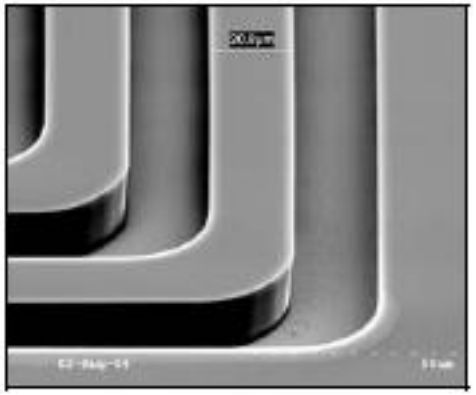
Fig. 2.5-12

Inductor Improvements

Symmetrical Layout:

- Good for differential circuits
- Higher Q
- Can achieve a center tap

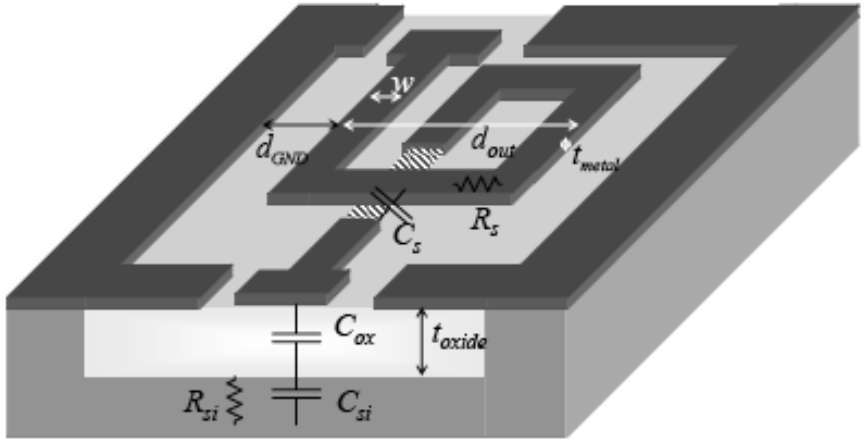




17 µm metal

Q Improvement:

- Substrate replaced with trenched silicon islands†

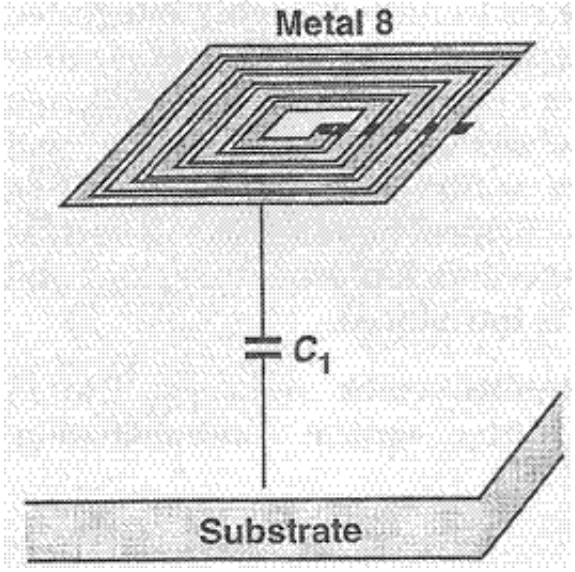


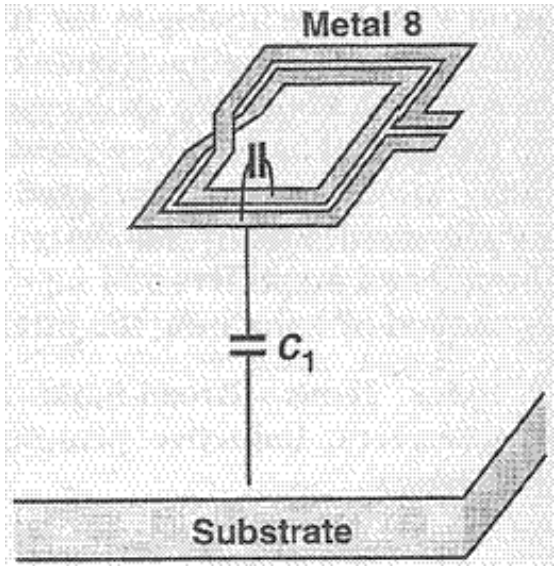
† M. Raieszadeh, Integrated Inductors on Trenched Silicon Islands, MS Thesis, School of Electrical and Computer Engineering, Georgia Institute of Technology, April 2005

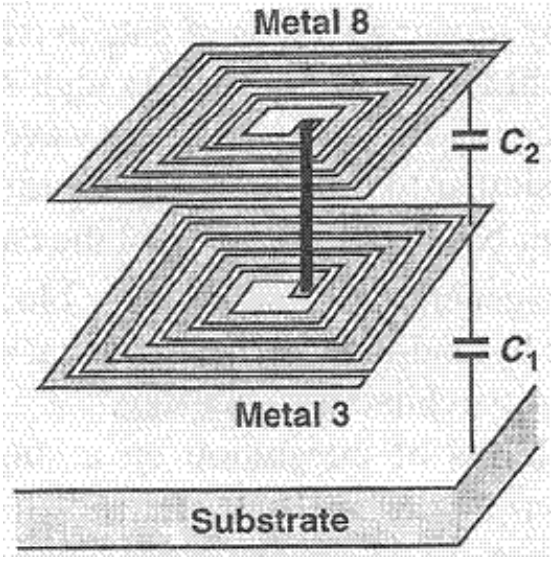
Multi-Level Spiral Inductors

Use of more than one level of metal to make the inductor.

- Can get more inductance per area
- Can increase the interwire capacitance so the different levels are often offset to get minimum overlap.
- Multi-level spiral inductors suffer from contact resistance (must have many parallel contacts to reduce the contact resistance).
- Metal especially designed for inductors is top level approximately 4μm thick.





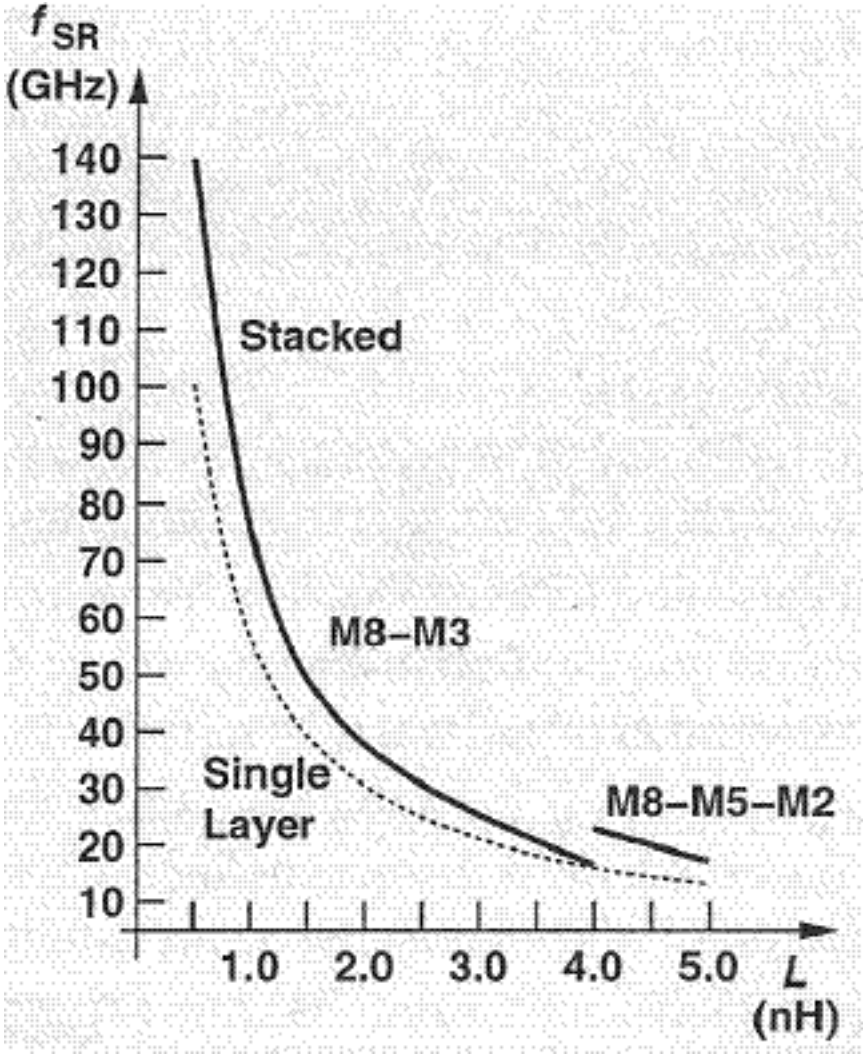


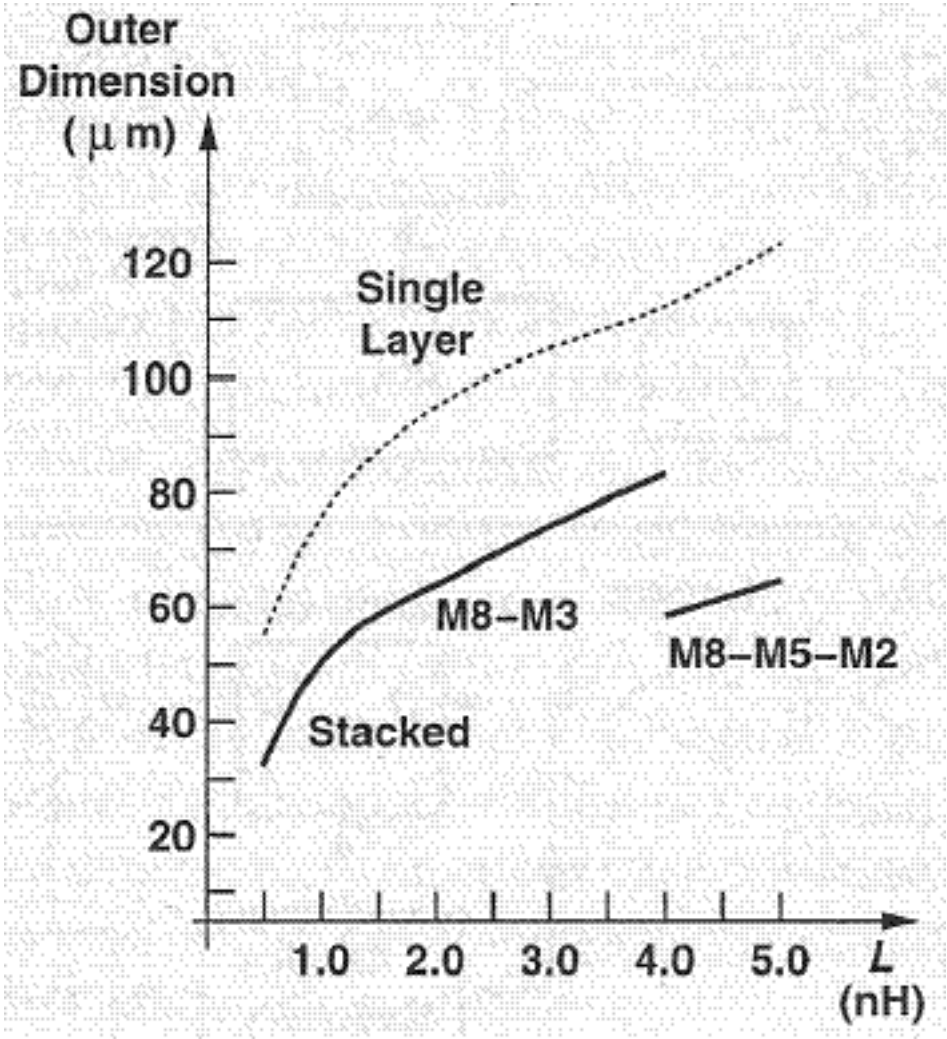
Q = 5-6, f_{SR} = 30-40GHz. Q = 10-11, f_{SR} = 15-30GHz[1]. Good for high L in small area.

[1] The skin effect and substrate loss appear to be the limiting factor at higher frequencies of self-resonance.

Inductors - Continued

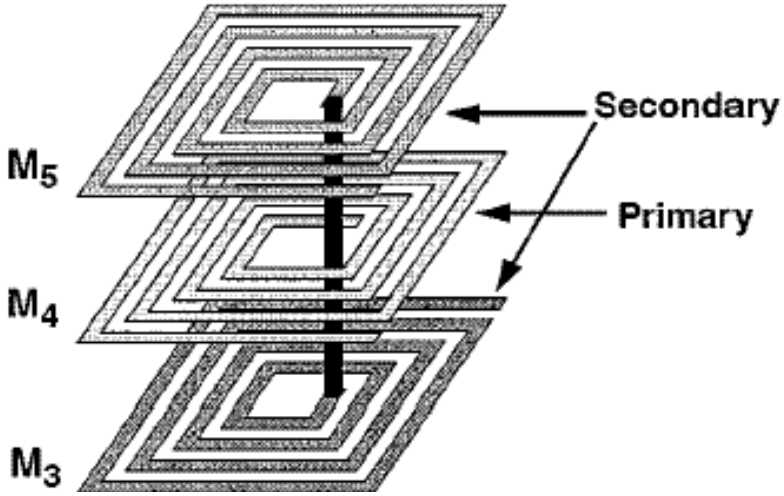
Self-resonance as a function of inductance. Outer dimension of inductors.



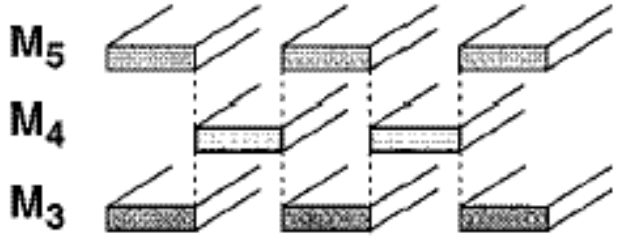


Transformers

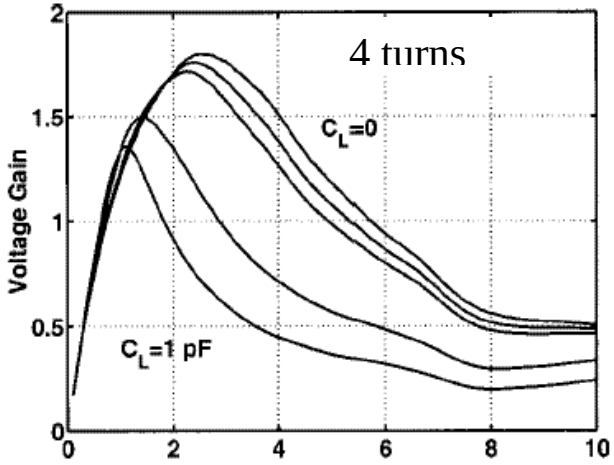
Transformer structures are easily obtained using stacked inductors as shown below for a 1:2 transformer.

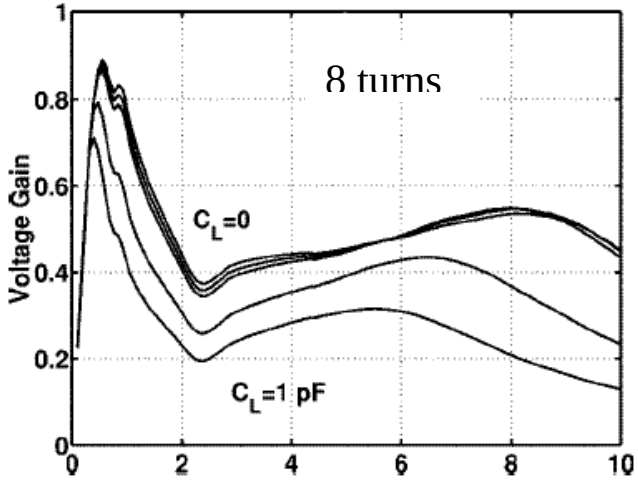


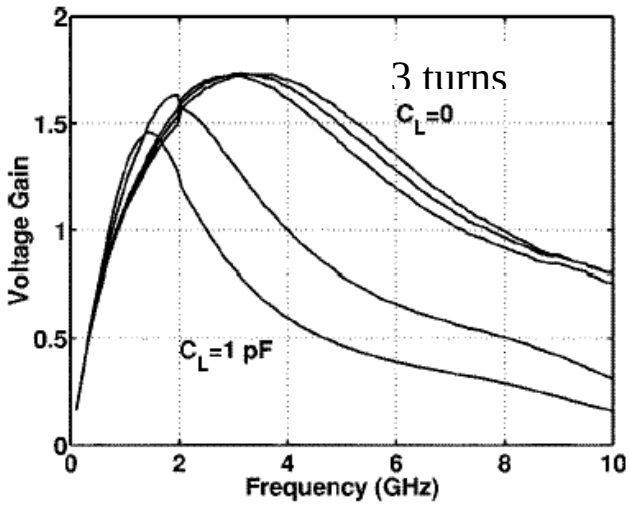
Method of reducing the inter-winding capacitances.



Measured 1:2 transformer voltage gains:



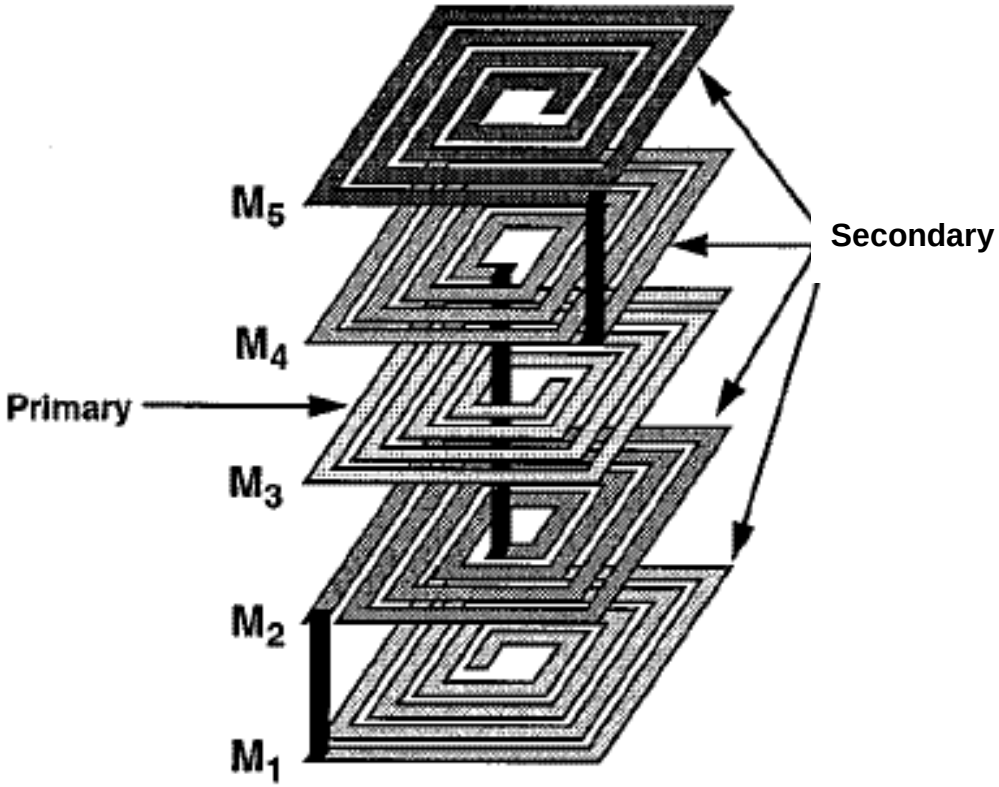




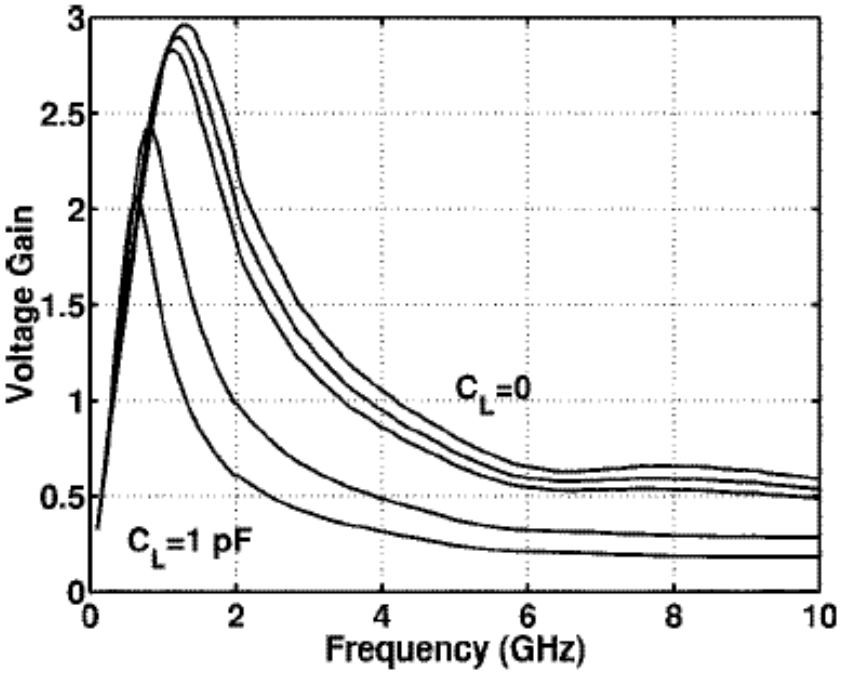
Transformers – Continued

A 1:4 transformer:

Structure-



Measured voltage gain-



(C_L = 0, 50fF, 100fF, 500fF and 1pF. C_L is the capacitive loading on the secondary.)

Summary of Inductors

Scaling? To reduce the size of the inductor would require increasing the flux density which is determined by the material the flux flows through. Since this material will not change much with scaling, the inductor size will remain constant.

Increase in the number of metal layers will offer more flexibility for inductor and transformer implementation.

Performance:

- Inductors
  - Limited to nanohenrys
  - Very low Q (3-5)
- Transformers
  - Reasonably easy to build and work well using stacked inductors

ASITIC[†] – A CAD tool that aids the RF circuit designer to optimize and model spiral inductors, transformers, capacitors, and substrate coupling. ASITIC calculations include the electrically induced losses and coupling as well as the magnetically induced eddy current losses. Skin effect and proximity effects, or eddy currents in the metallization, are also included.

[†] http://rfic.eecs.berkeley.edu/~niknejad/asitic.html

SUMMARY

- Types of resistors include diffused, well, polysilicon and metal
- Resistors are characterized by:
  - Value
  - Linearity
  - Power
  - Parasitics
- Technology effects on resistors includes:
  - Process bias
  - Diffusion interaction
  - Thermoelectric effects
  - Piezoresistive effects
- Inductors are made by horizontal metal spirals, typically in top metal
- Inductors are characterized by:
  - Value
  - Losses
  - Self-resonant frequency
  - Parasitics
- RF transformers are reasonably easy to build and work well using stacked inductors