LECTURE 06 - CAPACITORS

LECTURE ORGANIZATION

Outline

- Introduction
- *pn* junction capacitors
- MOSFET gate capacitors
- Conductor-insulator-conductor capacitors
- Deviation from ideal behavior in capacitors
- Summary

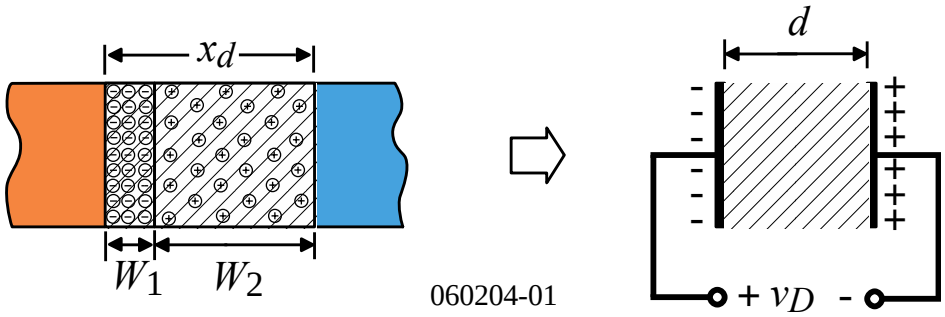
***CMOS Analog Circuit Design*, 3rd Edition Reference**

Pages 46-52 and 654-657

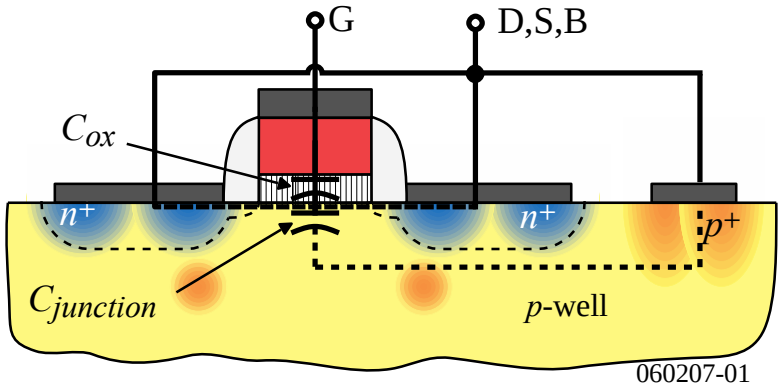
INTRODUCTION

Types of Capacitors for CMOS Technology

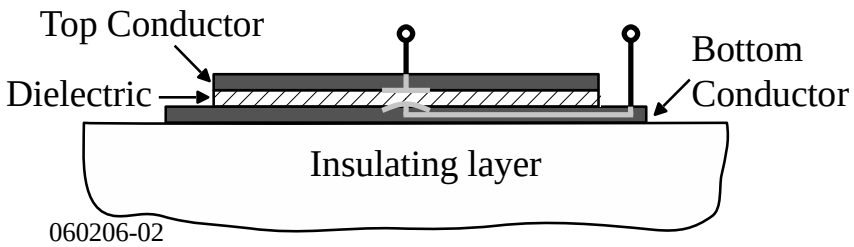
1.) *PN* junction (depletion) capacitors



2.) MOSFET gate capacitors



3.) Conductor-insulator-conductor capacitors



Characterization of Capacitors

What characterizes a capacitor?

1.) Losses in a capacitor characterized by the quality factor of a capacitor is a measure of the imaginary to real part of the impedance or admittance

$$Q = \frac{1}{\omega C R_s} = \omega C R_p$$

where R_p is the equivalent resistance in parallel with the capacitor, C, and R_s is the electrical series resistance (ESR) of the capacitor, C.

2.) Parasitic capacitors to ground from each node of the capacitor.

3.) The density of the capacitor in Farads/area.

4.) The absolute and relative accuracies of the capacitor.

5.) The C_{max}/C_{min} ratio which is the largest value of capacitance to the smallest when the capacitor is used as a variable capacitor (*varactor*).

6.) The variation of a variable capacitance with the control voltage.

7.) Linearity, $q = Cv$.

PN JUNCTION CAPACITORS

PN Junction Capacitors in a Well

Generally made by diffusion into the well.

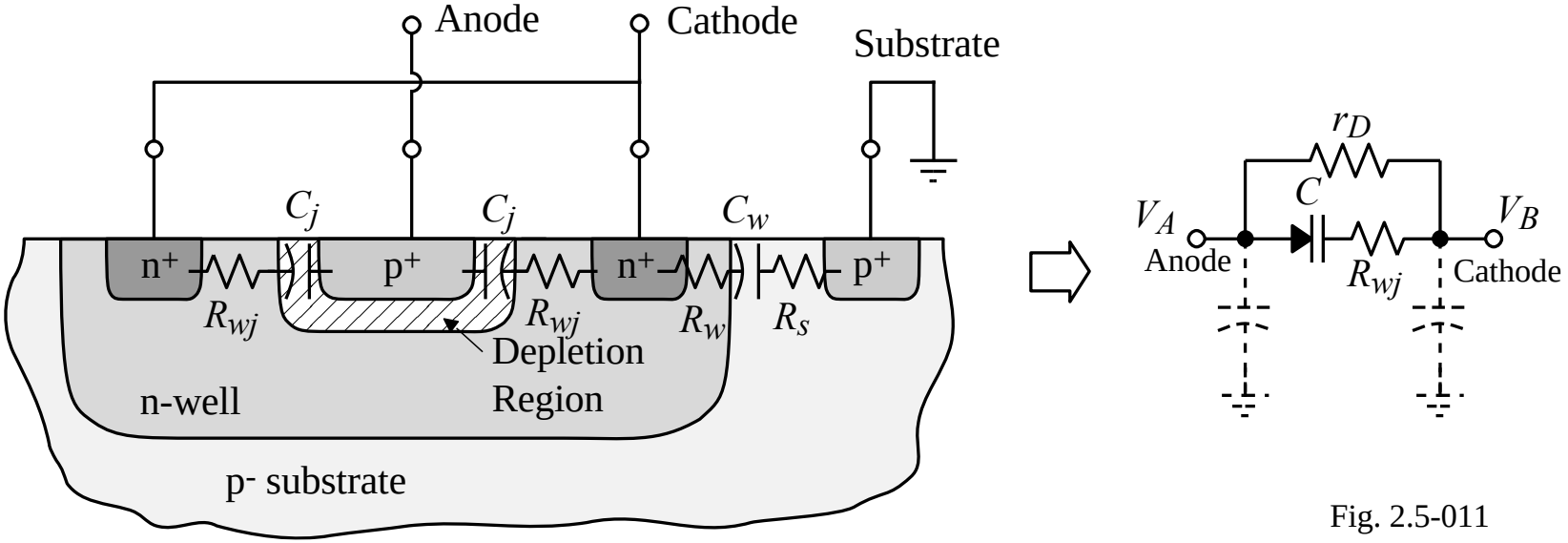


Fig. 2.5-011

Layout:

Minimize the distance between the p^+ and n^+ diffusions.

Two different versions have been tested.

1.) Large islands – 9µm on a side

2.) Small islands – 1.2µm on a side

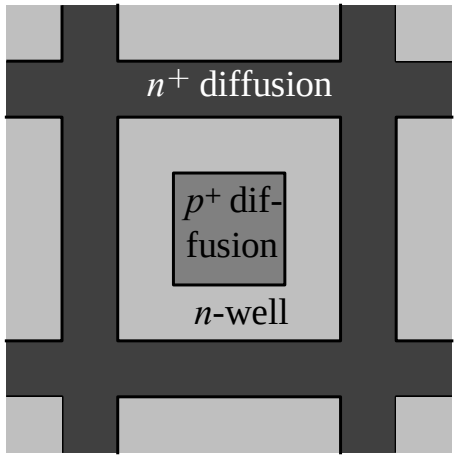
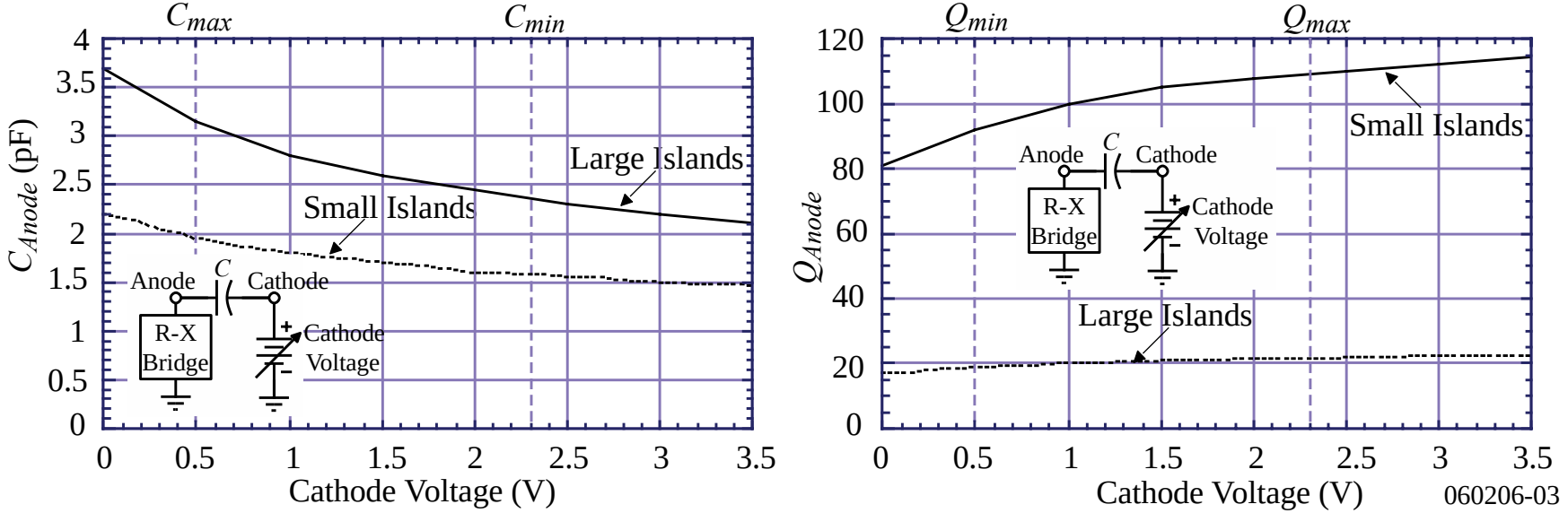


Fig. 2.5-1A

PN-Junction Capacitors – Continued

The anode should be the floating node and the cathode must be connected to ac ground.

Experimental data (Q at 2GHz, 0.5µm CMOS)†:



Terminal Under Test	Small Islands (598 1.2µm x1.2µm)			Large Islands (42 9µm x 9µm)		
	C_{max}/C_{min}	Q_{min}	Q_{max}	C_{max}/C_{min}	Q_{min}	Q_{max}
Anode	1.23	94.5	109	1.32	19	22.6
Cathode	1.21	8.4	9.2	1.29	8.6	9.5

Electrons as majority carriers lead to higher Q because of their higher mobility.

The resistance, R_{wj}, is reduced in small islands compared with large islands ⇒ higher Q

† E. Pedersen, "RF CMOS Varactors for 2GHz Applications," *Analog Integrated Circuits and Signal Processing*, vol. 26, pp. 27-36, Jan. 2001.

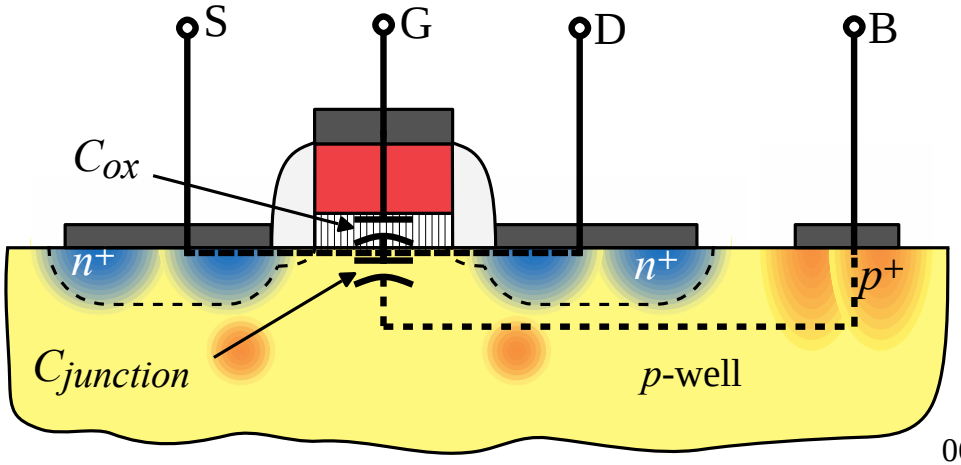
MOSFET GATE CAPACITORS

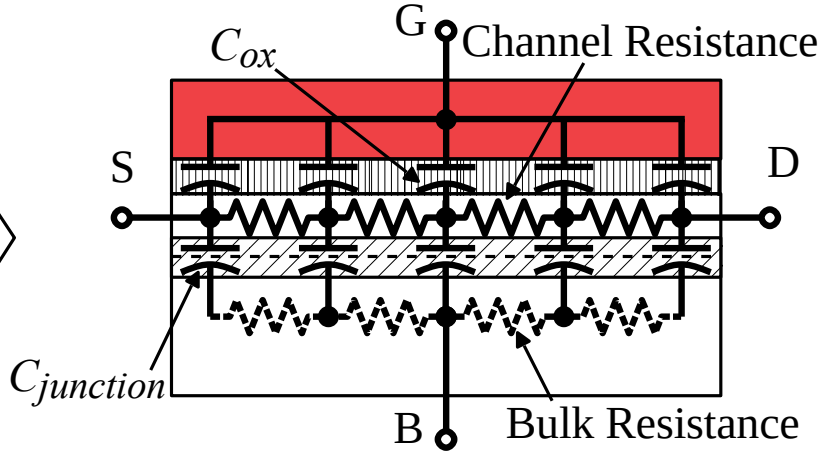
MOSFET Gate Capacitor Structure

The MOSFET gate capacitors have the gate as one terminal of the capacitor and some combination of the source, drain, and bulk as the other terminal.

In the model of the MOSFET gate capacitor shown below, the gate capacitance is really two capacitors in series depending on the condition of the channel.

$$C_{gate} = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_j}}$$





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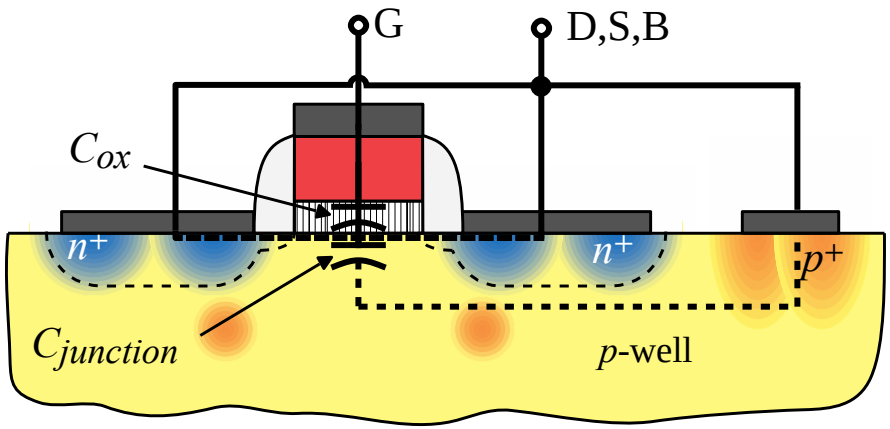
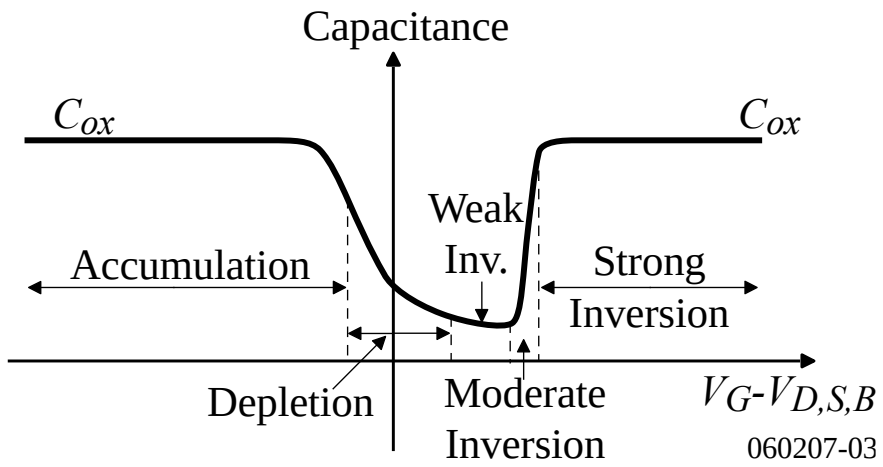
MOSFET Gate Capacitor as a function of V_{GS} with D=S=B





Operation:

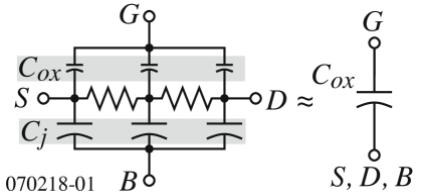
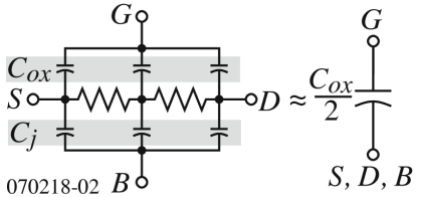
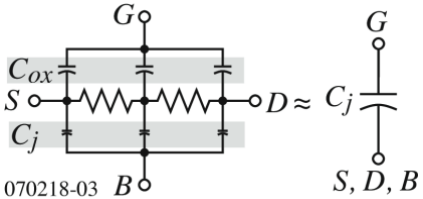
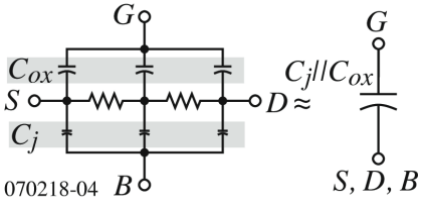
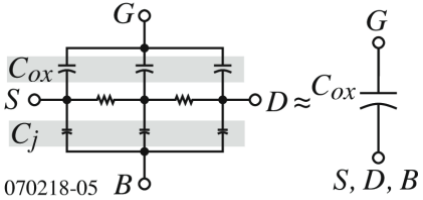
In this configuration, the MOSFET gate capacitor has 5 regions of operation as V_{GS} is varied. They are:

1.) Accumulation
2.) Depletion
3.) Weak inversion
4.) Moderate inversion
5.) Strong inversion

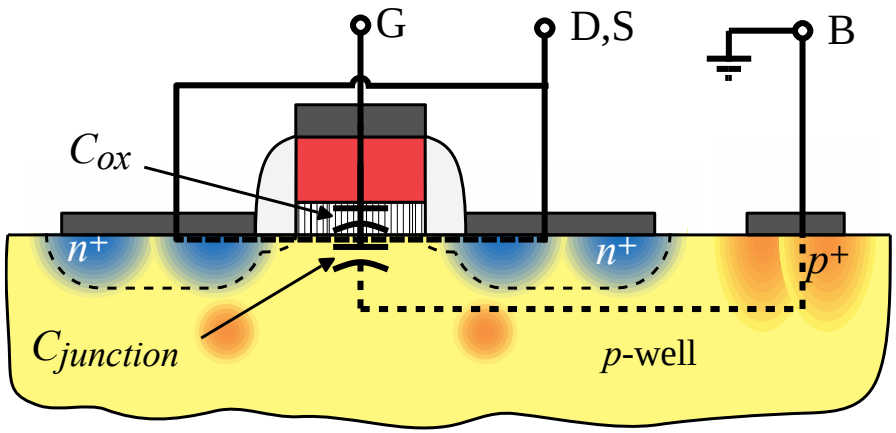
For the first four regions, the gate capacitance is the series combination of C_{ox} and C_j given as,

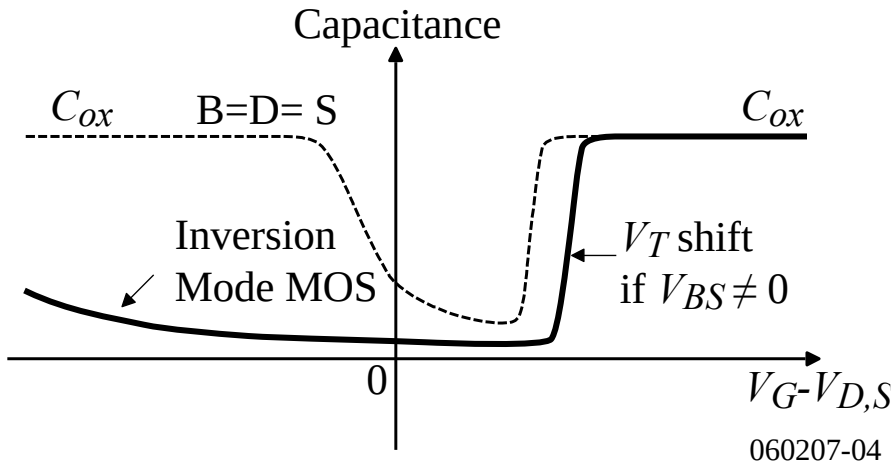
$$C_{\text{gate}} = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_j}}$$

Use of a 3 Segment Model to Explain the Gate Capacitor Variation

Region	Channel R	C_{ox} and C_j	C_{gate}	3-Segment Model
Accumulation	Large	In series and $C_j > C_{ox}$	$C_{\text{gate}} \approx C_{ox}$	
Depletion	Large	In series and $C_j \approx C_{ox}$	$C_{\text{gate}} \approx 0.5C_{ox} \approx 0.5C_j$	
Weak Inversion	Large	In series and $C_j < C_{ox}$	$C_{\text{gate}} \approx C_j$	
Moderate Inversion	Moderate	In series and $C_j < C_{ox}$	$C_j < C_{\text{gate}} < C_{ox}$	
Strong Inversion	Small	In parallel and $C_j < C_{ox}$	$C_{\text{gate}} \approx C_{ox}$	

MOSFET Gate Capacitor as a function of V_{GS} with Bulk Fixed (Inversion Mode)





Conditions:

- D = S, B = V_{SS}
- Accumulation region removed by connecting bulk to ground
- Nonlinear
- Channel resistance:

$$R_{on} = \frac{L}{12K_P'(V_{BG}-|V_T|)}$$

- LDD transistors will give lower Q because of the increased series resistance

Inversion Mode NMOS Capacitor

Best results are obtained when the drain-source are connected to ac ground.

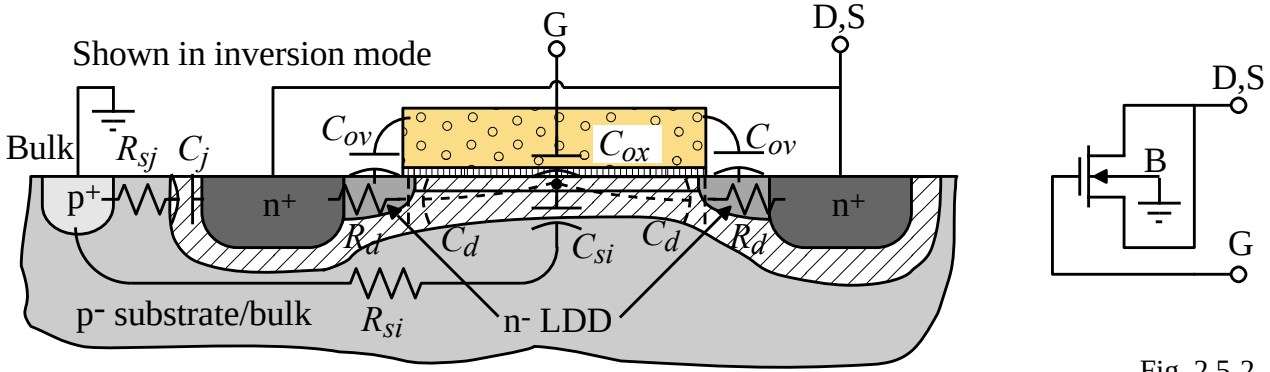
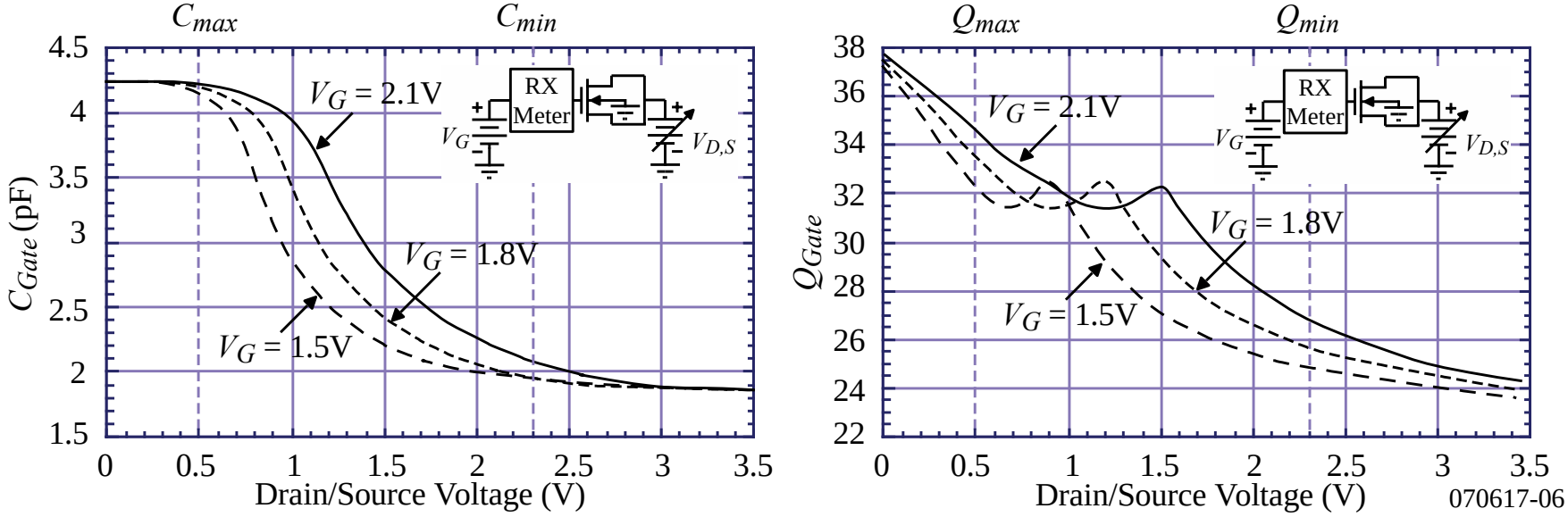


Fig. 2.5-2

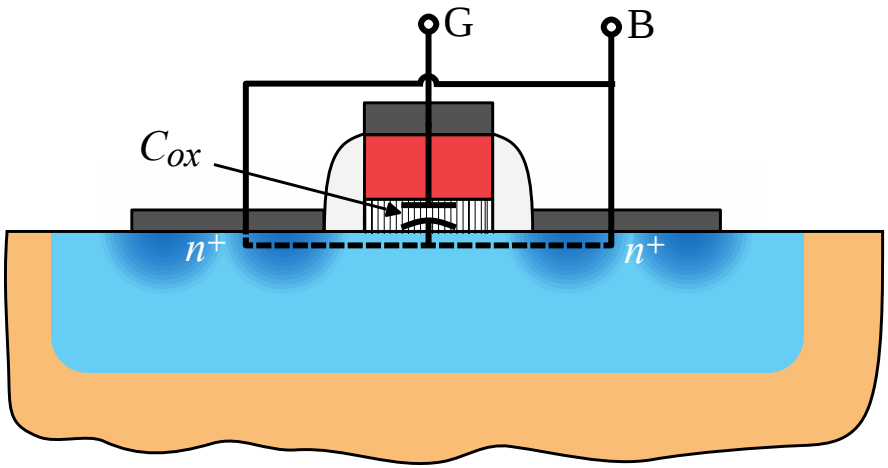
Experimental Results (Q at 2GHz, 0.5µm CMOS)†:

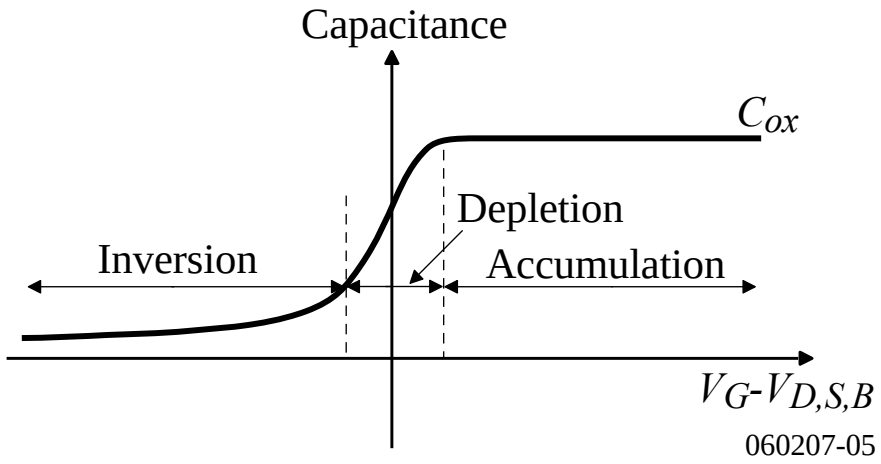


V_G =1.8V: C_{max}/C_{min} ratio = 2.15 (1.91), Q_{max} = 34.3 (5.4), and Q_{min} = 25.8(4.9)

† E. Pedersen, "RF CMOS Varactors for 2GHz Applications," *Analog Integrated Circuits and Signal Processing*, vol. 26, pp. 27-36, Jan. 2001.

Accumulation Mode NMOS Gate Capacitor





Conditions:

- Build the NMOS in a *n*-well or the PMOS in a *p*-well – channel is present with no bias
- Implements a variable capacitor with a larger transition region between the maximum and minimum values.
- Reasonably linear capacitor for values of V_G-$V_{D,S,B} > 0$

Accumulation Mode Capacitor – Continued

Best results are obtained when the drain-source are on ac ground.

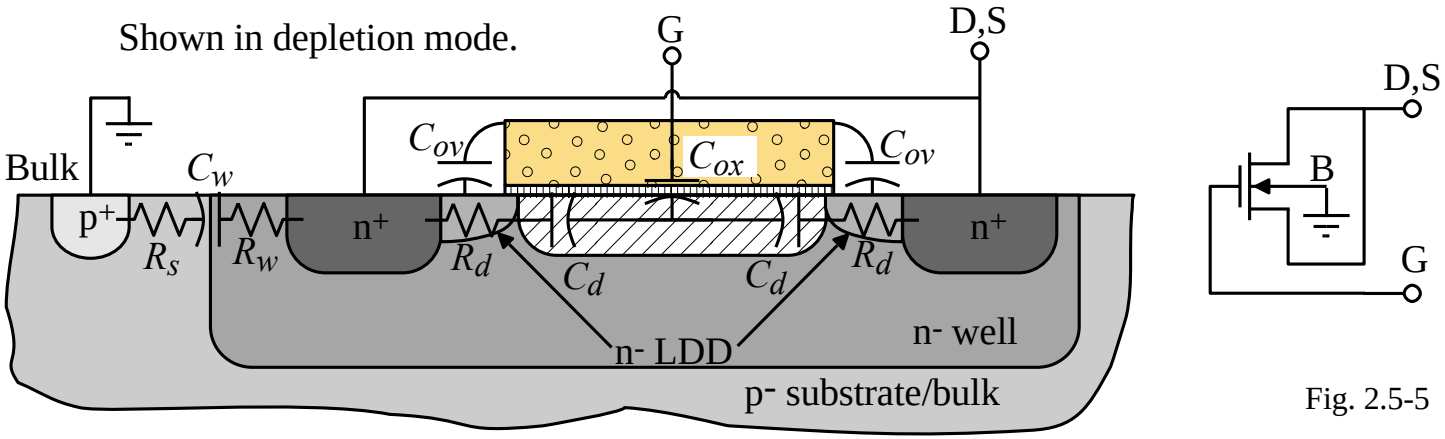
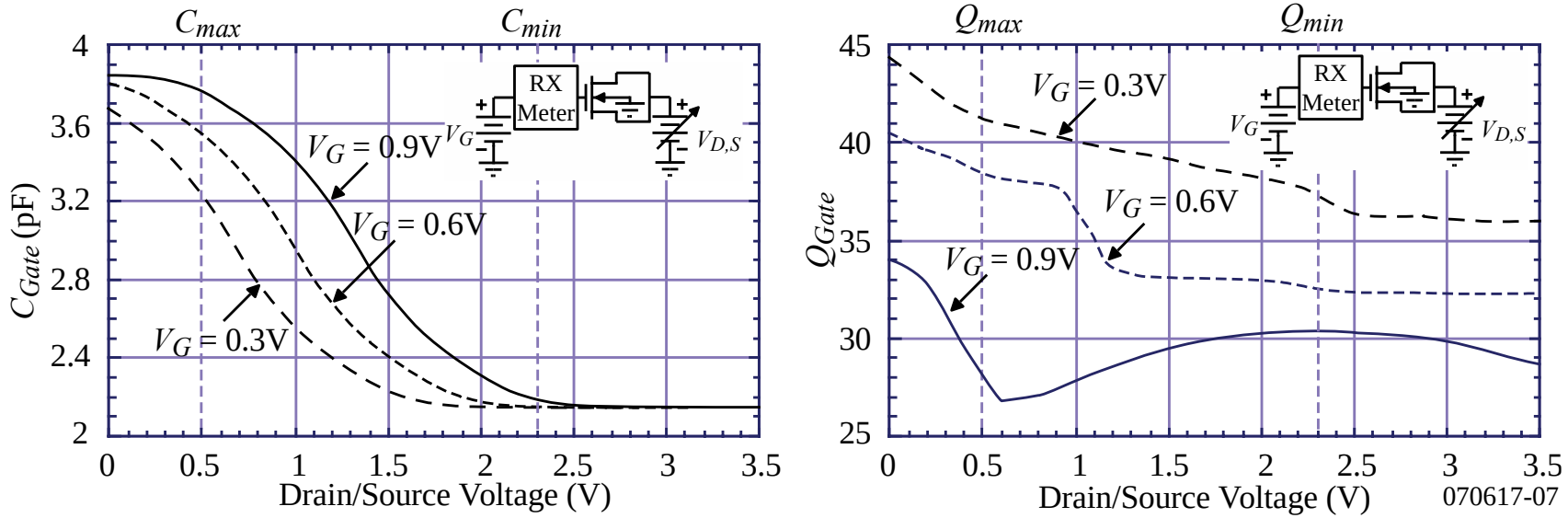


Fig. 2.5-5

Experimental Results (Q at 2GHz, 0.5µm CMOS)†:



V_G = 0.6V: C_{max}/C_{min} ratio = 1.69 (1.61), Q_{max} = 38.3 (15.0), and Q_{min} = 33.2(13.6)

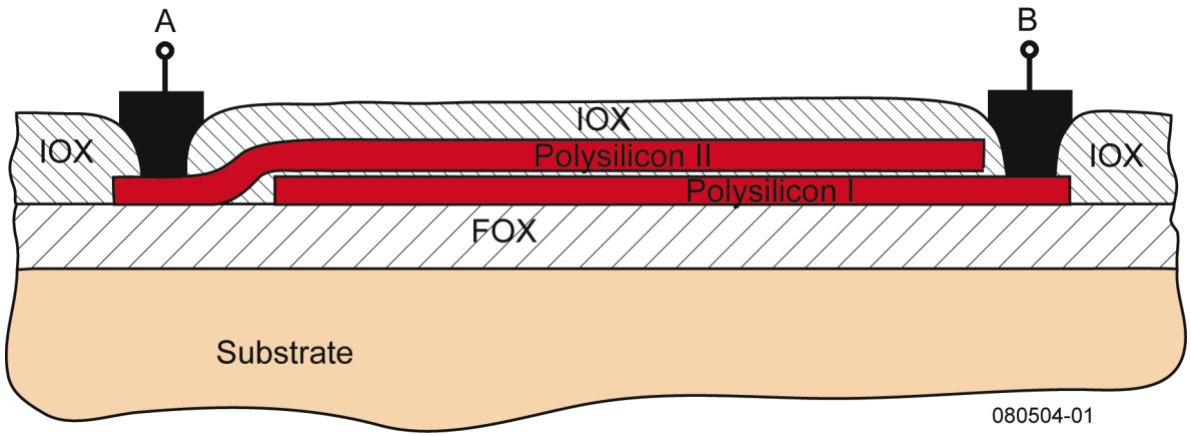
† E. Pedersen, "RF CMOS Varactors for 2GHz Applications," *Analog Integrated Circuits and Signal Processing*, vol. 26, pp. 27-36, Jan. 2001.

CONDUCTOR-INSULATOR-CONDUCTOR CAPACITORS

Polysilicon-Oxide-Polysilicon (Poly-Poly) Capacitors

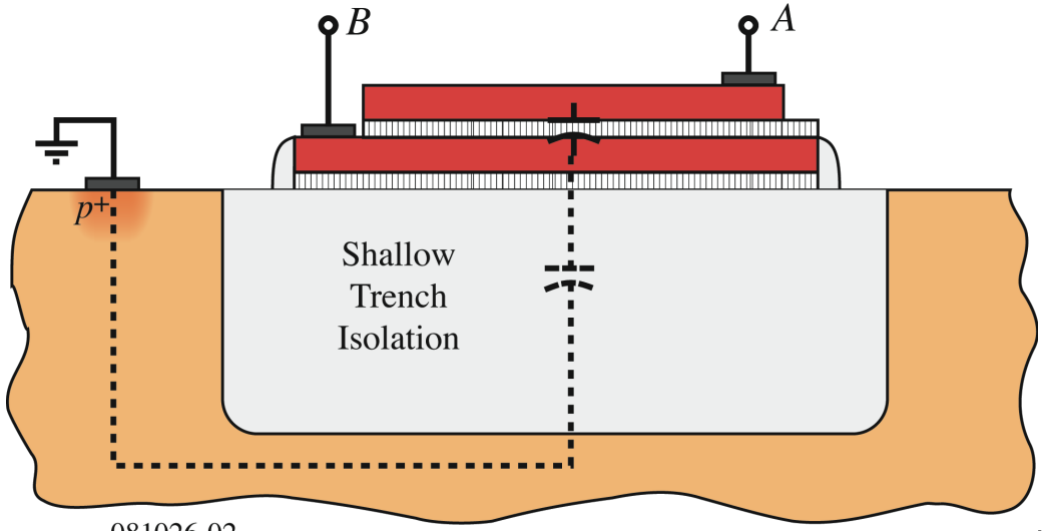
LOCOS Technology:

A very linear capacitor with minimum bottom plate parasitic.



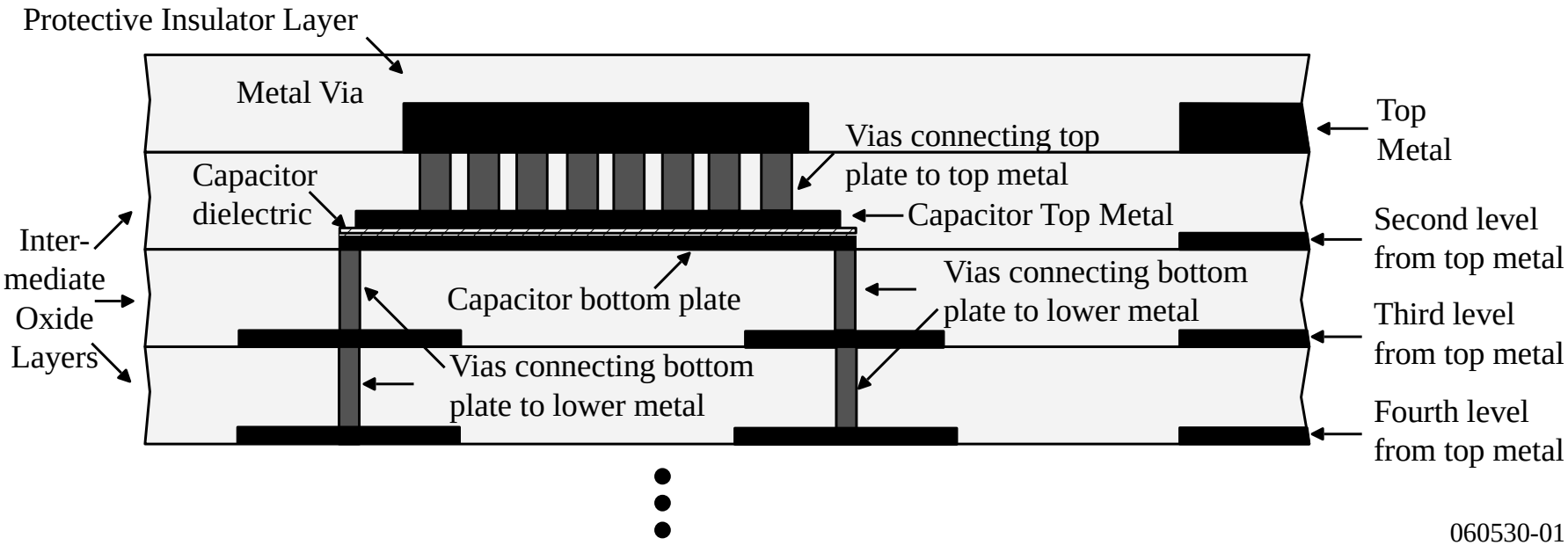
DSM Technology:

A very linear capacitor with small bottom plate parasitic.



Metal-Insulator-Metal (MiM) Capacitors

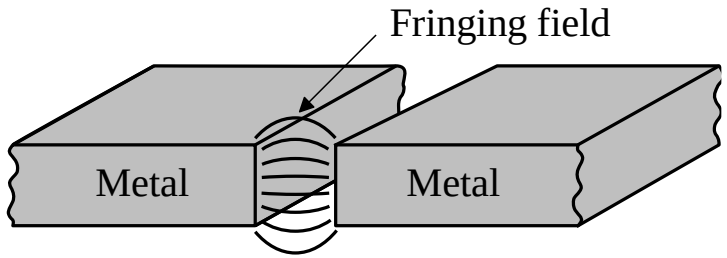
In some processes, there is a thin dielectric between a metal layer and a special metal layer called "capacitor top metal". Typically the capacitance is around 1fF/μm^2 and is at the level below top metal.



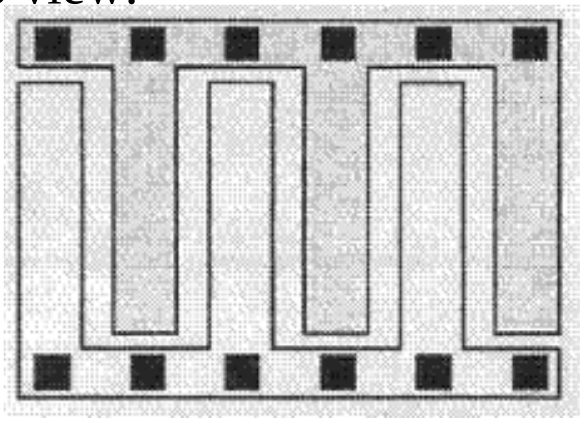
Good matching is possible with low parasitics.

Metal-Insulator-Metal Capacitors – Lateral and Vertical Flux

Capacitance between conductors on the same level and use lateral flux.



Top view:



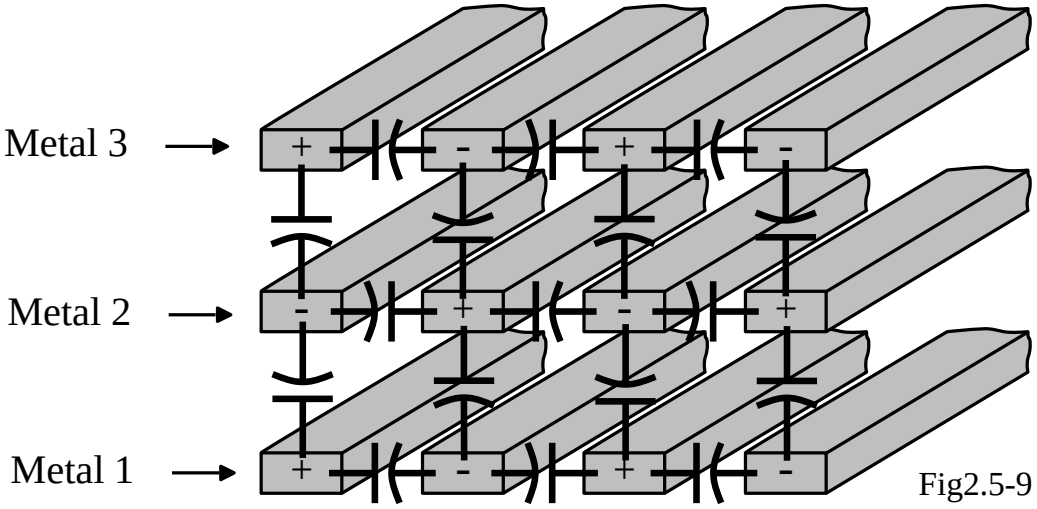
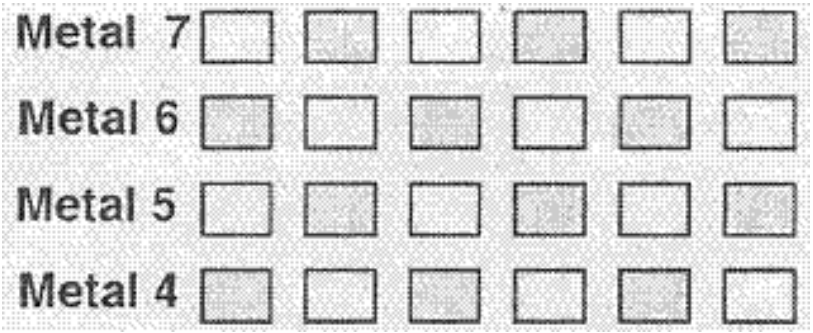


Fig2.5-9

Side view:

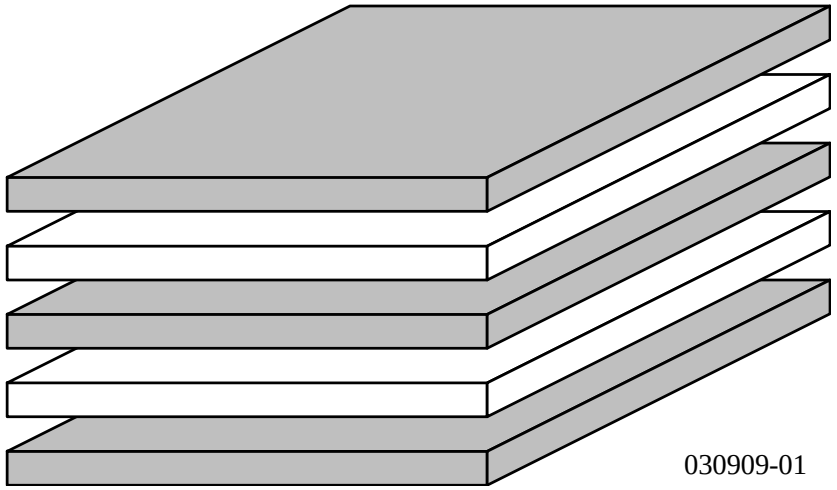


These capacitors are sometimes called fractal capacitors because the fractal patterns are structures that enclose a finite area with a near-infinite perimeter.
The capacitor/area can be increased by a factor of 10 over vertical flux capacitors.

More Detail on Horizontal Metal Capacitors†

Some of the possible metal capacitor structures include:

1.) Horizontal parallel plate (HPP).



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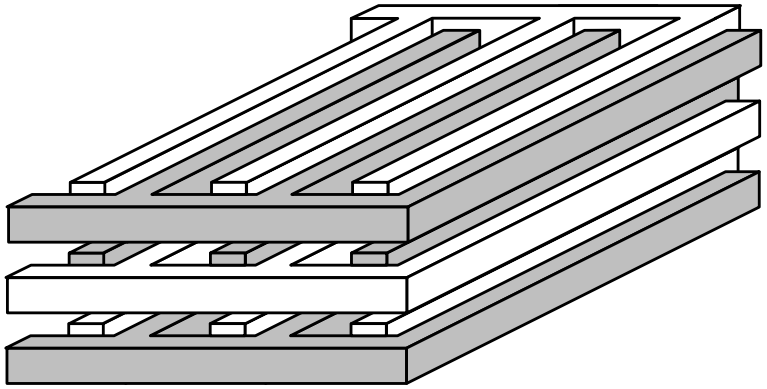
2.) Parallel wires (PW):



Lateral View

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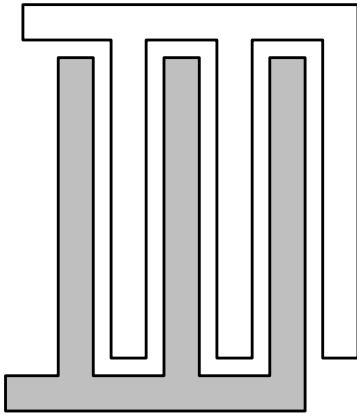
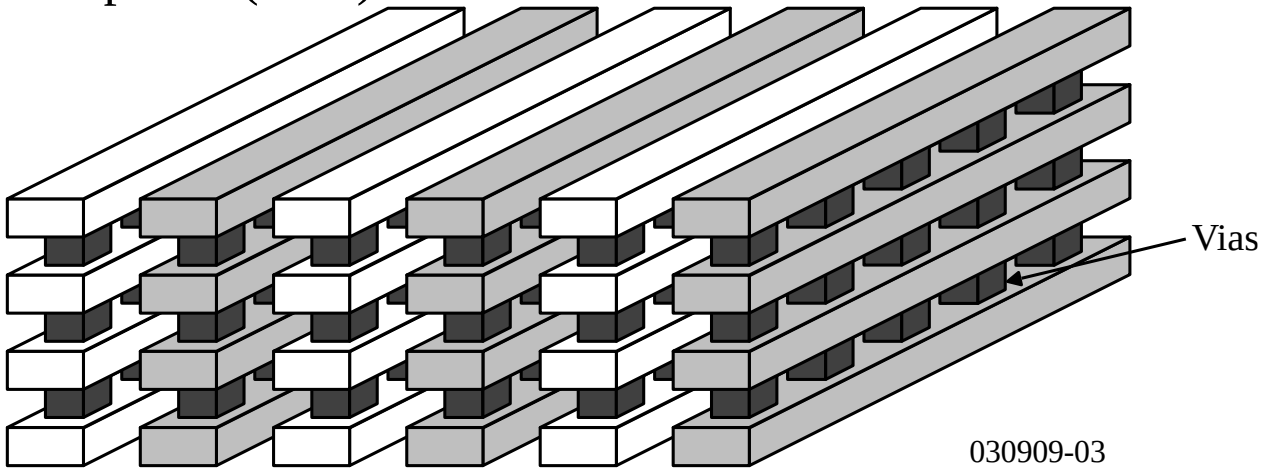


Top View

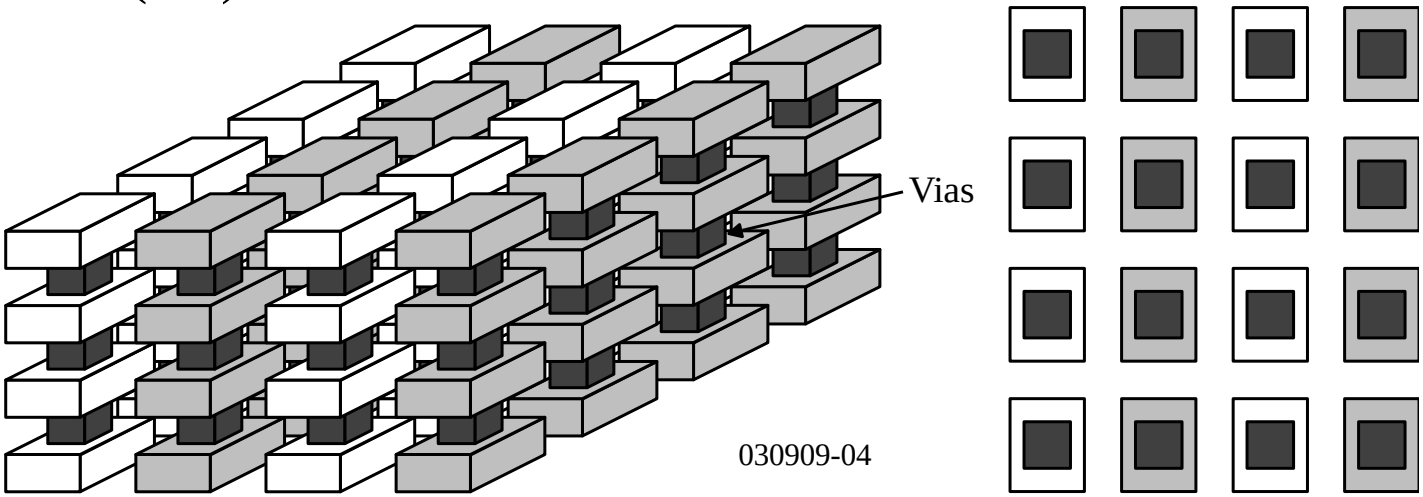
† R. Aparicio and A. Hajimiri, "Capacity Limits and Matching Properties of Integrated Capacitors, *IEEE J. of Solid-State Circuits*, vol. 37, no. 3, March 2002, pp. 384-393.

Horizontal Metal Capacitors - Continued

3.) Vertical parallel plates (VPP):



4.) Vertical bars (VB):

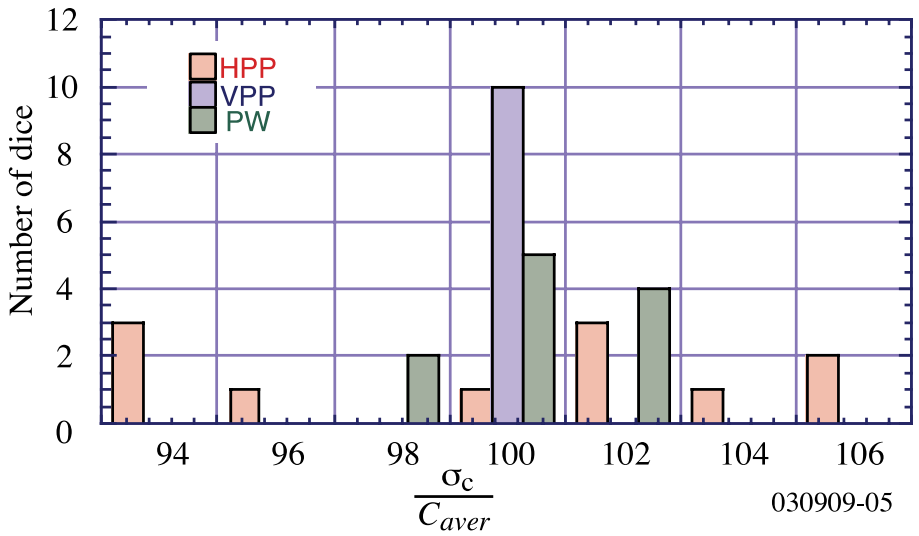


Horizontal Metal Capacitors - Continued

Experimental results for a digital CMOS process with 7 layers of metal, L_{min} =0.24µm, t_{ox} = 0.7µm and t_{metal} = 0.53µm for the bottom 5 layers of metal. All capacitors = 1pF.

Structure (1 pF)	Cap. Density (aF/µm^2)	$C_{aver.}$ (pF)	Area (µm^2)	Cap. Enhancement	Std. Dev. (fF)	$\frac{\sigma}{C_{aver.}}$	$f_{res.}$ (GHz)	Q @ 1 GHz	Break-down (V)
VPP	1512.2	1.01	670	7.4	5.06	0.0050	> 40	83.2	128
VB	1281.3	1.07	839.7	6.3	14.19	0.0132	37.1	48.7	124
HPP	203.6	1.09	5378	1.0	26.11	0.0239	21	63.8	500
MIM	1100	1.05	960.9	5.4	-	-	11	95	-

Histogram of the capacitance distribution:



Result: The horizontal metal capacitors have a matching accuracy that is equivalent of the better capacitors – poly-poly and MIM.

DEVIATION FROM IDEAL BEHAVIOR IN CAPACITORS

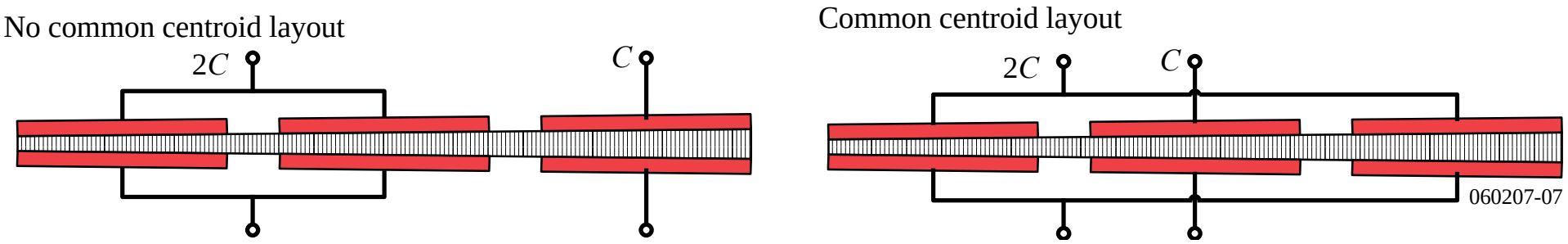
Capacitor Errors

1.) Dielectric gradients
2.) Edge effects
3.) Process biases
4.) Parasitics
5.) Voltage dependence
6.) Temperature dependence

Capacitor Errors - Oxide Gradients

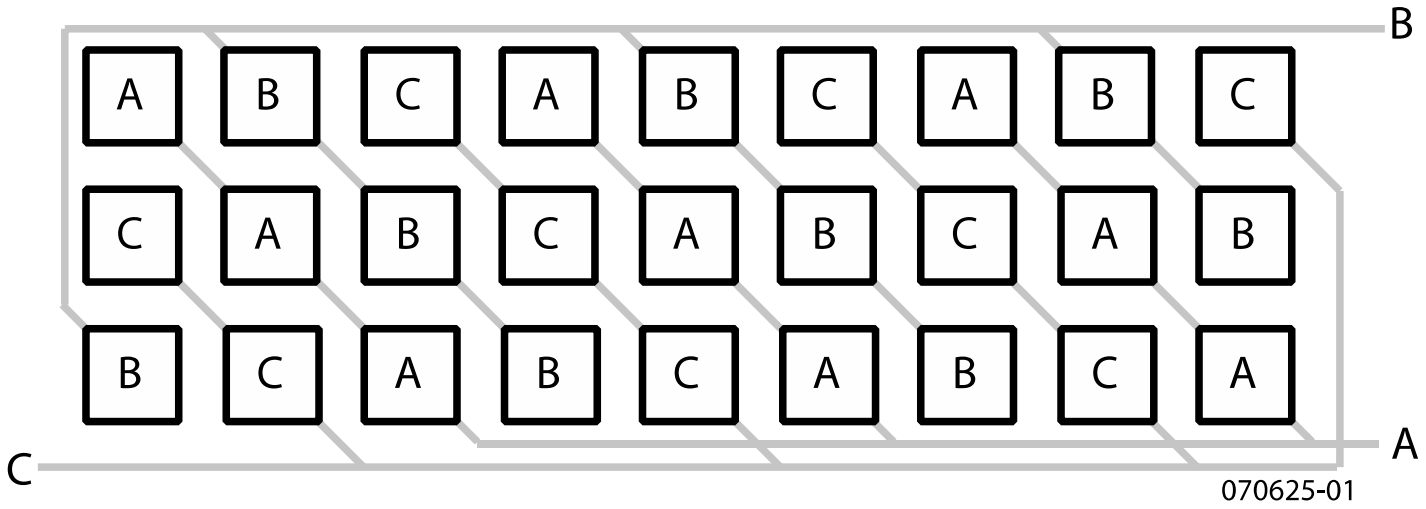
Error due to a variation in dielectric thickness across the wafer.

Common centroid layout - only good for one-dimensional errors:



An alternate approach is to layout numerous repetitions and connect them randomly to achieve a statistical error balanced over the entire area of interest.

Improved matching of three components, *A*, *B*, and *C*:



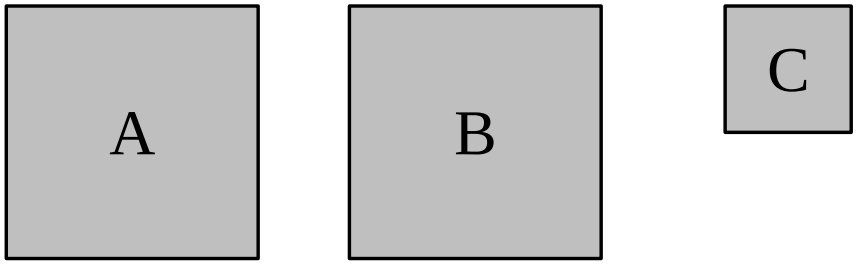
Capacitor Errors - Edge Effects

There will always be a randomness on the definition of the edge.

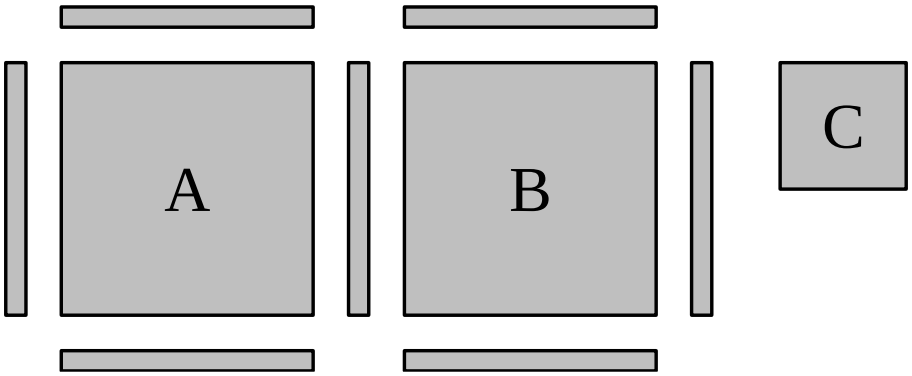
However, etching can be influenced by the presence of adjacent structures.

For example,

Matching of A and B are disturbed by the presence of C.

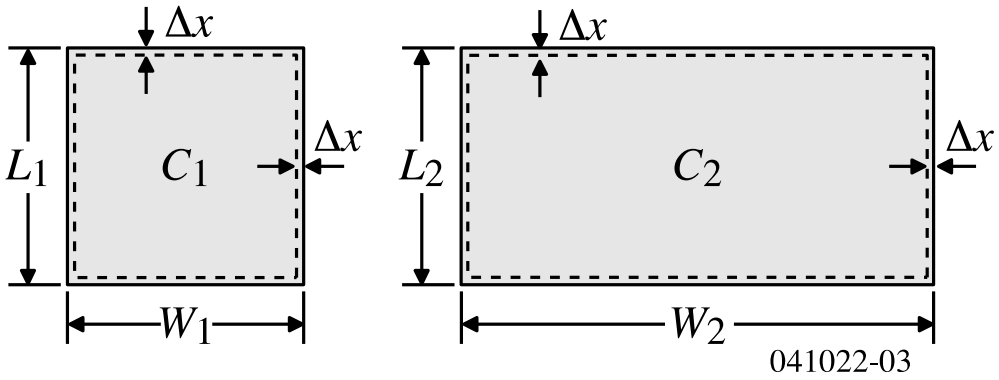


Improved matching achieve by matching the surroundings of A and B.



Process Bias on Capacitors

Consider the following two capacitors:



If $L_1 = L_2 = 2\mu m$, $W_2 = 2W_1 = 4\mu m$ and $\Delta x = 0.1\mu m$, the ratio of C_2 to C_1 can be written as,

$$\frac{C_2}{C_1} = \frac{(2\text{-}.2)(4\text{-}.2)}{(2\text{-}.2)(2\text{-}.2)} = \frac{3.8}{1.8} = 2.11 \quad \rightarrow \quad 5.6\% \text{ error in matching}$$

How can this matching error be reduced?

The capacitor ratios in general can be expressed as,

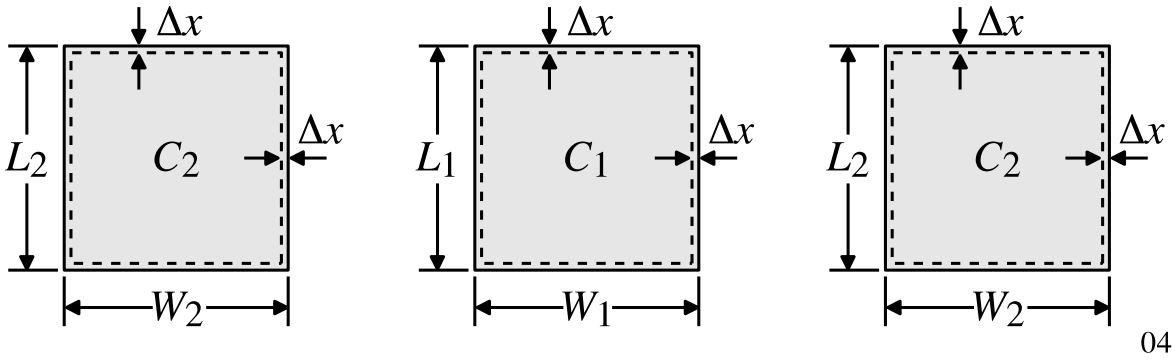
$$\frac{C_2}{C_1} = \frac{(L_2\text{-}2\Delta x)(W_2\text{-}2\Delta x)}{(L_1\text{-}2\Delta x)(W_1\text{-}2\Delta x)} = \frac{W_2}{W_1}\left(\frac{1 - \frac{2\Delta x}{W_2}}{1 - \frac{2\Delta x}{W_1}}\right) \approx \frac{W_2}{W_1}\left(1 - \frac{2\Delta x}{W_2}\right)\left(1 + \frac{2\Delta x}{W_1}\right) \approx \frac{W_2}{W_1}\left(1 - \frac{2\Delta x}{W_2} + \frac{2\Delta x}{W_1}\right)$$

Therefore, if $W_2 = W_1$, the matching error should be minimized. The best matching results between two components are achieved when their geometries are identical.

Replication Principle

Based on the previous result, a way to minimize the matching error between two or more geometries is to insure that the matched components have the same area to periphery ratio. Therefore, the replication principle requires that all geometries have the same area-periphery ratio.

Correct way to match the previous capacitors (the two C_2 capacitors are connected together):



If $L_1 = L_2 = 2\mu m$, $W_2 = 2W_1 = 2\mu m$ and $\Delta x = 0.1\mu m$, the ratio of C_2 to C_1 can be written as,

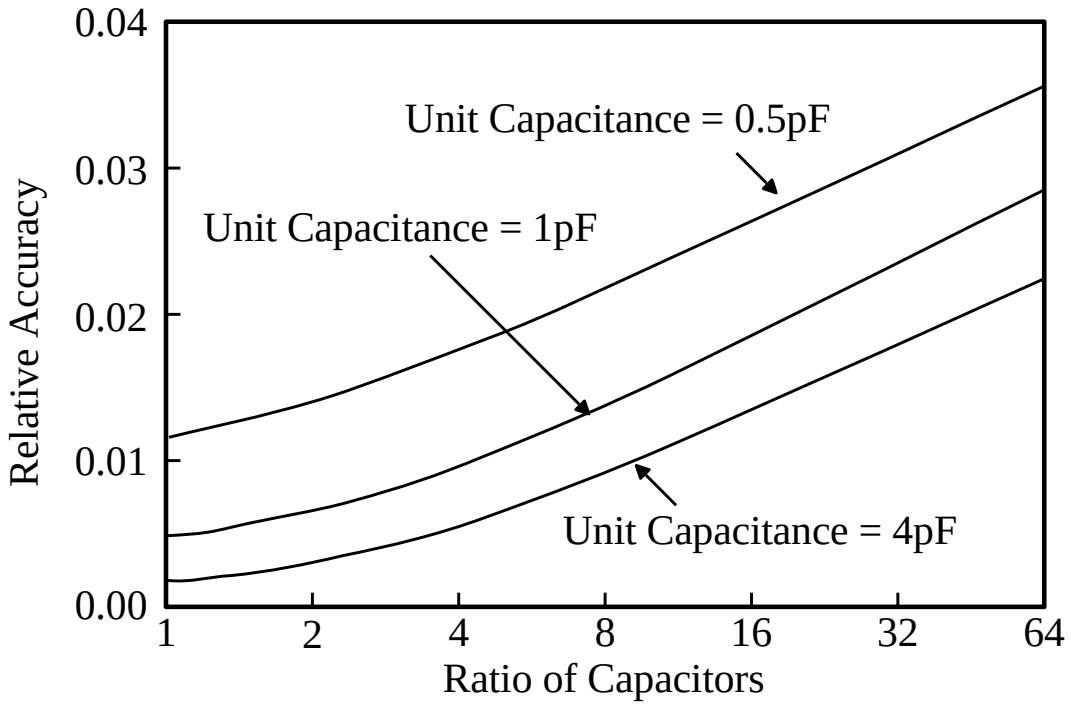
$$\frac{C_2}{C_1} = \frac{2(2\text{-}.2)(2\text{-}.2)}{(2\text{-}.2)(2\text{-}.2)} = \frac{2 \cdot 1.8}{1.8} = 2 \quad \rightarrow \text{ 0\% error in matching}$$

The replication principle works for any geometry and includes transistors, resistors as well as capacitors.

Capacitor Errors - Relative Accuracy

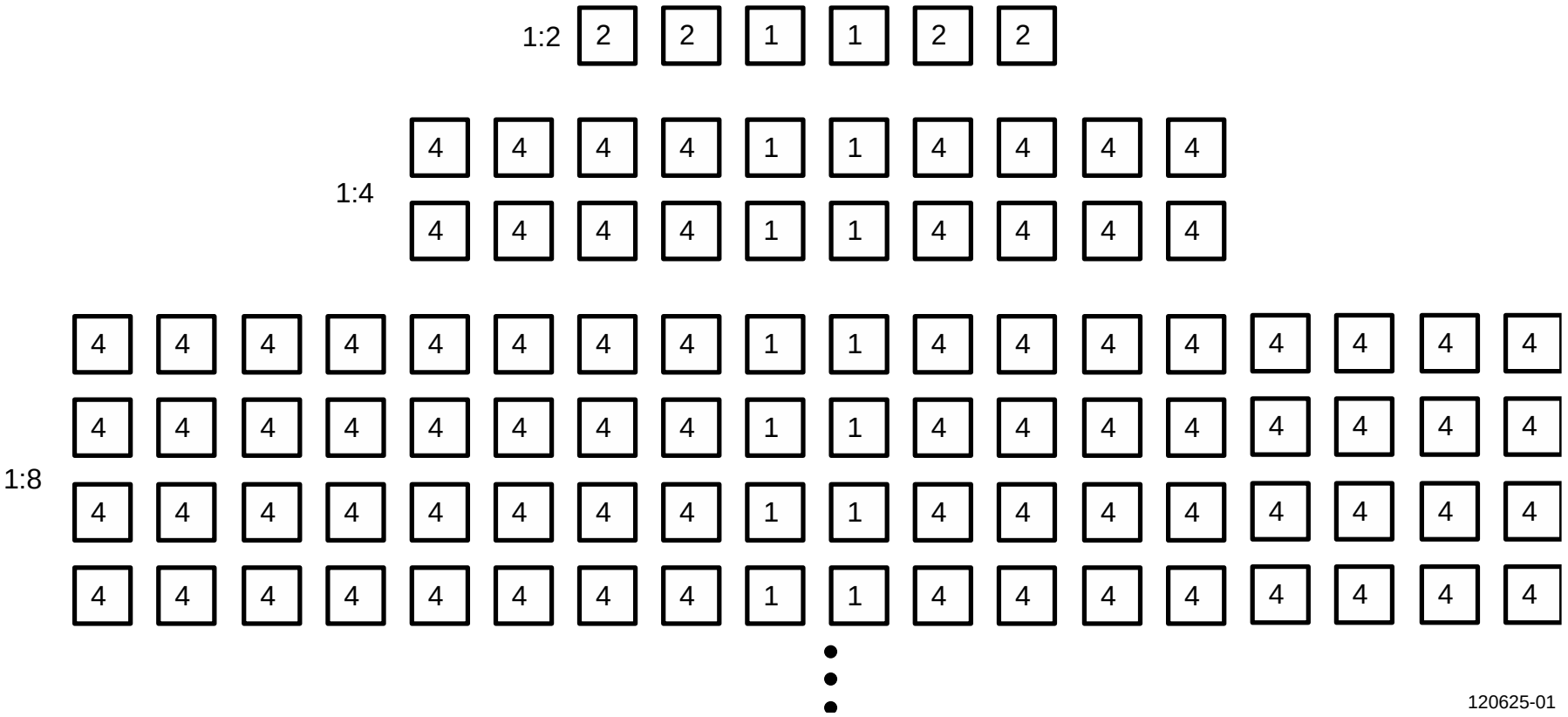
Capacitor relative accuracy is proportional to the area of the capacitors and inversely proportional to the difference in values between the two capacitors.

For example,



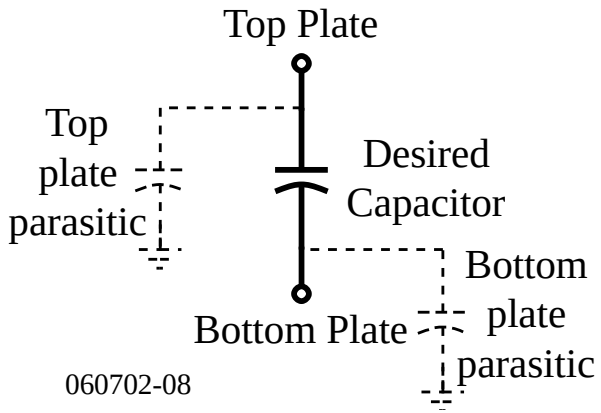
How to Keep the Relative Accuracy Constant as Ratio Increases

The following scheme will tend to keep the relative accuracy constant as a function of the ratio of capacitors. Of course the tradeoff for this accuracy is area.



Capacitor Errors - Parasitics

Parasitics are normally from the top and bottom plate to ac ground which is typically the substrate.

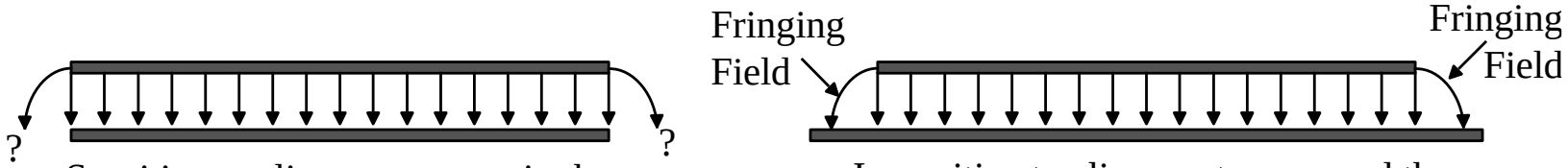


Top plate parasitic is 0.01 to 0.001 of $C_{desired}$

Bottom plate parasitic is 0.05 to 0.2 $C_{desired}$

Layout Considerations on Capacitor Accuracy

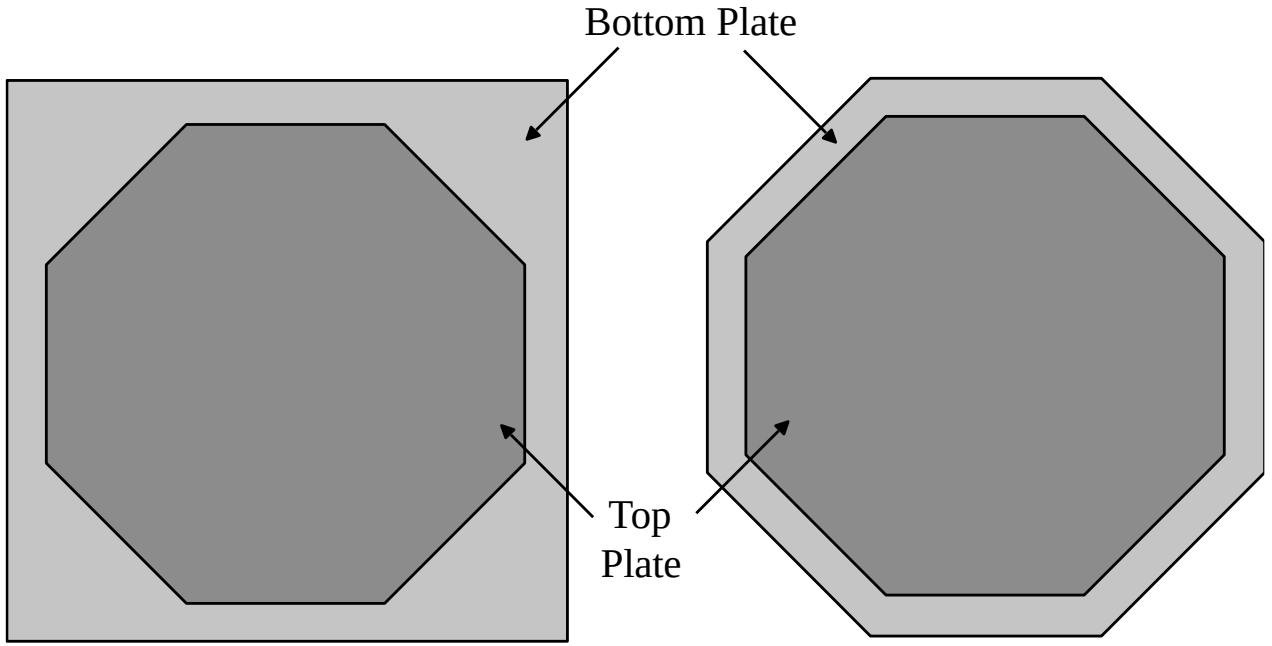
Decreasing Sensitivity to Edge Variation:



Sensitive to alignment errors in the upper and lower plates and loss of capacitance flux (smaller capacitance).

Insensitive to alignment errors and the flux reaching the bottom plate is larger resulting in large capacitance. 060207-09

A structure that minimizes the ratio of perimeter to area (circle is best).



060207-10

Reduced bottom plate parasitic.

Accurate Matching of Capacitors†

Accurate matching of capacitors depends on the following influence:

1.) Mismatched perimeter ratios

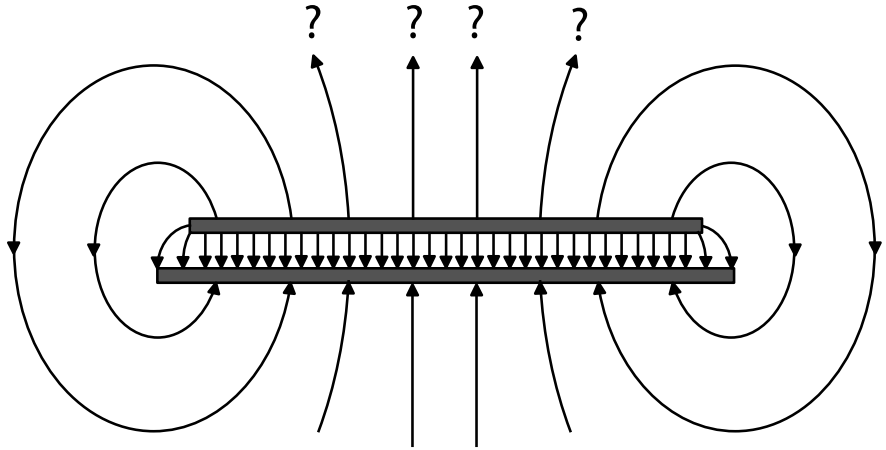
2.) Proximity effects in unit capacitor photolithography

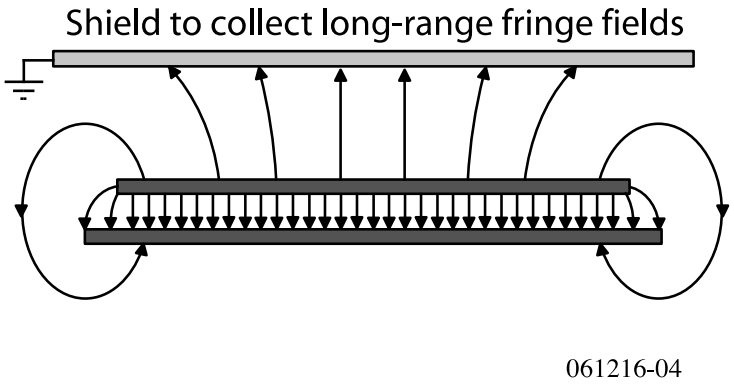
3.) Mismatched long-range fringe capacitance

4.) Mismatched interconnect capacitance

5.) Parasitic interconnect capacitance

Long-range fringe capacitance:





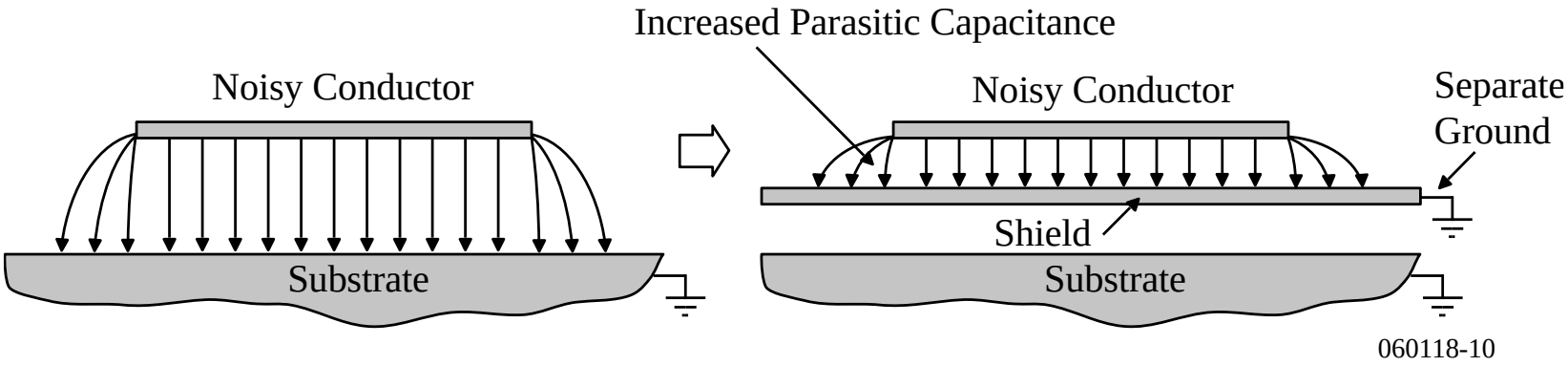
Obviously there will be a tradeoff between matching and speed.

† M.J. McNutt, S. LeMarquis and J.L.Dunkley, "Systematic Capacitance Matching Errors and Corrective Layout Procedures," *IEEE J. of Solid-State Circuit*, vo. 29, No. 5, May 1994, pp. 611-616.

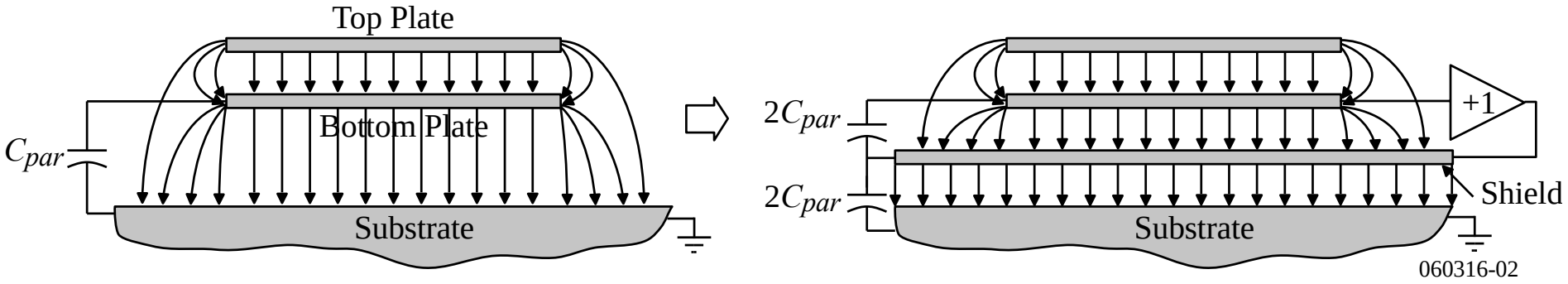
Shielding

The key to shielding is to determine and control the electric fields.

Consider the following noisy conductor and its influence on the substrate:



Use of bootstrapping to reduce capacitor bottom plate parasitic:



Definition of Temperature and Voltage Coefficients

In general a variable y which is a function of x, $y = f(x)$, can be expressed as a Taylor series,

$$y(x) \approx y(x_0) + a_1(x - x_0) + a_2(x - x_0)^2 + a_3(x - x_0)^3 + \cdots$$

where the coefficients, a_i, are defined as,

$$a_1 = \frac{df(x)}{dx}\Big|_{x=x_0}, \; a_2 = \frac{1}{2}\frac{d^2f(x)}{dx^2}\Big|_{x=x_0}, \; \ldots.$$

The coefficients, a_i, are called the first-order, second-order, …. temperature or voltage coefficients depending on whether x is temperature or voltage.

Generally, only the first-order coefficients are of interest.

In the characterization of temperature dependence, it is common practice to use a term called *fractional temperature coefficient*, TC_F, which is defined as,

$$TC_F(T=T_0) = \frac{1}{f(T=T_0)}\frac{df(T)}{dT}\Big|_{T=T_0} \text{ parts per million/°C (ppm/°C)}$$

or more simply,

$$TC_F = \frac{1}{f(T)}\frac{df(T)}{dT} \text{ parts per million/°C (ppm/°C)}$$

A similar definition holds for fractional voltage coefficient.

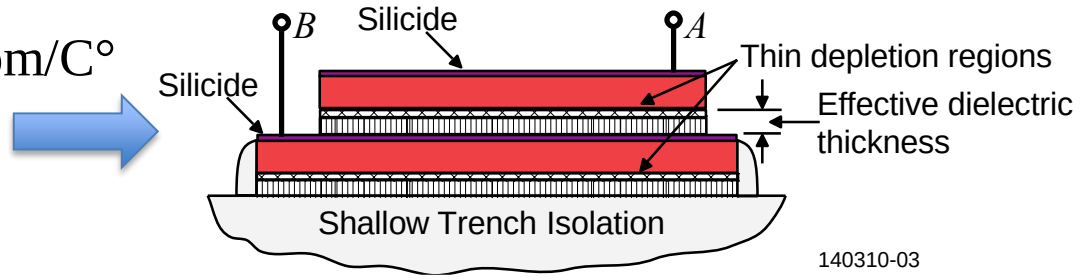
Capacitor Errors - Temperature and Voltage Dependence

MOSFET Gate Capacitors:

- Absolute accuracy ≈ ±10%
- Relative accuracy ≈ ±0.2%
- Temperature coefficient ≈ +25 ppm/C°
- Voltage coefficient ≈ -50ppm/V

Polysilicon-Oxide-Polysilicon Capacitors:

- Absolute accuracy ≈ ±10%
- Relative accuracy ≈ ±0.2%
- Temperature coefficient ≈ +25 ppm/C°
- Voltage coefficient ≈ -20ppm/V



Metal-Dielectric-Metal Capacitors:

- Absolute accuracy ≈ ±10%
- Relative accuracy ≈ ±0.6%
- Temperature coefficient ≈ +40 ppm/C°
- Voltage coefficient ≈ -20ppm/V, 5ppm/V^2

Accuracies depend upon the size of the capacitors.

SUMMARY

- Capacitors are made from:
  - *pn* junctions (depletion capacitors)
  - MOSFET gate capacitors
  - Conductor-insulator-conductor capacitors
- Capacitors are characterized by:
  - *Q*, a measure of the loss
  - Density
  - Parasitics
  - Absolute and relative accuracies
- Deviations from ideal capacitor behavior include;
  - Dielectric gradients
  - Edge effects (etching)
  - Process biases
  - Parasitics
  - Voltage and temperature dependence