LECTURE 04 - ULTRA-DEEP SUBMICRON AND BiCMOS TECHNOLOGIES

LECTURE ORGANIZATION

Outline

- Ultra-deep submicron CMOS technology
  - Features
  - Advantages
  - Problems
- BiCMOS technology process flow
  - CMOS is typical submicron (0.5 μm)
- Summary

***CMOS Analog Circuit Design*, 3rd Edition Reference**

New material

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ULTRA-DEEP SUBMICRON (UDSM) CMOS TECHNOLOGY

USDM Technology

- $L_{min} \leq 0.1$ microns
- Minimum feature size less than 100 nanometers
- Today's state of the art:
    - 22 nm drawn length
    - 5 nm lateral diffusion (12 nm gate length)
    - 1 nm transistor gate oxide
    - 8 layers of copper interconnect
- Specialized processing is used to increase drive capability and maintain low off currents

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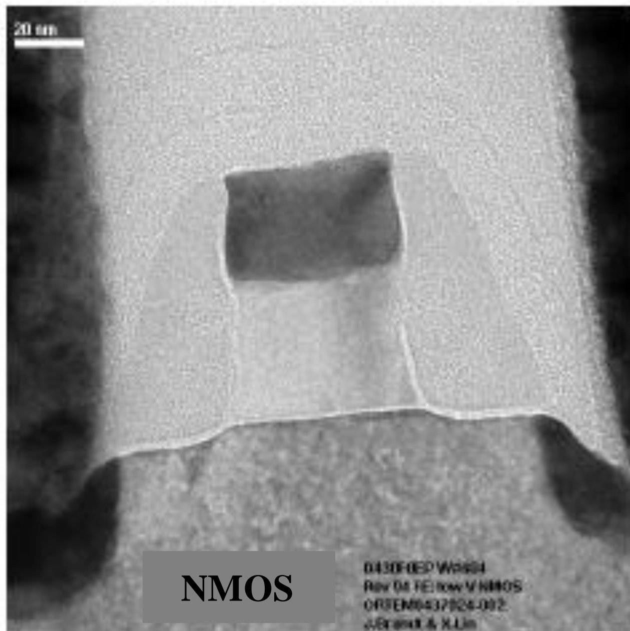
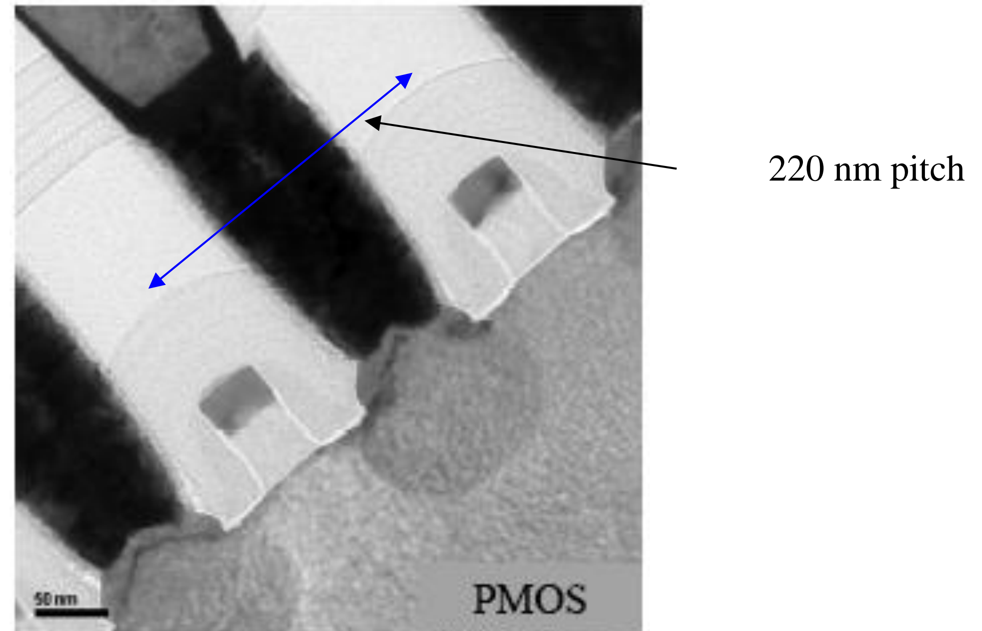
65 Nanometer CMOS Technology

TEM cross-section of a 35 nm NMOS and PMOS transistors.†

NMOS:



PMOS:



These transistors utilize enhanced channel strains to increase drive capability and to reduce off currents.

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† P. Bai, et. Al., "A 65nm Lobic Technology Featuring 35nm Gate Lengths, Enhanced Channel Strain, 8 Cu Interconnect Layers, Low-k ILD and 0.57 μm^2 SRAM Cell, *IEEE Inter. Electron Device Meeting*, Dec. 12-15, 2005.

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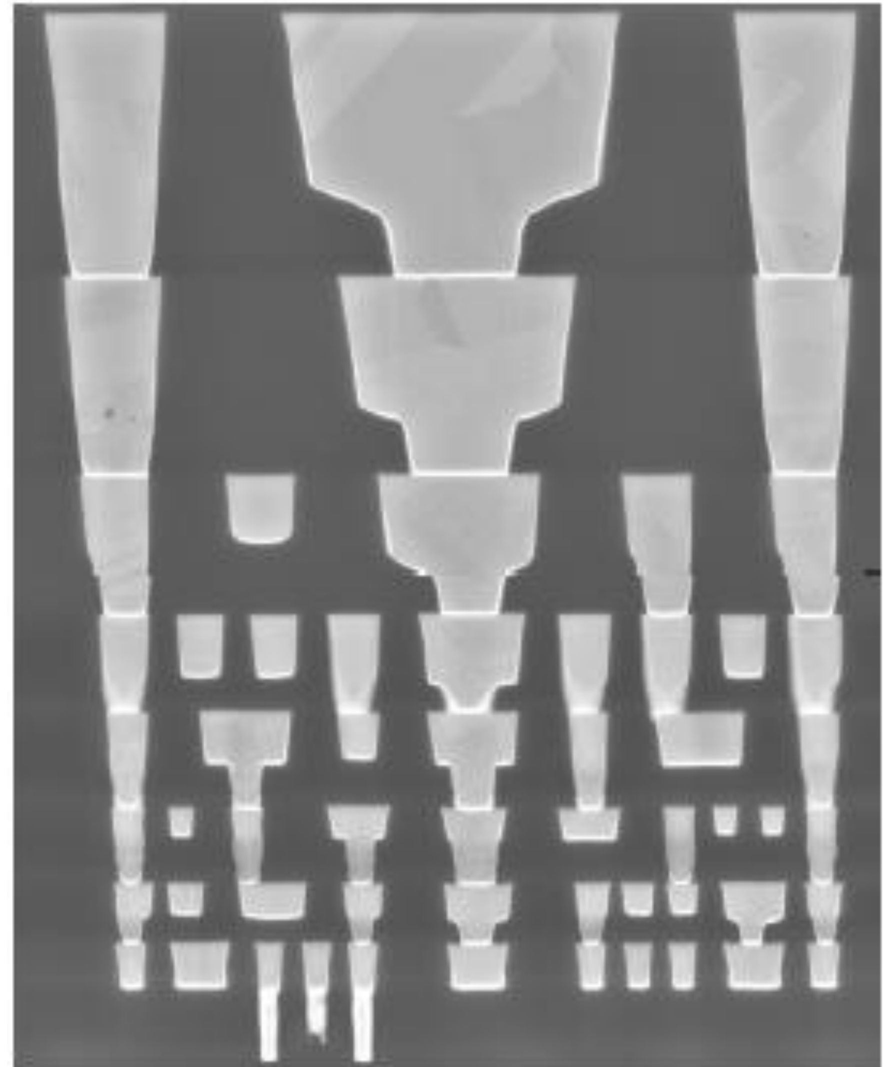
UDSM Metal and Interconnects

Physical aspects:

Layer	Pitch (nm)	Thickness (nm)	Aspect Ratio
Isolation	220	230	-
Polysilicon	220	90	-
Contacted Gate Pitch	220	-	-
Metal 1	210	170	1.6
Metal 2	210	190	1.8
Metal 3	220	200	1.8
Metal 4	280	250	1.8
Metal 5	330	300	1.8
Metal 6	480	430	1.8
Metal 7	720	650	1.8
Metal 8	1080	975	1.8



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What are the Advantages of UDSM CMOS Technology?

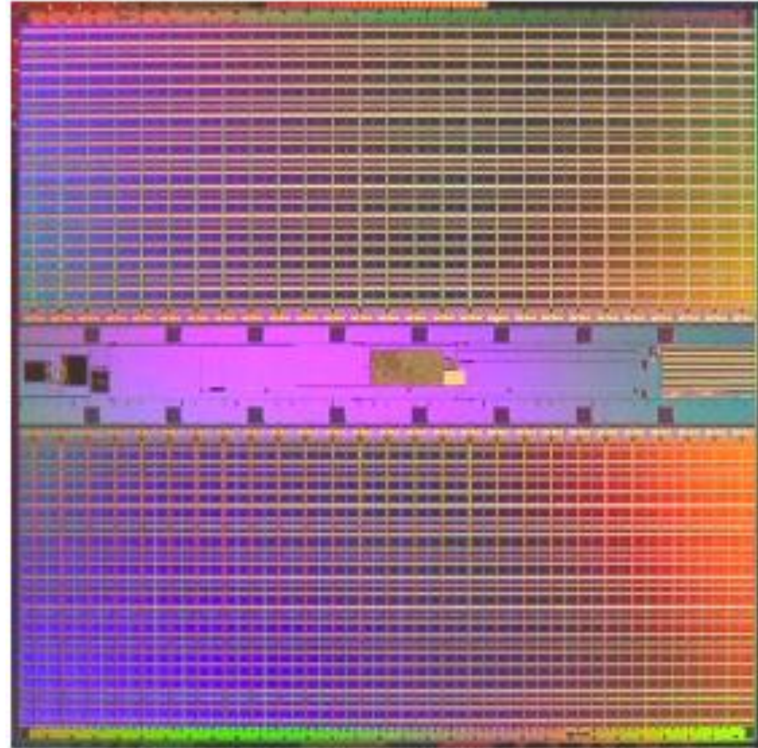
Digital Viewpoint:

- Improved I_{on}/I_{off}
- Reduced gate capacitance
- Higher drive current capability
- Reduced interconnect density
- Reduction of active power

Analog Viewpoint:

- More levels of metal
- Higher f_T
- Higher capacitance density
- Reduced junction capacitance per g_m
- More speed

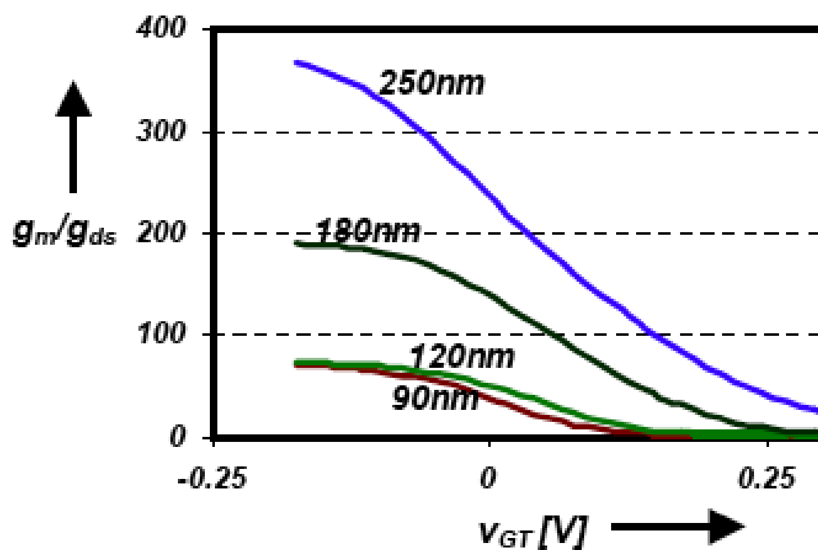
70 Mbit SRAM chip:

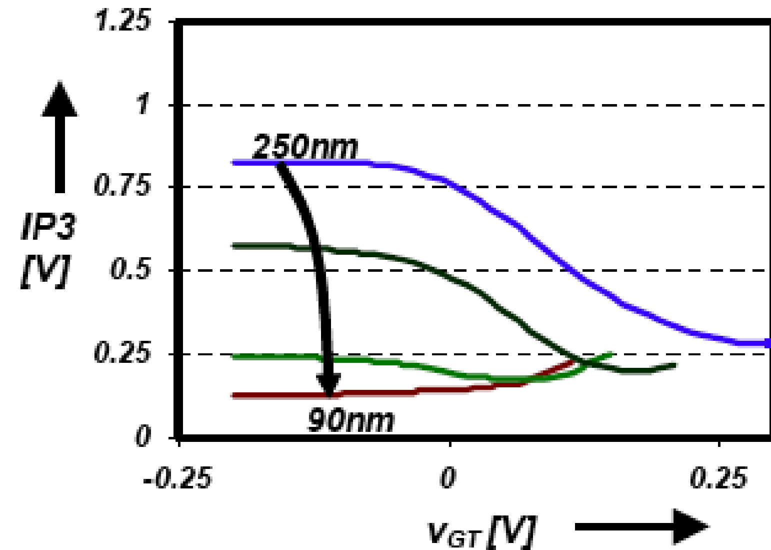


What are the Disadvantages of UDSM CMOS Technology (for Analog)?

- Reduction in power supply resulting in reduced headroom
- Gate leakage currents
- Reduced small-signal intrinsic gains
- Increased nonlinearity (IIP3)
- Increased noise and poorer matching (smaller area)

Intrinsic gain and IP3 as a function of the gate overdrive for decreasing V_{DS}:†





† Anne-Johan Annema, et. Al., "Analog Circuits in Ultra-Deep-Submicron CMOS," *IEEE J. of Solid-State Circuits*, Vol. 40, No. 1, Jan. 2005, pp. 132-143.

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What is the Gate Leakage Problem?

Gate current occurs in thin oxide devices due to direct tunneling through the thin oxide.

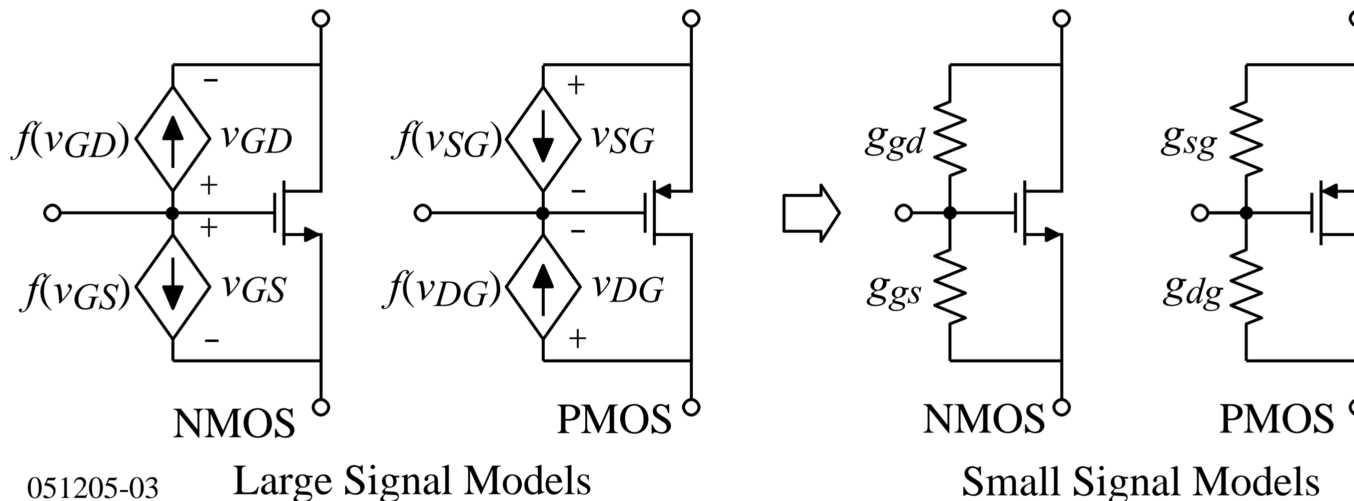
Gate current depends on:

1.) The gate-source voltage (and the drain-gate voltage)

$$i_{GS} = K_1 v_{GS} \exp(K_2 v_{GS}) \quad \text{and} \quad i_{GD} = K_3 v_{GD} \exp(K_4 v_{GD})$$

2.) Gate area – NMOS leakage ≈ 6nA/μm^2 and PMOS leakage ≈ 3nA/μm^2

Unfortunately, the gate leakage current is nonlinear with respect to the gate-source and gate-drain voltages. A possible model is:



Base current cancellation schemes used for BJTs are difficult to apply to the MOSFET.

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UDSM CMOS Technology Summary

- Increased transconductance and frequency capability
- Low power supply voltages
- Reduced parasitics
- Gate leakage causes challenges for analog applications of UDSM technology
  - Can no longer use the MOSFET for capacitance
  - Conflict between matching and gate leakage
- Other issues
  - Noise
  - Zero temperature coefficient behavior
  - Etc.

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BiCMOS TECHNOLOGY

Typical 0.5µm BiCMOS Technology

Masking Sequence:

1. Buried n^+ layer
2. Buried p^+ layer
3. Collector tub
4. Active area
5. Collector sinker
6. *n*-well
7. *p*-well
8. Emitter window
9. Base oxide/implant
10. Emitter implant
11. Poly 1
12. NMOS lightly doped drain
13. PMOS lightly doped drain
14. n^+ source/drain
15. p^+ source/drain
16. Silicide protection
17. Contacts
18. Metal 1
19. Via 1
20. Metal 2
21. Via 2
22. Metal 3
23. Nitride passivation

Notation used in the following slides:

BSPG = Boron and Phosphorus doped Silicate Glass (oxide)

Kooi Nitride = A thin layer of silicon nitride on the silicon surface as a result of the reaction of silicon with the HN3 generated, during the field oxidation.

TEOS = Tetro-Ethyl-Ortho-Silicate. A chemical compound used to deposit conformal oxide films.

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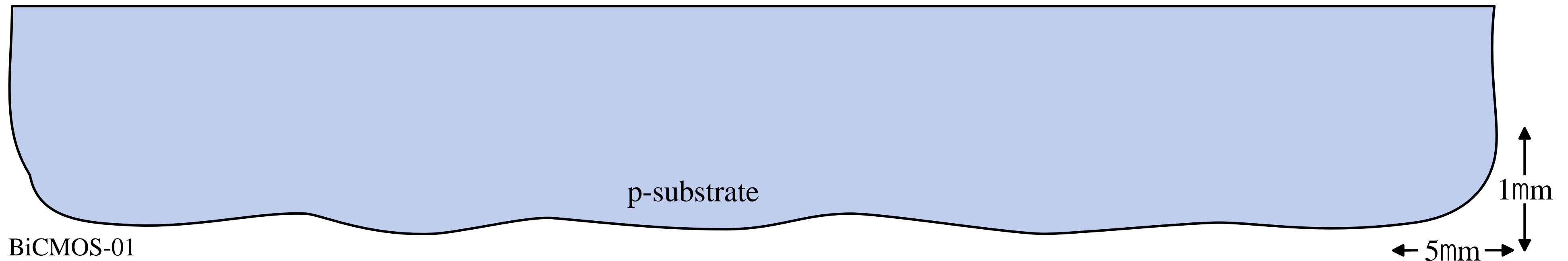
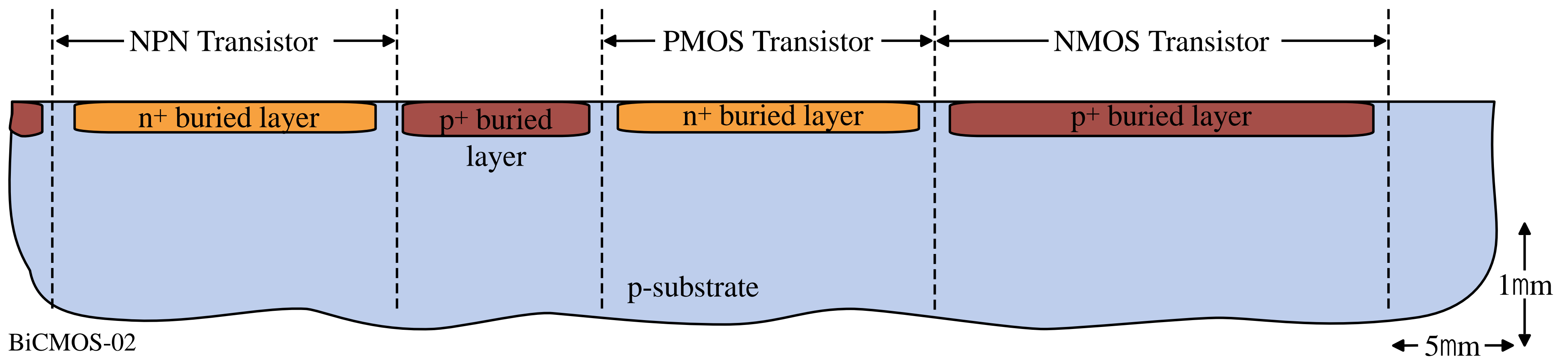
n^+ and p^+ Buried Layers

Starting Substrate:



n^+ and p^+ Buried Layers:



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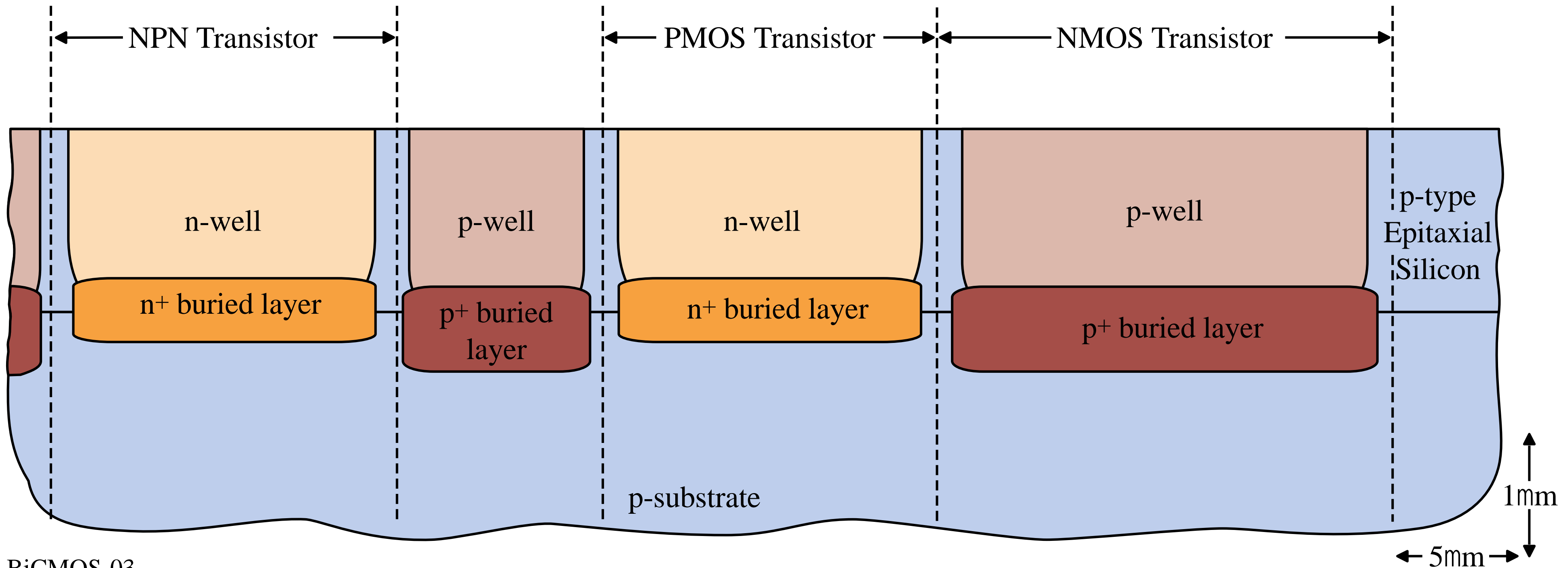
Epitaxial Growth



Comment:

- As the epi layer grows vertically, it assumes the doping level of the substrate beneath it.
- In addition, the high temperature of the epitaxial process causes the buried layers to diffuse upward and downward.

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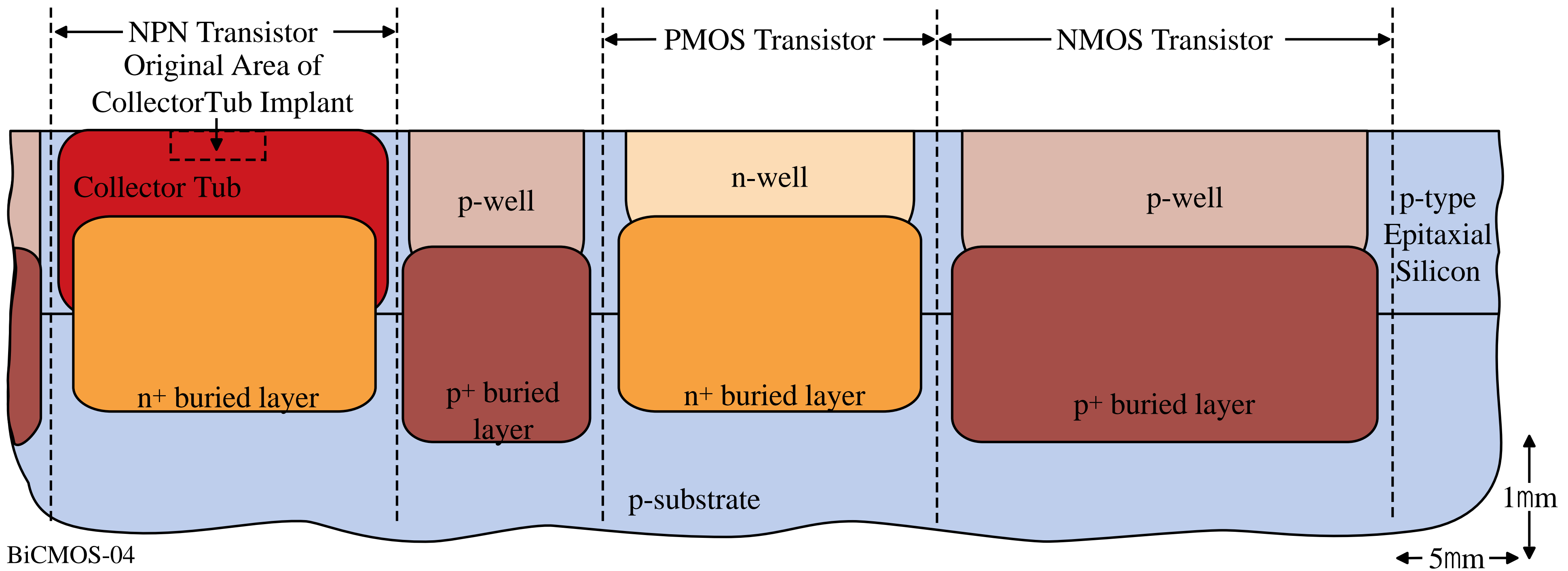
Collector Tub



Comment:

- The collector area is developed by an initial implant followed by a drive-in diffusion to form the collector tub.

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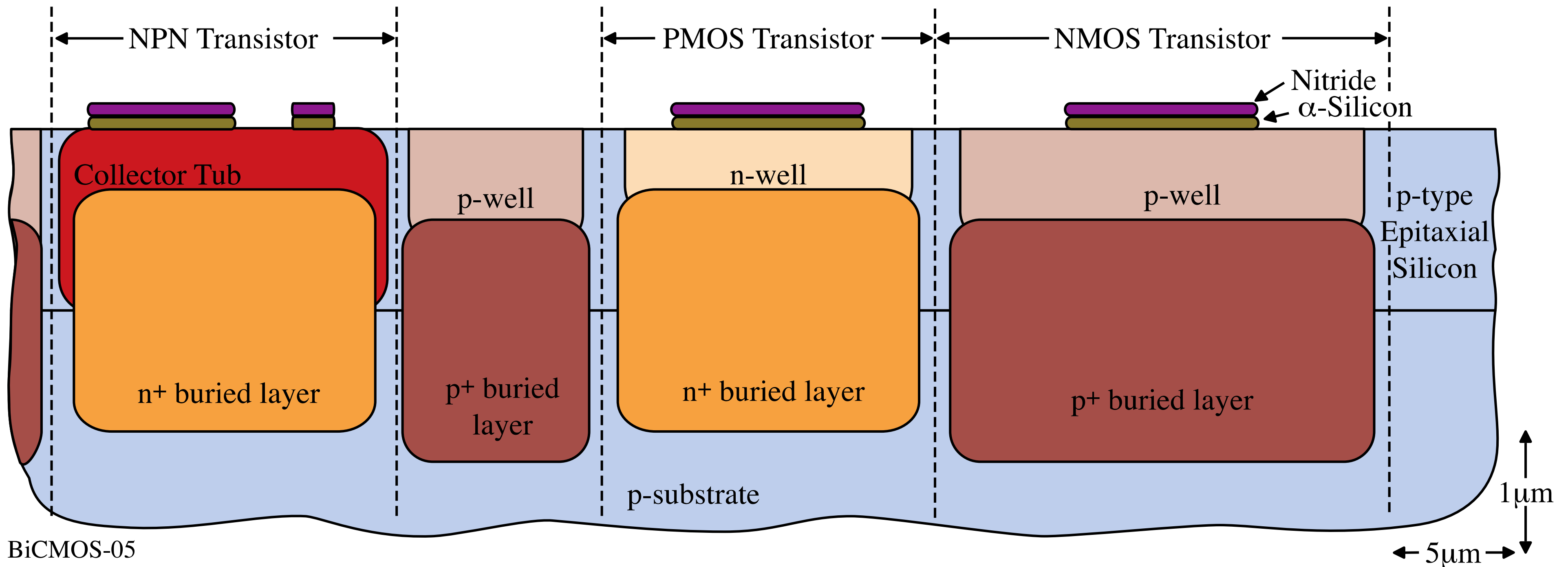
Active Area Definition



Comment:

- The silicon nitride is use to impede the growth of the thick oxide which allows contact to the substrate
- α-silicon is used for stress relief and to minimize the bird's beak encroachment

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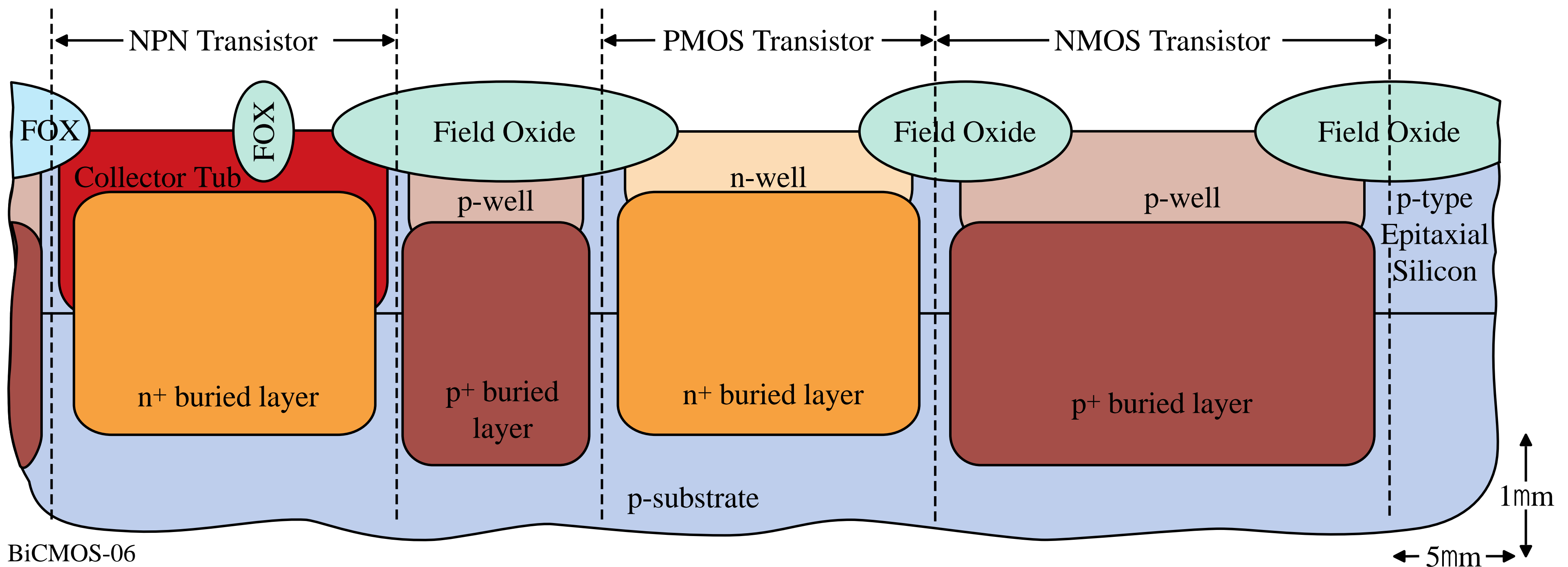
Field Oxide



Comments:

- The field oxide is used to isolate surface structures (i.e. metal) from the substrate

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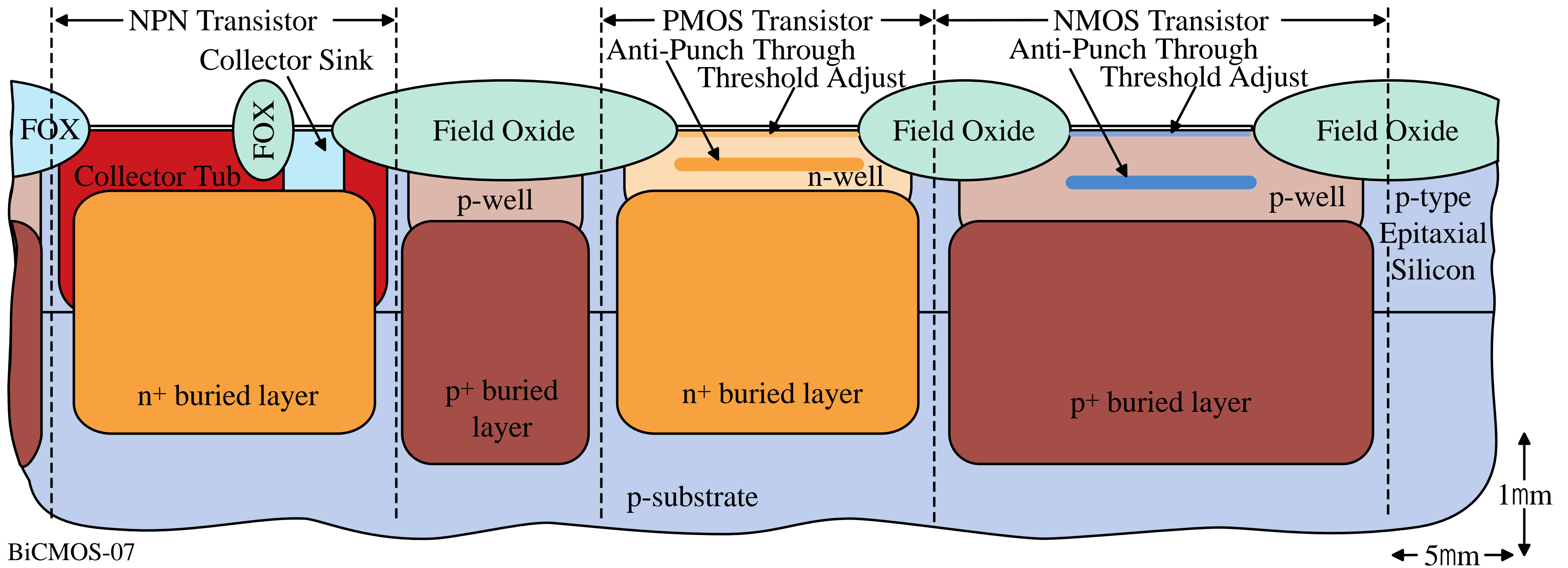
Collector Sink and n-Well and p-Well Definitions



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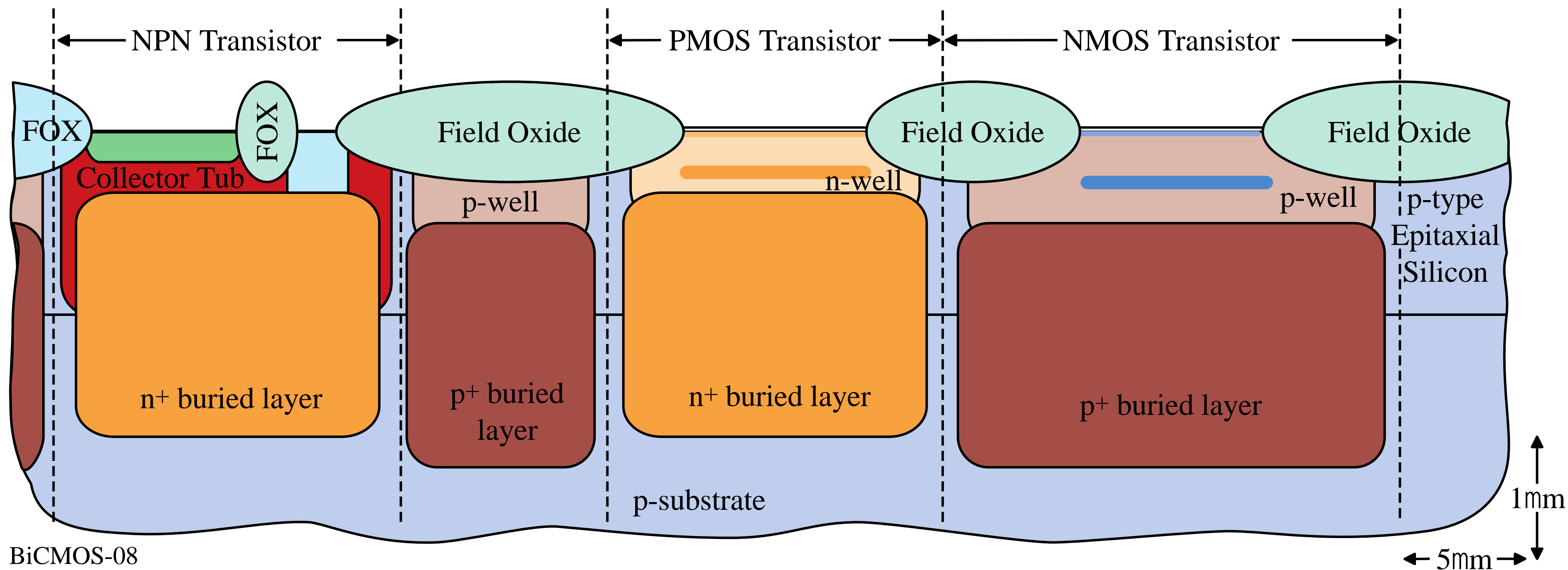
Base Definition



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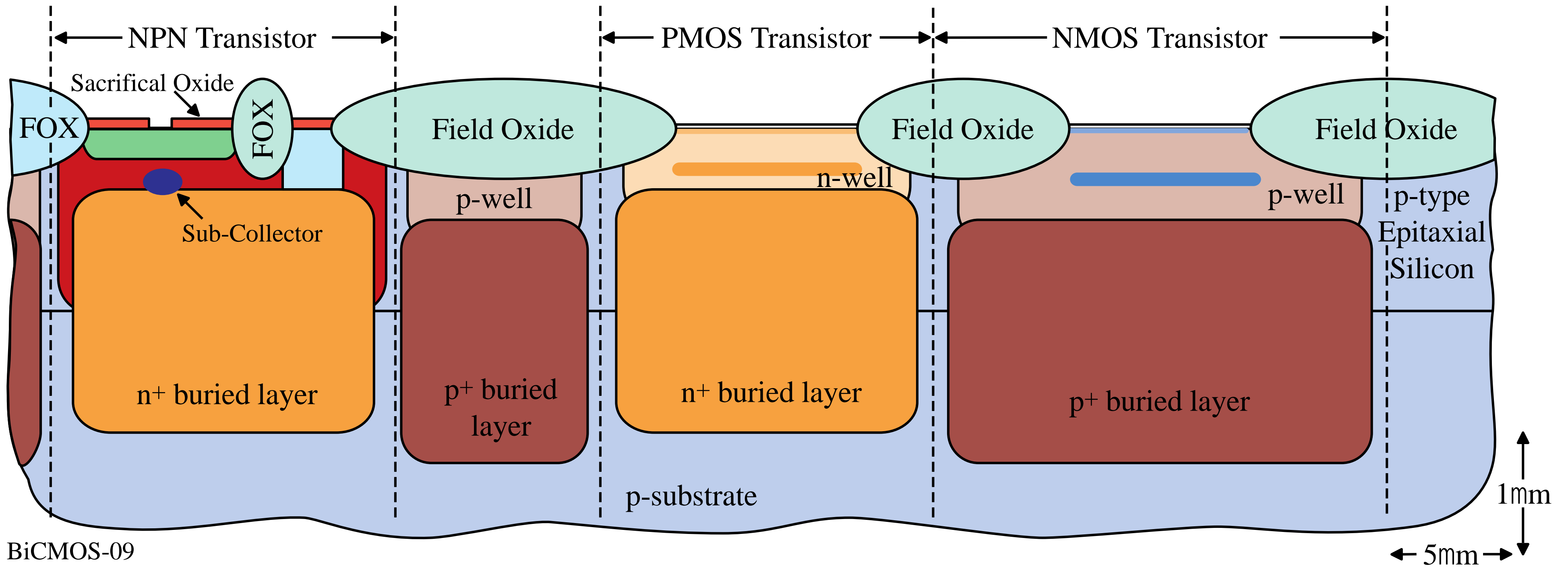
Definition of the Emitter Window and Sub-Collector Implant



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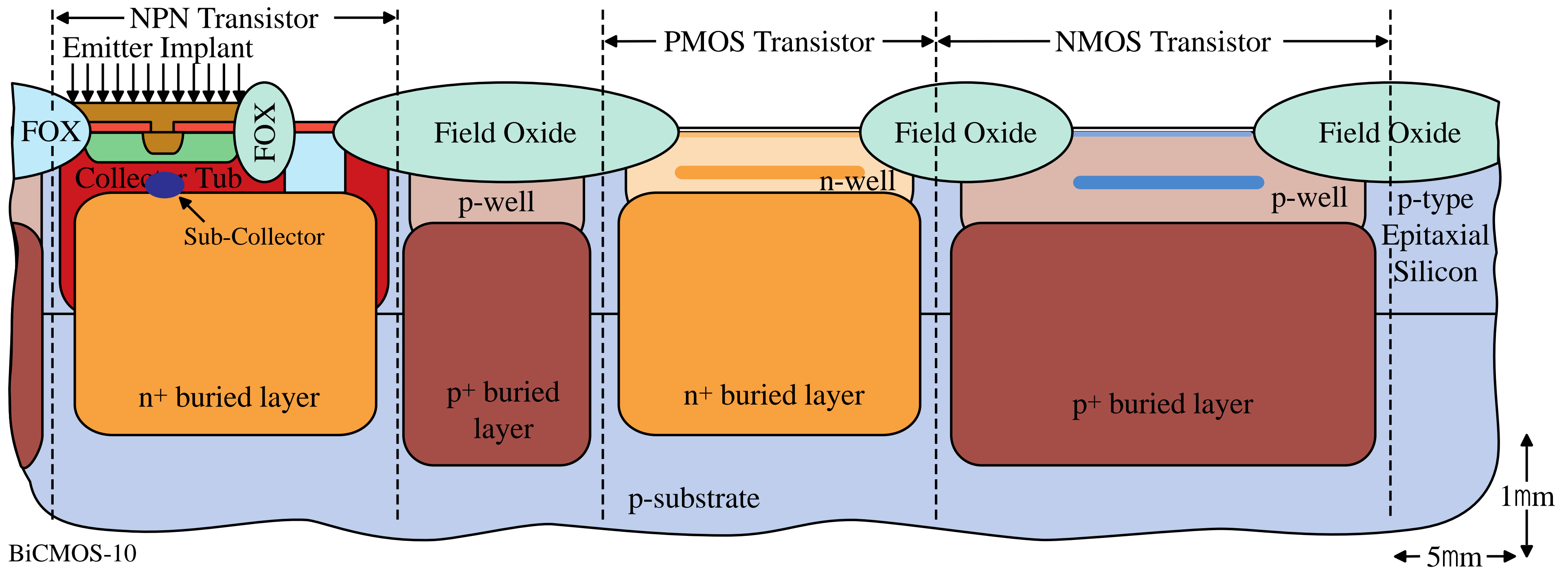
Emitter Implant



Comments:

- The polysilicon above the base is implanted with n-type carriers

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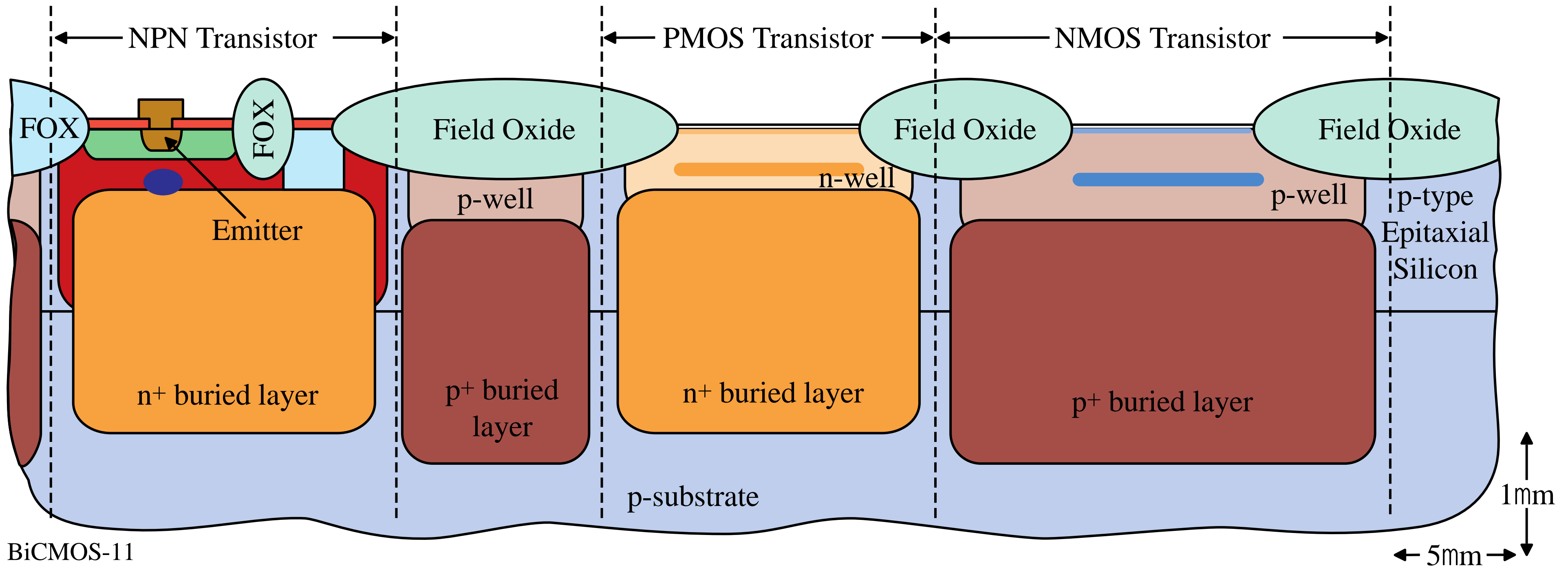
Emitter Diffusion



Comments:

- The polysilicon not over the emitter window is removed and the n-type carriers diffuse toward the base forming the emitter

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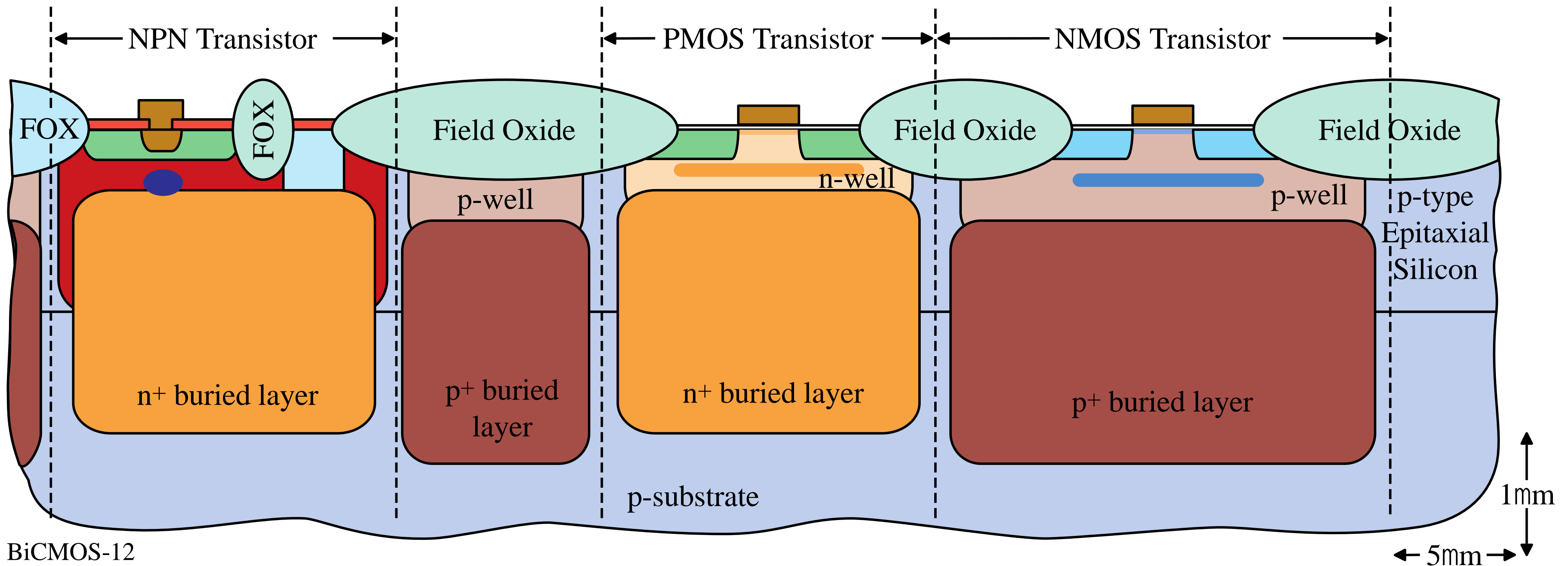
Formation of the MOS Gates and LD Drains/Sources



Comments:

- The surface of the region where the MOSFETs are to be built is cleared and a thin gate oxide is deposited with a polysilicon layer on top of the thin oxide
- The polysilicon is removed over the source and drain areas
- A light source/drain diffusion is done for the NMOS and PMOS (separately)

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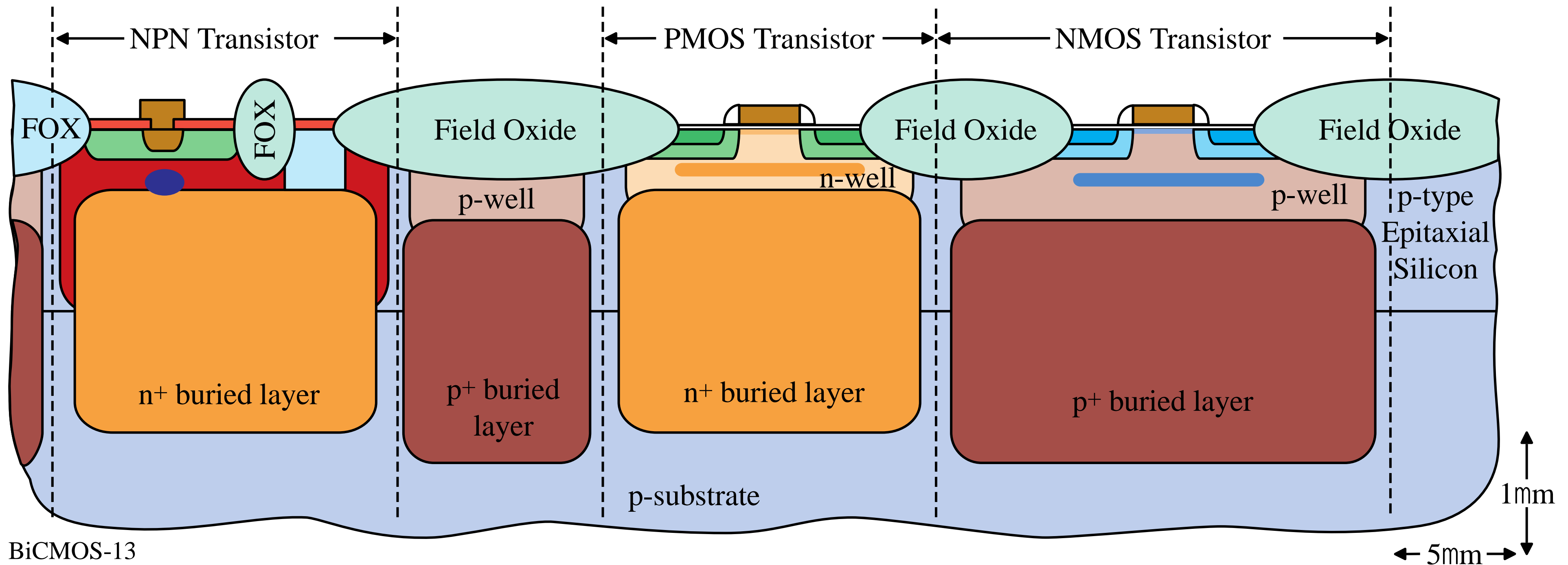
Heavily Doped Source/Drain



Comments:

- The sidewall spacers prevent the heavy source/drain doping from being near the channel of the MOSFET

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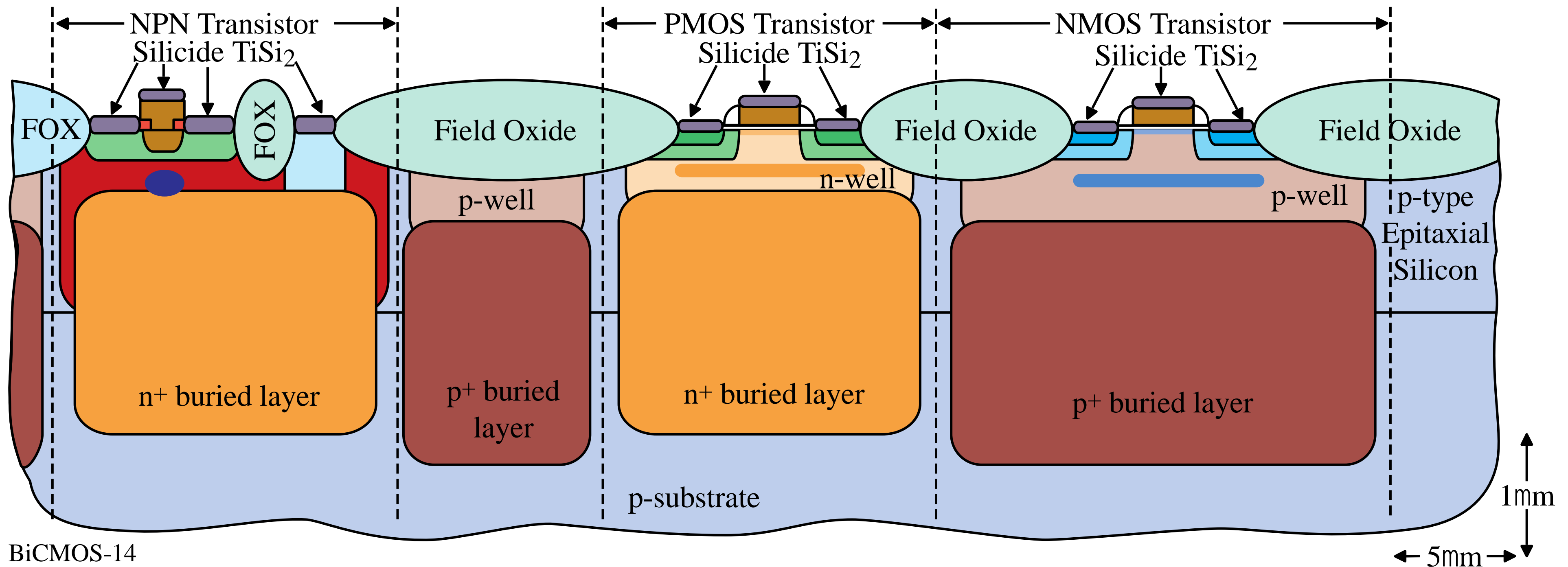
Siliciding



Comments:

- Siliciding is used to reduce the resistance of the polysilicon and to provide ohmic contacts to the base, emitter, collector, sources and drains

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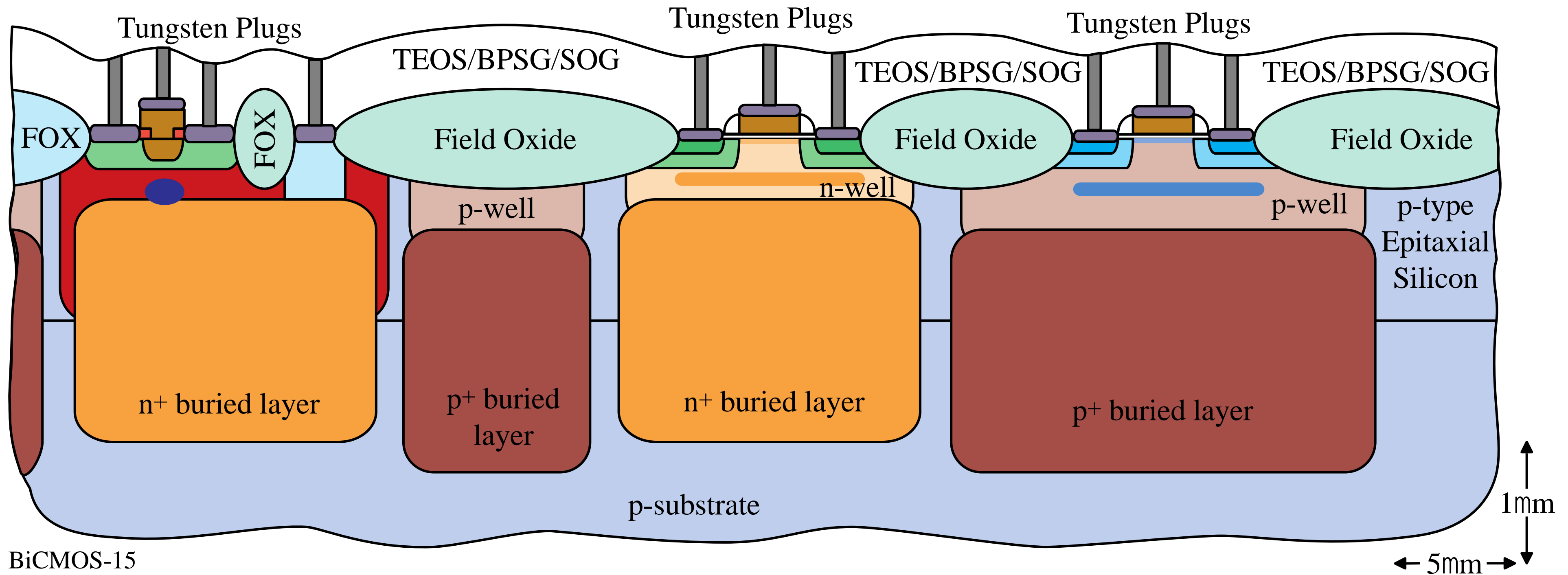
Contacts



Comments:

- A dielectric is deposited over the entire wafer
- One of the purposes of the dielectric is to smooth out the surface
- Tungsten plugs are used to make electrical contact between the transistors and metal1

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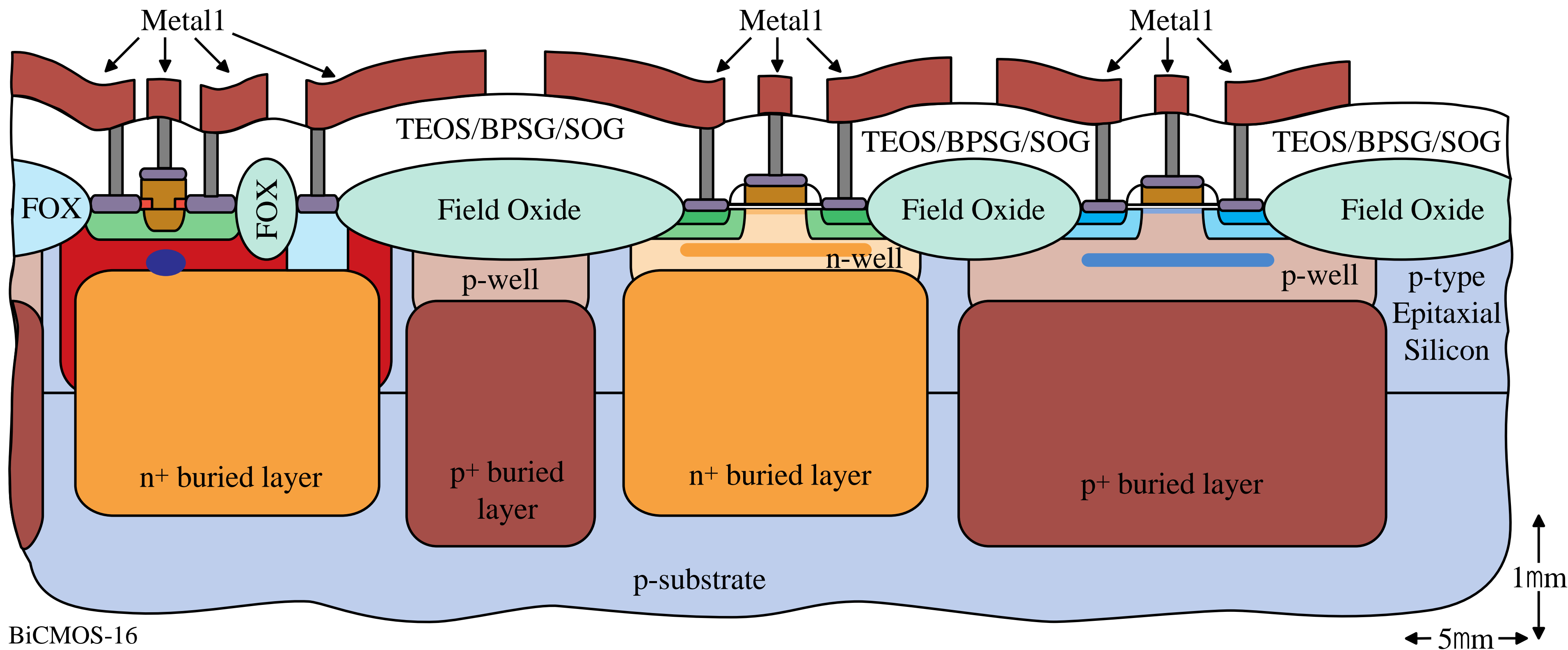
Metal1



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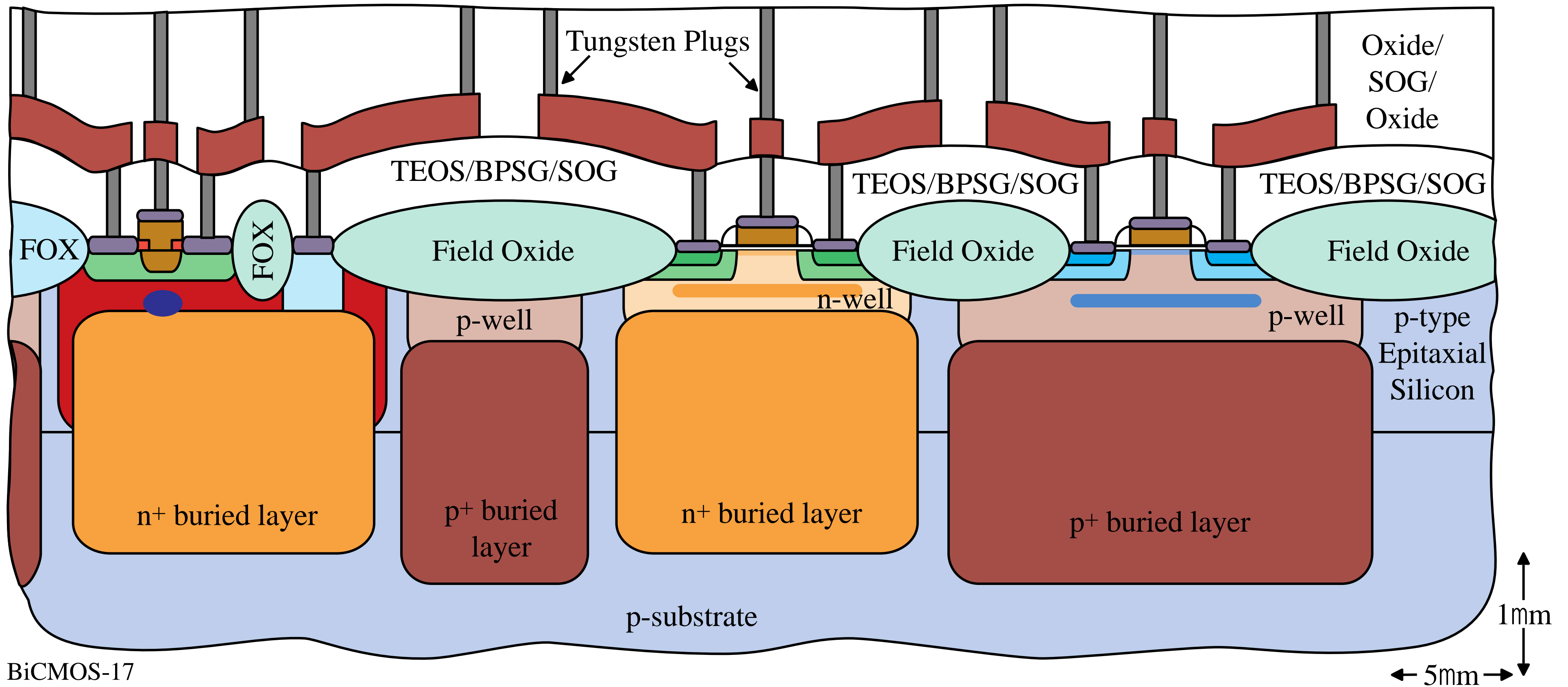
Metal1-Metal2 Vias



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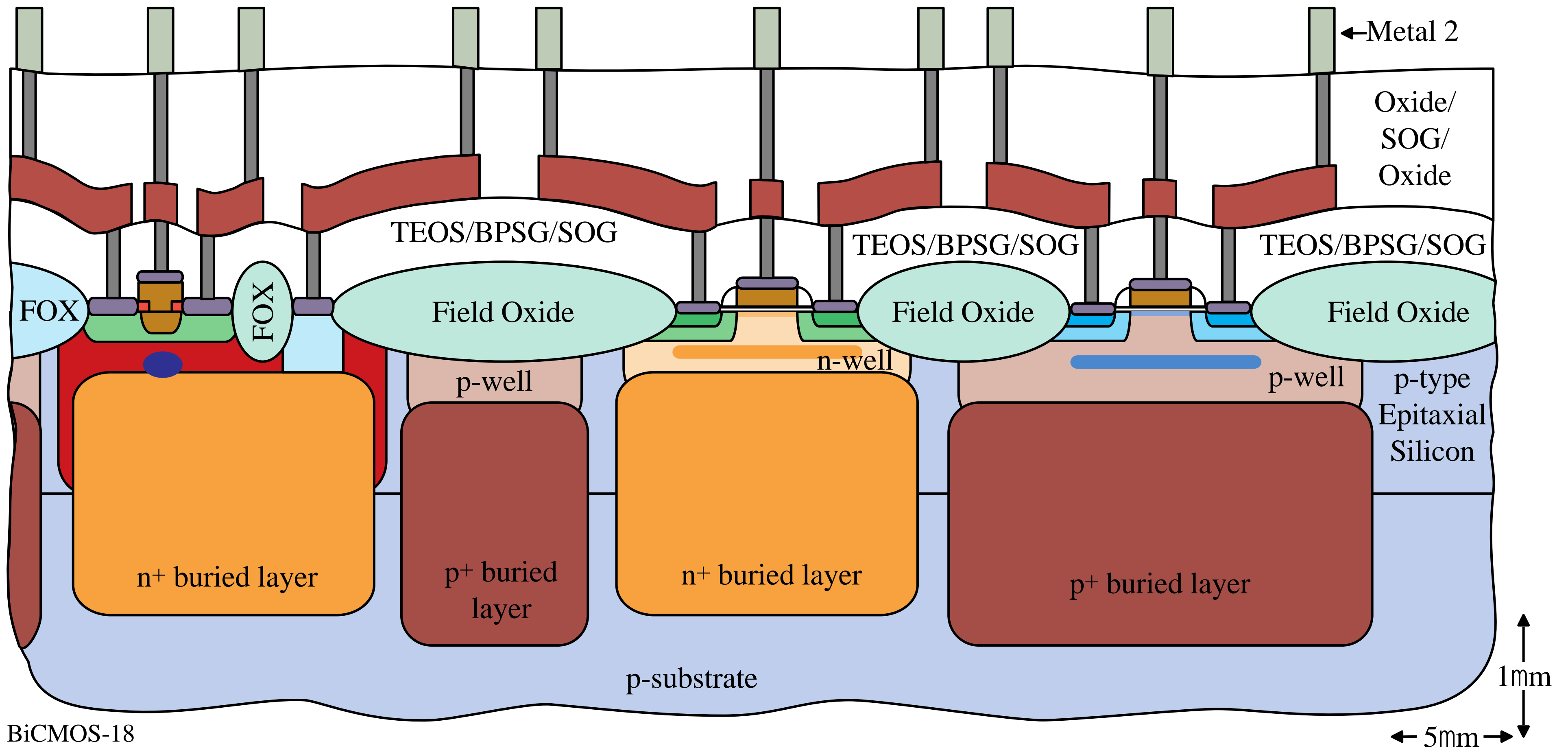
Metal2



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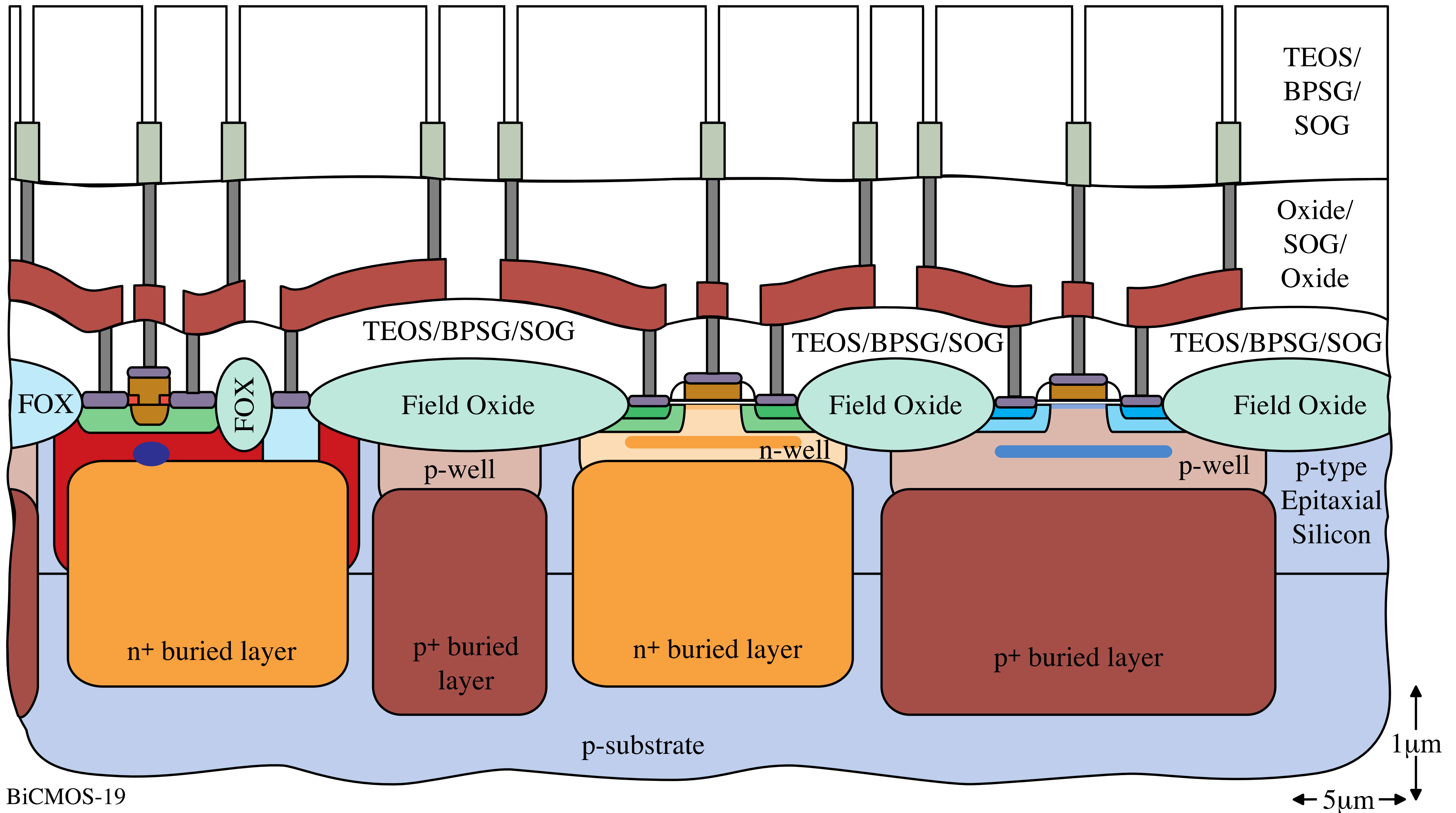
Metal2-Metal3 Vias



Comments:

- The metal2-metal3 vias will be filled with metal3 as opposed to tungsten plugs

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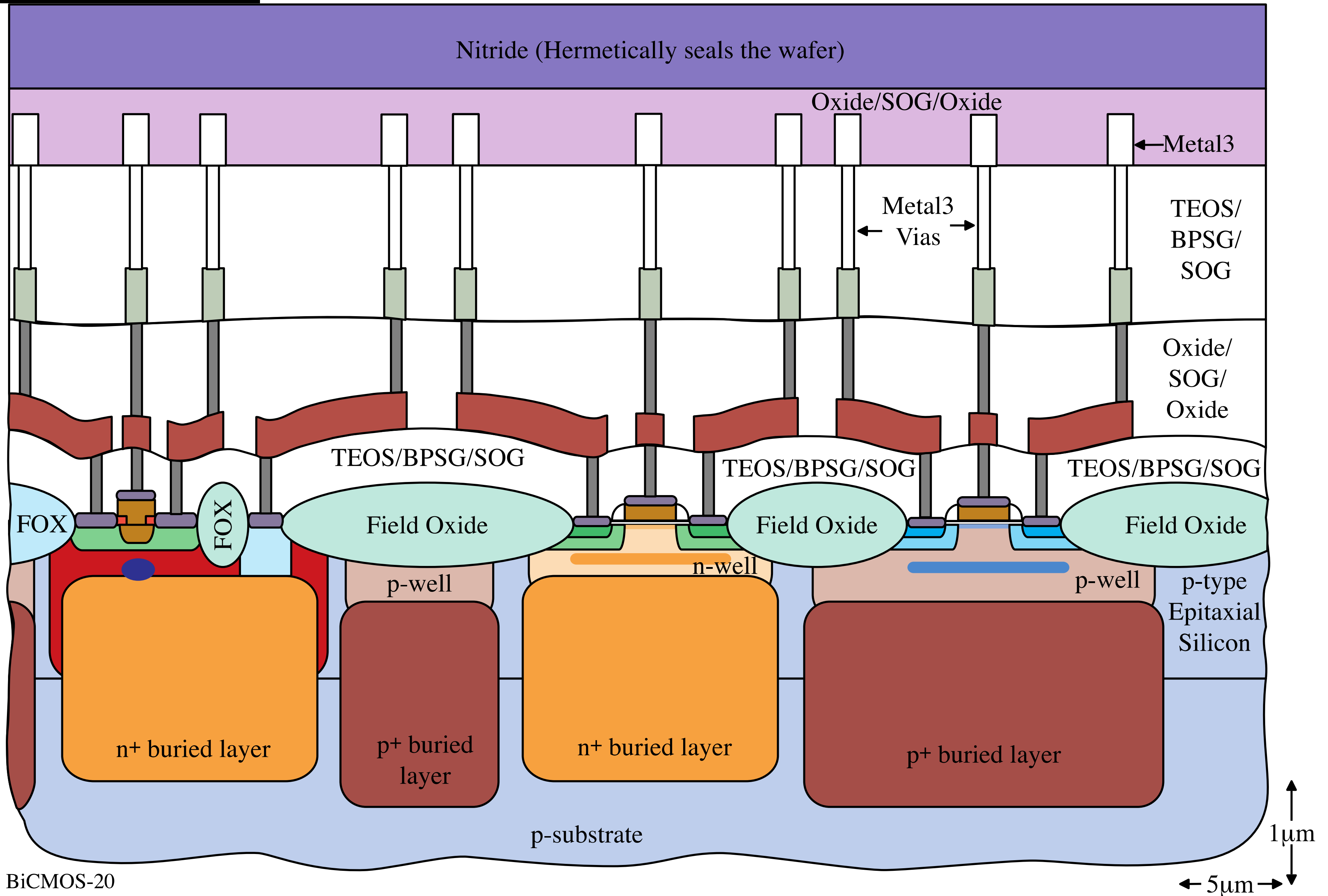
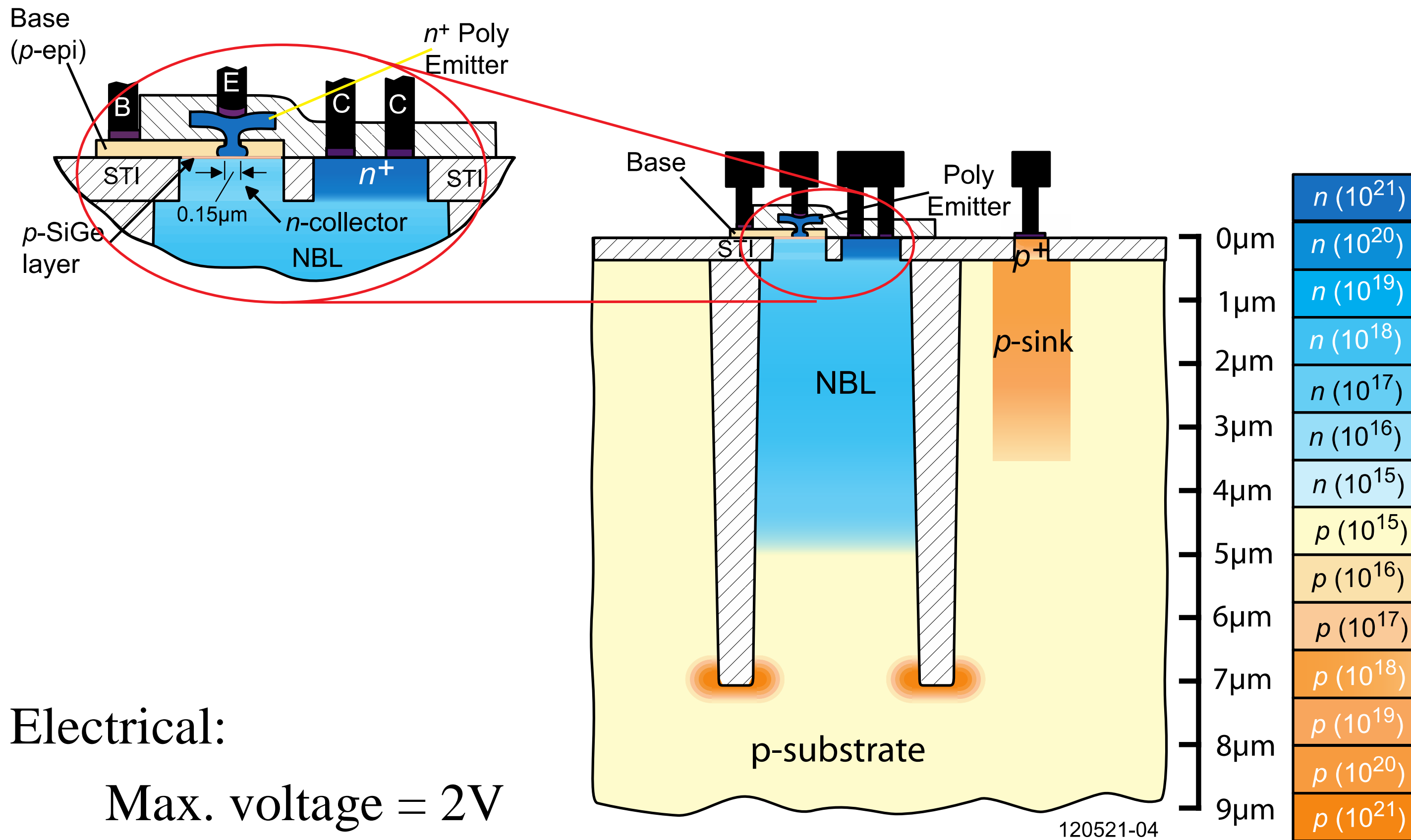
Completed Wafer



Silicon-Germanium

Physical Perspective (130nm):



Electrical:

Max. voltage = 2V

$\beta \approx 300$

$f_T \approx 100$ GHz

SUMMARY

- UDSM technology typically has a minimum channel length less than 0.1µm
- UDSM transistors utilize enhanced channel strains to increase drive capability and reduce off currents
- Advantages of UDSM technology include:
  - Smaller devices
  - Higher speeds and transconductances
  - Improved I_{on}/I_{off}
- Disadvantages of UDSM technology include:
  - Gate leakage currents
  - Reduced small signal gains
  - Increased nonlinearity
- BiCMOS technology
  - Offers both CMOS transistors and a high performance vertical BJT
  - CMOS is typically a generation behind
  - Silicon germanium can be used to enhance the BJT performance

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