LECTURE 02 - SUBMICRON CMOS TECHNOLOGY

LECTURE ORGANIZATION

Outline

- CMOS Technology
- Fundamental IC Process Steps
- Typical Submicron CMOS Fabrication Process
- Summary

***CMOS Analog Circuit Design*, 3rd Edition Reference**

Pages 18-33

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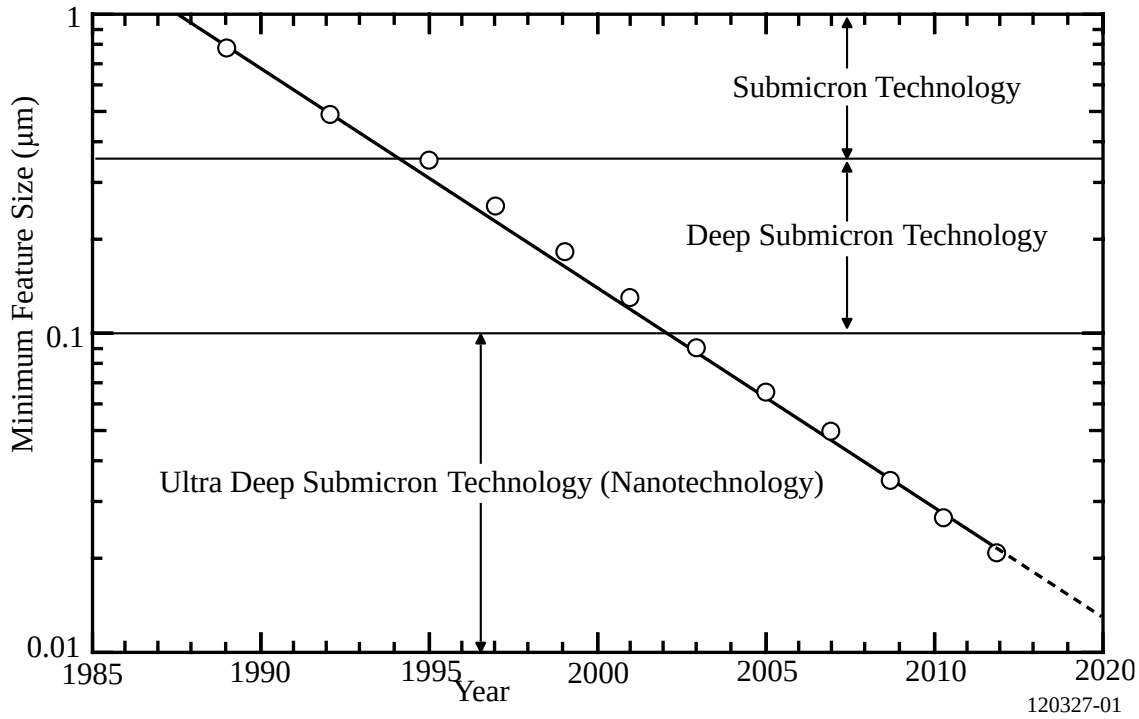
CMOS TECHNOLOGY

Categorization of CMOS Technology

• Minimum feature size as a function of time:



• Categories of CMOS technology:

1.) Submicron technology – $L_{min} \geq 0.35$ microns

2.) Deep Submicron technology (DSM) – 0.1 microns $\leq L_{min} \leq 0.35$ microns

3.) Ultra-Deep Submicron technology (UDSM) – $L_{min} \leq 0.1$ microns

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Why CMOS Technology?

Comparison of BJT and MOSFET technology from an analog viewpoint:

Comparison Feature	BJT	MOSFET
Cutoff Frequency(f_T)	100 GHz	50 GHz (0.25μm)
Noise (thermal about the same)	Less 1/f	More 1/f
DC Range of Operation	9 decades of exponential current versus v_{BE}	2-3 decades of square law behavior
Transconductance (Same current)	Larger by 10X	Smaller by 10X
Small Signal Output Resistance	Slightly larger	Smaller for short channel
Switch Implementation	Poor	Good
Capacitor	Voltage dependent	More options
Performance/Power Ratio	High	Low
Technology Improvement	Slower	Faster

Therefore,

- Almost every comparison favors the BJT, *however* a similar comparison made from digital viewpoint would come up on the side of CMOS.
- Therefore, since large-volume mixed-mode technology will be driven by digital demands, CMOS is an obvious result as the technology of availability.

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FUNDAMENTAL IC PROCESS STEPS

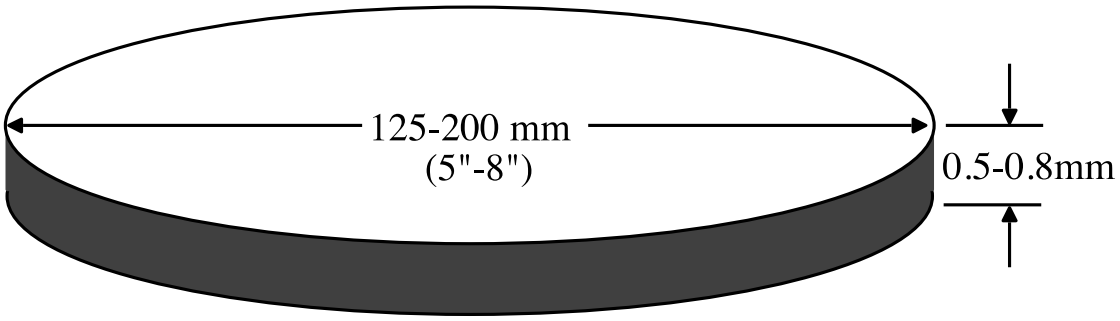
Basic Steps for a CMOS Submicron Process

- Oxide growth
- Thermal diffusion
- Ion implantation
- Deposition
- Etching
- Epitaxy

Photolithography

Photolithography is the means by which the above steps are applied to selected areas of the silicon wafer.

Silicon Wafer



n-type: 3-5 Ω-cm
p-type: 14-16 Ω-cm

Fig. 2.1-1r

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Oxidation

Description:

Oxidation is the process by which a layer of silicon dioxide is grown on the surface of a silicon wafer.

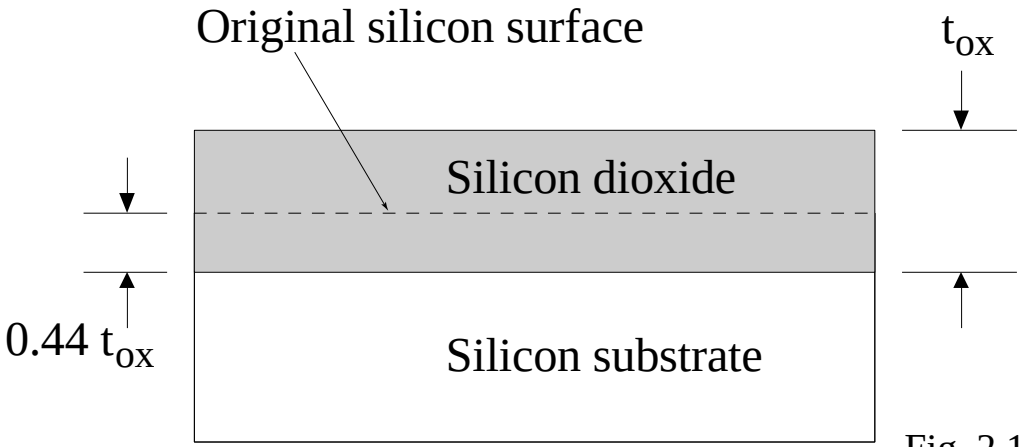

Fig. 2.1-2

Uses:

- Protect the underlying material from contamination
- Provide isolation between two layers.

Very thin oxides (100Å to 1000Å) are grown using dry oxidation techniques. Thicker oxides (>1000Å) are grown using wet oxidation techniques.

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Diffusion

Diffusion is the movement of impurity atoms at the surface of the silicon into the bulk of the silicon.

Always in the direction from higher concentration to lower concentration.

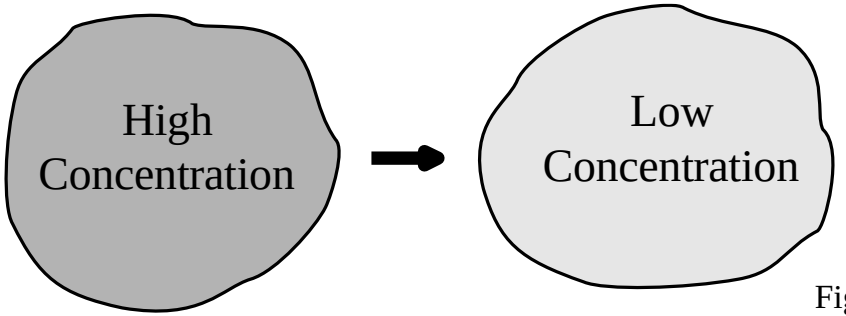
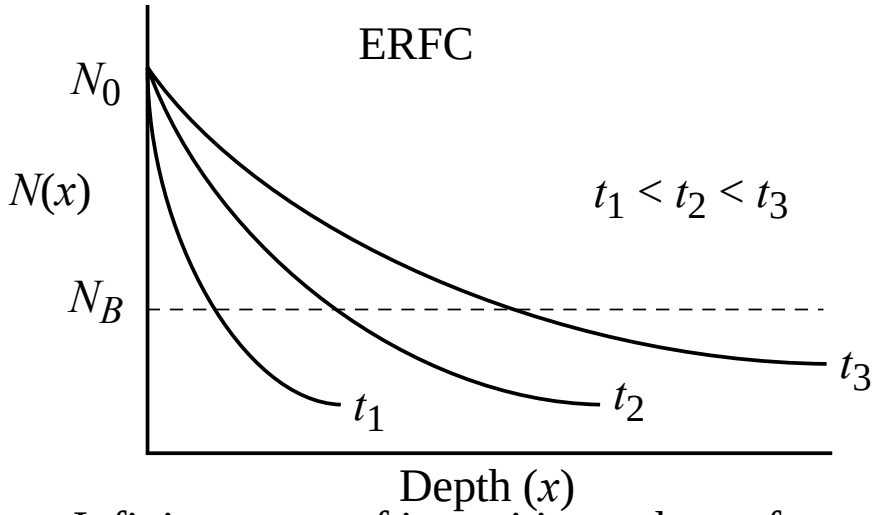
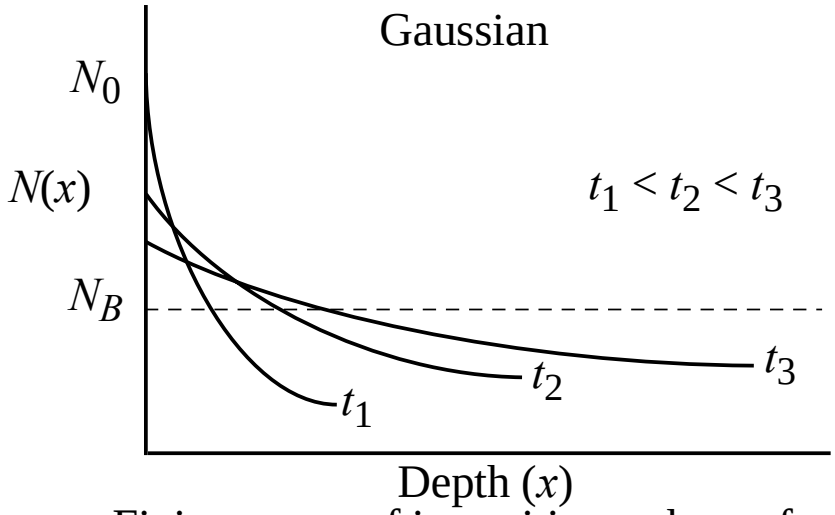


Fig. 150-04

Diffusion is typically done at high temperatures: 800 to 1400°C



Infinite source of impurities at the surface.



Finite source of impurities at the surface.

Fig. 150-05

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Ion Implantation

Ion implantation is the process by which impurity ions are accelerated to a high velocity and physically lodged into the target material.

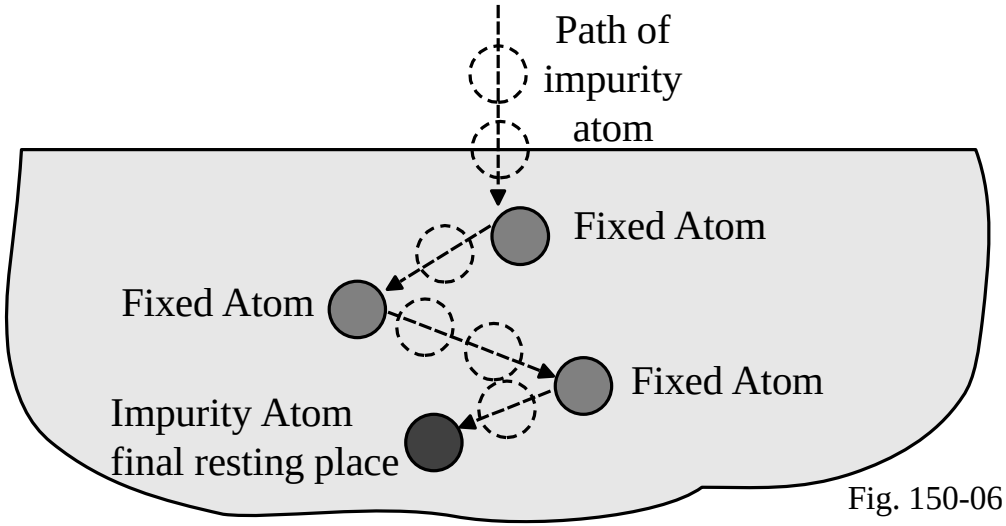

Fig. 150-06

- Annealing is required to activate the impurity atoms and repair the physical damage to the crystal lattice. This step is done at 500 to 800°C.
- Ion implantation is a lower temperature process compared to diffusion.
- Can implant through surface layers, thus it is useful for field-threshold adjustment.
- Can achieve unique doping profile such as buried concentration peak.

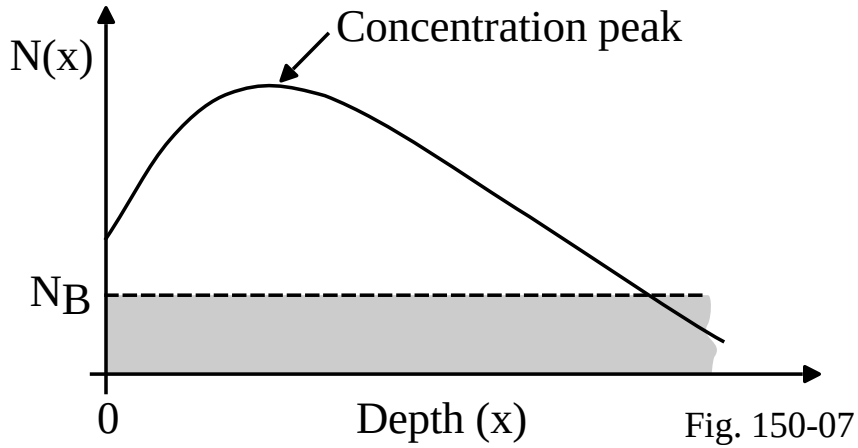

Fig. 150-07

Generally implant first then use diffusion to achieve the well or active area.

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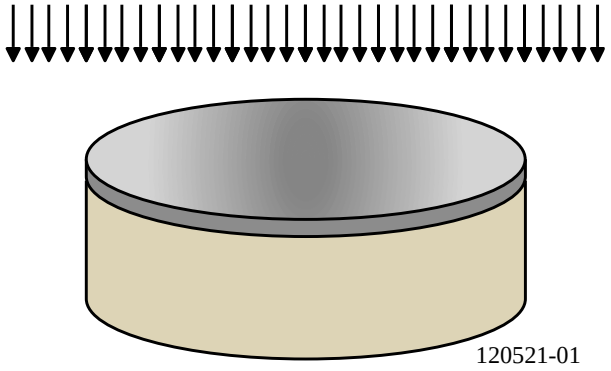
Deposition

Deposition is the means by which various materials are deposited on the silicon wafer.

Examples:

- Silicon nitride (Si_3N_4)
- Silicon dioxide (SiO_2)
- Aluminum
- Polysilicon



There are various ways to deposit a material on a substrate:

- Chemical-vapor deposition (CVD)
- Low-pressure chemical-vapor deposition (LPCVD)
- Plasma-assisted chemical-vapor deposition (PECVD)
- Sputter deposition

Material that is being deposited using these techniques covers the entire wafer and requires no mask.

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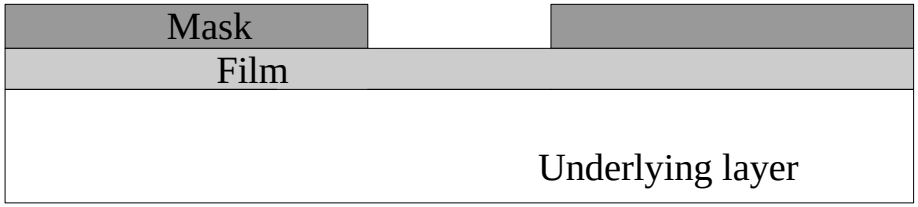
Etching

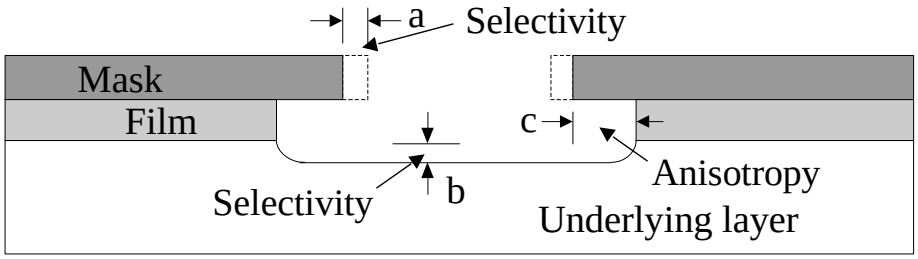
Etching is the process of selectively removing a layer of material.

When etching is performed, the etchant may remove portions or all of:

- The desired material
- The underlying layer
- The masking layer



(a) Portion of the top layer ready for etching.



(b) Horizontal etching and etching of underlying layer.

Fig. 150-08

Important considerations:

- *Anisotropy* of the etch is defined as,

$$A = 1-(\text{lateral etch rate/vertical etch rate})$$

- *Selectivity* of the etch (film to mask and film to substrate) is defined as,

$$S_{film\text{-}mask} = \frac{\text{film etch rate}}{\text{mask etch rate}}$$

$A = 1$ and $S_{film\text{-}mask} = \infty$ are desired.

There are basically two types of etches:

- Wet etch which uses chemicals
- Dry etch which uses chemically active ionized gases.

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Epitaxy

Epitaxial growth consists of the formation of a layer of single-crystal silicon on the surface of the silicon material so that the crystal structure of the silicon is continuous across the interfaces.

- It is done externally to the material as opposed to diffusion which is internal
- The epitaxial layer (epi) can be doped differently, even opposite to the material on which it is grown
- It is accomplished at high temperatures using a chemical reaction at the surface
- The epi layer can be any thickness, typically 1-20 microns

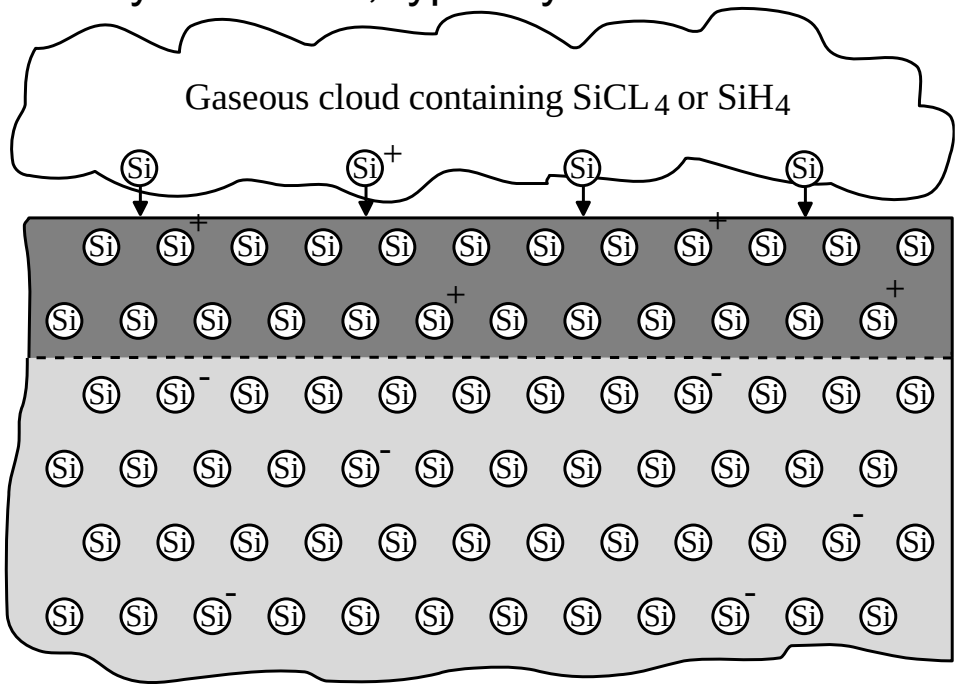

Fig. 150-09

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Photolithography

Components:

- Photoresist material
- Mask
- Material to be patterned (e.g., oxide)

Positive photoresist:

Areas exposed to UV light are soluble in the developer

Negative photoresist:

Areas not exposed to UV light are soluble in the developer

Steps:

1. Apply photoresist
2. Soft bake (drives off solvents in the photoresist)
3. Expose the photoresist to UV light through a mask
4. Develop (remove unwanted photoresist using solvents)
5. Hard bake ($\approx$ 100°C)
6. Remove photoresist (solvents)

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Illustration of Photolithography - Exposure

The process of exposing selective areas to light through a photo-mask is called *printing*.

Types of printing include:

- Contact printing
- Proximity printing
- Projection printing

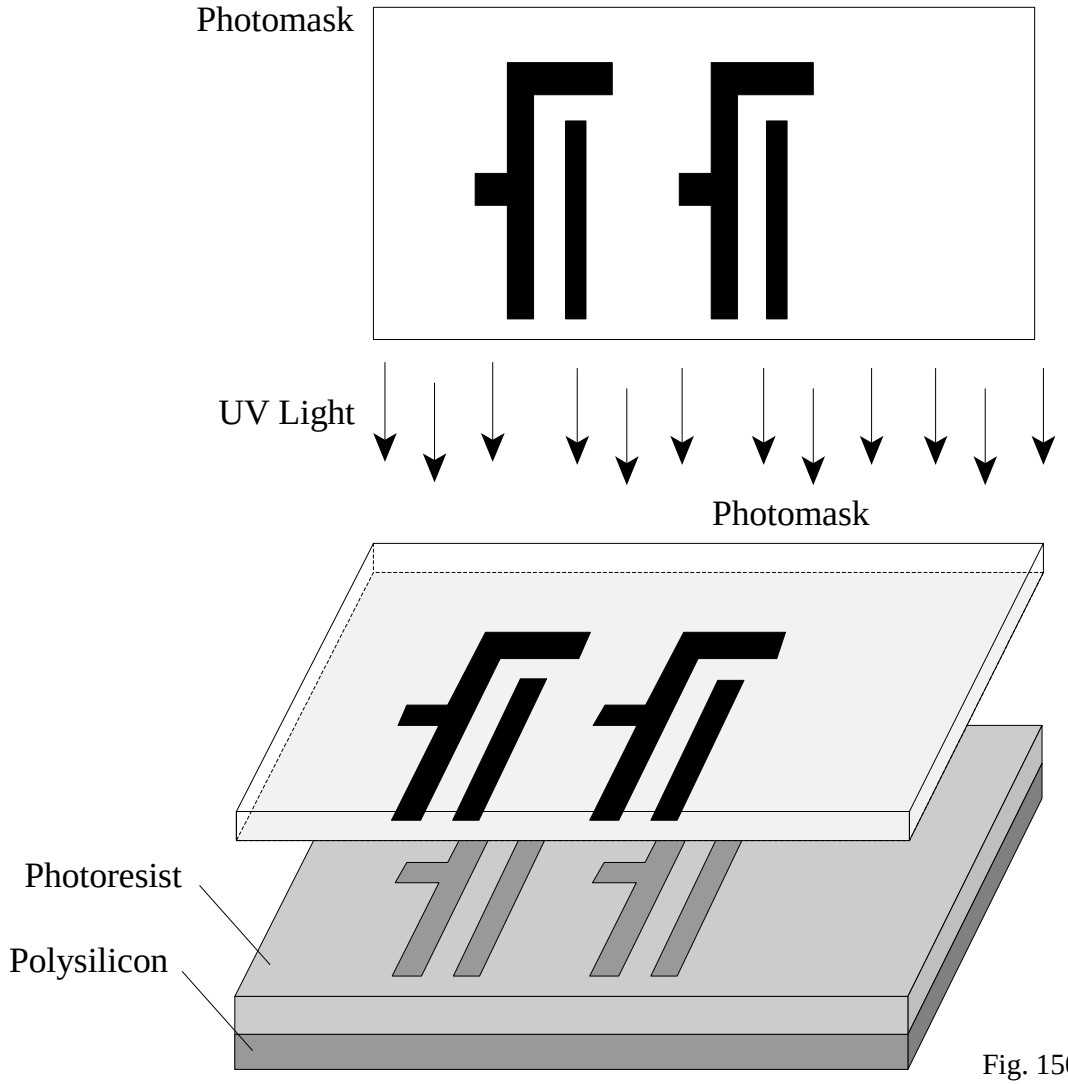

Fig. 150-10

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Illustration of Photolithography - Positive Photoresist

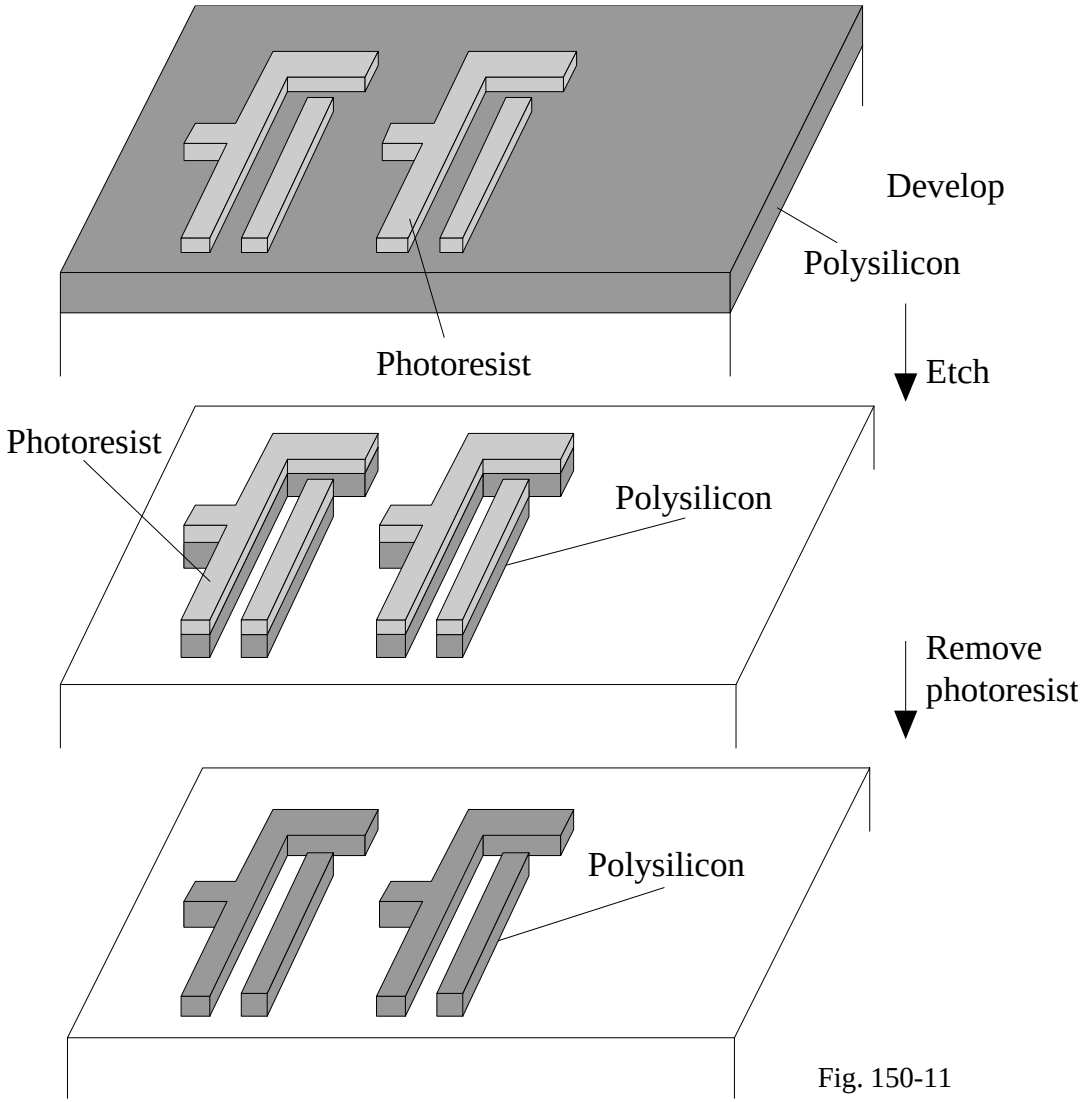

Fig. 150-11

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TYPICAL SUBMICRON CMOS FABRICATION PROCESS

N-Well CMOS Fabrication Major Steps

1.) Implant and diffuse the n-well
2.) Deposition of silicon nitride
3.) n-type field (channel stop) implant
4.) p-type field (channel stop) implant
5.) Grow a thick field oxide (FOX)
6.) Grow a thin oxide and deposit polysilicon
7.) Remove poly and form LDD spacers
8.) Implantation of NMOS S/D and n-material contacts
9.) Remove spacers and implant NMOS LDDs
10.) Repeat steps 8.) and 9.) for PMOS
11.) Anneal to activate the implanted ions
12.) Deposit a thick oxide layer (BPSG - borophosphosilicate glass)
13.) Open contacts, deposit first level metal and etch unwanted metal
14.) Deposit another interlayer dielectric (CVD SiO_2), open vias, deposit 2nd level metal
15.) Etch unwanted metal, deposit a passivation layer and open over bonding pads

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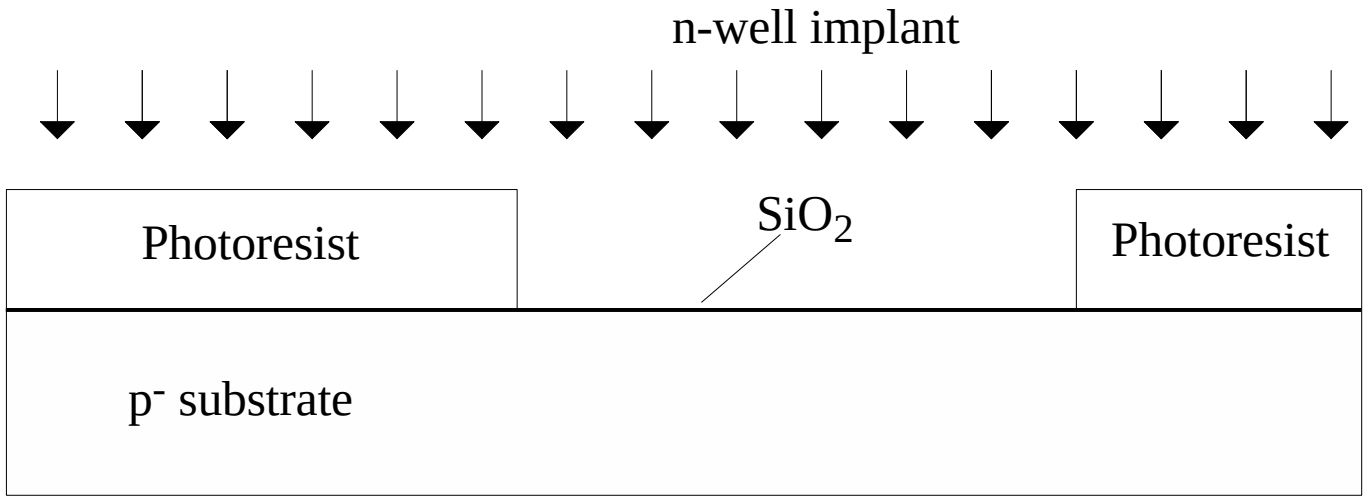
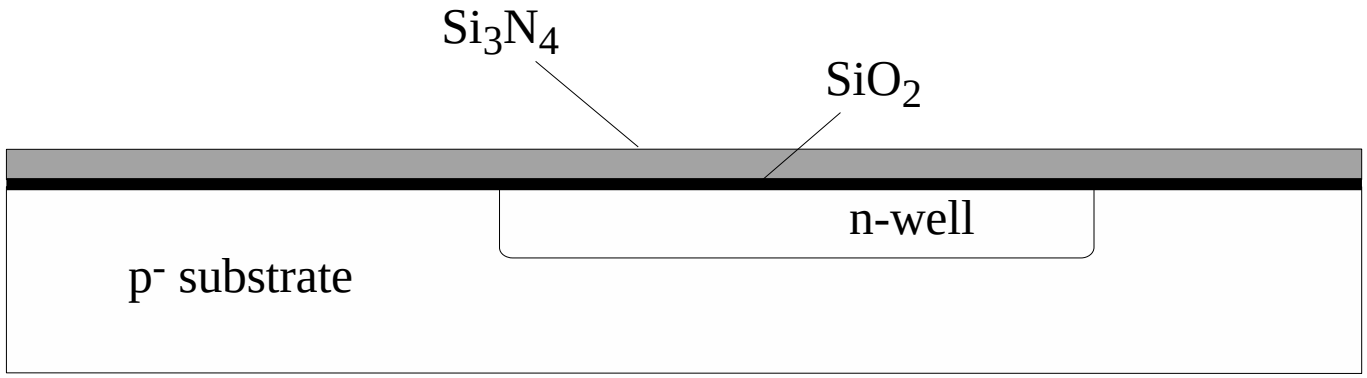
Major CMOS Process Steps

Step 1 - Implantation and diffusion of the n-wells



Step 2 - Growth of thin oxide and deposition of silicon nitride



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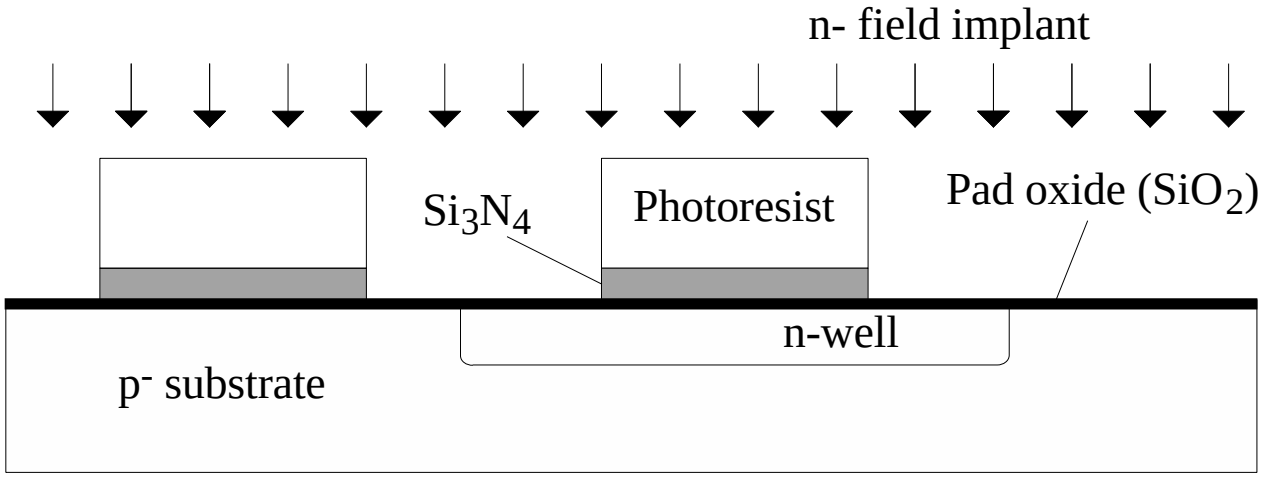
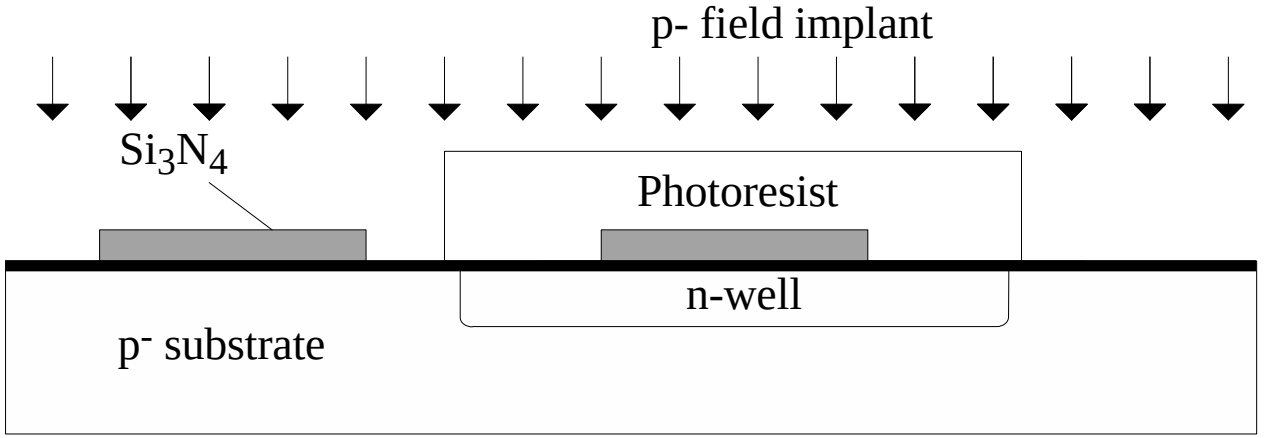
Major CMOS Process Steps – Continued

Step 3.) Implantation of the n-type field channel stop



Step 4.) Implantation of the p-type field channel stop



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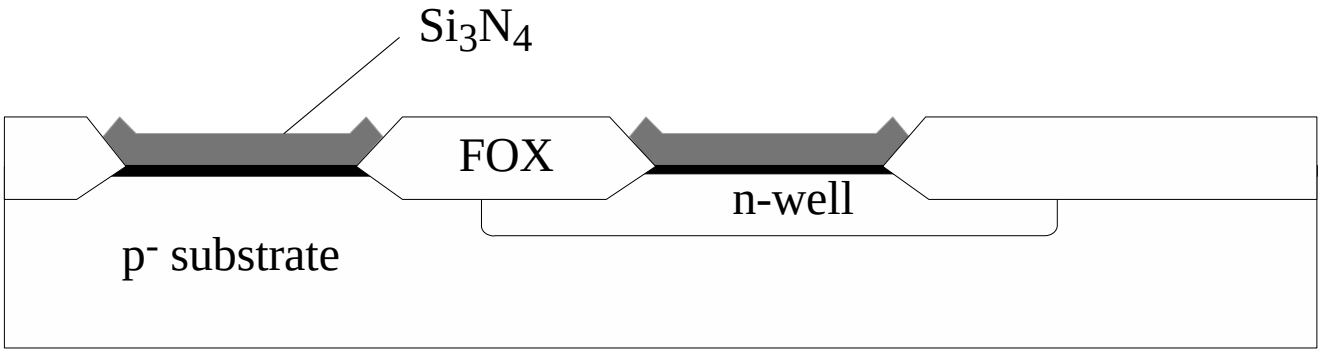
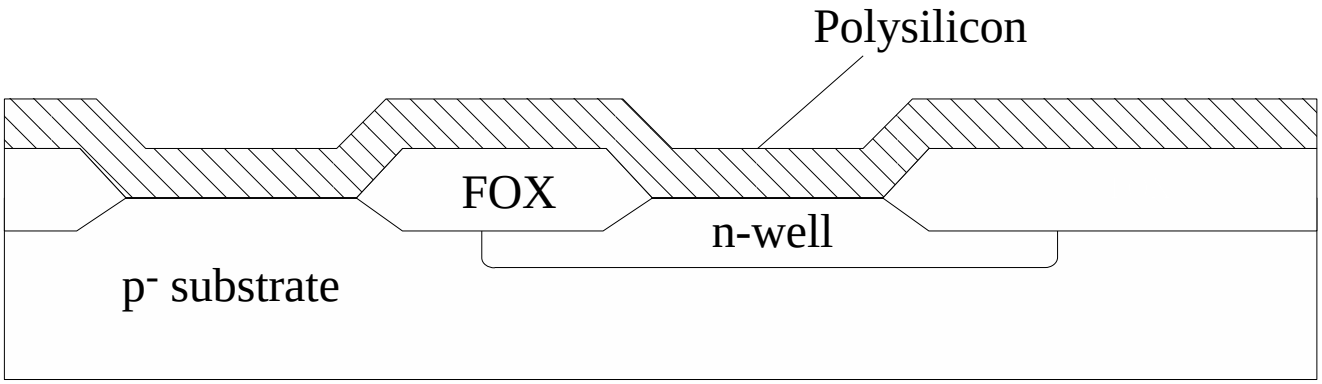
Major CMOS Process Steps – Continued

Step 5.) Growth of the thick field oxide (LOCOS - *loc*alized *o*xidation of *s*ilicon)



Step 6.) Growth of the gate thin oxide and deposition of polysilicon. The thresholds can be shifted by an implantation before the deposition of polysilicon.



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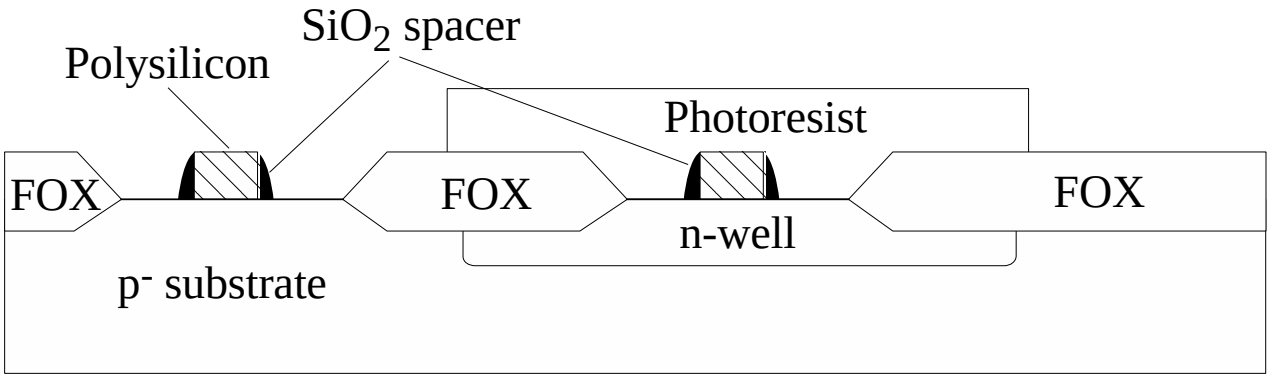
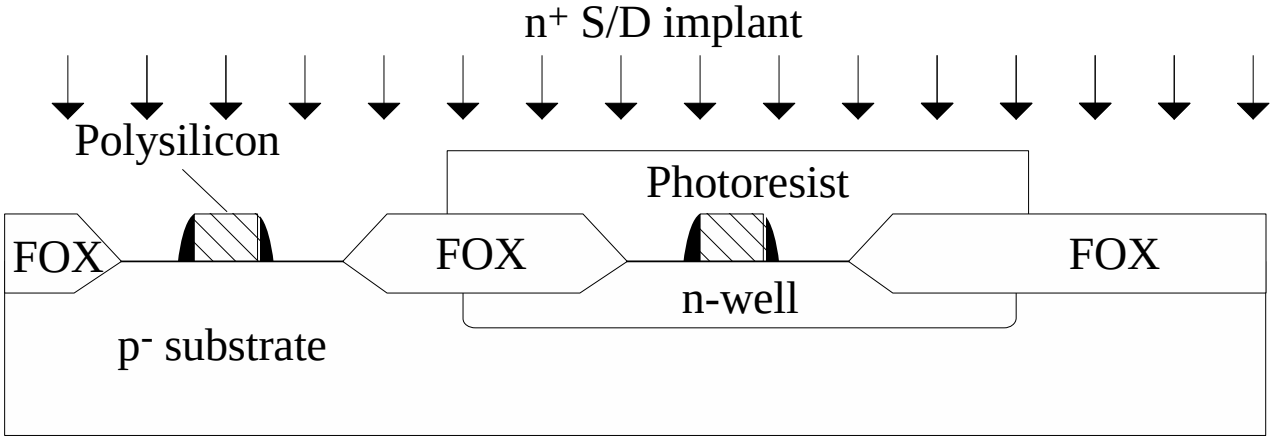
Major CMOS Process Steps – Continued

Step 7.) Removal of polysilicon and formation of the sidewall spacers



Step 8.) Implantation of NMOS source and drain and contact to n-well (not shown)



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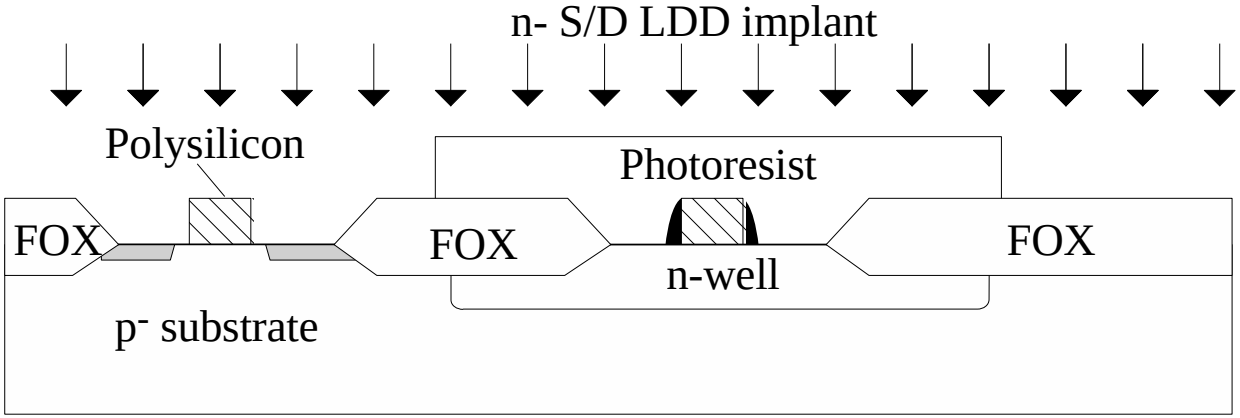
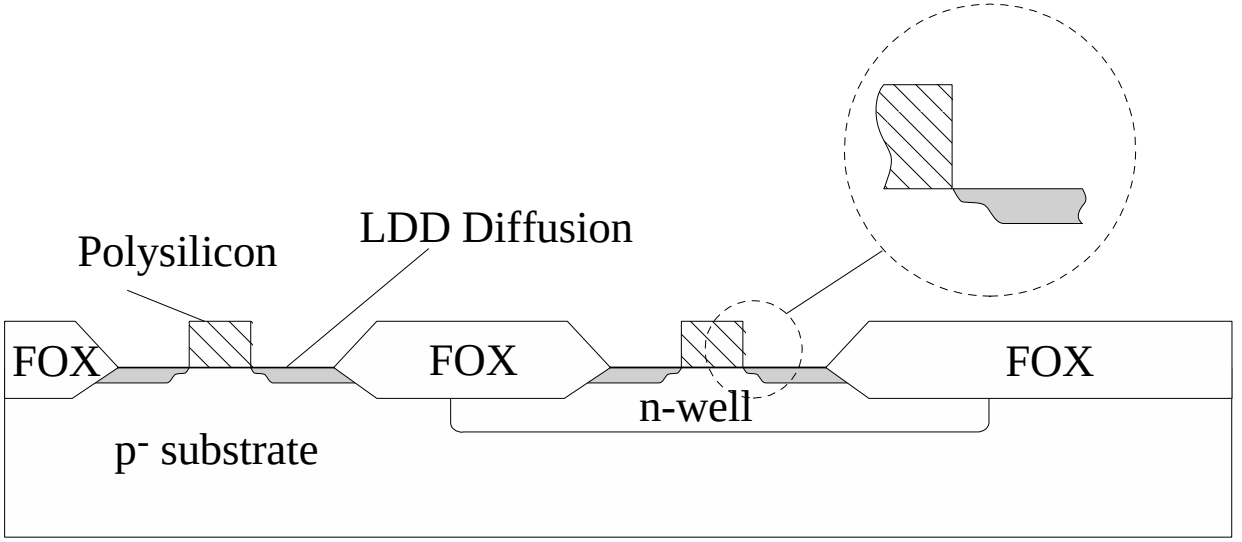
Major CMOS Process Steps - Continued

Step 9.) Remove sidewall spacers and implant the NMOS lightly doped source/drains



Step 10.) Implant the PMOS source/drains and contacts to the p - substrate (not shown), remove the sidewall spacers and implant the PMOS lightly doped source/drains



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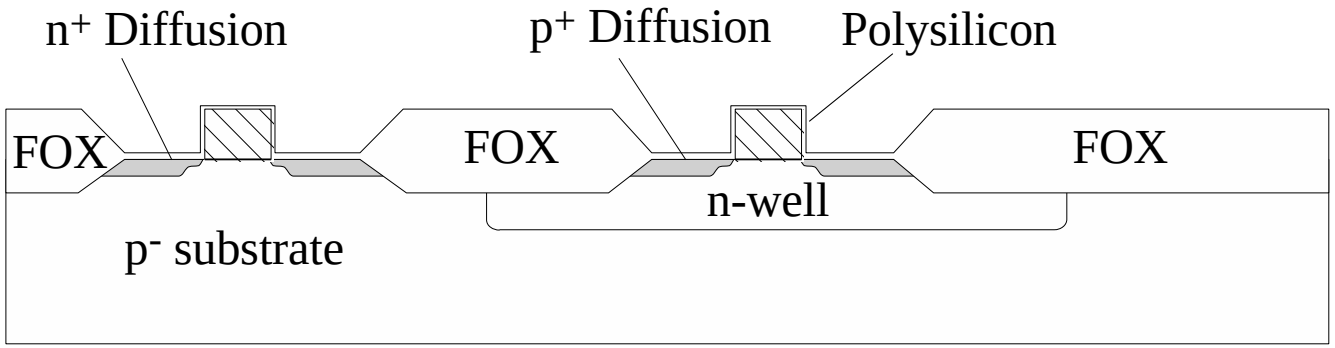
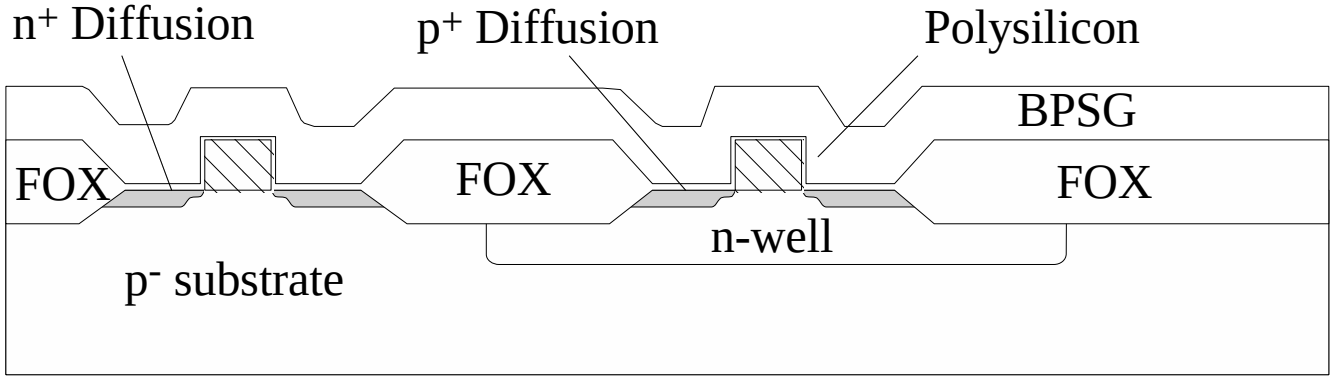
Major CMOS Process Steps – Continued

Step 11.) Anneal to activate the implanted ions



Step 12.) Deposit a thick oxide layer (BPSG - borophosphosilicate glass)



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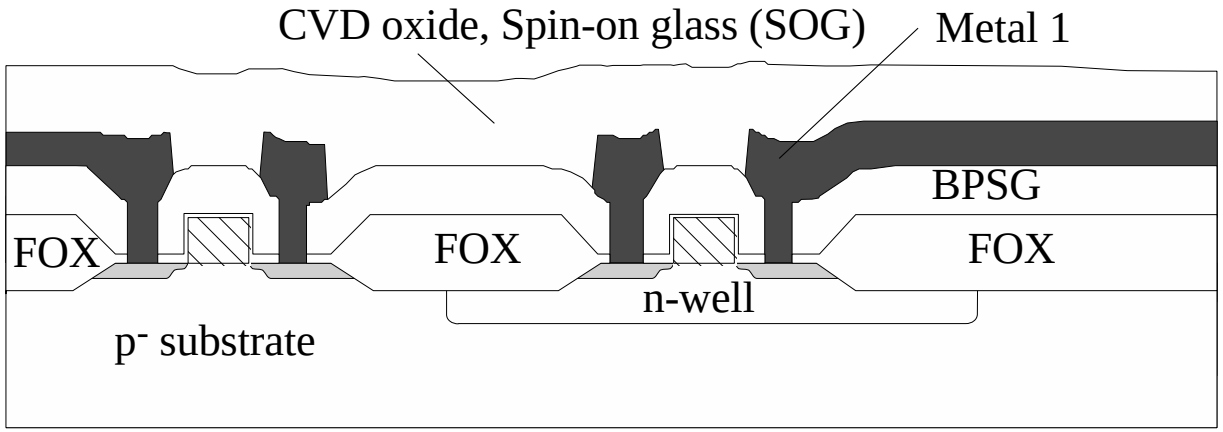
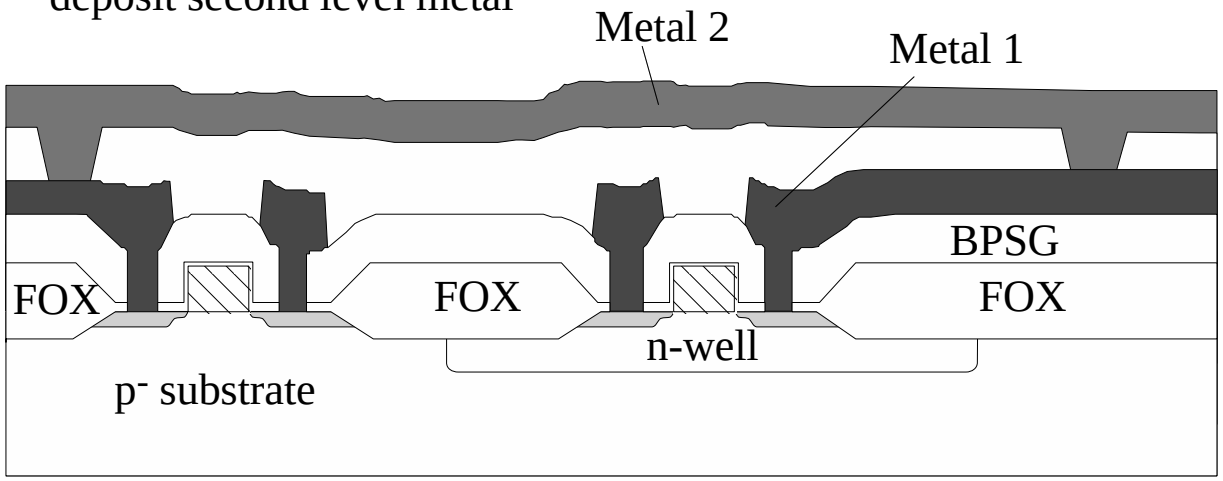
Major CMOS Process Steps - Continued

Step 13.) Open contacts, deposit first level metal and etch unwanted metal



Step 14.) Deposit another interlayer dielectric (CVD SiO_2), open contacts, deposit second level metal



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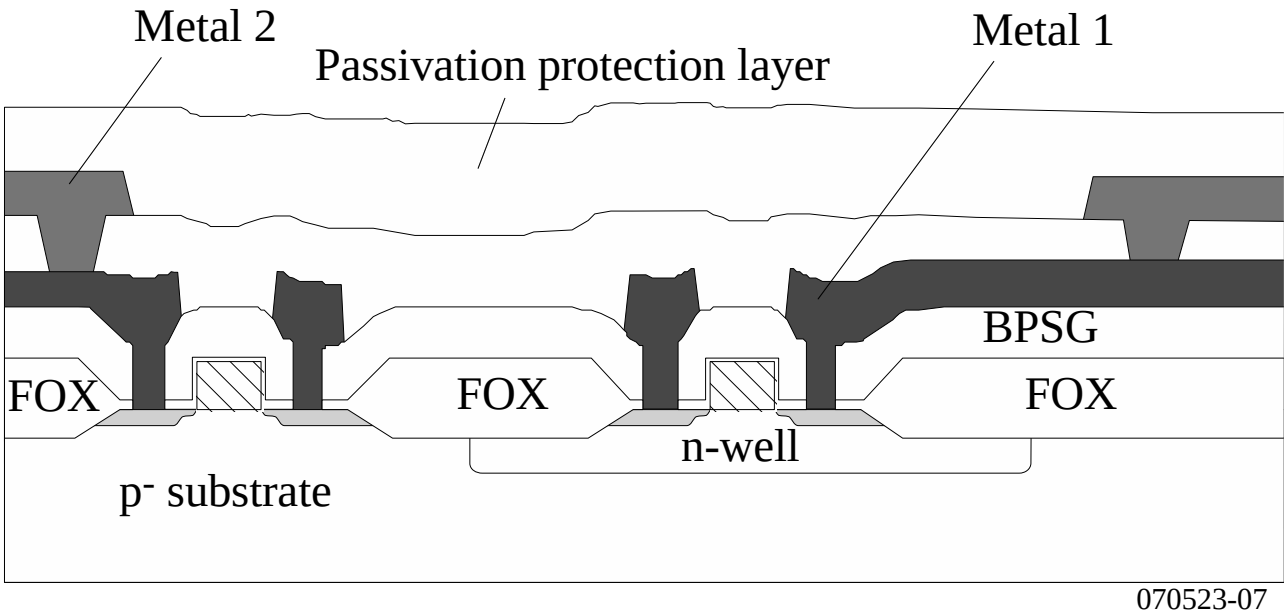
Major CMOS Process Steps – Continued

Step 15.) Etch unwanted metal and deposit a passivation layer and open over bonding pads



p-well process is similar but starts with a p-well implant rather than an n-well implant.

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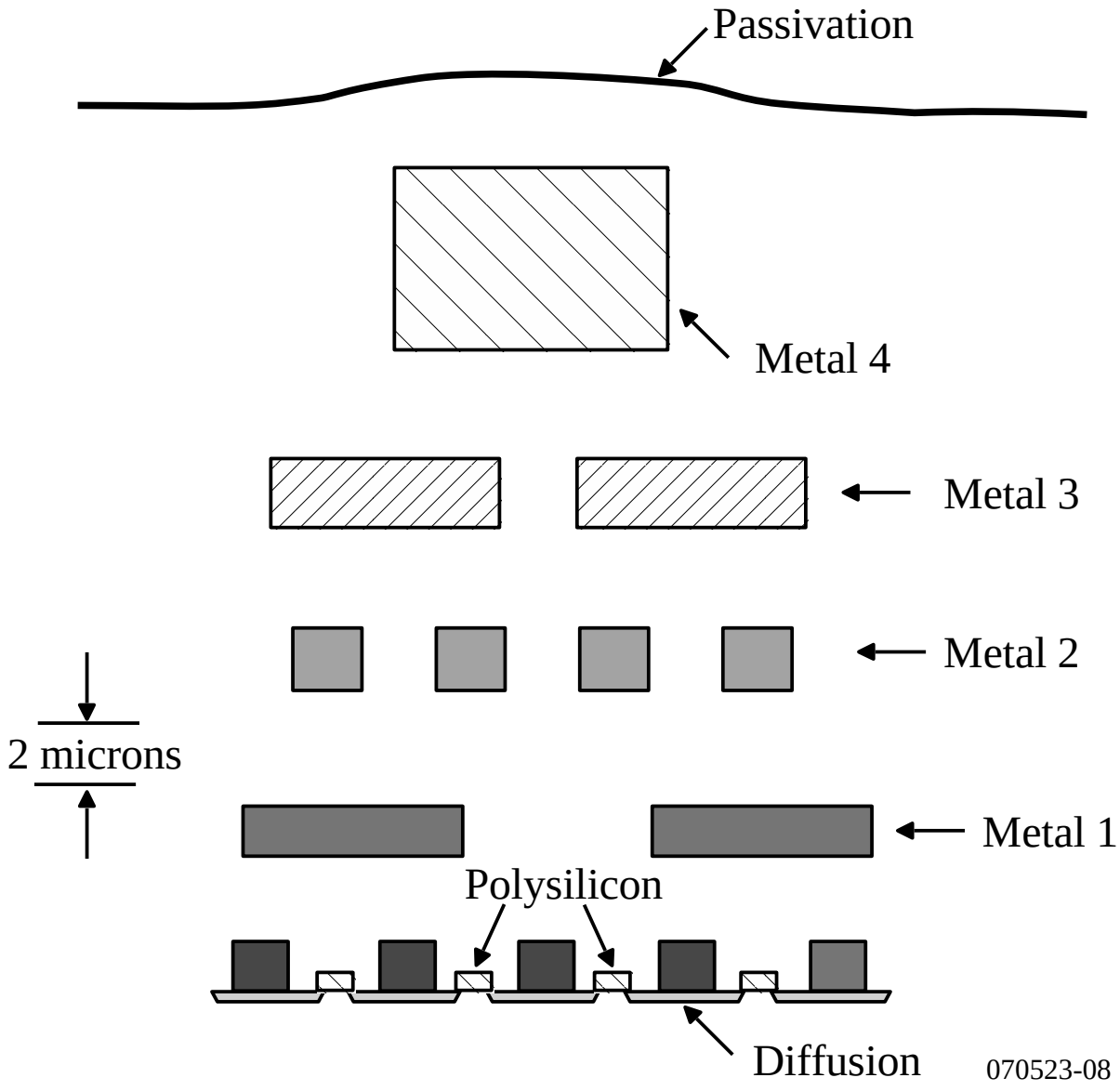
Approximate Side View of CMOS Fabrication



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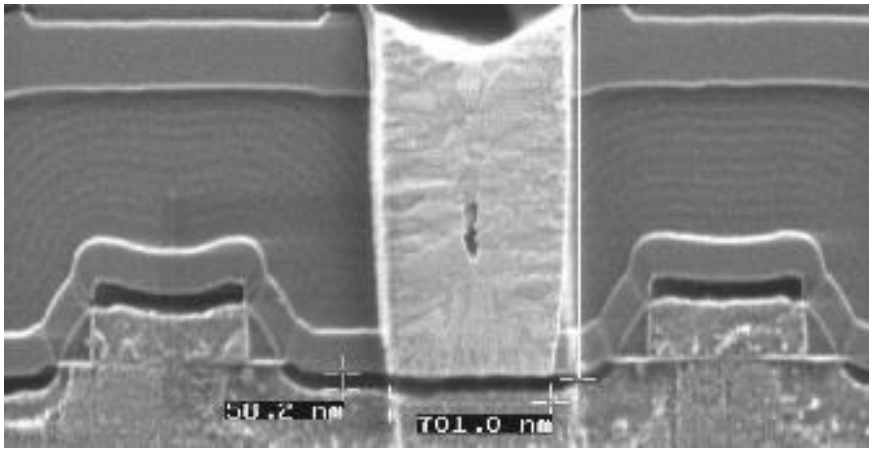
Planarization

Planarization attempts to minimize the variation in surface height of the wafer.

Planarization techniques

- Repeated applications of SOG
- Resist etch-back – highest areas of oxide are exposed longest to the etchant and therefore erode away the most.



Influence of planarization on analog design:

+ Number of levels of metal and the metal integrity depends on planarization
+ Thin film components at the surface require good planarization
+ Without planarization, resistance of conductors increases
+ Planarization at the top level leads to less package induced stress (trimming?)
+ Planarized passivation helps printing when the depth of field is small.
- With planarization, the capacitance of the interdielectric isolation can vary (a good reason to extract capacitance!)
- Significant difference in contact aspect ratio (deep versus shallow contacts)

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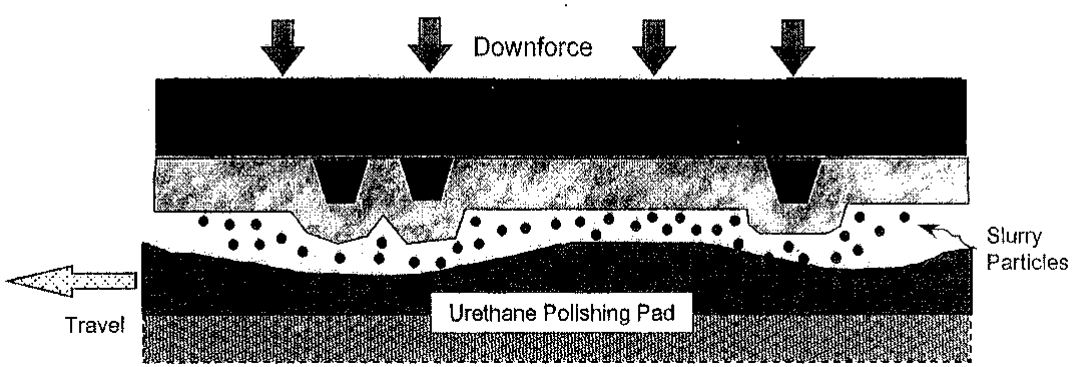
Chemical Mechanical Polishing

CMP produces the required degree of planarization for modern submicron technology.

Schematic diagram of the dielectric planarization process



Comments:

- Both chemical effect (slurry) and mechanical (pad pressure) take place.
- Although CMP is superior to SOG and resist etchback, large areas devoid of underlying metal or poly produce low regions in the final surface.
- Challenge: Achieve a highly planarized surface over a wide range of pattern density.

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Chemical Mechanical Polishing – Continued

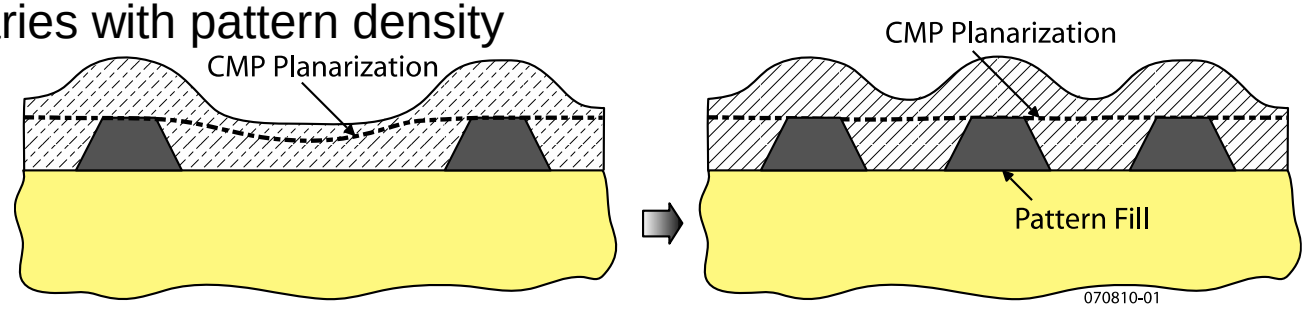
Impact on analog design:

+ Makes the surface flatter

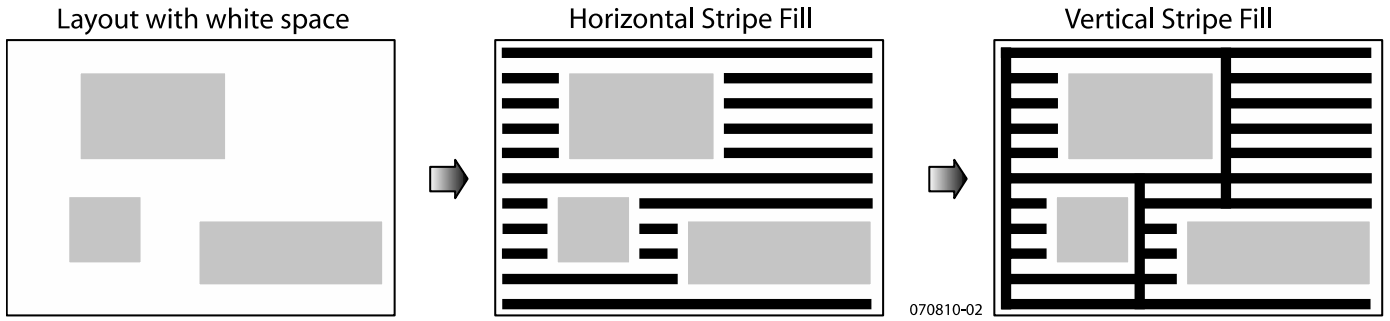
- Vias and plugs can become longer adding resistance

+ More uniform surface giving better metal coverage and foundation for thin film components

- Thickness varies with pattern density



Examples of pattern fill:



Pattern density design rules are both local and global.

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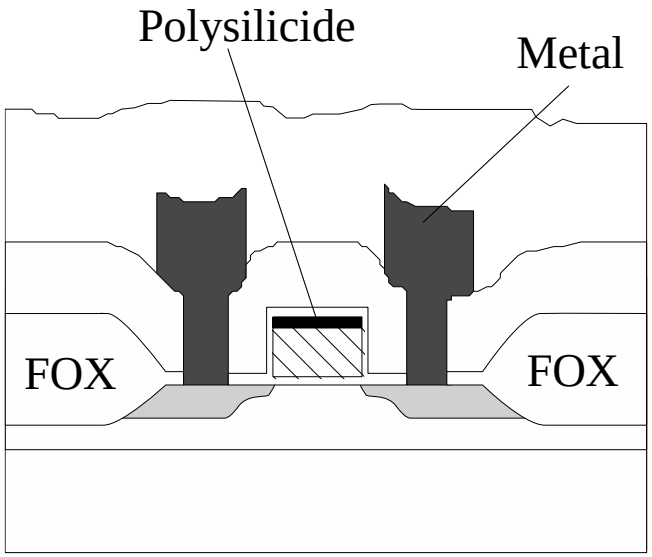
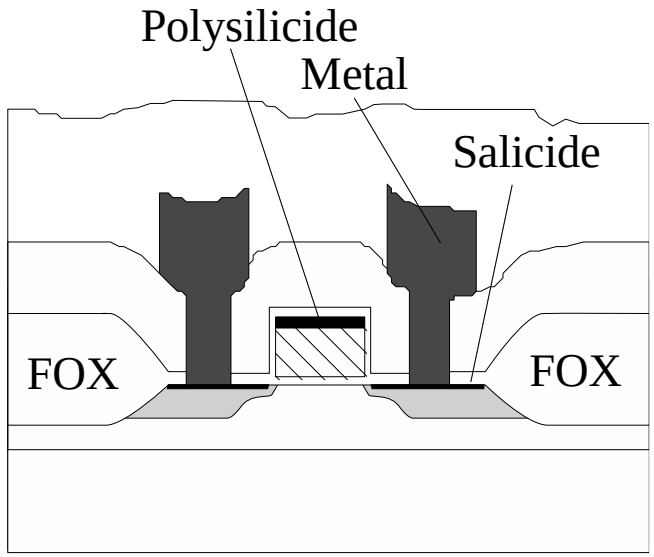
Silicide/Salicide Technology

Used to reduce interconnect resistivity by placing a low-resistance silicide such as $TiSi_2$, WSi_2, $TaSi_2$, etc. on top of polysilicon

Salicide technology (self-aligned silicide) provides low resistance source/drain connections as well as low-resistance polysilicon.



Polycide structure



Salicide structure

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SUMMARY

- Fabrication is the means by which the circuit components, both active and passive, are built as an integrated circuit.
- Basic process steps include:

  1.) Oxide growth 2.) Thermal diffusion 3.) Ion implantation

  4.) Deposition 5.) Etching 6.) Epitaxy
- The complexity of a process can be measured in the terms of the number of masking steps or masks required to implement the process.
- Major CMOS Processing Steps:

  1.) Well definition

  2.) Definition of active areas and substrate/well contacts (SiNi3)

  3.) Thick field oxide (FOX)

  4.) Thin field oxide and polysilicon

  5.) Diffusion of the source and drains (includes the LDD)

  6.) Dielectric layer/Contacts (planarization)

  7.) Metallization

  8.) Dielectric layer/Vias

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