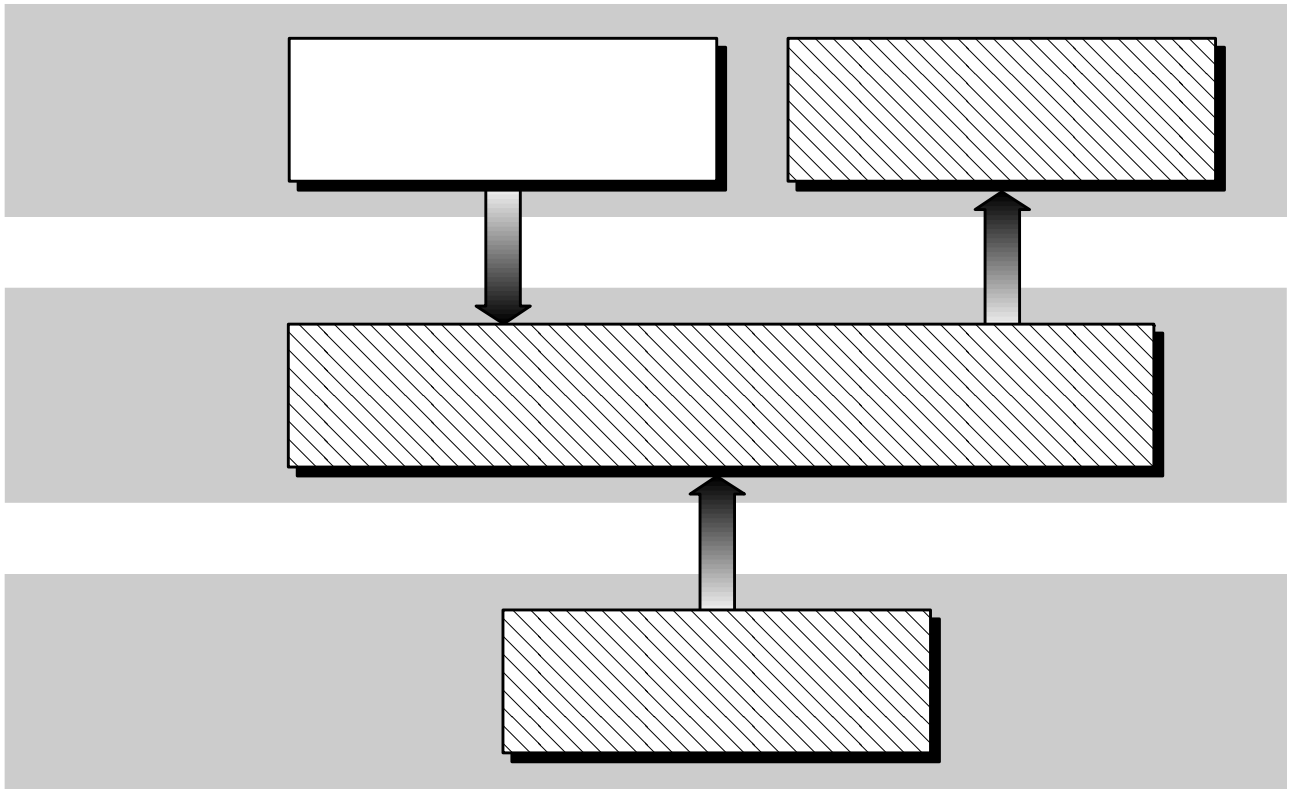
LECTURE 6 –DIGITAL PHASE LOCK LOOPS (DPLLs)

INTRODUCTION

Topics

- Noise Performance of the DPLL
- DPLL Design Procedure
- DPLL System Simulation

Organization:



NOISE PERFORMANCE OF THE DPLL

Combination of Noise and Information

In the LPLL, the noise and information signals are added because of the linear multiplier PD.

The noise supression of DPLL's is generally better than LPLL's but no theory of noise exists for the DPLL.

The following pages provide some insight into the noise performance of the DPLL.

Noise Performance of a DPLL with an EXOR PD

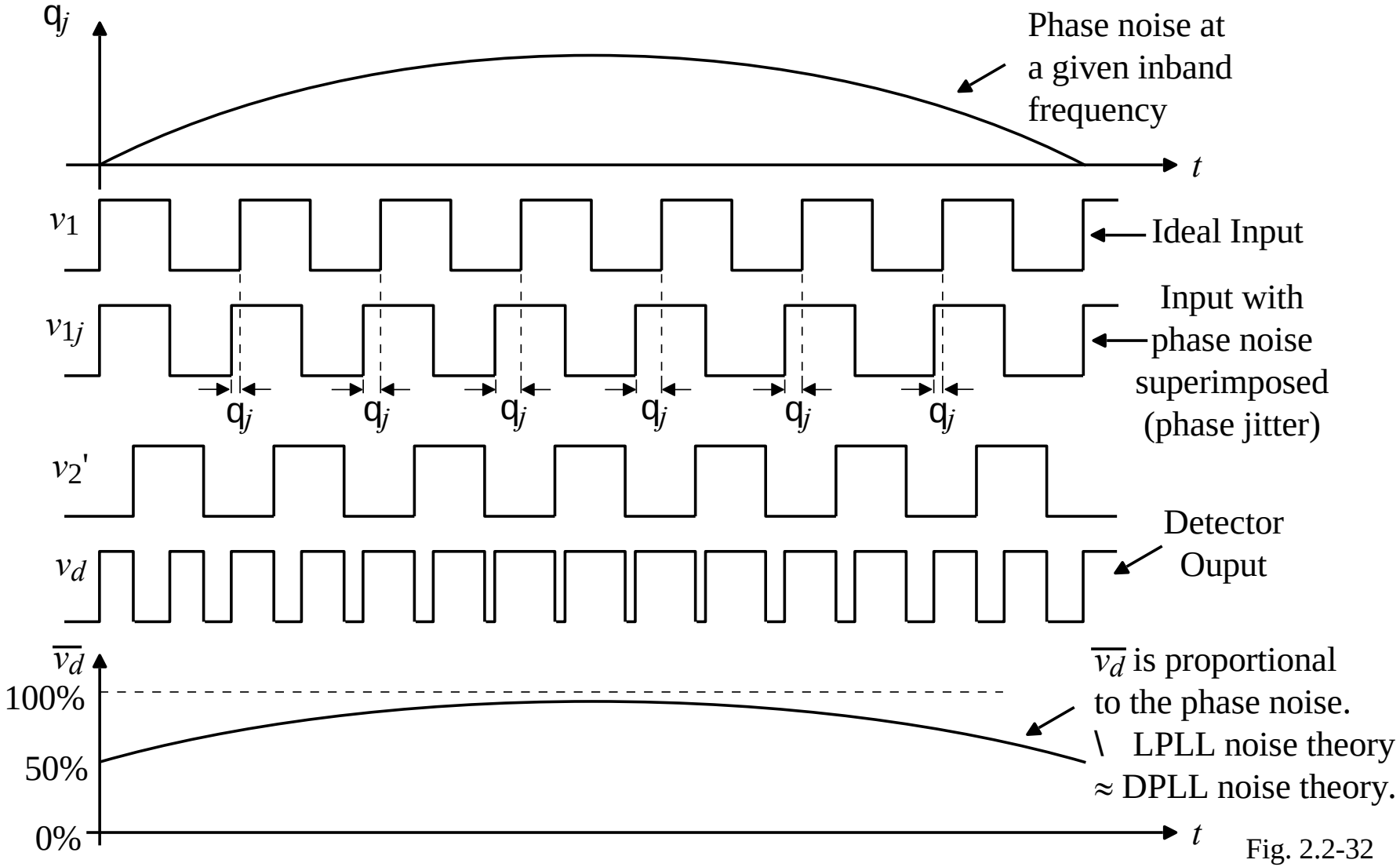
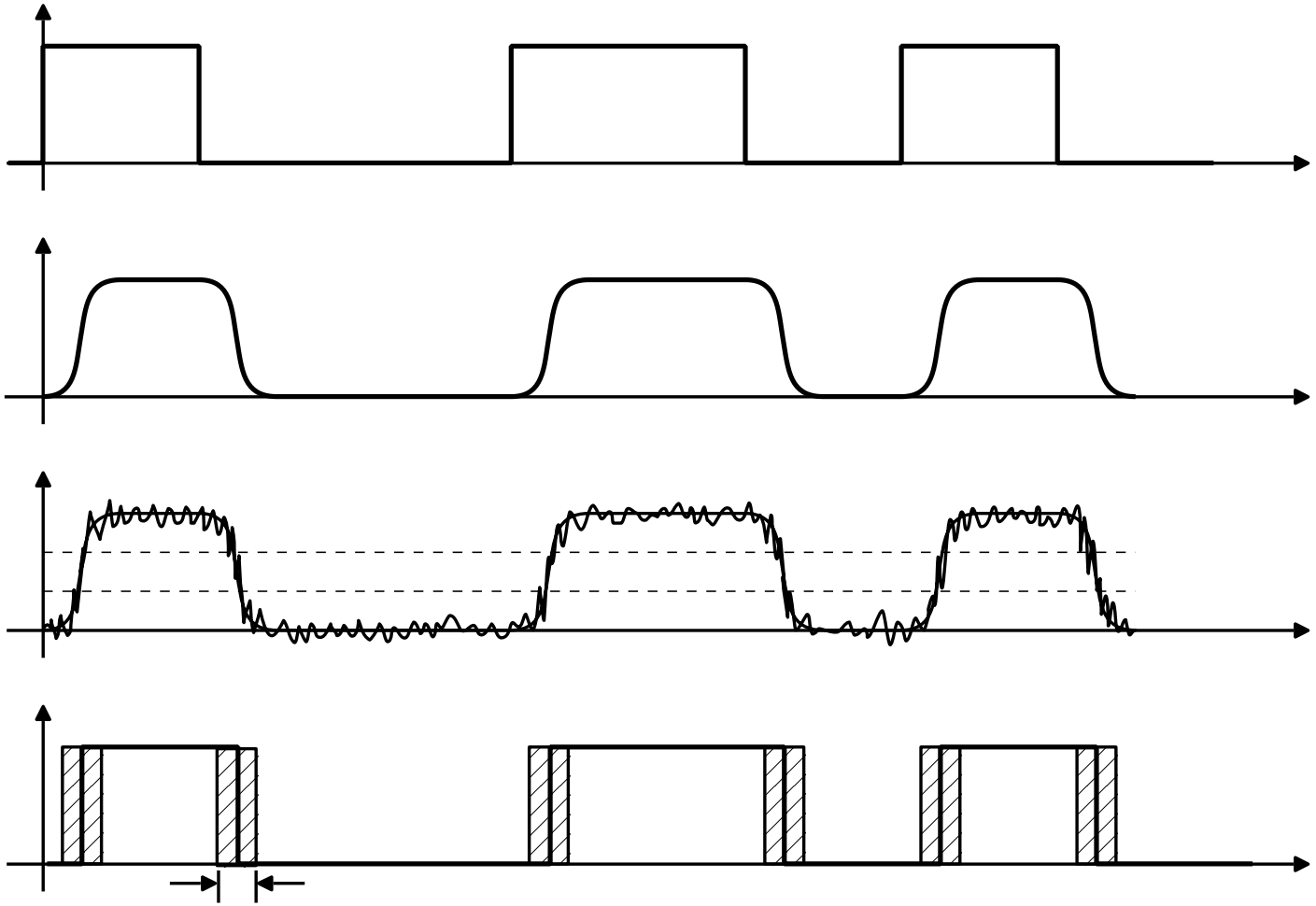


Fig. 2.2-32

Phase Noise in a Communication Signal

Consider the following simple noise model-



Input Signal-to-Noise Ratio

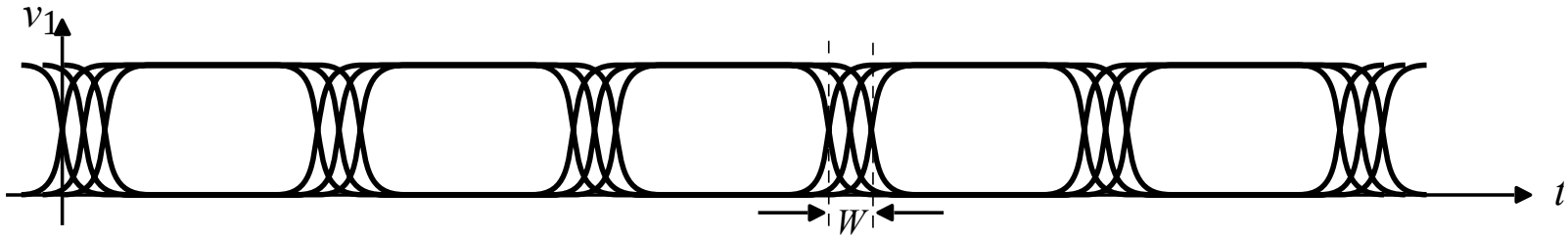
The input signal noise ratio of a pulse with phase jitter is defined as,

$$SNR_i = \frac{1}{2\,\overline{\theta_{n1}{}^2}}$$

where

$$\overline{\theta_{n1}{}^2} \approx \frac{W^2}{36}$$

where,



Phase Noise in a DPLL with a JK Flip-Flop and a PFD

The basic difference is that the JK Flip-flop and PFD are edge-triggered.

When the input signal fades ($v_1 \rightarrow 0$), the reshaped signal can stick at a distinct logic level.

Conclusion:

The noise suppression of the DPLL is about the same for all phase detectors as long as none of the edges of the reference get lost by fading. If fading occurs, the EXOR offers better noise performance.

Summary of DPLL Noise Performance:

P_s = input signal power

P_n = input noise power

B_i = input noise bandwidth

B_L = noise bandwidth $\approx \frac{\omega_n}{2}\left(\zeta + \frac{1}{4\zeta}\right)$

SNR_i = SNR of the input signal = $\frac{P_s}{P_n}$

SNR_L = SNR of the loop = $SNR_i \ \frac{B_i}{2B_L}$

DPLL DESIGN PROCEDURE

Design Procedure

Objective: Design K_o, K_d, ζ, and $F(s)$

Given: Phase detector and VCO

Steps:

1.) Specify $f_1(min)$, $f_1(max)$, $f_2(min)$, and $f_2(max)$.

2.) Design N unless otherwise specified.

Given: $\omega_n(min) < \omega_n < \omega_n(max)$ and $\zeta_{min} < \zeta < \zeta_{max}$

For these ranges we get approximately,

$$\frac{\omega_n(max)}{\omega_n(min)} = \sqrt{\frac{N_{max}}{N_{min}}} \quad \text{and} \quad \frac{\zeta_{max}}{\zeta_{min}} = \sqrt{\frac{N_{max}}{N_{min}}} \rightarrow \quad N = N_{mean} = \sqrt{N_{max}N_{min}}$$

3.) Determine ζ. Typically, $\zeta \approx 0.7$.

4.) If noise is of concern, continue with the next step, otherwise go to step 12.

5.) If there are missing edges in the input signal (fading), go to step 6, otherwise go to step 7.

6.) Choose an EXOR phase detector. Continue with step 8.

$$K_d = \frac{V_{OH}\text{-}V_{OL}}{\pi}$$

Design Procedure – Continued

7.) Choose the JK Flip-flop or PFD as the phase detector.

$$K_d = \frac{V_{OH}\text{-}V_{OL}}{2\pi} \qquad \text{(JK flip-flop)}$$

$$K_d = \frac{V_{OH}\text{-}V_{OL}}{4\pi} \qquad \text{(PFD)}$$

8.) Specify B_L.

B_L should be chosen so that $SNR_i \dfrac{B_i}{2B_L} \geq 4$

$\overline{\theta_{n1}{}^2} \rightarrow SNR_i$ and $B_i \Rightarrow B_L$

- If N changes, this can create a problem because

$$B_L = \frac{\omega_n}{2}\left(\zeta + \frac{1}{4\zeta}\right)$$

and both ω_n and ζ vary with N.

- Need to check that $B_L(min)$ is large enough.
- If B_L is too small, then N should be increased.

Design Procedure – Continued

9.) Find K_o.

$$K_o = \frac{\omega_2(max)-\omega_2(min)}{v_f(max)-v_f(min)}$$

10.) Find ω_n given B_L and ζ.

$$\omega_n = \frac{8B_L\zeta}{1+4\zeta}$$

If N is variable, use B_L and ζ correspondingly to $N = N_{mean}$.

11.) Specify the loop filter.

Given ω_n, ζ, K_o, K_d, and N find τ_1, τ_2, and K_a (K_a>1).

Go to step 19.

12.) Continued from step 4.

Choose the PFD $\rightarrow$ $K_d = \frac{V_{OH}-V_{OL}}{4\pi}$

13.) Find K_o.

$$K_o = \frac{\omega_2(max)-\omega_2(min)}{v_f(max)-v_f(min)}$$

Design Procedure – Continued

14.) Specify the type of loop filter. Use the passive lag filter as the others offer no benefits.

15.) Determine ω_n.

a.) Fast switching (T_p). Go to step 16.

b.) DPLL does not lock out when switching from $N_o f_{ref}$ to $(N_o+1)\, f_{ref}$. $\therefore\ \Delta\omega_{po} < f_{ref}$. Go to step 20.

c.) Neither the pull-in time nor the pull-out range are critical. Go to step 21.

16.) Given the maximum T_p allowed for the largest frequency step, solve for τ_1 or $\tau_1+\tau_2$.

17.) Find ω_n.

Loop filter is passive: $$\omega_n = \sqrt{\frac{K_o K_d}{N(\tau_1+\tau_2)}}$$

Active lag filter: $$\omega_n = \sqrt{\frac{K_o K_d K_a}{N\tau_1}}$$

Active PI filter: $$\omega_n = \sqrt{\frac{K_o K_d}{N\tau_1}}$$

Design Procedure – Continued

18.) Given ω_n and ζ, find τ_2.

$$\tau_2 = \frac{2\zeta}{\omega_n}$$

If the system cannot be realized (negative values of τ_1 or τ_2), modify ω_n and ζ appropriately.

19.) Given τ_1 and τ_2 (and K_a), determine the filter components.

20.) Given $\Delta\omega_{po}$ and ζ, find ω_n.

$$\omega_n \approx \frac{\Delta\omega_{po}}{11.55(\zeta+0.5)}$$

21.) Given T_L, find ω_n from $\omega_n \approx 2\pi/T_L$.

22.) Given ω_n, find τ_1 and $\tau_1+\tau_2$.

Passive lag filter: $$\tau_1+\tau_2 = \frac{K_o K_d}{N\omega_n^2}$$

Active lag filter: $$\tau_1 = \frac{K_o K_d K_a}{N\omega_n^2}$$

Active PI filter: $$\tau_1 = \frac{K_o K_d}{N\omega_n^2}$$

Flowchart of the DPLL Design Procedure

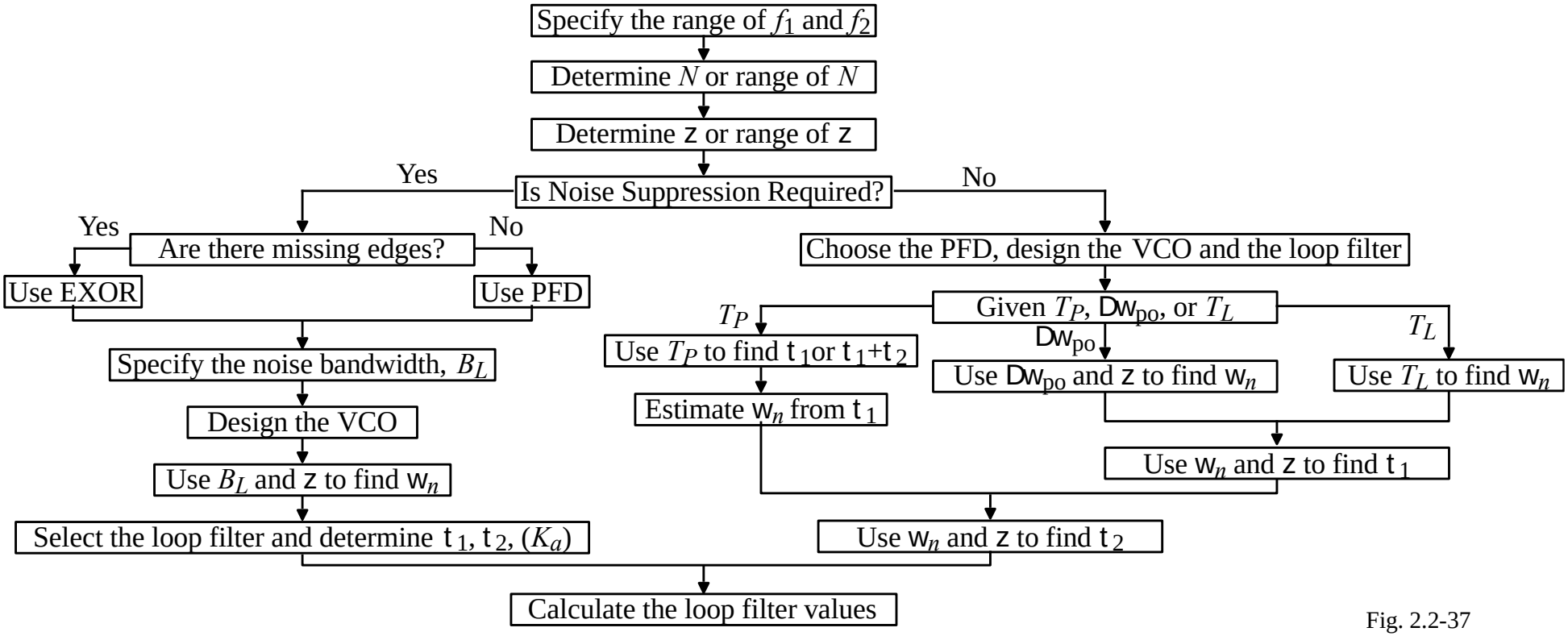


Fig. 2.2-37

Design Example – A Frequency Synthesizer Using the 74HC/HCT4076

Design a DPLL frequency synthesizer using the CMOS 74HC/HCT4076 PLL. The frequency sythesizer should be able to produce a set of frequencies in the range of 1MHz to 2MHz with a channel spacing of 10kHz. Use a PFD and a passive lag-lead filter.

Design:

1.)Determine the ranges of the input and output frequencies.

f_1 is constant at 10kHz. $f_2(min)$ = 1MHz and $f_2(max)$ = 2MHz

2.) Choose N.

$$N_{max} = \frac{2\text{MHz}}{10\text{kHz}} = 200 \qquad \text{and} \qquad N_{min} = \frac{1\text{MHz}}{10\text{kHz}} = 100$$

$$\therefore \quad N_{mean} = \sqrt{N_{max} \cdot N_{min}} = 141$$

3.)Find ζ. Start by choosing $\zeta = 0.7$ and find ζ_{max} and ζ_{min}.

$$\frac{\zeta_{max}}{\zeta_{min}} = \sqrt{\frac{N_{max}}{N_{min}}} = \sqrt{2} \qquad \text{and} \qquad \zeta = \sqrt{\zeta_{max} \cdot \zeta_{min}} = 0.7$$

$$\therefore \quad \zeta_{min}{}^2\sqrt{2} = 0.49 \quad \rightarrow \quad \zeta_{min} = 0.59 \quad \text{and} \quad \zeta_{max} = 0.59\sqrt{2} = 0.83$$

$$\therefore \quad 0.59 < \zeta < 0.83 \quad \text{which is consistent with our choice of } \zeta.$$

4.)Select the PFD as the phase detector. For the 74HC/HCT4076, V_{OH} = 5V and V_{OL}=0V. This gives a $K_d = 5\text{V}/4\pi = 0.4$ V/rad.

Design Example – Continued

5.) According to the data sheet of the 74HC4046A, the VCO operates linearly in the voltage range of v_f = 1.1V to 3.9V as shown.

$$\therefore K_o = \frac{2\text{x}10^6\text{x}2\pi}{3.9\text{-}1.1} = 2.2\text{x}10^6 \text{ rads/V}\cdot\text{sec}$$

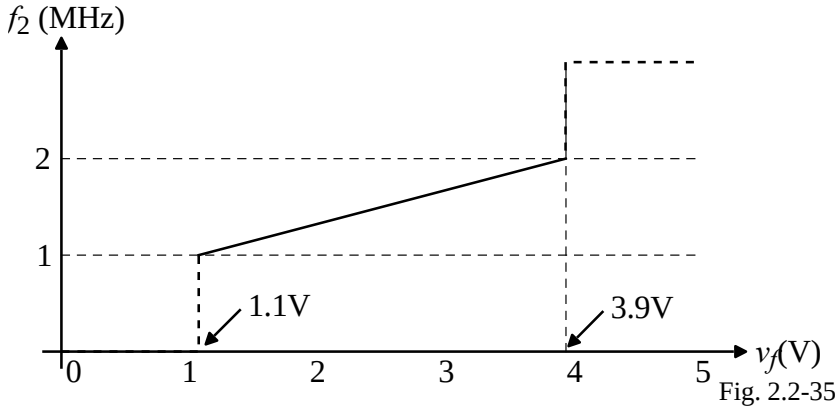


Fig. 2.2-35

The data sheet also requires calculation of two resistors, R_1 and R_2, and a capacitor, C_1.

Using the graphs from the data sheet gives,

R_1 = 47kΩ, R_2 = 130kΩ, and C_1 = 100pF.

6.)Assume the loop should lock with 1ms.

$$\therefore \quad T_L = 1\text{ms} \quad \rightarrow \quad \omega_n = 2\pi/T_L = 6280 \text{ rads/sec.}$$

7.)Using a passive loop filter we get,

$$\tau_1+\tau_2 = \frac{K_oK_d}{N\omega_n^2} = \frac{2.2\text{x}10^6\cdot 0.4}{141\cdot 6280^2} = 161\mu\text{s}$$

8.) $\tau_2 = \dfrac{2\zeta}{\omega_n} = \dfrac{2\cdot 0.7}{6280} = 223\mu\text{s!!!}$ (The problem is that $\tau_1+\tau_2$ is too small)

Go back and choose T_L = 2ms $\rightarrow$ $\omega_n = 2\pi/T_L = 3140$ rads/sec.

$$\tau_1+\tau_2 = \frac{K_oK_d}{N\omega_n^2} = \frac{2.2\text{x}10^6\cdot 0.4}{141\cdot 3140^2} = 633\mu\text{s} \text{ and } \tau_2 = \frac{2\zeta}{\omega_n} = \frac{2\cdot 0.7}{3140} = 446\mu\text{s} \rightarrow \tau_1 = 187\mu\text{s}$$

Design Problem – Continued

9.)Design the loop filter.

For optimum sideband supression, C should be large. Choose $C = 0.33\mu F$.

$$\therefore \quad R_1 = \frac{\tau_1}{C} = \frac{187\text{x}10^{-6}}{0.33\text{x}10^{-6}} = 567\Omega \qquad \text{and} \qquad R_2 = \frac{\tau_2}{C} = \frac{446\text{x}10^{-6}}{0.33\text{x}10^{-6}} = 1.351\Omega$$

The data sheet requires that $R_1+R_2 \geq 470\Omega$ which is satisfied.

Block diagram of the DPLL frequency synthesizer design of this example:

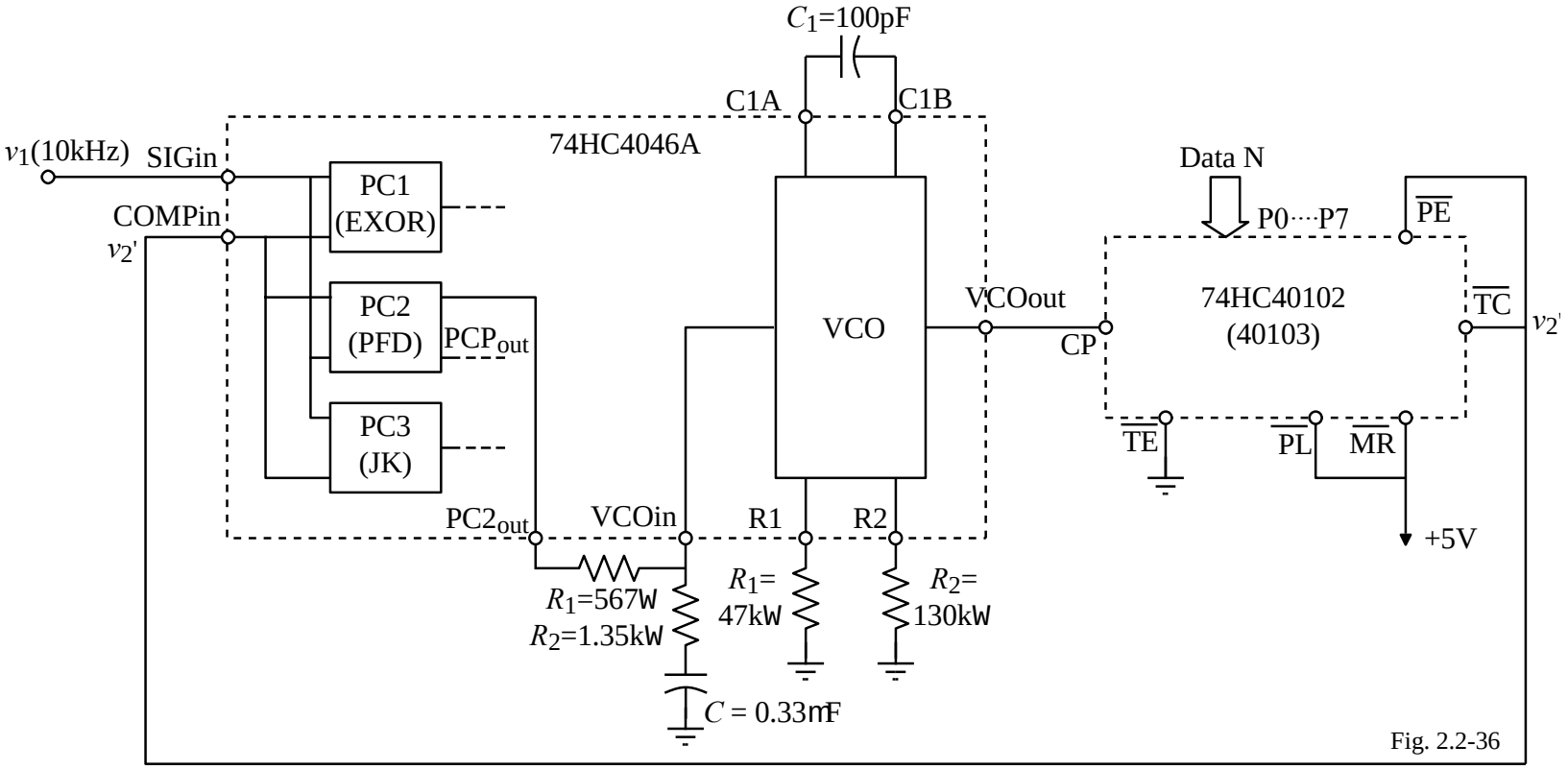


Fig. 2.2-36

Simulation of the DPLL Example

The block diagram of this example is shown below.

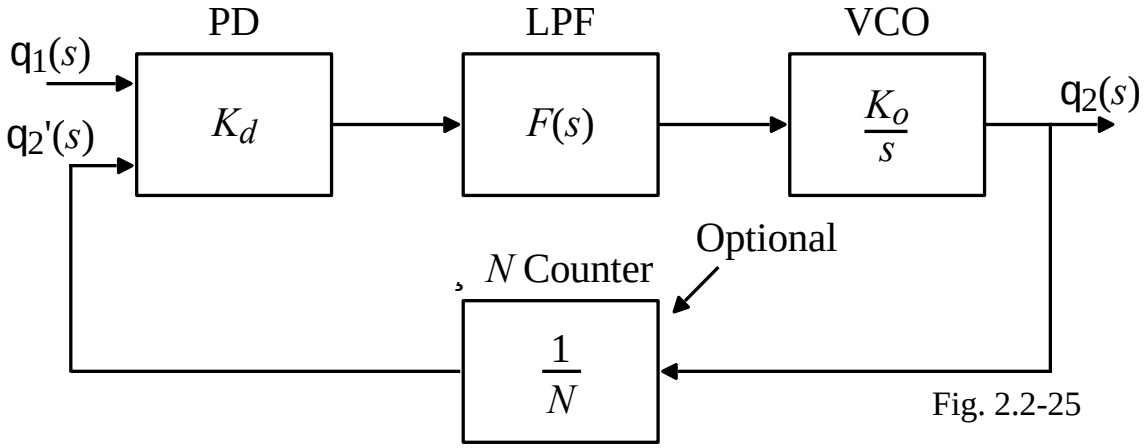


Fig. 2.2-25

The PFD-charge pump combination can be approximated as†

$$\text{“}K_dF(s)\text{”} = \frac{K_d(1+s\tau_2)}{s(\tau_1+\tau_2)}$$

Therefore, the loop gain becames

$$LG(s) = \frac{K_oK_d(1+s\tau_2)}{s^2(\tau_1+\tau_2)} = \frac{K_v(1+s\tau_2)}{(s+\varepsilon)^2(\tau_1+\tau_2)}$$ (the factor ε is used for simulation purposes)

For this problem,

K_d = 0.4V/rad., K_o = 2.2x10^6, τ_2 = 446µs, and $\tau_2+\tau_2$ = 633µs. Also choose ε = 0.01.

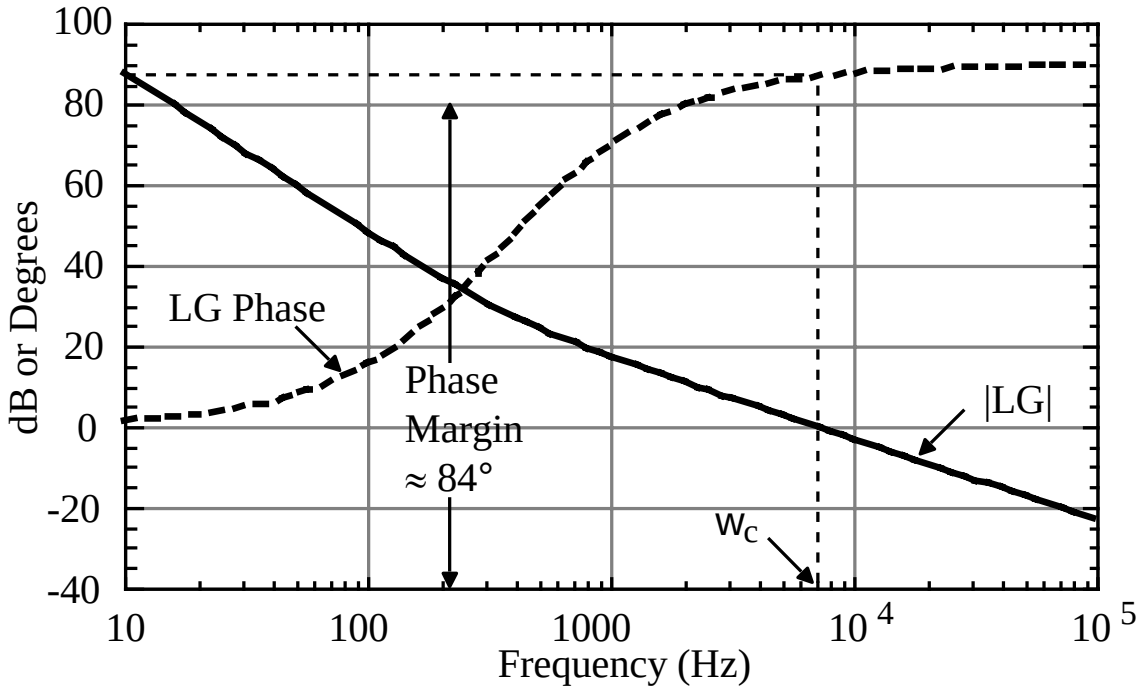
† R.E. Best, “Phase-Locked Loops – Design, Simulation, and Applications,” 4th Ed., McGraw-Hill, NY, p. 103

Simulation of the DPLL Example – Continued

PSPICE Input File

```
DPLL Design Problem-Open Loop Response - Best
VS 1 0 AC 1.0
R1 1 0 10K
* Loop bandwidth = Kv =8.8x10E5 sec.-1   Tau1=187E-6  Tau2=446E-6 N=141
ELPLL 2 0 LAPLACE {V(1)}= {8.8E+6/(S+0.01)/141*(0.446E-3*S+1)/(S+0.01)/0.633E-3}
R2 2 0 10K
*Steady state AC analysis
.AC DEC 20 10 100K
.PRINT AC VDB(2) VP(2)
.PROBE
.END
```

Simulation Results:



Note that the phase is very close to 0° and |LG|>>1 at low frequencies which is typical of type II systems.

DPLL SYSTEM SIMULATION

Examples of Case Studies using the Best Software†

PLL Parameters-

Supply voltages:

Positive supply = 5V Negative supply = -5V

Phase detector:

V_{sat}^{+} = 4.5V V_{sat}^{-} = 0.5V

Loop filter:

τ_1 = 500μs τ_2 = 50μs

Oscillator:

K_o = 130,000 rads/V·sec V_{sat}^{+} = 4.5V V_{sat}^{-} = 0.5V

The simulation program will be used to verify the following calculated values:

ω_n = 17,347 rads/sec. (calculated prior to simulation)

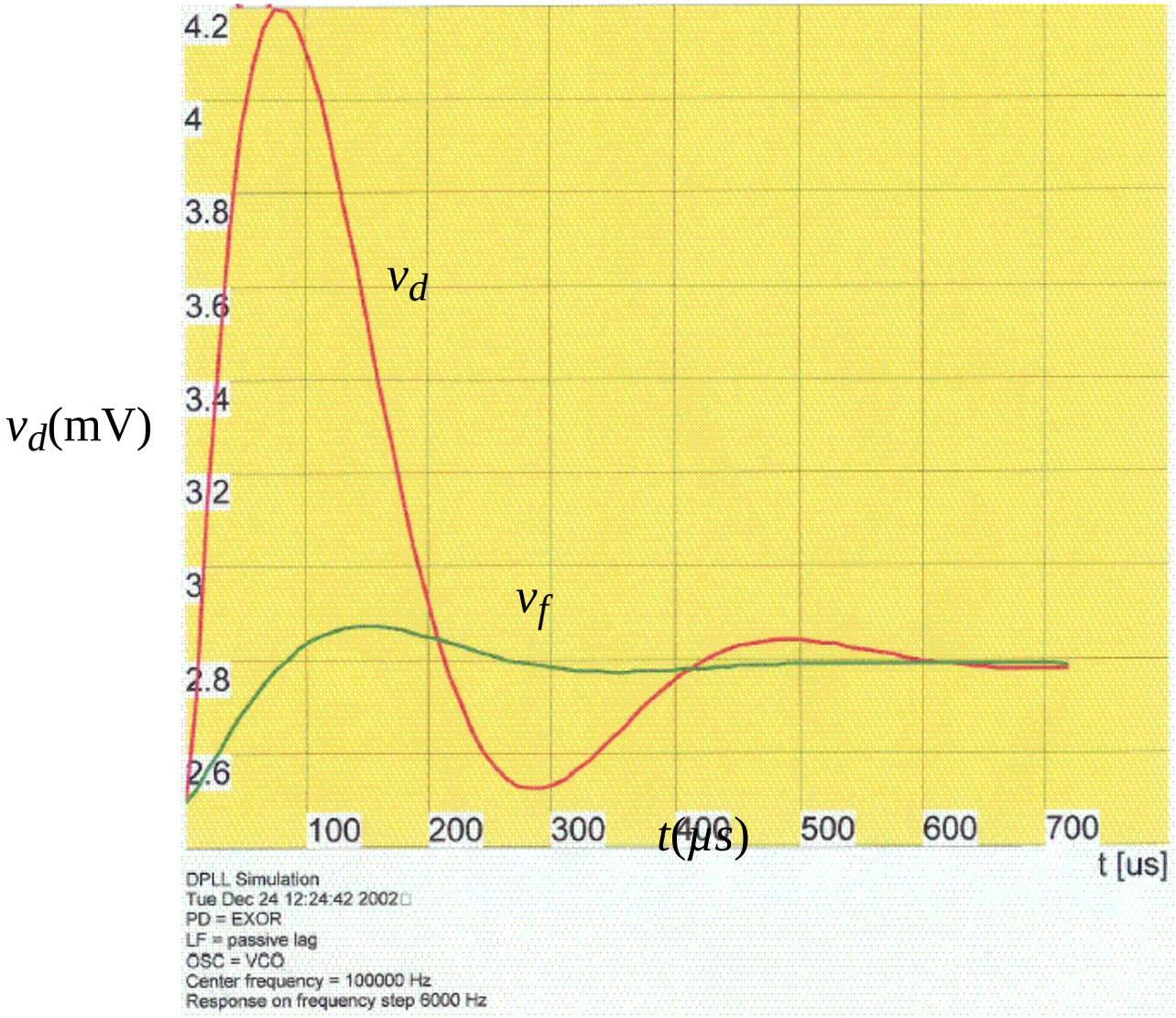
ζ = 0.486 (calculated prior to simulation)

Δf_{po} = 7719 Hz

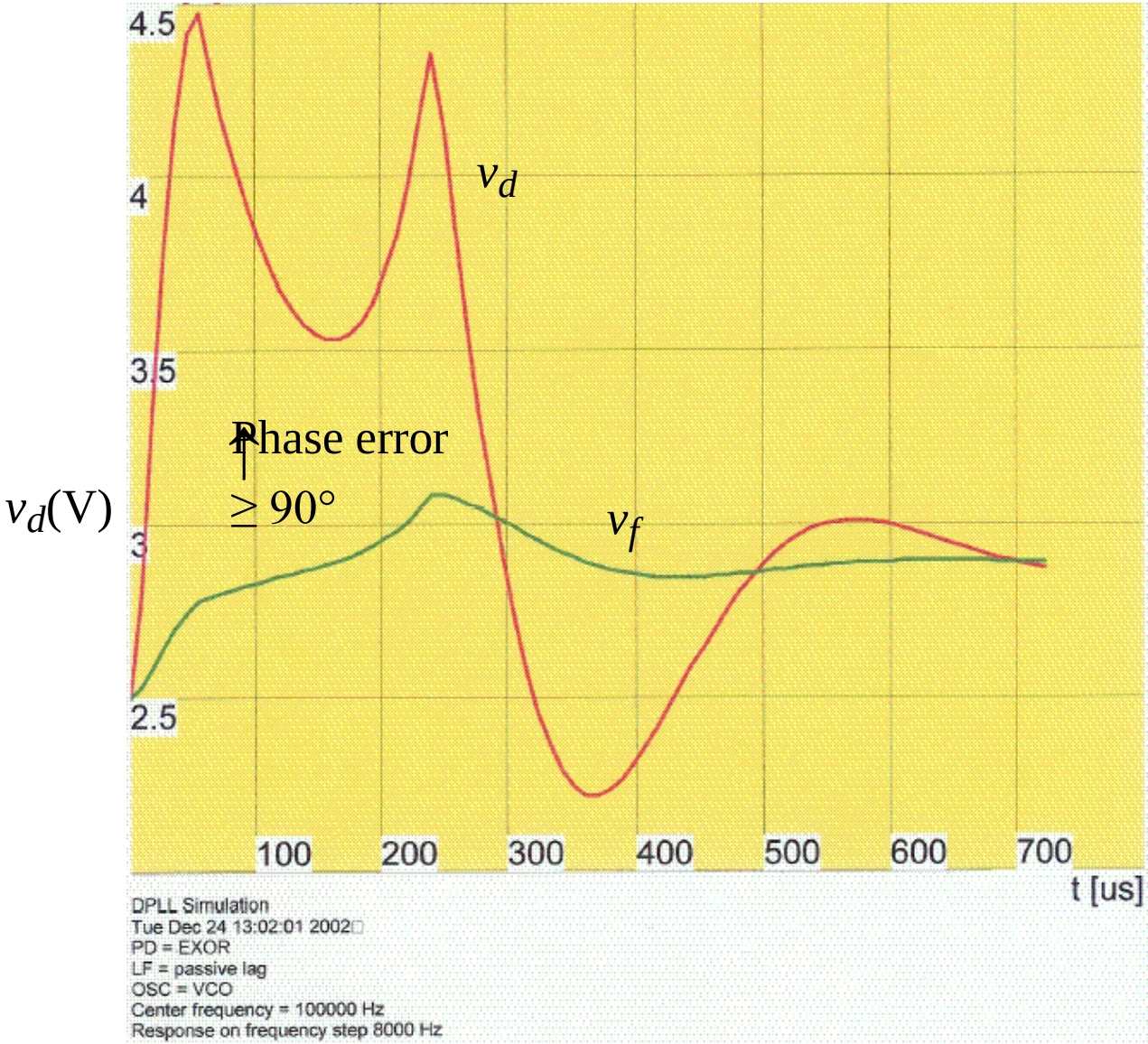
Δf_p = 13,192 Hz

† Roland E. Best, Phase-Locked Loops – Design, Simulation, and Applications, 4th ed., McGraw-Hill Book Co., 1999, New York, NY

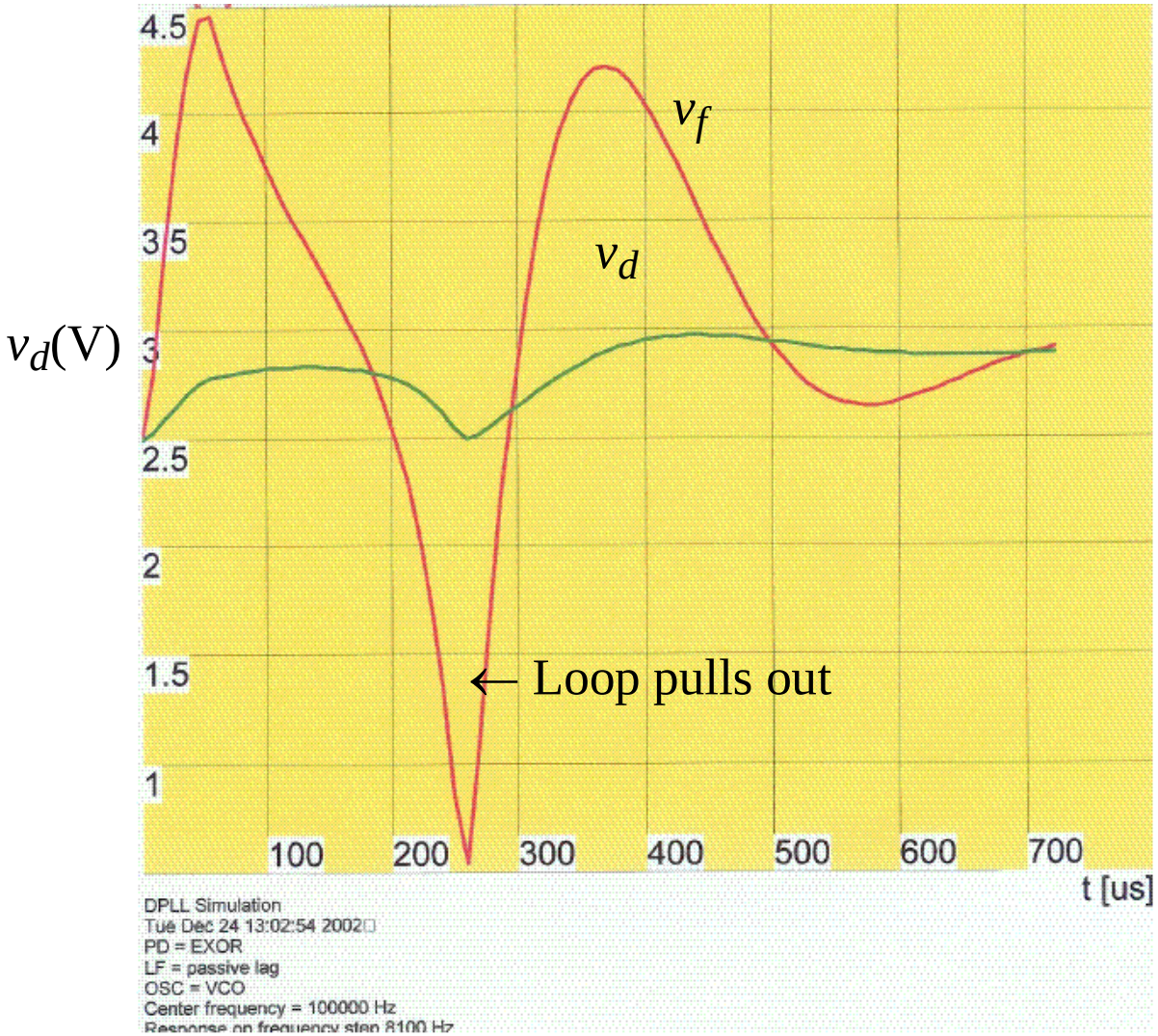
Case 1 – System Benchmark



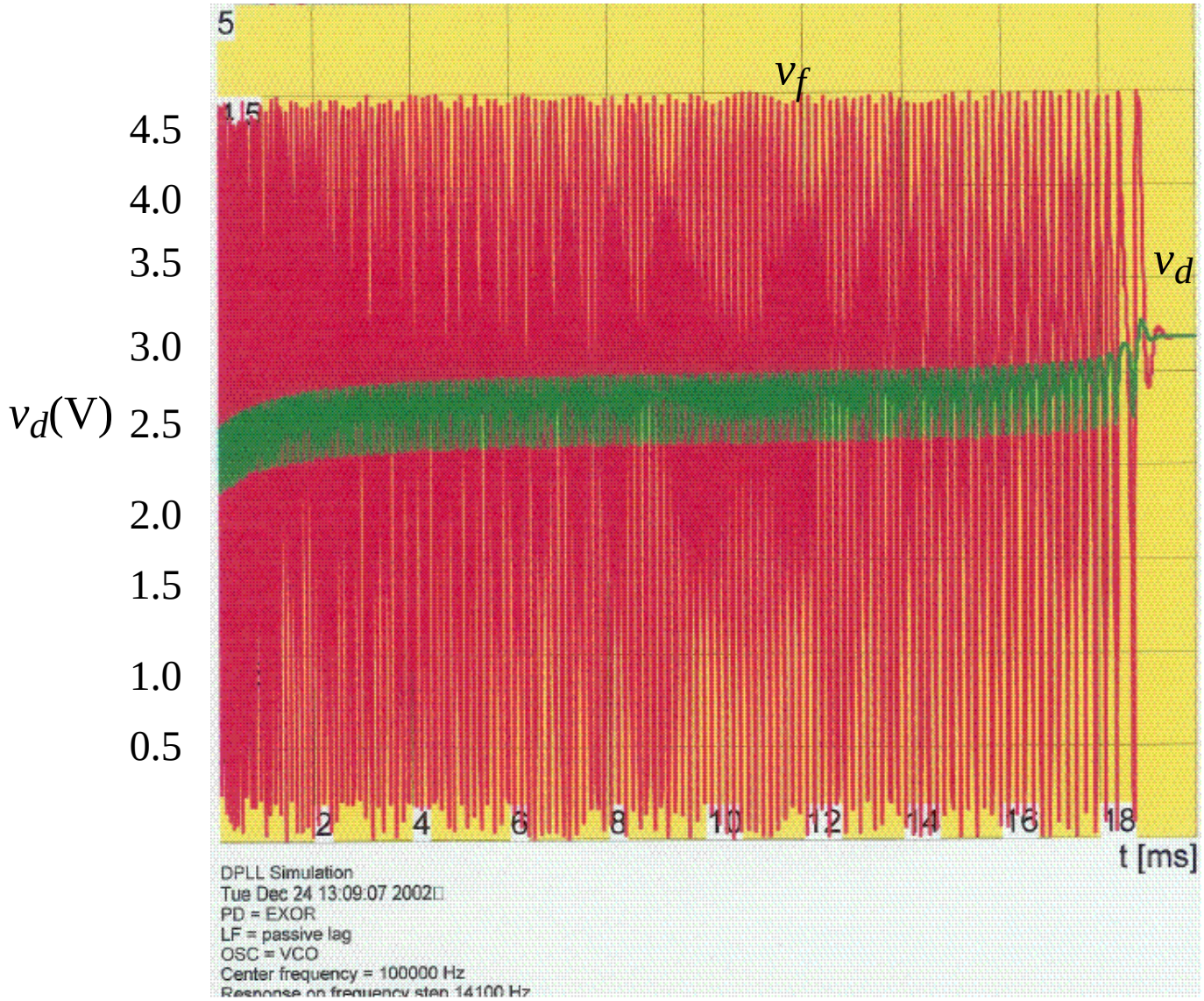
Case 2 - Δf = 8000Hz



Case 3 – Loop Just Locks Out



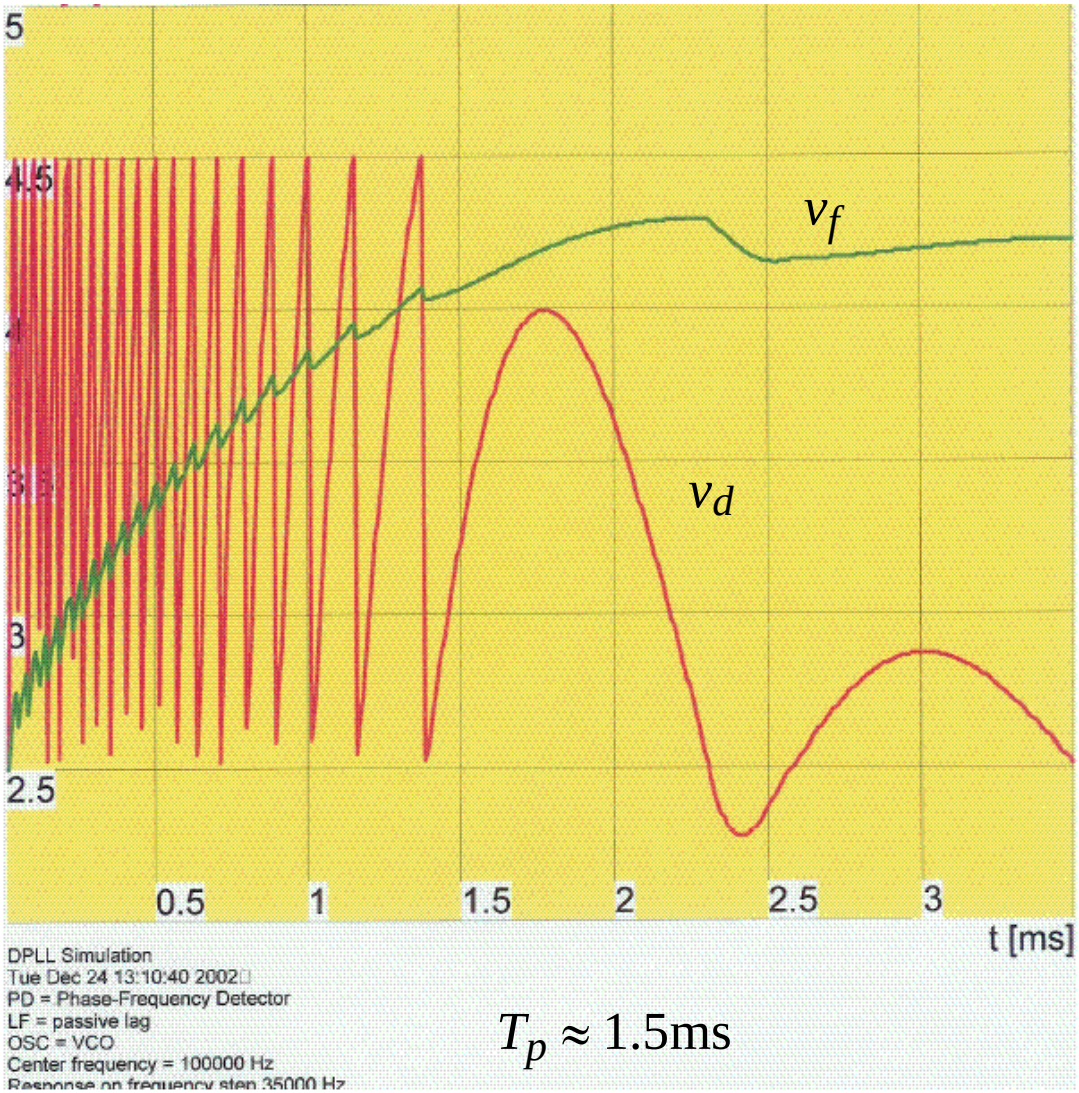
Case 4 – Pull-In Range Verification



Loop will not pull back in for $df > 14{,}200$ Hz

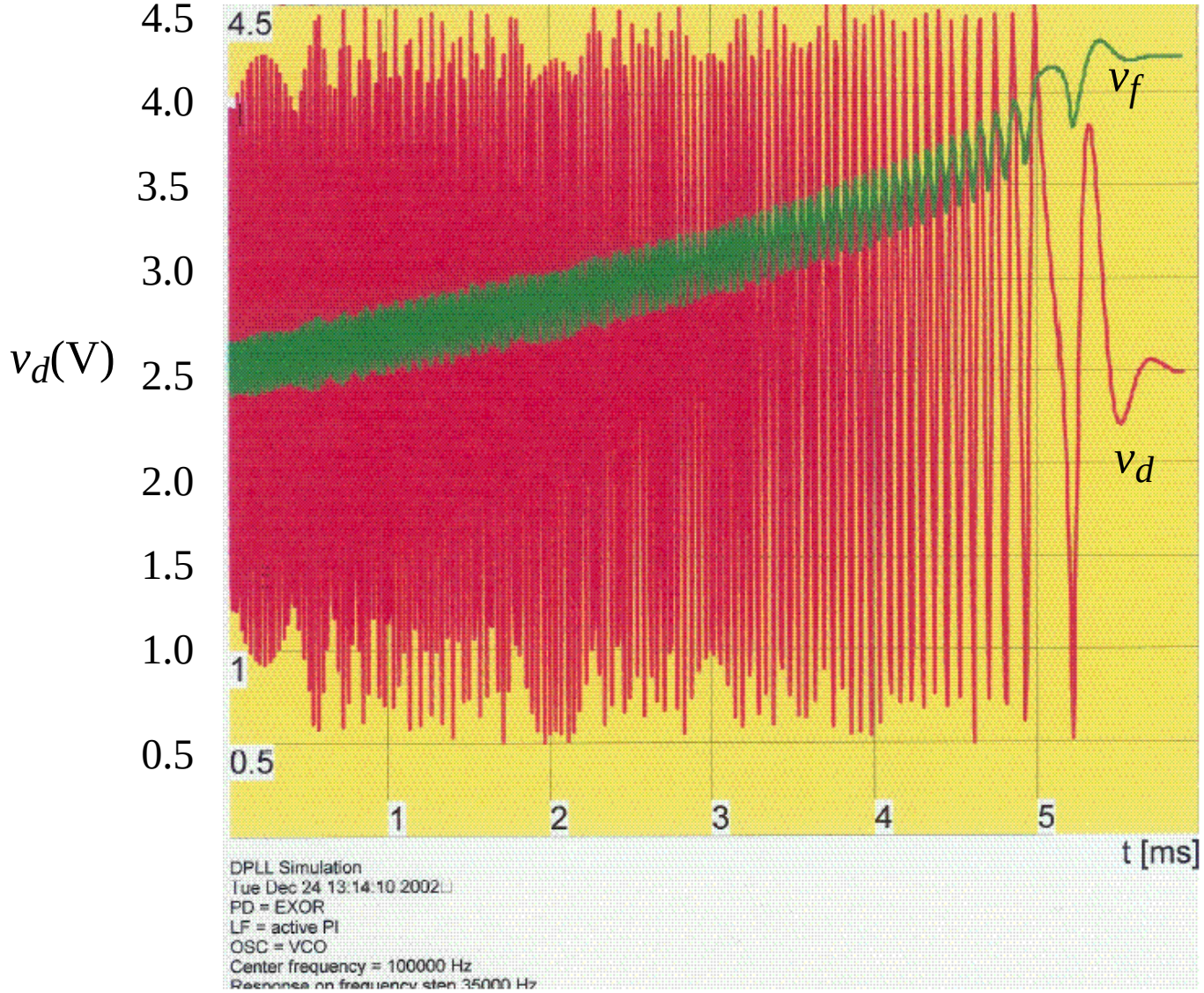
Case 5 – PFD and Illustration of a Virtually Infinite Pull-In Range

$\Delta f_p = \pm 40$kHz $\Delta f = 35$ kHz to avoid clipping of v_f.



$T_p \approx 1.5$ms

Case 6 – EXOR with Active PI Filter



SUMMARY

- Illustrated the Noise Performance of the DPLL
- Presented a DPLL Design Procedure
- Showed how to do DPLL System Simulation
- The DPLL is much more compatible with IC technology and is the primary form of PLL used for frequency synthesizers