LECTURE 6 –DIGITAL PHASE LOCK LOOPS (DPLLs)

INTRODUCTION

Topics
• Noise Performance of the DPLL
• DPLL Design Procedure
• DPLL System Simulation

Organization:
NOISE PERFORMANCE OF THE DPLL

Combination of Noise and Information

In the LPLL, the noise and information signals are added because of the linear multiplier PD.

The noise suppression of DPLL’s is generally better than LPLL’s but no theory of noise exists for the DPLL.

The following pages provide some insight into the noise performance of the DPLL.
Noise Performance of a DPLL with an EXOR PD

Phase noise at a given inband frequency

Ideal Input

Input with phase noise superimposed (phase jitter)

Detector Output

$\overline{v_d}$ is proportional to the phase noise. LPLL noise theory $\approx$ DPLL noise theory.

Fig. 2.2-32
Phase Noise in a Communication Signal
Consider the following simple noise model-

\[ \text{Diagram of phases and noise models} \]
Input Signal-to-Noise Ratio

The input signal noise ratio of a pulse with phase jitter is defined as,

\[ SNR_i = \frac{1}{2 \theta_n^2} \]

where

\[ \theta_n^2 \approx \frac{W^2}{36} \]

where,
Phase Noise in a DPLL with a JK Flip-Flop and a PFD

The basic difference is that the JK Flip-flop and PFD are edge-triggered.

When the input signal fades ($v_1 \rightarrow 0$), the reshaped signal can stick at a distinct logic level.

Conclusion:

The noise suppression of the DPLL is about the same for all phase detectors as long as none of the edges of the reference get lost by fading. If fading occurs, the EXOR offers better noise performance.

Summary of DPLL Noise Performance:

- $P_s = \text{input signal power}$
- $P_n = \text{input noise power}$
- $B_i = \text{input noise bandwidth}$

$$B_L = \text{noise bandwidth} \approx \frac{\omega_n}{2} \left( \zeta + \frac{1}{4\zeta} \right)$$

$$SNR_i = \text{SNR of the input signal} = \frac{P_s}{P_n}$$

$$SNR_L = \text{SNR of the loop} = SNR_i \frac{B_i}{2B_L}$$
DPLL DESIGN PROCEDURE

Design Procedure
Objective: Design $K_o$, $K_d$, $\zeta$, and $F(s)$

Given: Phase detector and VCO

Steps:
1.) Specify $f_1(\text{min})$, $f_1(\text{max})$, $f_2(\text{min})$, and $f_2(\text{max})$.
2.) Design $N$ unless otherwise specified.
   
   Given: $\omega_n(\text{min}) < \omega_n < \omega_n(\text{max})$ and $\zeta_{\text{min}} < \zeta < \zeta_{\text{max}}$
   
   For these ranges we get approximately,
   
   $$\frac{\omega_n(\text{max})}{\omega_n(\text{min})} = \sqrt{\frac{N_{\text{max}}}{N_{\text{min}}}} \quad \text{and} \quad \frac{\zeta_{\text{max}}}{\zeta_{\text{min}}} = \sqrt{\frac{N_{\text{max}}}{N_{\text{min}}}} \rightarrow N = N_{\text{mean}} = \sqrt{N_{\text{max}}N_{\text{min}}}$$

3.) Determine $\zeta$. Typically, $\zeta \approx 0.7$.
4.) If noise is of concern, continue with the next step, otherwise go to step 12.
5.) If there are missing edges in the input signal (fading), go to step 6, otherwise go to step 7.
6.) Choose an EXOR phase detector. Continue with step 8.
   
   $$K_d = \frac{V_{OH}-V_{OL}}{\pi}$$
Design Procedure – Continued

7.) Choose the JK Flip-flop or PFD as the phase detector.

\[ K_d = \frac{V_{OH} - V_{OL}}{2\pi} \quad \text{(JK flip-flop)} \]

\[ K_d = \frac{V_{OH} - V_{OL}}{4\pi} \quad \text{(PFD)} \]

8.) Specify \( B_L \).

\( B_L \) should be chosen so that

\[ SNR_i \frac{B_i}{2B_L} \geq 4 \]

\[ \theta_{n1}^2 \rightarrow SNR_i \quad \text{and} \quad B_i \Rightarrow B_L \]

- If \( N \) changes, this can create a problem because

\[ B_L = \frac{\omega_n}{2} \left( \zeta + \frac{1}{4\zeta} \right) \]

and both \( \omega_n \) and \( \zeta \) vary with \( N \).

- Need to check that \( B_L(\text{min}) \) is large enough.

- If \( B_L \) is too small, then \( N \) should be increased.
**Design Procedure – Continued**

9.) Find $K_o$.

\[
K_o = \frac{\omega_2(\text{max}) - \omega_2(\text{min})}{v_f(\text{max}) - v_f(\text{min})}
\]

10.) Find $\omega_n$ given $B_L$ and $\zeta$.

\[
\omega_n = \frac{8B_L\zeta}{1 + 4\zeta}
\]

If $N$ is variable, use $B_L$ and $\zeta$ correspondingly to $N = N_{\text{mean}}$.

11.) Specify the loop filter.

Given $\omega_n$, $\zeta$, $K_o$, $K_d$, and $N$ find $\tau_1$, $\tau_2$, and $K_a$ ($K_a > 1$).

Go to step 19.

12.) Continued from step 4.

Choose the PFD $\rightarrow$ \[ K_d = \frac{V_{OH} - V_{OL}}{4\pi} \]

13.) Find $K_o$.

\[
K_o = \frac{\omega_2(\text{max}) - \omega_2(\text{min})}{v_f(\text{max}) - v_f(\text{min})}
\]
Design Procedure – Continued

14.) Specify the type of loop filter. Use the passive lag filter as the others offer no benefits.

15.) Determine $\omega_n$.
   
   a.) Fast switching ($T_p$). Go to step 16.
   
   b.) DPLL does not lock out when switching from $N_o f_{ref}$ to $(N_o+1)f_{ref}$.  \[ \Delta \omega_{po} < f_{ref}. \]
   
   Go to step 20.
   
   c.) Neither the pull-in time nor the pull-out range are critical. Go to step 21.

16.) Given the maximum $T_p$ allowed for the largest frequency step, solve for $\tau_1$ or $\tau_1+\tau_2$.

17.) Find $\omega_n$.

Loop filter is passive:  
\[ \omega_n = \sqrt{\frac{K_oK_d}{N(\tau_1+\tau_2)}} \]

Active lag filter:  
\[ \omega_n = \sqrt{\frac{K_oK_dK_a}{N\tau_1}} \]

Active PI filter:  
\[ \omega_n = \sqrt{\frac{K_oK_d}{N\tau_1}} \]
Design Procedure – Continued

18.) Given $\omega_n$ and $\zeta$, find $\tau_2$.

$$\tau_2 = \frac{2\zeta}{\omega_n}$$

If the system cannot be realized (negative values of $\tau_1$ or $\tau_2$), modify $\omega_n$ and $\zeta$ appropriately.

19.) Given $\tau_1$ and $\tau_2$ (and $K_a$), determine the filter components.

20.) Given $\Delta\omega_{po}$ and $\zeta$, find $\omega_n$.

$$\omega_n \approx \frac{\Delta\omega_{po}}{11.55(\zeta+0.5)}$$

21.) Given $T_L$, find $\omega_n$ from $\omega_n \approx 2\pi / T_L$.

22.) Given $\omega_n$, find $\tau_1$ and $\tau_1 + \tau_2$.

Passive lag filter: $\tau_1 + \tau_2 = \frac{K_oK_d}{N\omega_n^2}$

Active lag filter: $\tau_1 = \frac{K_oK_dK_a}{N\omega_n^2}$

Active PI filter: $\tau_1 = \frac{K_oK_d}{N\omega_n^2}$
Flowchart of the DPLL Design Procedure

1. Specify the range of $f_1$ and $f_2$
2. Determine $N$ or range of $N$
3. Determine $z$ or range of $z$
4. Is Noise Suppression Required?
   - Yes
     - Are there missing edges?
       - Yes
         - Use EXOR
         - Specify the noise bandwidth, $B_L$
         - Design the VCO
         - Use $B_L$ and to find $n$
       - No
         - Use PFD
         - Select the loop filter and determine $t_1, (K_a)$
         - Calculate the loop filter values
   - No
     - Choose the PFD, design the VCO and the loop filter
     - Given $T_P, po.$ or $T_L$
     - Use $T_L$ to find $n$
     - Use $T_P$ to find $1$ or $1 + 2$
     - Estimate $n$ from $1$
     - Use $po.$ and to find $n$
     - Use $n$ and to find $t_1$
     - Use $n$ and to find $2$

Fig. 2.2-37
**Design Example – A Frequency Synthesizer Using the 74HC/HCT4076**

Design a DPLL frequency synthesizer using the CMOS 74HC/HCT4076 PLL. The frequency synthesizer should be able to produce a set of frequencies in the range of 1MHz to 2MHz with a channel spacing of 10kHz. Use a PFD and a passive lag-lead filter.

**Design:**

1.) Determine the ranges of the input and output frequencies.

   \[ f_1 \text{ is constant at 10kHz.} \quad f_2(\text{min}) = 1\text{MHz} \quad \text{and} \quad f_2(\text{max}) = 2\text{MHz} \]

2.) Choose \( N \).

   \[
   N_{\text{max}} = \frac{2\text{MHz}}{10\text{kHz}} = 200 \quad \text{and} \quad N_{\text{min}} = \frac{1\text{MHz}}{10\text{kHz}} = 100
   \]

   \[
   \therefore \quad N_{\text{mean}} = \sqrt{N_{\text{max}} \cdot N_{\text{min}}} = 141
   \]

3.) Find \( \zeta \). Start by choosing \( \zeta = 0.7 \) and find \( \zeta_{\text{max}} \) and \( \zeta_{\text{min}} \).

   \[
   \frac{\zeta_{\text{max}}}{\zeta_{\text{min}}} = \sqrt{\frac{N_{\text{max}}}{N_{\text{min}}}} = \sqrt{2} \quad \text{and} \quad \zeta = \sqrt{\zeta_{\text{max}} \cdot \zeta_{\text{min}}} = 0.7
   \]

   \[
   \therefore \quad \zeta_{\text{min}}^2 \sqrt{2} = 0.49 \quad \rightarrow \quad \zeta_{\text{min}} = 0.59 \quad \text{and} \quad \zeta_{\text{max}} = 0.59 \sqrt{2} = 0.83
   \]

   \[
   \therefore \quad 0.59 < \zeta < 0.83 \quad \text{which is consistent with our choice of} \quad \zeta.
   \]

4.) Select the PFD as the phase detector. For the 74HC/HCT4076, \( V_{OH} = 5\text{V} \) and \( V_{OL} = 0\text{V} \). This gives a \( K_d = \frac{5\text{V}}{4\pi} = 0.4 \text{ V/rad} \).
Design Example – Continued

5.) According to the data sheet of the 74HC4046A, the VCO operates linearly in the voltage range of \( V_f = 1.1\text{V} \) to \( 3.9\text{V} \) as shown.

\[
\therefore K_o = \frac{2 \times 10^6 \cdot 2\pi}{3.9 - 1.1} = 2.2 \times 10^6 \text{ rads/V\cdot sec}
\]

The data sheet also requires calculation of two resistors, \( R_1 \) and \( R_2 \), and a capacitor, \( C_1 \).

Using the graphs from the data sheet gives,

\( R_1 = 47k\Omega, \ R_2 = 130k\Omega, \) and \( C_1 = 100\text{pF} \).

6.) Assume the loop should lock with 1ms.

\[
\therefore T_L = 1\text{ms} \quad \rightarrow \quad \omega_n = 2\pi/T_L = 6280 \text{ rads/sec}.
\]

7.) Using a passive loop filter we get,

\[
\tau_1 + \tau_2 = \frac{K_o K_d}{N \omega_n^2} = \frac{2.2 \times 10^6 \cdot 0.4}{141 \cdot 6280^2} = 161\mu\text{s}
\]

8.) \( \tau_2 = \frac{2\zeta}{\omega_n} = \frac{2 \cdot 0.7}{6280} = 223\mu\text{s} \)!!!(The problem is that \( \tau_1 + \tau_2 \) is too small)

Go back and choose \( T_L = 2\text{ms} \quad \rightarrow \quad \omega_n = 2\pi/T_L = 3140 \text{ rads/sec} \).

\[
\tau_1 + \tau_2 = \frac{K_o K_d}{N \omega_n^2} = \frac{2.2 \times 10^6 \cdot 0.4}{141 \cdot 3140^2} = 633\mu\text{s} \quad \text{and} \quad \tau_2 = \frac{2\zeta}{\omega_n} = \frac{2 \cdot 0.7}{3140} = 446\mu\text{s} \quad \rightarrow \quad \tau_1 = 187\mu\text{s}
\]
Design Problem – Continued
9.) Design the loop filter.

For optimum sideband suppression, $C$ should be large. Choose $C = 0.33\mu F$.

\[
R_1 = \frac{\tau_1}{C} = \frac{187 \times 10^{-6}}{0.33 \times 10^{-6}} = 567\Omega \quad \text{and} \quad R_2 = \frac{\tau_2}{C} = \frac{446 \times 10^{-6}}{0.33 \times 10^{-6}} = 1.351\Omega
\]

The data sheet requires that $R_1 + R_2 \geq 470\Omega$ which is satisfied.

Block diagram of the DPLL frequency synthesizer design of this example:
Simulation of the DPLL Example
The block diagram of this example is shown below.

![Block Diagram](image)

The PFD-charge pump combination can be approximated as†

\[ "K_dF(s)" = \frac{K_d(1+s\tau_2)}{s(\tau_1+\tau_2)} \]

Therefore, the loop gain becomes

\[ LG(s) = \frac{K_oK_d(1+s\tau_2)}{s^2(\tau_1+\tau_2)} = \frac{K_v(1+s\tau_2)}{(s+\varepsilon)^2(\tau_1+\tau_2)} \]

(the factor \( \varepsilon \) is used for simulation purposes)

For this problem,

\( K_d = 0.4\text{V/rad.}, K_o = 2.2 \times 10^6, \tau_2 = 446\mu\text{s}, \text{and} \ \tau_2+\tau_2 = 633\mu\text{s}. \) Also choose \( \varepsilon = 0.01. \)

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CMOS Phase Locked Loops

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Simulation of the DPLL Example – Continued

PSPICE Input File

DPLL Design Problem–Open Loop Response – Best
VS 1 0 AC 1.0
R1 1 0 10K
* Loop bandwidth = Kv =8.8x10E5 sec.-1  Tau1=187E-6  Tau2=446E-6 N=141
ELPLL 2 0 LAPLACE {V(1)}= {8.8E+6/(S+0.01)/141*(0.446E-3*S+1)/(S+0.01)/0.633E-3}
R2 2 0 10K
*Steady state AC analysis
.AC DEC 20 10 100K
.PRINT AC VDB(2) VP(2)
.PROBE
.END

Simulation Results:

Note that the phase is very close to 0° and |LG|>>1 at low frequencies which is typical of type II systems.
DPLL SYSTEM SIMULATION

Examples of Case Studies using the Best Software†

PLL Parameters-

Supply voltages:
- Positive supply = 5V
- Negative supply = -5V

Phase detector:
- \( V_{sat^+} = 4.5V \)
- \( V_{sat^-} = 0.5V \)

Loop filter:
- \( \tau_1 = 500\mu s \)
- \( \tau_2 = 50\mu s \)

Oscillator:
- \( K_o = 130,000 \text{ rads/V·sec} \)
- \( V_{sat^+} = 4.5V \)
- \( V_{sat^-} = 0.5V \)

The simulation program will be used to verify the following calculated values:
- \( \omega_n = 17,347 \text{ rads/sec.} \) (calculated prior to simulation)
- \( \zeta = 0.486 \) (calculated prior to simulation)
- \( \Delta f_{po} = 7719 \text{ Hz} \)
- \( \Delta f_p = 13,192 \text{ Hz} \)

Case 1 – System Benchmark

\[ v_d (\text{mV}) \]

\[ v_f \]

Diagram showing waveforms for \( v_d \) and \( v_f \) with respect to time \( t \).
**Case 2 - \(\Delta f = 8000\text{Hz}\)**

![Graph showing \(v_d(V)\) and \(v_f\) with phase error \(\geq 90^\circ\)]
Case 3 – Loop Just Locks Out

\[ v_d \] (V)

\[ v_f \]

\[ v_d \]

\[ 100 \quad 200 \quad 300 \quad 400 \quad 500 \quad 600 \quad 700 \]

\[ t [\text{us}] \]

\[ \text{Loop pulls out} \]
Case 4 – Pull-In Range Verification

Loop will not pull back in for $df > 14,200$ Hz
Case 5 – PFD and Illustration of a Virtually Infinite Pull-In Range

\[ \Delta f_p = \pm 40\text{kHz} \quad \Delta f = 35 \text{ kHz} \] to avoid clipping of \( v_f \).

\[ v_d(V) \]

\[ T_p \approx 1.5\text{ms} \]
Case 6 – EXOR with Active PI Filter

\[ v_d(V) \]

\[ v_f \]

\[ t \text{ [ms]} \]

DPLL Simulation:
Tue Dec 24 13:14:10 2002
PD = EXOR
LP = active PI
OSC = VCO
Center frequency = 100000 Hz
Power-on start: 0900 MHz

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SUMMARY

• Illustrated the Noise Performance of the DPLL
• Presented a DPLL Design Procedure
• Showed how to do DPLL System Simulation
• The DPLL is much more compatible with IC technology and is the primary form of PLL used for frequency synthesizers