LECTURE 5 –DIGITAL PHASE LOCK LOOPS (DPLLs)

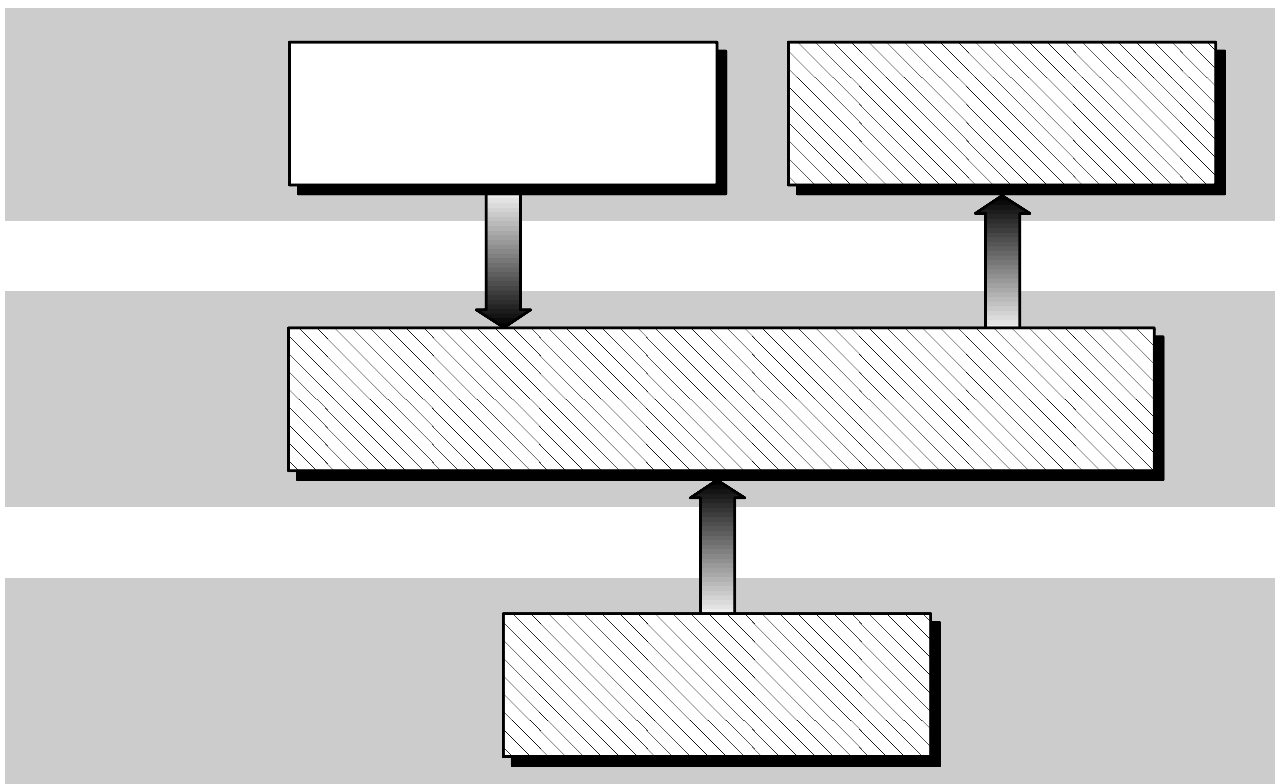
INTRODUCTION

Topics

• Building Blocks of the DPLL

• Dynamic Performance of the DPLL

Organization:



BUILDING BLOCKS OF THE DPLL

Block Diagram of the DPLL

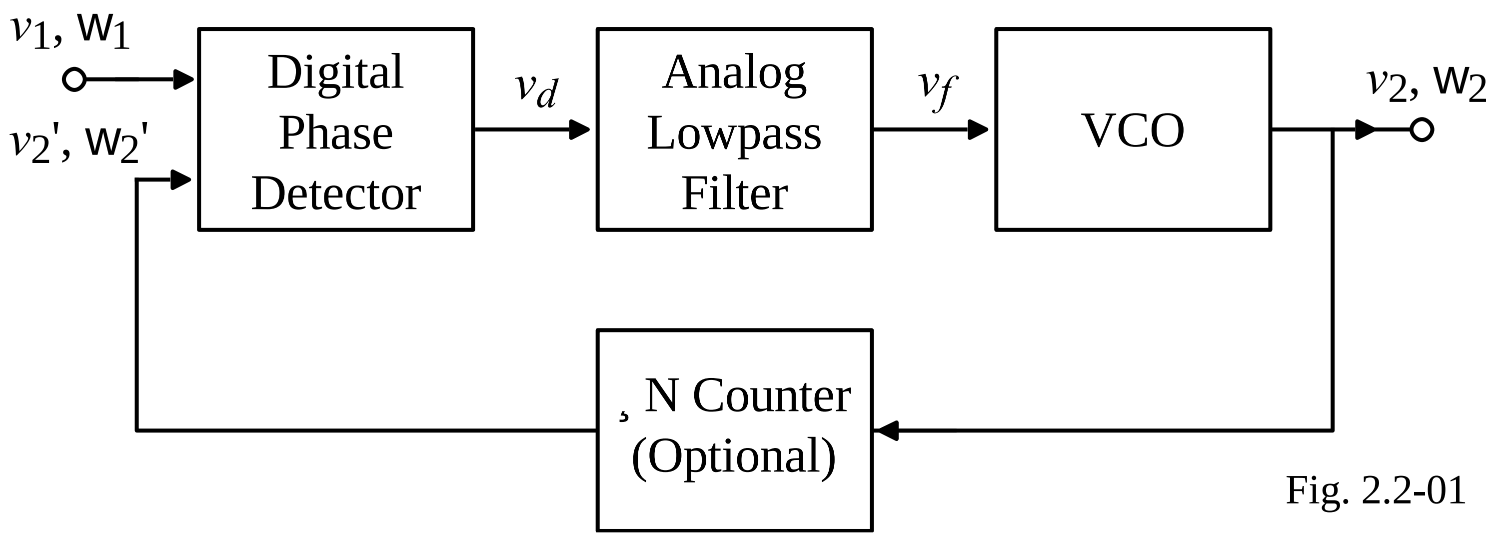


Fig. 2.2-01

- The only digital block is the phase detector and the remaining blocks are similar to the LPLL
- The divide by N counter is used in frequency synthesizer applications.

$$\omega_2' = \omega_1 = \frac{\omega_2}{N} \quad \rightarrow \quad \omega_2 = N\,\omega_1$$

DIGITAL PHASE DETECTORS

Introduction

Key assumption in digital phase detectors: $v_1(t)$ and $v_2(t)$ are square waves. This may require amplification and limiting.

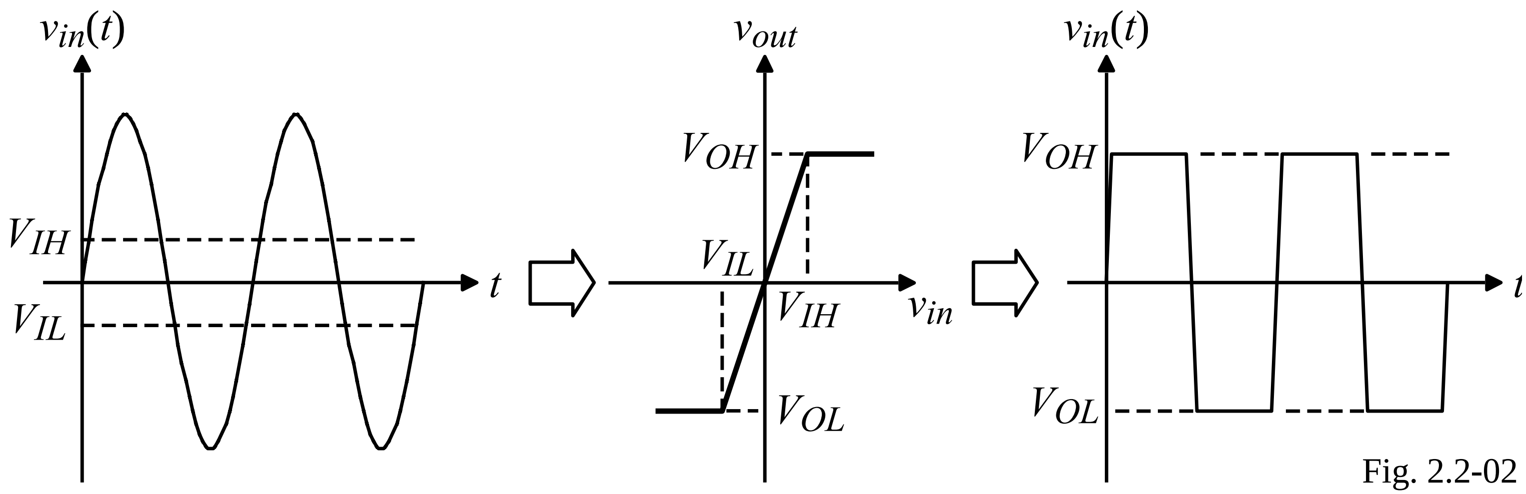


Fig. 2.2-02

Types of digital phase detectors:

1.) EXOR gate
2.) The edge-triggered JK flip-flop
3.) The phase-frequency detector

The EXOR Gate

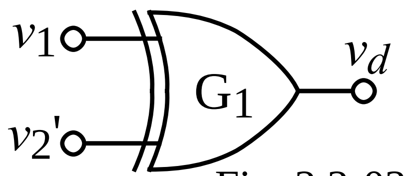


Fig. 2.2-03

v_1	v_2’	v_d
0	0	0
0	1	1
1	0	1
1	1	0

Zero Phase Error:

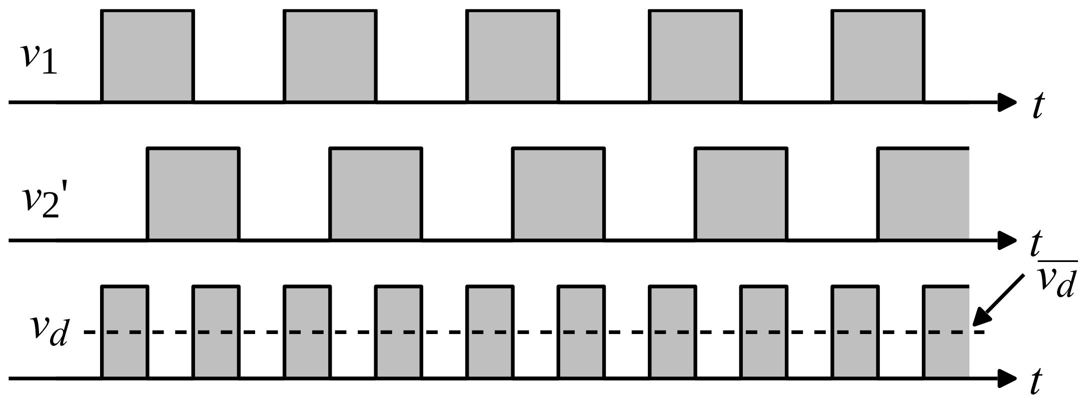


Fig. 2.2-04

Positive Phase Error:

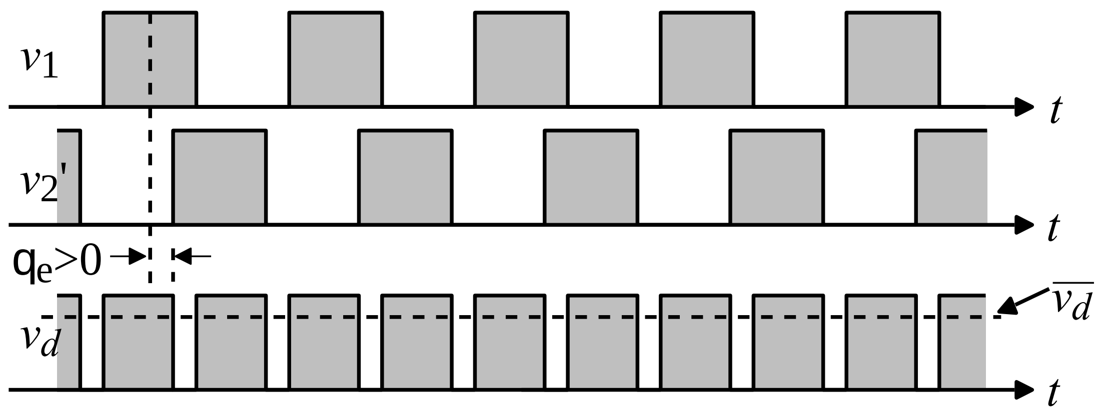
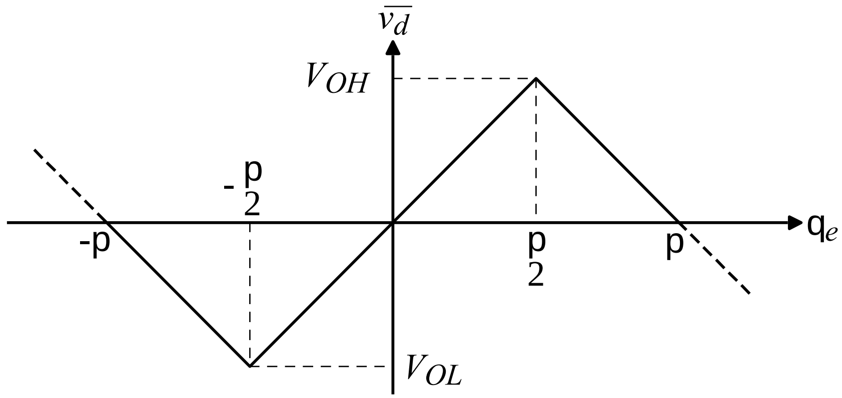


Fig. 2.2-05

EXOR Gate – Continued

Assume that the average value of v_d, is shifted to zero for zero phase error, θ_e. $\overline{v_d}$ can be plotted as,



$$K_d = \frac{V_{OH}-V_{OL}}{\pi}$$

Fig. 2.2-06

If v_1 and v_2' are asymmetrical (have different duty cycles), then $\overline{v_d}$ becomes,

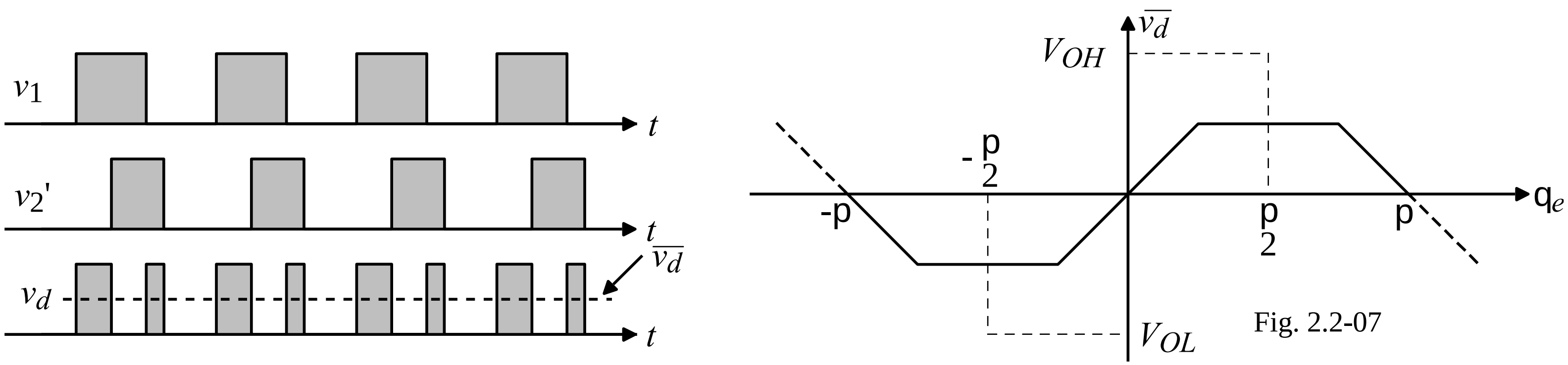


Fig. 2.2-07

The effect of waveform asymmetry is to reduce the loop gain of the DPLL and also results in a smaller lock range, pull-in range, etc.

JK Flip-Flop

The JK Flip-Flop is not sensitive to waveform asymmetry because it is edge-triggered.

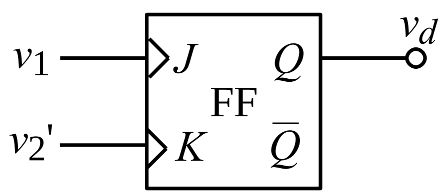


Fig. 2.2-08

v_1	v_2'	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$

Zero Phase Error (Assume rising edge triggered):

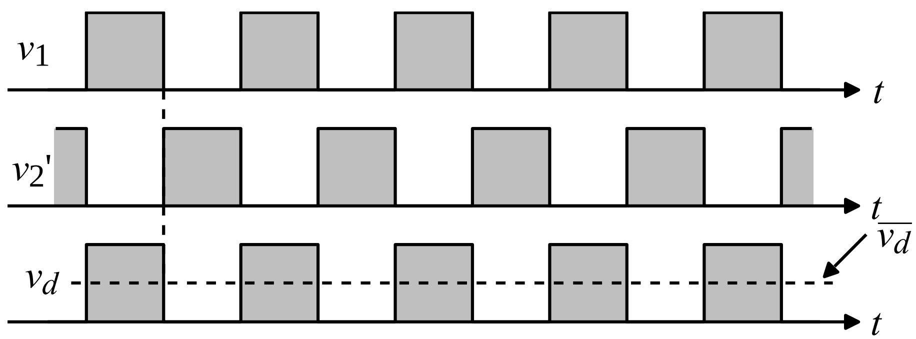


Fig. 2.2-09

Positive Phase Error:

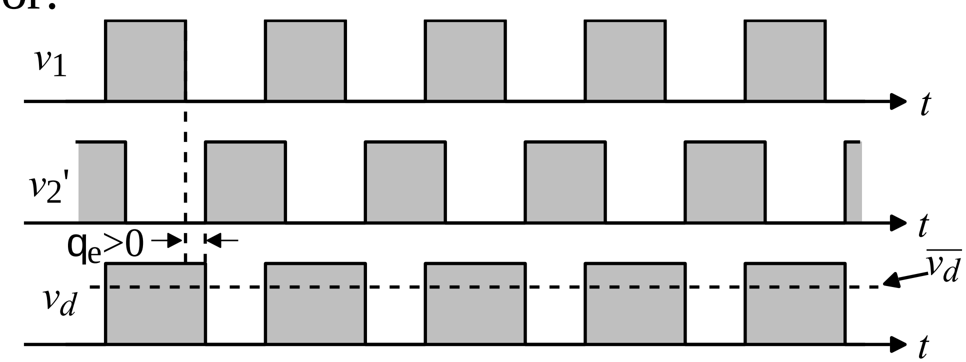
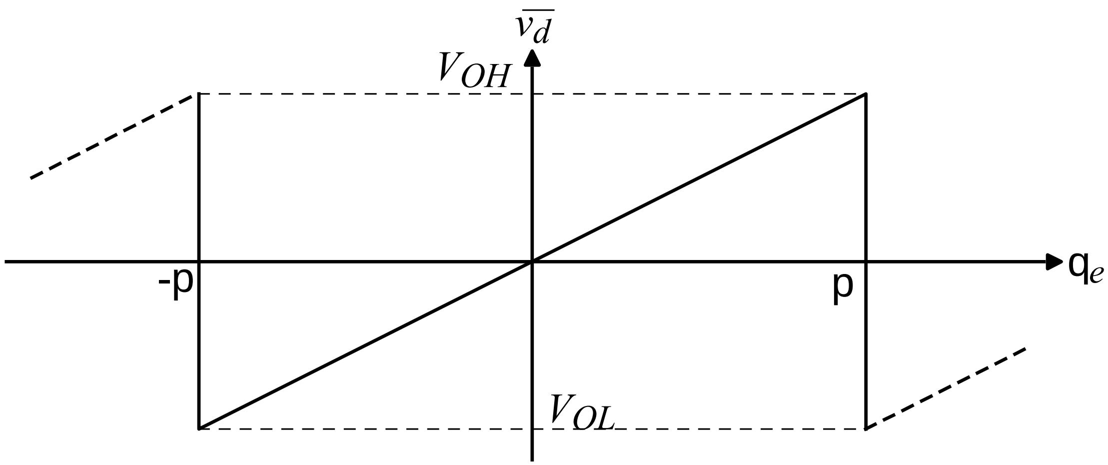


Fig. 2.2-10

JK Flip-Flop Phase Detector – Continued

Input-Output Characteristic:



$$K_d = \frac{V_{OH}-V_{OL}}{2p}$$

Fig. 2.2-11

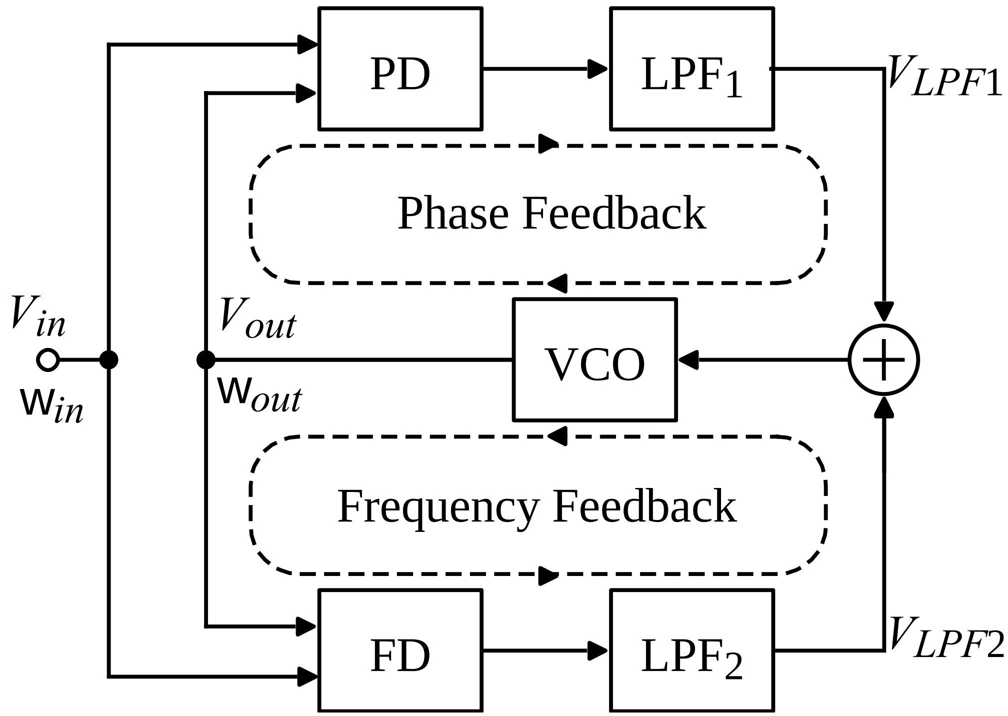
Comments:

- Symmetry of v_1 and v_2’ is unimportant
- Both the EXOR and the JK flip-flop have a severely limited pull-in range if the loop filter does not have a pole at zero.

The Phase-Frequency Detector (PFD)

The PFD can detect both the phase and frequency difference between v_1 and v_2'.

Conceptual diagram:



The output signal of the PFD depends on the phase error in the locked state and on the frequency error in the unlocked state.

Consequently, the PFD will lock under any condition, irrespective of the type of loop filter used.

The PFD – Continued

PFD implementation:

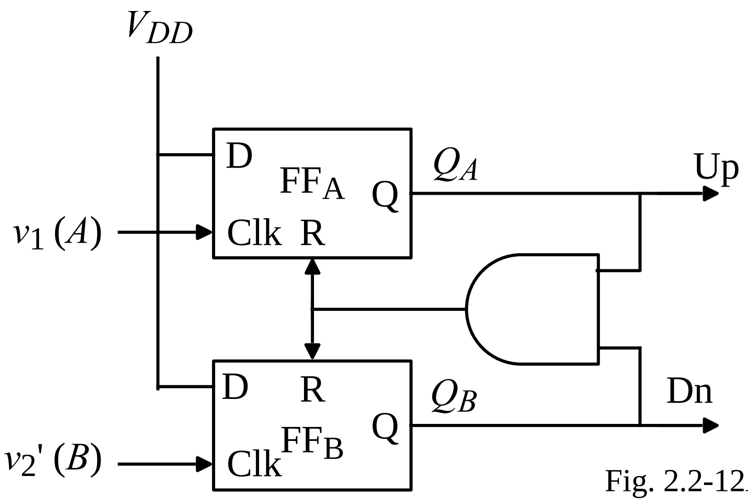


Fig. 2.2-12A

PFD

No AND Gate	
Q_A	Q_B
0	0
1	0
0	1
1	1

With AND Gate	
Q_A	Q_B
1	0→State=+1
0	0→State = 0
0	1→State=-1

State Diagram:

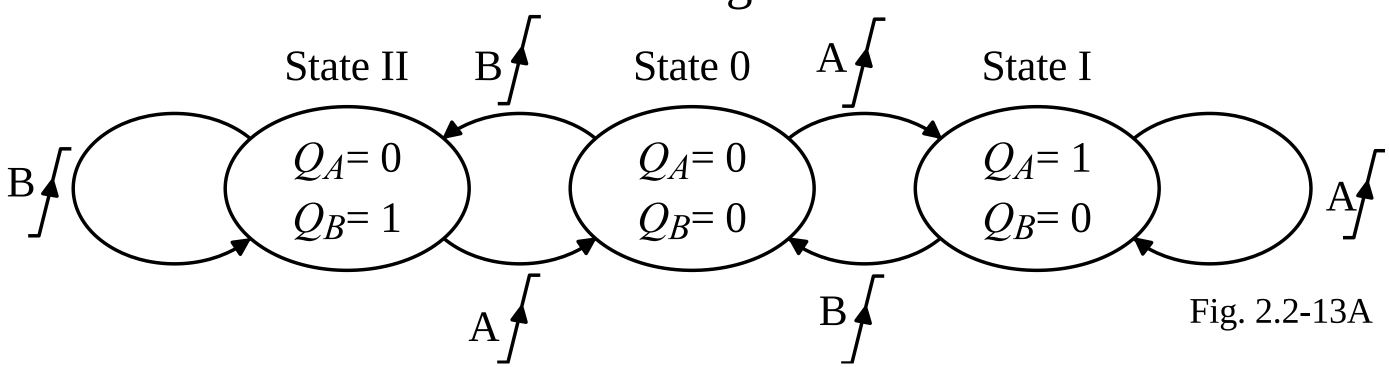


Fig. 2.2-13A

Unlike the EXOR gates and the R-S latches, the PFD generates two outputs which are not complementary.

Illustration of a PFD

PFD ($\omega_A = \omega_B$):

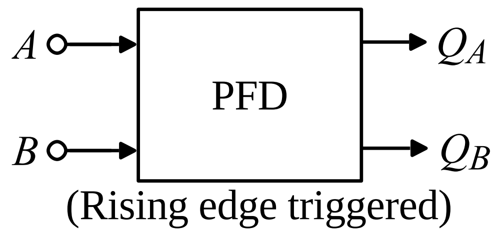


Fig. 2.2-14

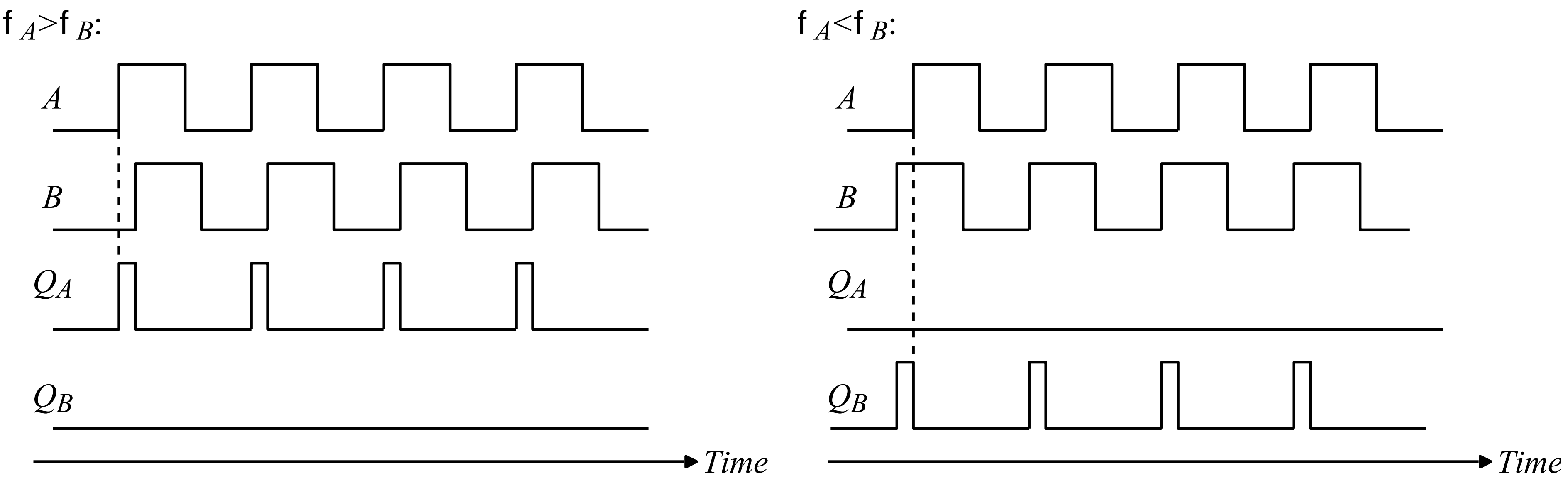


Fig. 2.2-15

Illustration of the PFD- Continued

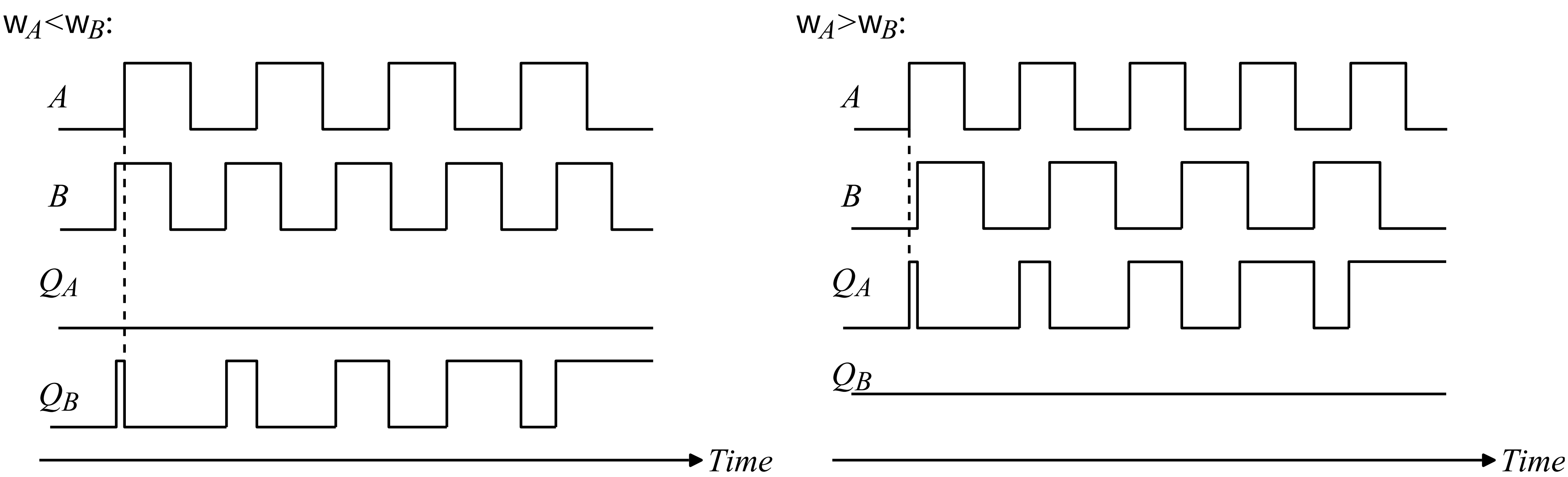


Fig. 2.2-16

PFD – Continued

Plot of the PFD output versus phase error:

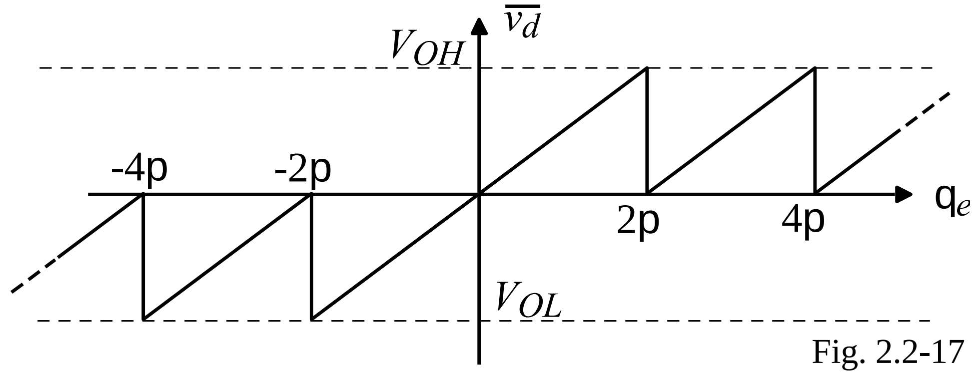


Fig. 2.2-17

When θ_e exceeds $\pm 2\pi$, the PFD behaves as if the phase error recycled at zero.

$$\therefore \quad K_d = \frac{V_{OH}\text{-}V_{OL}}{4\pi}$$

A plot of the averaged duty cycle of v_d versus ω_1/ω_2' (ω_A/ω_B) in the unlocked state of the DPLL:

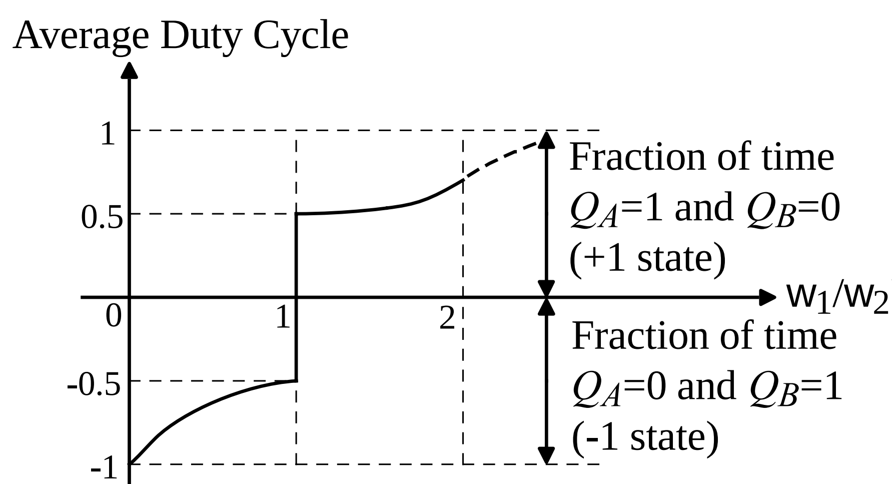
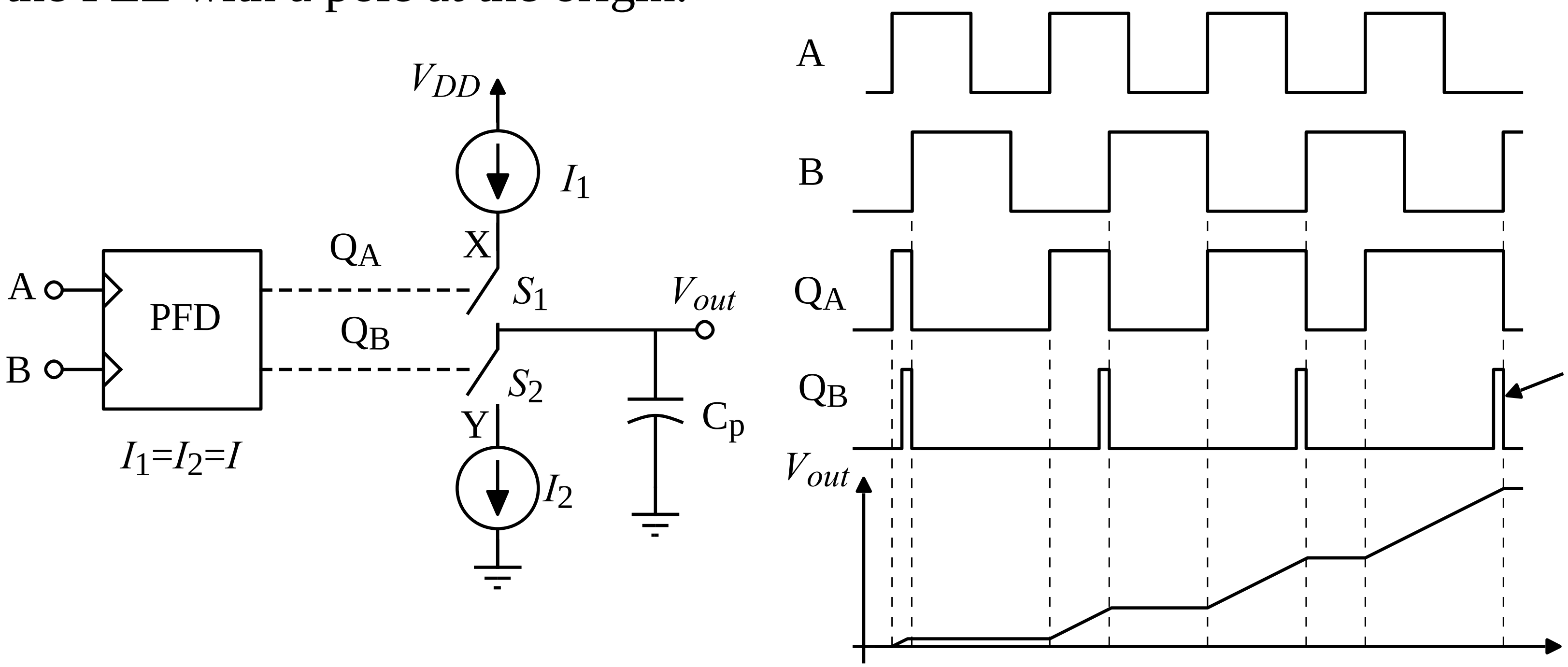


Fig. 2.2-18

CHARGE PUMPS

What is a Charge Pump?

A charge pump consists of two switched current sources controlled by Q_A and Q_B which drive a capacitor or a combination of a resistor and a capacitor to form a filter for the PLL with a pole at the origin.



Q_A and Q_B are simultaneously high for the duration given by the delay of the AND gate and the reset path of the flip-flops.

Fig. 2.2-19

$\omega_A > \omega_B$ or $\omega_A = \omega_B$ but $\theta_A > \theta_B$: S_1 is on and V_{out} increases.

$\omega_A < \omega_B$ or $\omega_A = \omega_B$ but $\theta_A < \theta_B$: S_2 is on and V_{out} decreases.

A Charge-Pump PLL

Block diagram:

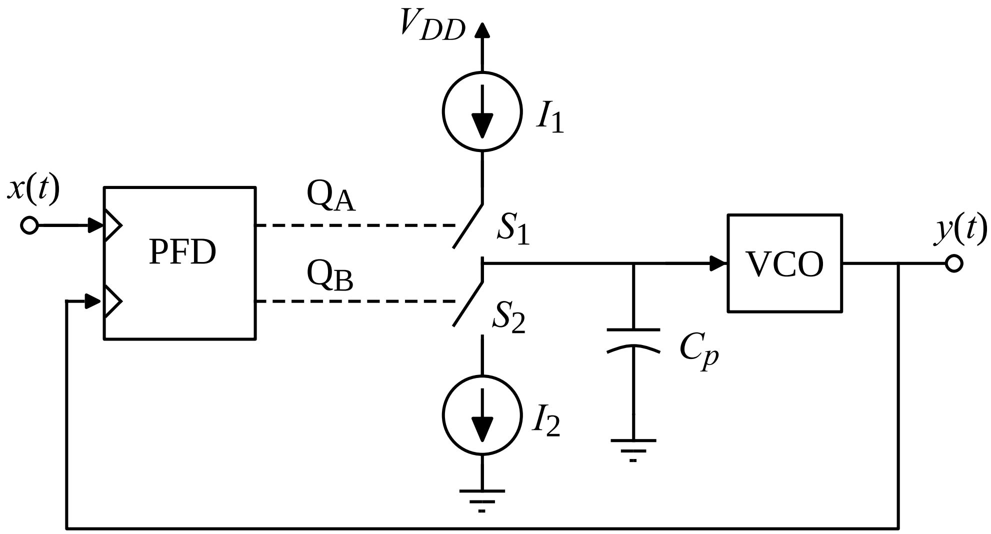


Fig. 2.2-20

The charge pump and capacitor C_p serve as the loop filter for the PLL.

The charge pump can provide infinite gain for a static phase shift.

Step Response of a Charge Pump PLL

Assume that the period of the input is T_1 and the charge pump provides a current of $\pm I_p$ to the capacitor C_p.

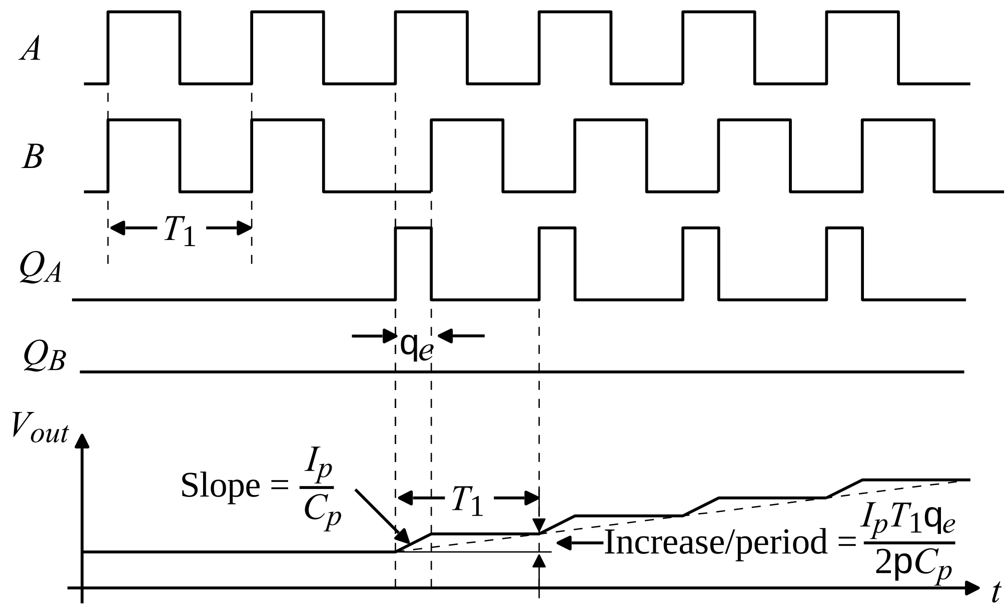


Fig. 2.2-195

Detector gain?

Since the steady-state gain = ∞, it is more meaningful to define K_d as follows,

Amount of $v_d(t)$ increase per period $(T_1) = \frac{I_p}{C_p} \text{ x } \frac{\theta_e}{2\pi/T_1} = \frac{I_p T_1 \theta_e}{2\pi C_p}$

Average slope per period $= \frac{I_p T_1 \theta_e}{2\pi C_p} \text{ x } \frac{1}{T_1} = \frac{I_p \theta_e}{2\pi C_p}$

$$v_d(t) = \text{Average Slope}\cdot \Delta\theta = \frac{I_p}{2\pi C_p} \cdot \theta_e \mu(t)$$

Taking the Laplace transform gives, $V_d(s) = \frac{I_p}{2\pi C_p}\frac{\theta_e}{s} \rightarrow K_d = \frac{I_p}{2\pi C_p}\frac{\text{V}}{\text{rads}}$

A Charge-Pump PLL – Continued

$$\frac{Y(s)}{X(s)} = \frac{V_2(s)}{V_1(s)} = ?$$

$$Y(s) = \frac{K_o}{s} V_d(s) = \frac{K_oK_d}{s^2}[X(s) - Y(s)] \quad \rightarrow \quad \frac{Y(s)}{X(s)} = \frac{K_oK_d}{s^2 + K_oK_d}$$

which has poles at $\pm j\sqrt{K_oK_d}$. To avoid instability, a zero must be introduced by the resistor in series with C_p.

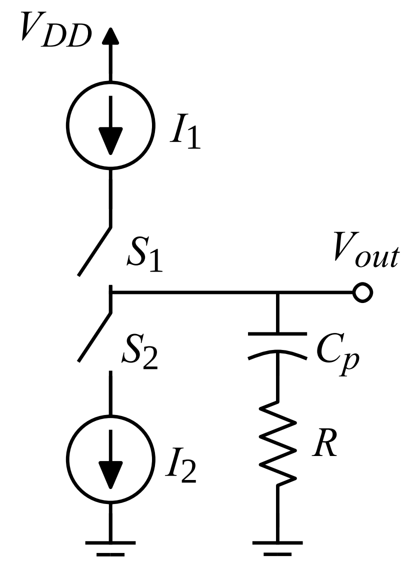


Fig. 2.2-21

$$V_d(s) = \frac{I}{2\pi}\left(R + \frac{1}{sC_p}\right) = \frac{I}{s2\pi C_p}(sRC_p + 1) = \frac{K_d}{s}(s\tau_p + 1)$$

$$\therefore \quad Y(s) = \frac{K_o}{s} V_d(s) = \frac{K_oK_d}{s^2}(s\tau_p + 1)[X(s) - Y(s)]$$

$$Y(s)\left[1 + \frac{K_oK_d}{s^2}(s\tau_p + 1)\right] = \frac{K_oK_d}{s^2}(s\tau_p + 1)X(s)$$

$$\frac{Y(s)}{X(s)} = \frac{K_oK_d(s\tau_p + 1)}{s^2 + K_oK_d\tau_p s + K_oK_d}$$

Equating to the standard second-order denominator gives,

$$\omega_n = \sqrt{K_oK_d} \text{ and } \zeta = \frac{\omega_n \tau_p}{2}$$

Nonideal Effects of Charge-Pumps

1.) Dead zone.

A dead zone occurs when Q_A or Q_B do not reach their full logic levels. This is due to delay differences in the AND gate and the flip-flops. It is removed by proper synchronization of the delays.

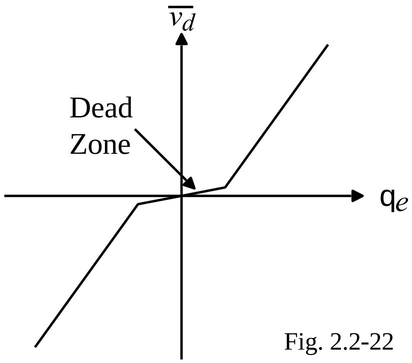


Fig. 2.2-22

2.) Mismatch between I_1 and I_2.

To eliminate the dead zone, Q_A and Q_B can be simultaneously high for a small time. If $I_1 \neq I_2$, the output varies even though $\theta_e = 0$. (Can introduce spurs.)

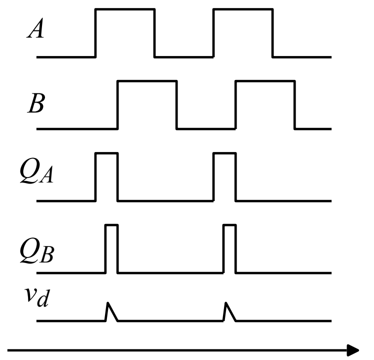


Fig. 2.2-23

3.) Charge injection.

When the S_1 and S_2 switches turn off, they can inject/remove charge from C_p. Changes ω_2.

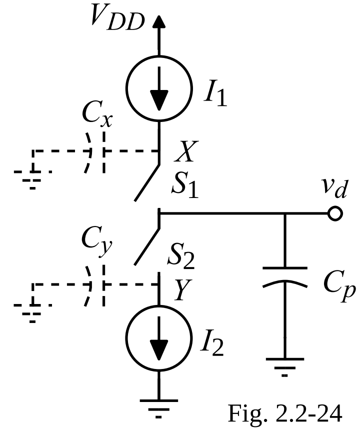


Fig. 2.2-24

4.) Charge sharing.

If $X \rightarrow V_{DD}$ and $Y = 0$ when S_1 and S_2 are off, the VCO will experience a jump when S_1 or S_2 turns on. This periodic effect introduces sidebands (spurs) at the output.

DYNAMIC PERFORMANCE OF THE DPLL

Types of PLLs

Type I – Open-loop transfer function has one pole at the origin.

Type II – Open-loop transfer function has two poles at the origin.

The above transfer functions may also have other roots but not at the origin.

Model for the DPLL

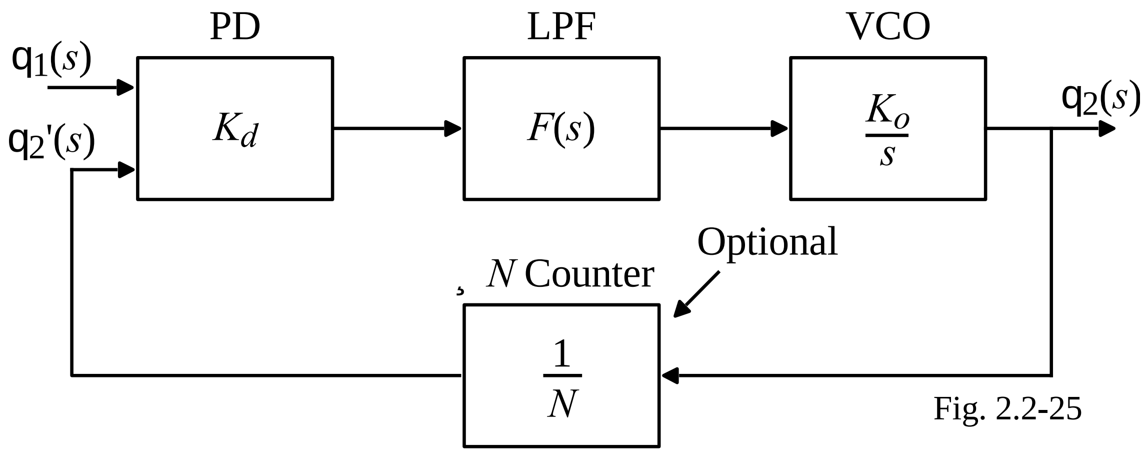


Fig. 2.2-25

Various configurations of the DPLL:

1.) Phase detector – EXOR, J-K flip-flop, or PFD

2.) Filter –

Passive lag with or without a charge pump
Active lag with or without a charge pump
Active PI with or without a charge pump

Loop Filters

1.) Passive lag-

PD $\rightarrow$ $$F(s) = \frac{1 + s\tau_2}{1 + s(\tau_1 + \tau_2)}$$

PFD $\rightarrow$ $$F(s) \approx \frac{1 + s\tau_2}{s(\tau_1 + \tau_2)}$$

Experimental results using the PFD with a passive lag filter show that the gain of the passive filter is not constant. As a result, the filter dynamics become nonlinear.

2.) Active lag-

PD $\rightarrow$ $$F(s) = K_a \frac{1 + s\tau_2}{1 + s\tau_1}$$

PFD $\rightarrow$ $$F(s) \approx \frac{1 + s\tau_2}{s\tau_1}$$

3.) Active PI-

PD or PFD $\rightarrow$ $$F(s) = \frac{1 + s\tau_2}{s\tau_1}$$

The Hold Range, $\Delta\omega_H$

The hold range, $\Delta\omega_H$, is the frequency range within which the PLL operation is statically stable. The hold range for various types of DPLLs are:

Type of PD	EXOR	EXOR	EXOR	JK-FF	JK-FF	JK-FF	PFD
Loop Filter	Passive Lag	Active Lag	Active PI	Passive Lag	Active Lag	Active PI	All Filters
$\Delta\omega_H$	$\frac{K_oK_d(\pi/2)}{N}$	$\frac{K_oK_d(\pi/2)}{N}$	∞	$\frac{K_oK_d\pi}{N}$	$\frac{K_oK_dK_a\pi}{N}$	∞	∞

Some Considerations of Importance

As we examine the lock range of the DPLL using EXOR, JK-FF, and PFD detectors, the following comparison will be useful.

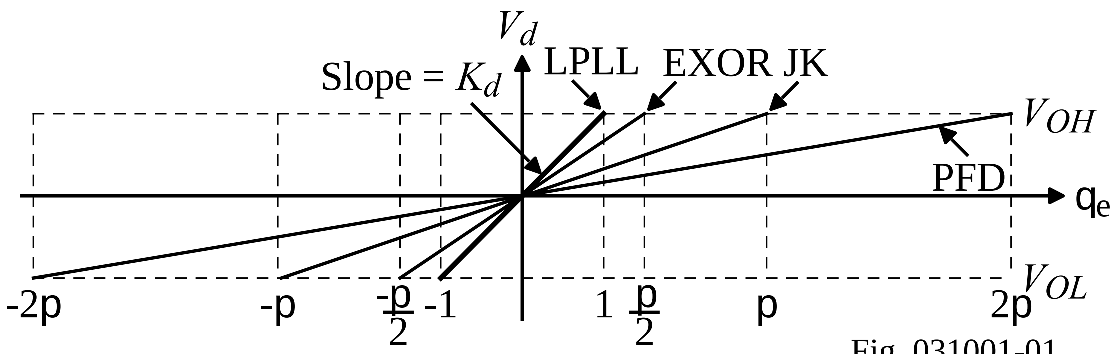


Fig. 031001-01

The Lock Range, $\Delta\omega_L$

The lock range is the offset between ω_1 and ω_2/N that causes the DPLL to acquire lock with one beat note between ω_1 and $\omega_2' = \omega_2/N$.

1.) PD = EXOR

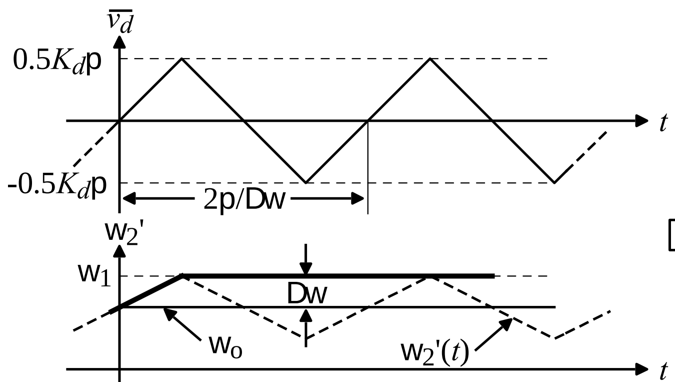


Fig. 2.2-26

Recall that $\Delta\omega_L(\text{LPLL}) = 2\zeta\omega_n$

and $\Delta\omega_L \propto$ Range of $\theta_e = \Delta\theta_e$

But, $\Delta\theta_e(\text{EXOR}) = 0.5\pi\,\Delta\theta_e(\text{LPLL})$

$\Rightarrow \therefore\ \Delta\omega_L = 0.5\pi(2\zeta\omega_n) = \pi\zeta\omega_n$

$$\boxed{\Delta\omega_L = \pi\zeta\omega_n}$$

2.) PD =JK-Flip flop

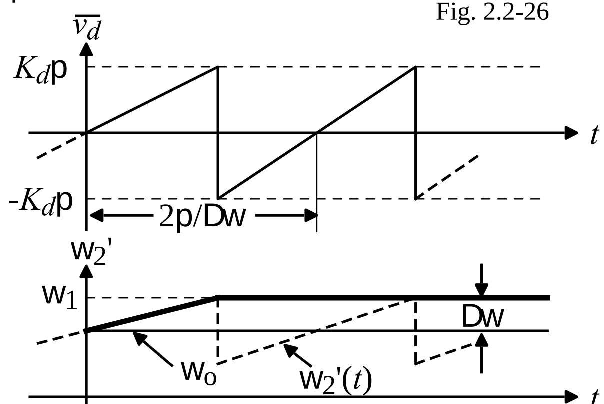


Fig. 2.2-27

$\Delta\theta_e(\text{EXOR}) = \pi\,\Delta\theta_e(\text{LPLL})$

$\Rightarrow \therefore\ \Delta\omega_L = \pi(2\zeta\omega_n)$

$$\boxed{\Delta\omega_L = 2\pi\zeta\omega_n}$$

3.) PD = PFD

$\Delta\theta_e(\text{PFD}) = 2\pi\,\Delta\theta_e(\text{LPLL}) \quad \rightarrow \quad \Delta\omega_L = 2\pi(2\zeta\omega_n) \rightarrow \boxed{\Delta\omega_L = 4\pi\zeta\omega_n}$

The lock time for all cases is $T_p \approx 2\pi/\omega_n$.

The Pull-In Range, $\Delta\omega_p$, and the Pull-In Time, T_p

The pull-in range, $\Delta\omega_p$, is the largest $\Delta\omega=|\omega_1-\omega_2'|$ for which an unlocked loop will lock.

The pull-in time, T_p, is the time required for the loop to lock.

EXOR as the PD:

Waveforms-

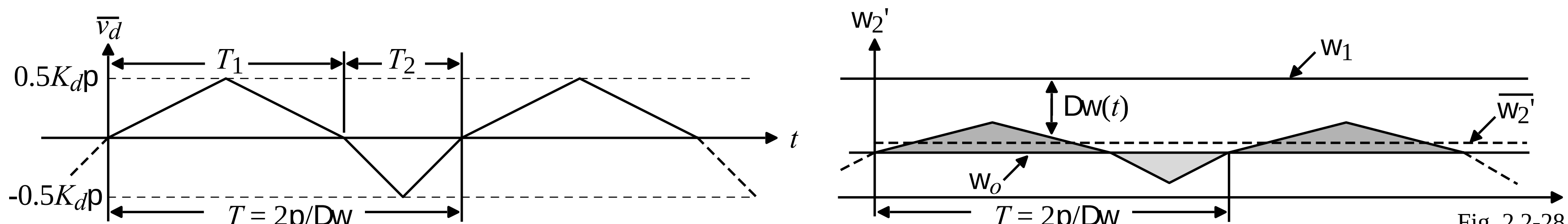


Fig. 2.2-28

$T_1 > T_2$ because $\Delta\omega$ is smaller when $\overline{v_d}$ is positive and larger when $\overline{v_d}$ is negative.

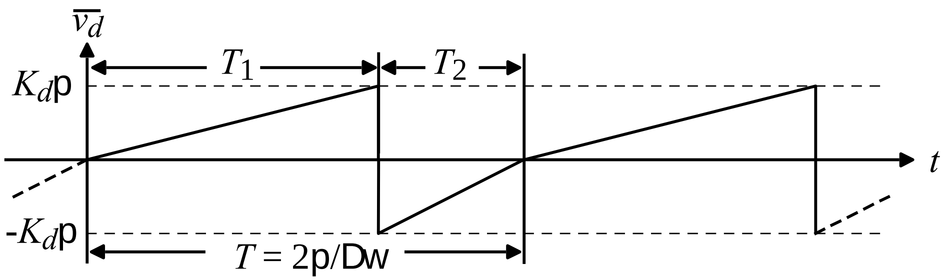
Results-

Type of Filter	$\Delta\omega_p$ (Low loop gains)	$\Delta\omega_p$ (High loop gains)	Pull-in Time, T_p
Passive Lag	$\frac{\pi}{2}\sqrt{2\zeta\omega_n K_o K_d - \omega_n^2}$	$\frac{\pi}{\sqrt{2}}\sqrt{\zeta\omega_n K_o K_d}$	$\frac{4}{\pi^2}\frac{\Delta\omega_o^2}{\zeta\omega_n^3}$
Active Lag	$\frac{\pi}{2}\sqrt{2\zeta\omega_n K_o K_d - \frac{\omega_n^2}{K_a}}$	$\frac{\pi}{\sqrt{2}}\sqrt{\zeta\omega_n K_o K_d}$	$\frac{4}{\pi^2}\frac{\Delta\omega_o^2}{\zeta\omega_n^3}$
Active PI	∞	∞	$\frac{4}{\pi^2}\frac{\Delta\omega_o^2}{\zeta\omega_n^3}$

The Pull-In Range, $\Delta\omega_p$, and the Pull-In Time, T_p-Continued

JK Flip-Flop as the PD:

Waveforms-



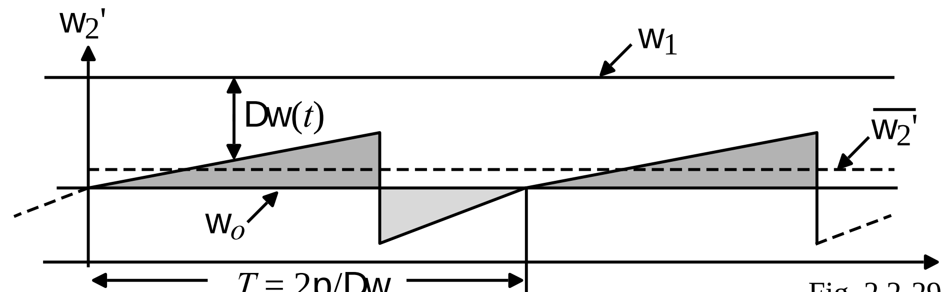


Fig. 2.2-29

$T_1 > T_2$ because $\Delta\omega$ is smaller when $\overline{v_d}$ is positive and larger when $\overline{v_d}$ is negative.

Results-

Type of Filter	$\Delta\omega_p$ (Low loop gains)	$\Delta\omega_p$ (High loop gains)	Pull-in Time, T_p
Passive Lag	$\pi\sqrt{2\zeta\omega_n K_o K_d - \omega_n^2}$	$\pi\sqrt{2}\sqrt{\zeta\omega_n K_o K_d}$	$\frac{1}{\pi^2}\frac{\Delta\omega_o^2}{\zeta\omega_n^2}$
Active Lag	$\pi\sqrt{2\zeta\omega_n K_o K_d - \frac{\omega_n^2}{K_a}}$	$\pi\sqrt{2}\sqrt{\zeta\omega_n K_o K_d}$	$\frac{1}{\pi^2}\frac{\Delta\omega_o^2}{\zeta\omega_n^2}$
Active PI	∞	∞	$\frac{4}{\pi^2}\frac{\Delta\omega_o^2}{\zeta\omega_n^2}$

$\Delta\omega_p$ and T_p for the PFD

Assume that the PFD uses a single power supply of V_{DD}. The various waveforms are,

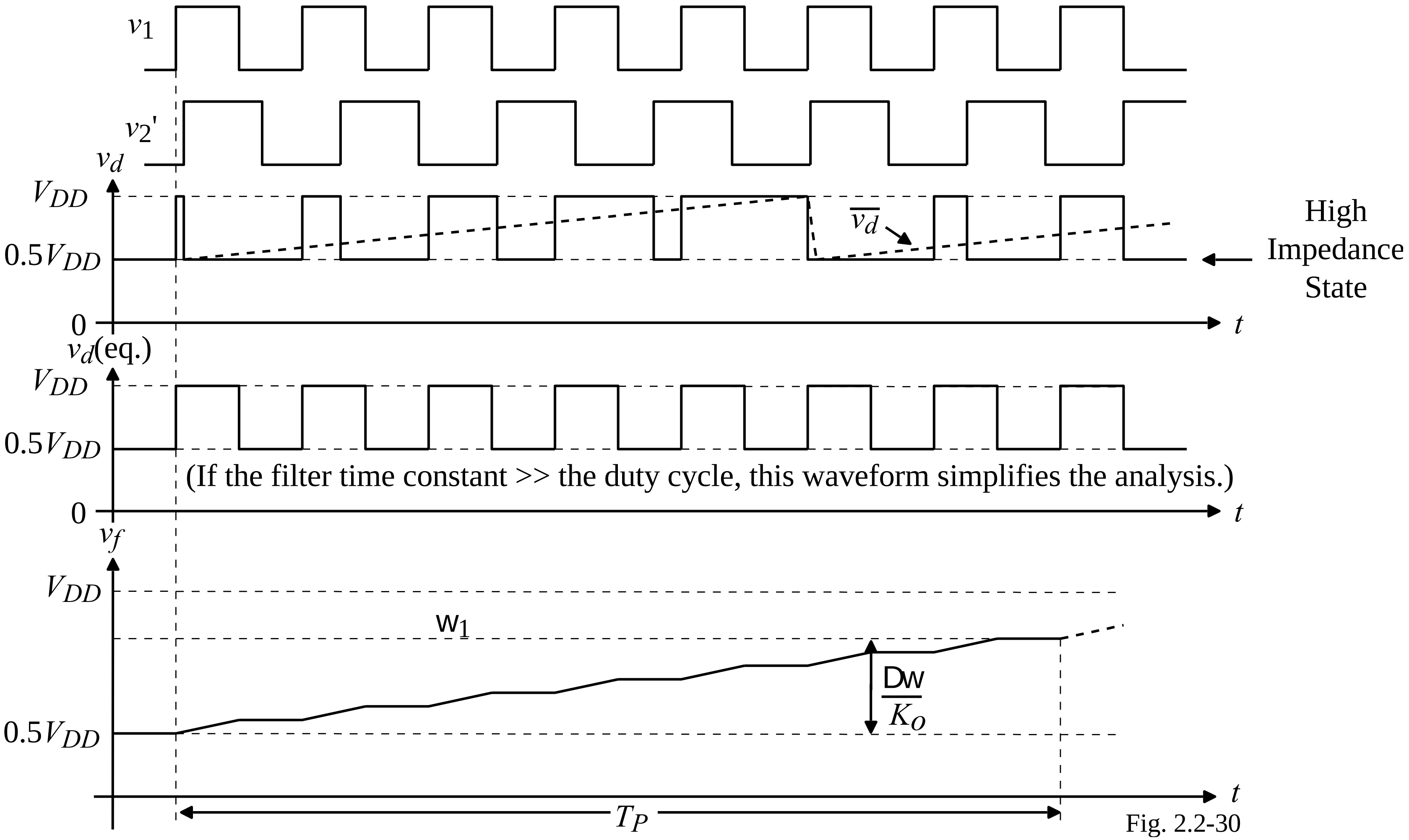
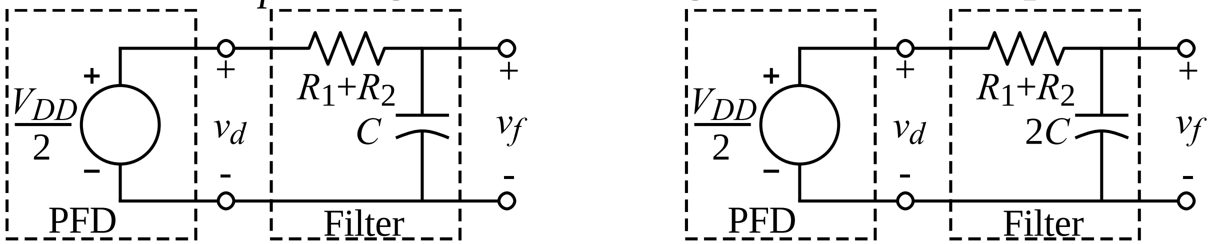


Fig. 2.2-30

v_d(eq.) is a 50% duty cycle model of the PFD to find T_p.

$\Delta\omega_p$ and T_p for the PFD – Continued

Since $\Delta\omega_p = \infty$, let us find T_p using the following model for the passive lag filter:



100% Duty Cycle 50% Duty Cycle Fig. 2.2-31

Use the 50% duty cycle model, solve for the time necessary to increase v_f by $\Delta\omega/K_o$.

1.) Loop filter = Passive lag

$$T_p = 2(\tau_1 + \tau_2)\, ln\left(\frac{K_oV_{DD}/2}{K_oV_{DD}/2 - \Delta\omega_o}\right)$$

2.) Loop filter = Active lag

$$T_p = 2\tau_1\, ln\left(\frac{K_oK_aV_{DD}/2}{K_oK_aV_{DD}/2 - \Delta\omega_o}\right)$$

3.) Loop filter = Active PI

$$T_p = \frac{2\tau_1\Delta\omega_o}{K_oV_{DD}/2}$$

For split power supplies, replace V_{DD} with $(V_{OH}\text{-}V_{OL})$.

The Pull-Out Range, $\Delta\omega_{po}$

The pull-out range is the size of the frequency step applied to the reference input that causes the PLL to lose phase tracking.

1.) EXOR: $\Delta\omega_{po} \approx 2.46\omega_n(\zeta + 0.65)$ for $0.1 < \zeta < 3$

2.) JK Flip-flop:

$$\Delta\omega_{po} = \pi\omega_n \exp\left[\frac{\zeta}{\sqrt{1-\zeta^2}} \tan^{-1}\left(\frac{\sqrt{1-\zeta^2}}{\zeta}\right)\right], \quad \zeta < 1$$

$$\Delta\omega_{po} = \pi\omega_n e, \quad \zeta = 1$$

$$\Delta\omega_{po} = \pi\omega_n \exp\left[\frac{\zeta}{\sqrt{1-\zeta^2}} \tanh^{-1}\left(\frac{\sqrt{1-\zeta^2}}{\zeta}\right)\right], \quad \zeta > 1$$

$$\Delta\omega_{po} \approx 5.78\omega_n(\zeta + 0.5) \text{ for all } \zeta$$

3.) PFD:

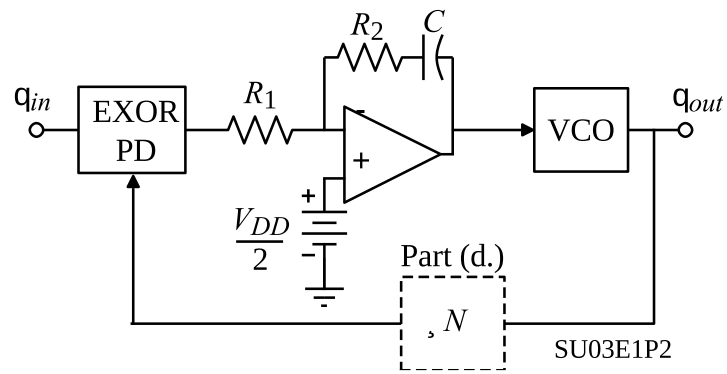
$$\Delta\omega_{po} = 2\pi\omega_n \exp\left[\frac{\zeta}{\sqrt{1-\zeta^2}} \tan^{-1}\left(\frac{\sqrt{1-\zeta^2}}{\zeta}\right)\right], \quad \zeta < 1$$

$$\Delta\omega_{po} = 2\pi\omega_n e, \quad \zeta = 1$$

$$\Delta\omega_{po} = 2\pi\omega_n \exp\left[\frac{\zeta}{\sqrt{1-\zeta^2}} \tanh^{-1}\left(\frac{\sqrt{1-\zeta^2}}{\zeta}\right)\right], \quad \zeta > 1$$

$$\Delta\omega_{po} \approx 11.55\omega_n(\zeta + 0.5) \text{ for all } \zeta$$

Example 1 – A Simple CMOS PLL



Consider the PLL shown. Assume that: 1.) the phase detector is a simple CMOS EXOR whose logic levels are ground and V_{DD} = 5V, 2.) both the input to the loop and the VCO output are square waves that swing between ground and V_{DD}, and 3.) that the VCO has a perfectly linear relationship between the control voltage and output frequency of 10 MHz/V. The polarities are such that an increase in control voltage causes an increase in the VCO frequency.

(a.) Derive the expression for the open-loop transmission and the transfer function $\theta_{out}(s)/\theta_{in}(s)$.

(b.) Initially assume R_2 = 0 and R_1 = 10kΩ. What value of C gives a loop crossover frequency of 100kHz? What is the phase margin? Assume the op amp is ideal.

(c.) With the value of C from part (b.), what value of R_2 will provide a phase margin of 45° while preserving a 100 kHz crossover frequency?

(d.) Now assume that a frequency divider of factor N is inserted into the feedback path. With the component values of part (c.), what is the largest value of N that can be tolerated without shrinking the phase margin below 14°?

Example 1 - Continued

Solution

(a.) $\theta_{out}(s) = \frac{K_o}{s} F(s)K_d\left(\theta_{in}(s) + \frac{\theta_{out}(s)}{N}\right) = \frac{5K_o}{s\pi} F(s)\left(\theta_{in}(s) + \frac{\theta_{out}(s)}{N}\right)$

$$K_d = \frac{5\text{V}}{\pi} \quad \text{and} \quad F(s) = -\frac{R_2+(1/sC)}{sR_1C} = -\frac{sR_2C+1}{sR_1C} = -\frac{s\tau_2+1}{s\tau_1}, \ \tau_1 = R_1C \ \text{ and } \ \tau_2 = R_2C$$

$$\therefore\ \theta_{out}(s) = -\frac{5K_o}{s\pi}\left(\frac{s\tau_2+1}{s\tau_1}\right)\left(\theta_{in}(s) + \frac{\theta_{out}(s)}{N}\right) \rightarrow \theta_{out}(s)\left[1 + \frac{5K_o}{s\pi N}\left(\frac{s\tau_2+1}{s\tau_1}\right)\right] = \frac{5K_o}{s\pi}\left(\frac{s\tau_2+1}{s\tau_1}\right)\theta_{in}(s)$$

$$\frac{\theta_{out}(s)}{\theta_{in}(s)} = \frac{-\frac{5K_o}{\pi\tau_1}(s\tau_2+1)}{s^2+\frac{5K_o}{\pi N}\frac{\tau_2}{\tau_1}s+\frac{5K_o}{\pi N\tau_1}}$$

$$\boxed{\frac{\theta_{out}(s)}{\theta_{in}(s)} = \frac{-\frac{5K_o}{\pi\tau_1}(s\tau_2+1)}{s^2+\frac{5K_o}{\pi N}\frac{\tau_2}{\tau_1}s+\frac{5K_o}{\pi N\tau_1}} \ \text{and the loop gain} \ = LG = -\frac{5K_o}{sN\pi}\left(\frac{s\tau_2+1}{s\tau_1}\right)}$$

Assume $N = 1$ to get the answer to part (a.).

Example 1 - Continued

(b.) With $R_2 = 0$, $\tau_2 = 0$ so that the loop gain becomes,

$$LG = -\frac{5K_o}{s^2\tau_1 N\pi} = \frac{5\cdot 2\pi x10^7}{s^2\tau_1\pi} = \frac{10^8}{\omega_c{}^2\tau_1} = 1 \quad\rightarrow\quad \tau_1 = \frac{10^8}{(2\pi\cdot 10^5)^2} = 253.3\mu\text{sec.}$$

$\tau_1 = R_1C \rightarrow$ 253.3μsec. = 10kΩC $\rightarrow$ $\underline{\underline{C = 25.3\text{nF}}}$

The phase margin is 0°.

(c.) The phase margin is totally due to τ_2. It is written as,

$$\text{PM} = tan^{-1}(\omega_c\tau_2) = 45° \quad\rightarrow\quad \omega_c\tau_2 = 1 \rightarrow \tau_2 = \frac{1}{\omega_c} = \frac{1}{2\pi x10^5} = 1.5915\mu\text{s} = R_2C$$

$$\therefore\; R_2 = \frac{1}{2\pi x10^5 25.3x10^{-9}} = \underline{\underline{62.83\Omega}}$$

(d.) N does not influence the phase shift so we can write,

$$tan^{-1}(\omega_c\tau_2) = 14° \rightarrow \omega_c{}'\tau_2 = 0.2493 \rightarrow \omega_c{}' = 0.2493\,\omega_c = 156{,}657 \text{ rads/sec.}$$

Now the loop gain at ω_c’ must be unity.

$$LG = -\frac{5K_o}{\omega_c{}'N\pi}\left(\frac{\sqrt{(\omega_c{}'\tau_2)^2+1}}{\omega_c{}'\tau_1}\right) = 1 \rightarrow N = \frac{5K_o}{(\omega_c{}')^2\pi\tau_1}\sqrt{(\omega_c{}'\tau_2)^2+1}$$

$$N = \frac{10^8}{(156.657\text{krads/sec.})^2 253.3x10^{-6}}\sqrt{(0.2493)^2+1} = 16.58 = \underline{\underline{16}}$$

SUMMARY

- The DPLL has a digital phase detector and the remainder of the blocks are analog
- Digital phase detectors
  - EXOR Gate
  - JK Flip-Flop
  - Phase-Frequency Detector
- Charge pump – a filter implementation using currents sources and a capacitor that works with the PFD
- Charge pumps implement a pole at the origin to result in zero phase error

