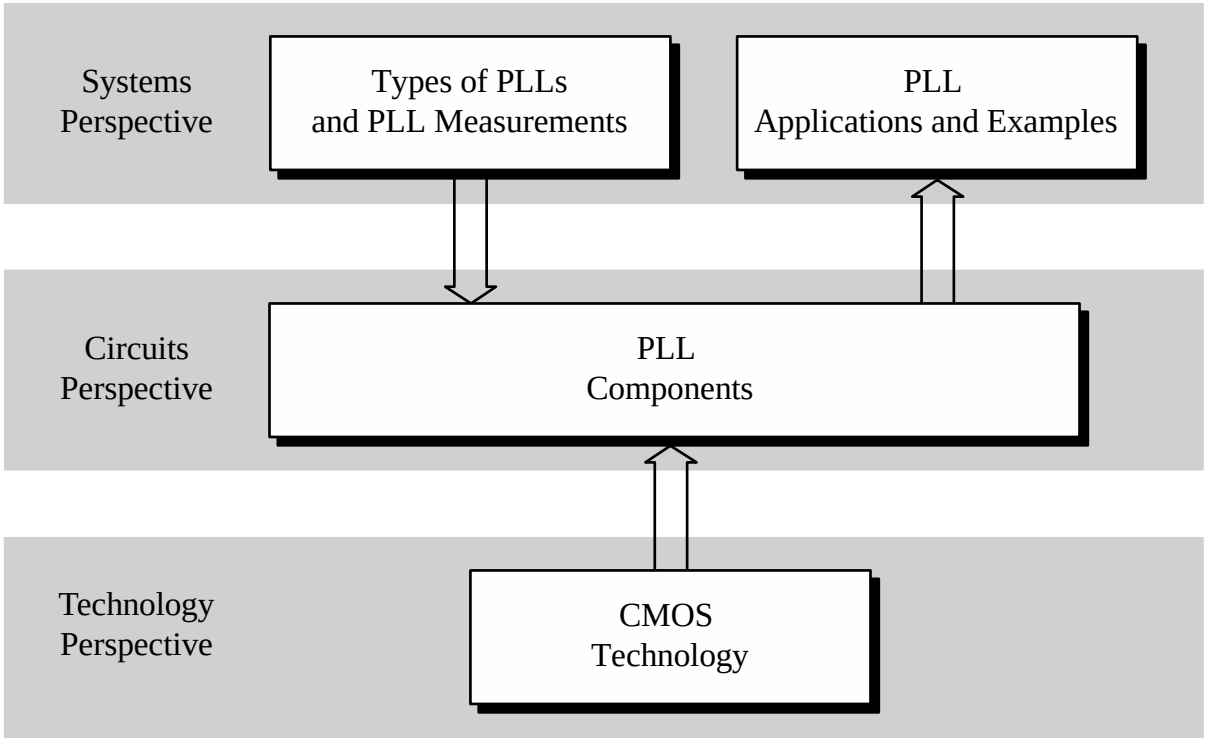
LECTURE 4 – CMOS PHASE LOCKED LOOPS

Topics

- LPLL system design – design procedure
- Simulation of LPLL systems

Organization:



LPLL SYSTEM DESIGN

Design Procedure

Objective: Design the parameters K_o, K_d, ζ, and the filter $F(s)$ of the LPLL.

Given: The phase detector and VCO and pertinent information concerning these blocks.

Steps:

1.) Specify the center frequency, ω_o, and its range $\omega_{o\min}$ and $\omega_{o\max}$.

2.) Select the value of ζ. Small values give an overshoot and large values are slow. $\zeta = 0.7$ is typically a good value to choose.

3.) Specify the lock range $\Delta\omega_L$.

a.) If noise can be neglected, then the selected value of $\Delta\omega_L$ is chosen.

b.) If noise cannot be neglected, then use the input noise SNR, $(SNR)_i$ and the input noise bandwidth, B_i, to find the noise bandwidth, B_L. Later when we find ω_n, the value of $\Delta\omega_L$ will be specified.

4.) Specify the frequency range of the LPLL as $\omega_{2\min}$ and $\omega_{2\max}$ as,

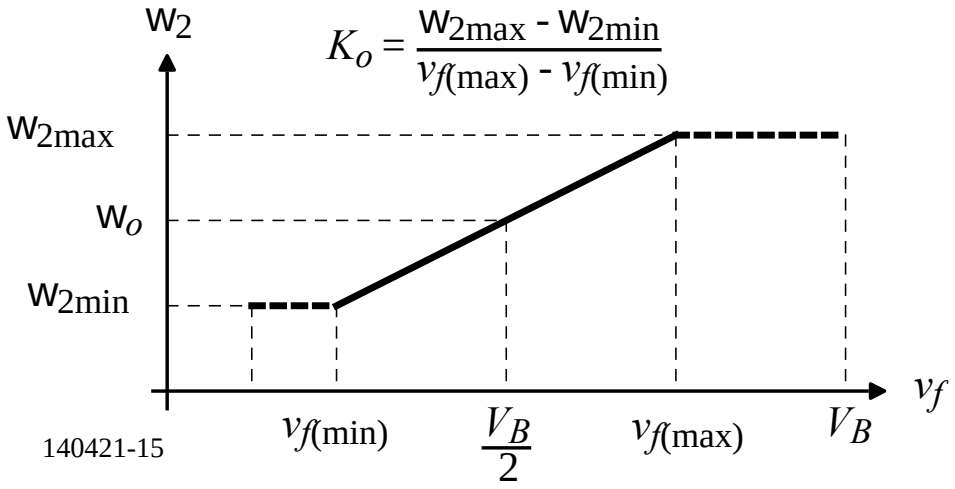
$\omega_{2\min} < \omega_{o\min} - \Delta\omega_L$ and $\omega_{2\max} > \omega_{o\max} + \Delta\omega_L$

Some practical limits are,

$\omega_{2\min} = \omega_{o\min} - 1.5\Delta\omega_L$ and $\omega_{2\max} = \omega_{o\max} + 1.5\Delta\omega_L$

Design Procedure – Continued

5.) Design of the VCO. From the power supply voltage or data sheet find the value of K_o as shown below.



6.) Determine the value of K_d from the data sheet. K_d will depend upon the signal level. It is preferred to have a large value of K_d.

7.) Determine the natural frequency, ω_n.

a.) Lock range has been specified in step 3.).

$$\omega_n = \frac{\Delta\omega_L}{2\zeta}$$

b.) Noise bandwidth has been specified in step 3.)

$$\omega_n = \frac{2B_L}{\zeta + 0.25\zeta}$$

Design Procedure – Continued

8.) Select the type of loop filter.

a.) Passive lag filter:

Solve for τ_1 and τ_2 from the following equations. Normally, τ_1 should be 5-10 times τ_2. If this is not the case, choose another type of filter.

$$\omega_n = \sqrt{\frac{K_o K_d}{\tau_1 + \tau_2}} \qquad \text{and} \qquad \zeta = \frac{\omega_n}{2}\left(\tau_2 + \frac{1}{K_o K_d}\right)$$

b.) Active lag filter:

Use the following equations to solve for τ_1, τ_2, and K_a. It will be necessary to choose one of these parameters because there are only two equations.

$$\omega_n = \sqrt{\frac{K_o K_d K_a}{\tau_1}} \qquad \text{and} \qquad \zeta = \frac{\omega_n}{2}\left(\tau_2 + \frac{1}{K_o K_d K_a}\right)$$

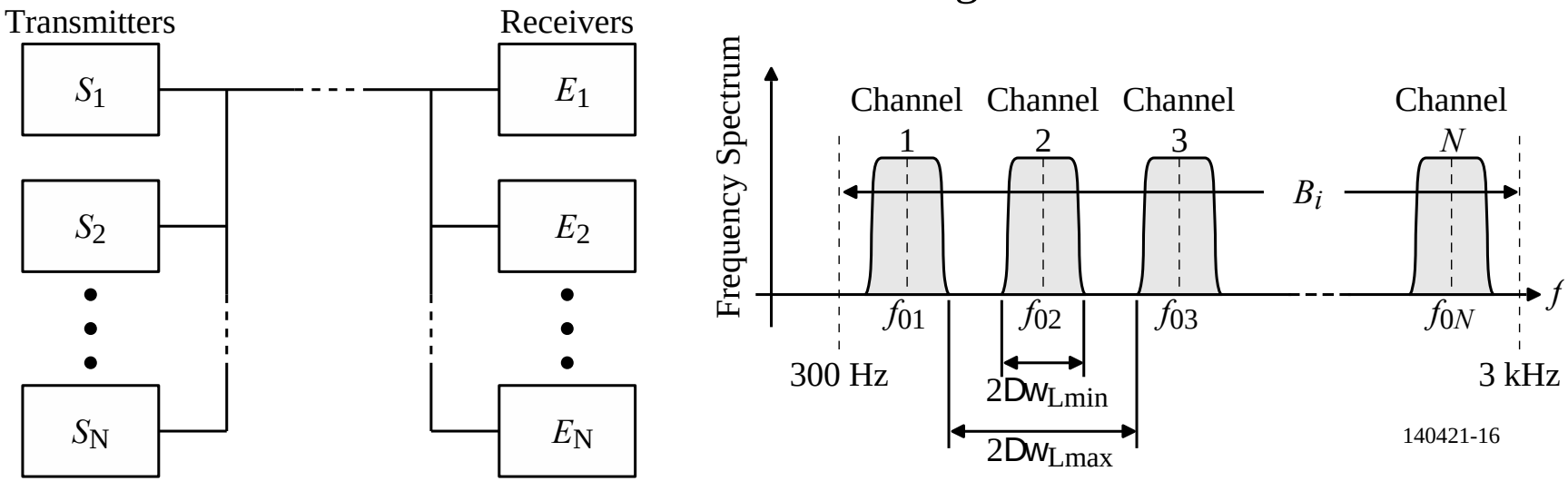
c.) Active PI filter:

Use the following equations to solve for τ_1 and τ_2. Because this filter has a pole at $s = 0$, it is not necessary for τ_1 to be larger than τ_2.

$$\omega_n = \sqrt{\frac{K_o K_d}{\tau_1}} \qquad \text{and} \qquad \zeta = \frac{\omega_n \tau_2}{2}$$

LPLL Design Example

Consider the multichannel telemetry system shown where one single, voice-grade communication line is used to transmit a number of signal channels.



Each transmitter is to transmit a binary signal with a baud rate of 50 bits/sec. The signal is encoded in a non-return to zero format which means that the bandwidth required is half the baud rate or 25 Hz. The spectrum of the FM-modulated carrier consists of the carrier frequency and a number of sidebands displaced by ±25 Hz, ±2·25 Hz, etc. from the carrier frequency.

Assuming that a narrow-band FM is used, the channel spacing will be selected as 60 Hz. The channel is assumed to be an ordinary telephone cable with a bandwidth of 300 Hz to 3000 Hz giving B_i = 2700 Hz. Therefore, the maximum number of channels is

Max. no. of channels = B_i/Channel spacing = 2700/60 = 45 channels.

LPLL Design Example – Continued

Design one of the receivers using the procedure outlined above assuming the carrier frequency is 1000 Hz. Assume the VCO is an XR-215†

1.) The angular frequency, ω_o, is $2\pi \cdot 1000 = 6280$ sec.$^{-1}$.

2.) Select $\zeta = 0.7$.

3.)In this problem the noise cannot be neglected. Therefore, we must find the noise bandwidth, B_L, of the loop and not the lock-range $\Delta\omega_L$. The input *SNR* is given as

$$(SNR)_i = \frac{P_s}{P_n}$$

Because the other 44 channels act like noise to our particular channel, let $P_n = 44P_s$.

Therefore, $$(SNR)_i = \frac{P_s}{P_n} = \frac{1}{44} \approx 0.023$$

To enable locking onto the carrier, the *SNR* of the loop should be approximately 4.

$$\therefore \quad B_L = \frac{(SNR)_i B_i}{(SNR)_L 2} = \frac{0.023 \cdot 2700}{4 \cdot 2} = 7.67 \text{ Hz}$$

4.)Determine the lock range. Because the noise bandwidth, B_L, is very small, the lock range will be small and will be determined in step 7.

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† *Phase-Locked Loop Data Book*, Exar Integrated Systems, Sunnyvale, CA, 1981.(http://www.exar.com/products/XR215A.html)

LPLL Design Example – Continued

5.) From the data sheet of the VCO we get,

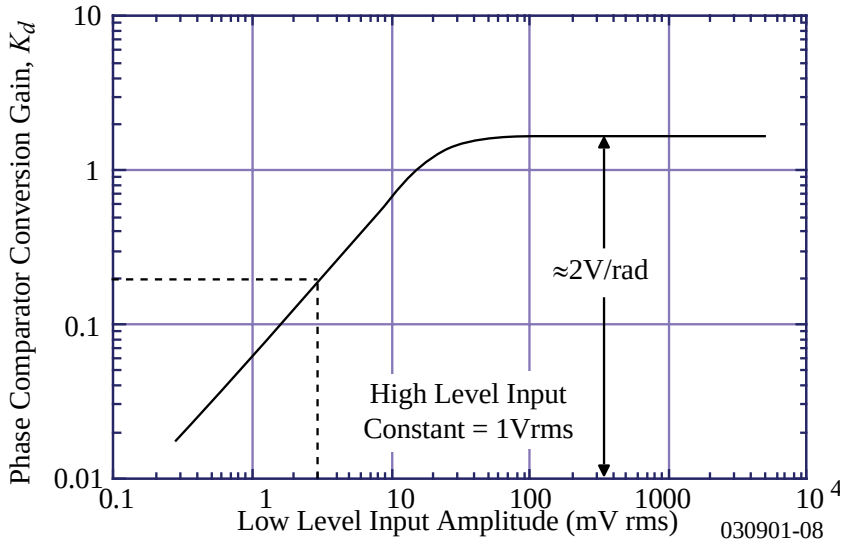
$$f_o = \frac{200}{C_o}\left(1 + \frac{0.6}{R_x}\right) \qquad \text{and } K_o = \frac{700}{C_o R_o}$$

where the resistors are in kΩ and the capacitors in μF.
Choosing C_o = 0.27μF and R_x = 1.71kΩ gives the required center frequency of 1000 Hz. The data sheet specifies that R_o should be in the range of 1 to 10 kΩ. Therefore, we see that K_o can be in the range of 260 rads/sec·V to 2600 rads/sec·V. Choosing R_o as 10 kΩ, gives K_o = 260 rads/sec·V.

This means that the VCO can change its frequency by $260/2\pi$ = 41.4 Hz. We will have to check in step 7 that this range is sufficient to enable locking within the $\Delta\omega_L$ lock range.

6.) Determine K_d. A plot of the data sheet is shown. In the application we are considering, the input signal level is 3mV(rms).

$\therefore K_d \approx 0.2$ V/rad/



LPLL Design Example – Continued

7.) ω_n is calculated from B_L and ζ and is,

$$\omega_n = \frac{2B_L}{\zeta + 0.25\zeta} = \frac{2 \cdot 7.67}{0.7 \cdot 1.25} = 17.53 \text{ sec.}^{-1}$$

The lock-in range is found as,

$$\Delta\omega_L = 2\zeta\omega_n = 24.54 \text{ sec.}^{-1}$$

8.) Solve for τ_1 and τ_2 from the equations below.

$$\omega_n = \sqrt{\frac{K_o K_d}{\tau_1 + \tau_2}} \qquad \text{and} \qquad \zeta = \frac{\omega_n}{2}\left(\tau_2 + \frac{1}{K_o K_d}\right)$$

$$\tau_2 = \frac{2\zeta}{\omega_n} - \frac{1}{K_o K_d} = 60.6 \text{ ms}$$

$$\tau_1 + \tau_2 = \frac{K_o K_d}{\omega_n^2} = 169.2 \text{ ms} \quad \rightarrow \quad \tau_1 = 108.6 \text{ ms}$$

The resistor R_1 is already integrated on the chip as 6 kΩ.

9.) Finally, determine R_1, R_2, and C of the filter. The data sheet shows that the resistor, R_1, is already integrated on the chip as 6 kΩ. (Note: Two passive lag filters are needed.)

$$\therefore \quad C = \frac{\tau_1}{R_1} = \frac{108.6 \text{ ms}}{6 \text{ k}\Omega} = 18.1 \text{ µF} \qquad \text{and} \qquad R_2 = \frac{\tau_2}{C} = \frac{60.6 \text{ ms}}{18.1 \text{ µF}} = 3.35 \text{ k}\Omega$$

Simulation of the LPLL Design Example

The open loop transfer function is,

$$LG(s) = \frac{K_v}{s}\left(\frac{1+s\tau_1}{1+s(\tau_1+\tau_2)}\right) = \frac{52}{s}\left(\frac{1+s60.6x10^{-3}}{1+s169.2x10^{-3}}\right)$$

Cutoff frequency:

$$\omega_c = \omega_n\sqrt{2\zeta^2+\sqrt{4\zeta^4+1}} = 17.53\sqrt{2\cdot 0.7^2+\sqrt{4\cdot 0.7^4+1}} = 27.045 \text{ rads/sec} \quad (4.3 \text{ Hz})$$

The phase margin can be written as,

$$PM = 180° - 90° + \tan^{-1}(\omega_c \cdot 60.6x10^{-3}) - \tan^{-1}(\omega_c \cdot 169.2x10^{-3})$$

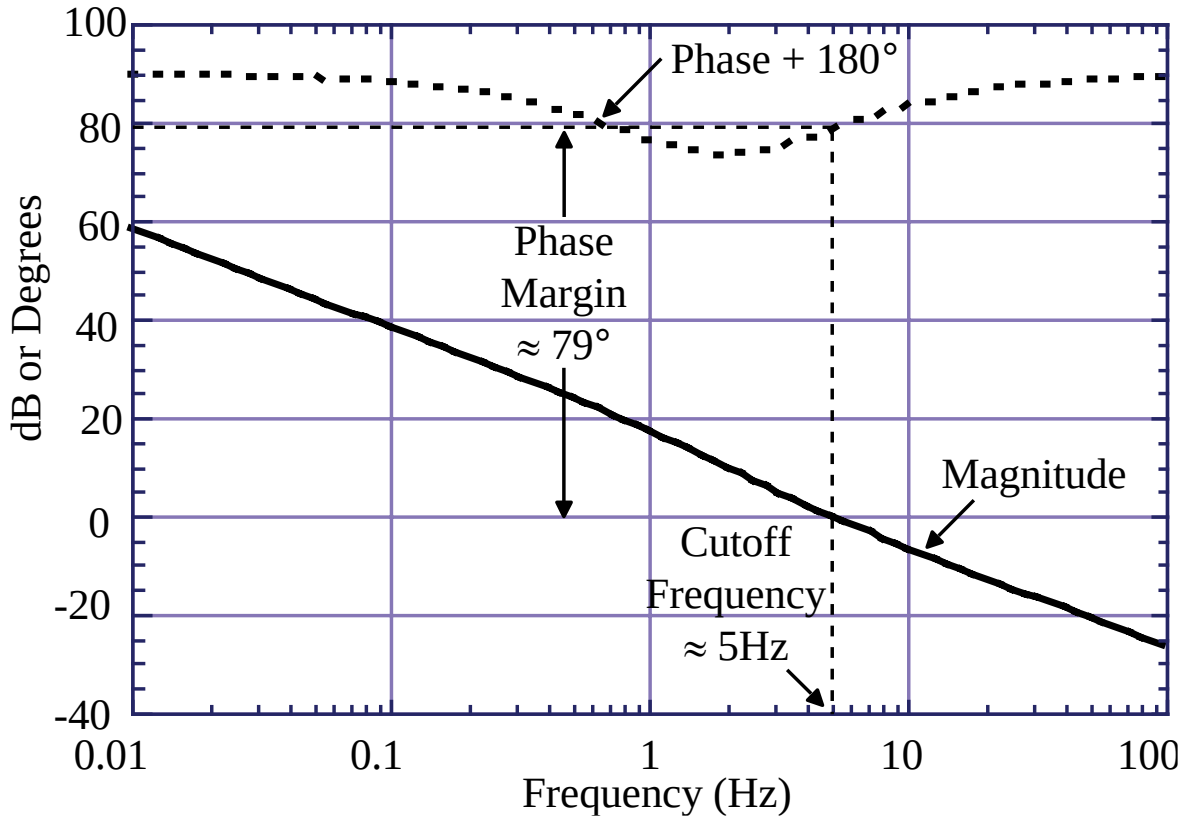
$$= 90° + 58.61° - 77.67° = 70.94°$$

PSPICE Input File:

```
LPLL Design Problem-Open Loop Response
VS 1 0 AC 1.0
R1 1 0 10K
* Loop bandwidth = Kv =52 sec.-1   Tau1=60.6E-3  Tau2=108.6E-3
ELPLL 2 0 LAPLACE {V(1)}= {(52/(S+0.00001))*((1+60.6E-3*S)/(1+169.2E-3*S))}
R2 2 0 10K
*Steady state AC analysis
.AC DEC 20 0.01 100
.PRINT AC VDB(2) VP(2)
.PROBE
.END
```

Simulation of the LPLL Design Example - Continued

Open Loop Response

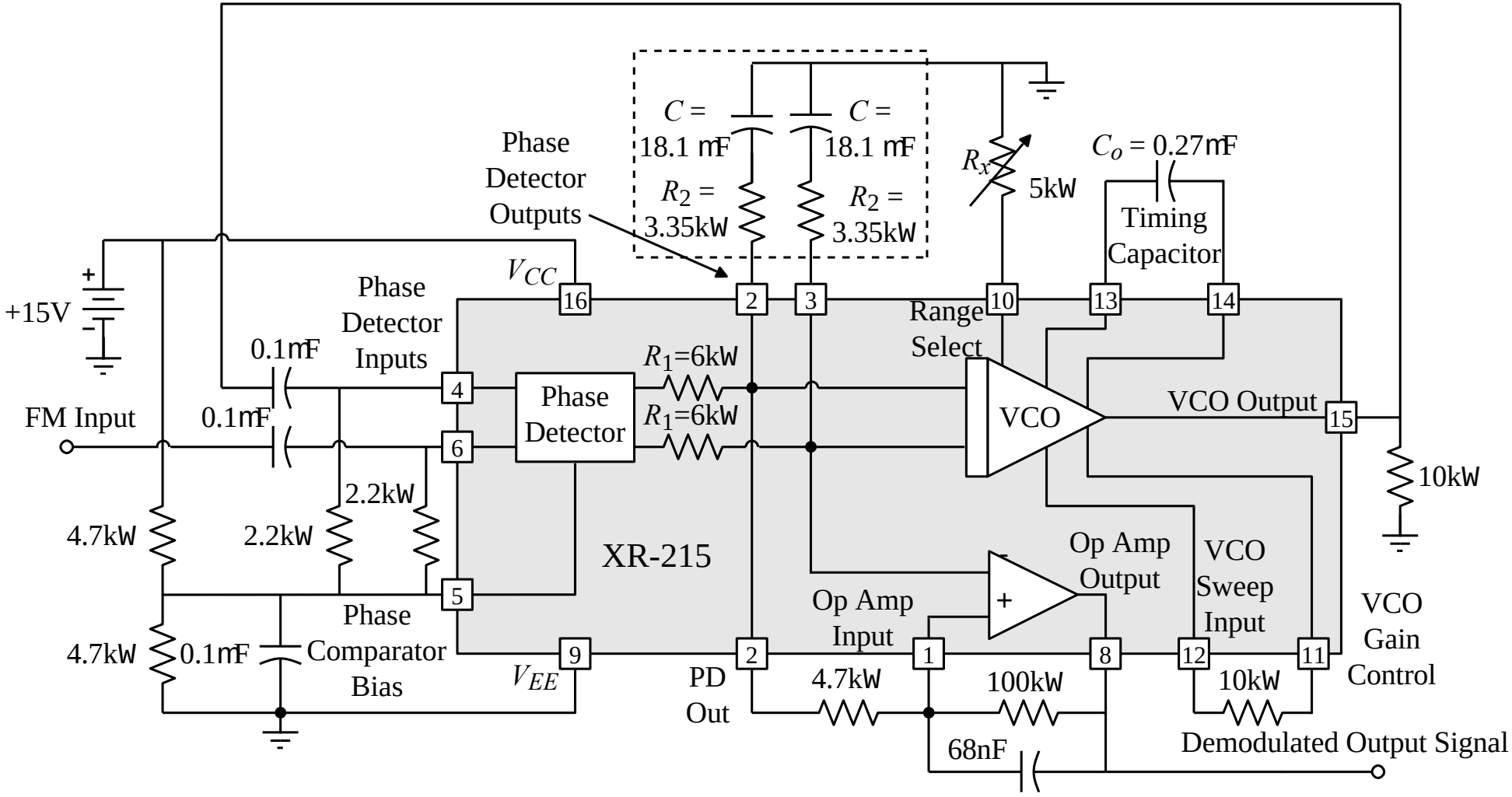


Cutoff frequency ≈ 5Hz

Phase margin ≈ 79°

LPLL Design Example – Continued

Implementation of the FSK Demodulator:



LPLL SYSTEM SIMULATION

Approaches

At least two methods are available:

1.) Behavioral modeling of PSPICE (illustrated on the previous example)

2.) PC-based simulator developed by R.M. Best

PSPICE

The Laplace transform behavioral model of PSPICE uses controlled voltage sources to implement linear frequency domain transfer functions in the linear domain.

General Form:

E <*name*> <(+)*node*> <(-)*node*> LAPLACE {<*expression*>} = {<*transform*>}

Example:

Plot $LG(s) = \frac{V_2}{V_1} = \frac{K_v}{s}\left(\frac{1+s\tau_1}{1+s(\tau_1+\tau_2)}\right) = \frac{52}{s}\left(\frac{1+s60.6\text{x}10^{-3}}{1+s169.2\text{x}10^{-3}}\right)$

```
VS 1 0 AC 1.0
R1 1 0 10K
* Loop bandwidth = Kv =52 sec.-1   Tau1=60.6E-3  Tau2=108.6E-3
ELPLL 2 0 LAPLACE {V(1)}= {(52/(S+0.00001))*((1+60.6E-3*S)/(1+169.2E-3*S))}
R2 2 0 10K
.AC DEC 20 0.01 100
.PRINT AC VDB(2) VP(2)
.PROBE
.END
```

PC-Based PLL Simulation Program

A PC-based simulation program developed by R.M. Best and found as part of the 4th edition is used as an example of PLL simulation at the systems level. The description of how to use this program is found on the CD or described in the text, *Phase-Locked Loops-Design, Simulation, and Applications*, 4th ed., 1999, McGraw-Hill Book Co.

The simulation flow chart is show below and follows the previous design procedure.

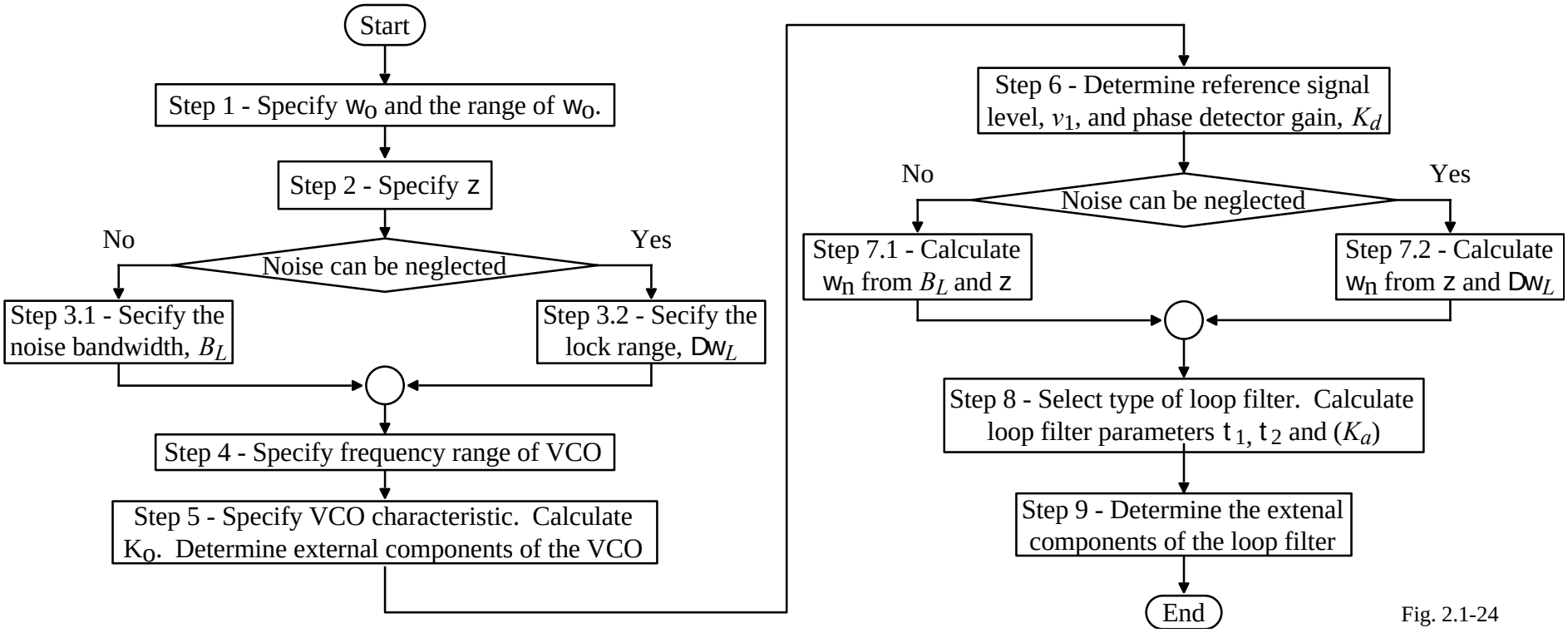


Fig. 2.1-24

Example of LPPL Simulation

PLL selected is:

1.) Architecture - LPLL, Passive Lag, and VCO

2.) Parameters –

Power supply = +5V and 0V

Phase detector: K_d = 1.0, V_{sat}^+ = 4.5V and V_{sat}^- = 0.5V

Loop filter: τ_1 = 500 µsec. and τ_2 = 50 µsec.

Oscillator: K_o = 130,000 rads/sec·V, V_{sat}^+ = 4.5V and V_{sat}^- = 0.5V

The simulator program calculates ω_n = 15,374.12 rads/sec. and ζ = 0.443.

Using the developed formulas, we can compute the key LPLL parameters as:

1.) Lock range: $\Delta\omega_L$ = 13,621 rads/sec. $\rightarrow$ Δf_L = 2169 Hz

2.) Pull-out range: $\Delta\omega_{PO}$ = 39,932 rads/sec. $\rightarrow$ Δf_{PO} = 6358 Hz

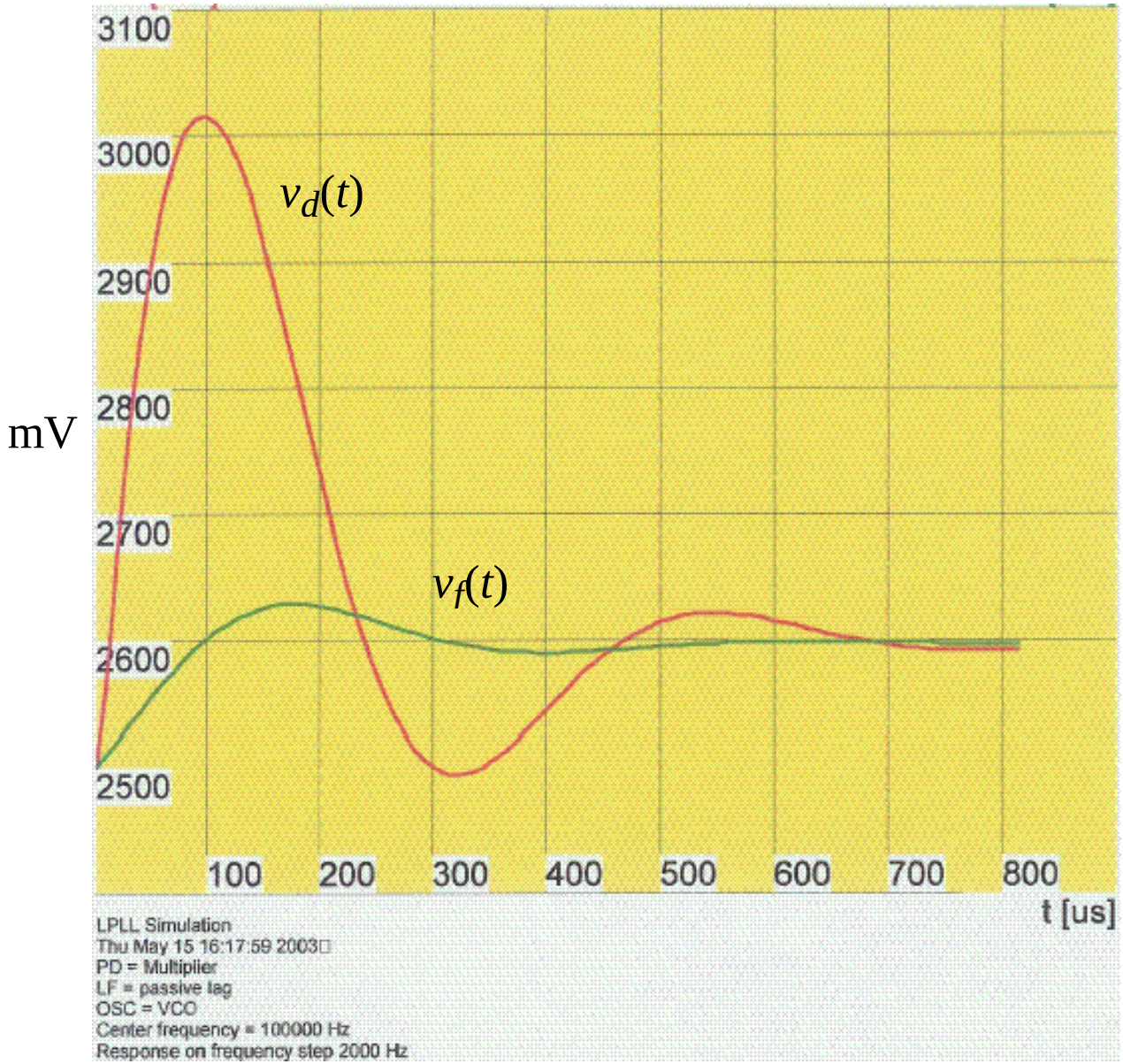
3.) Pull-in range: $\Delta\omega_P$ = 53,597 rads/sec. $\rightarrow$ Δf_P = 8534 Hz

(The ratio $\frac{\omega_n}{K_o K_d}$ = 0.12 and can be considered a high-gain loop)

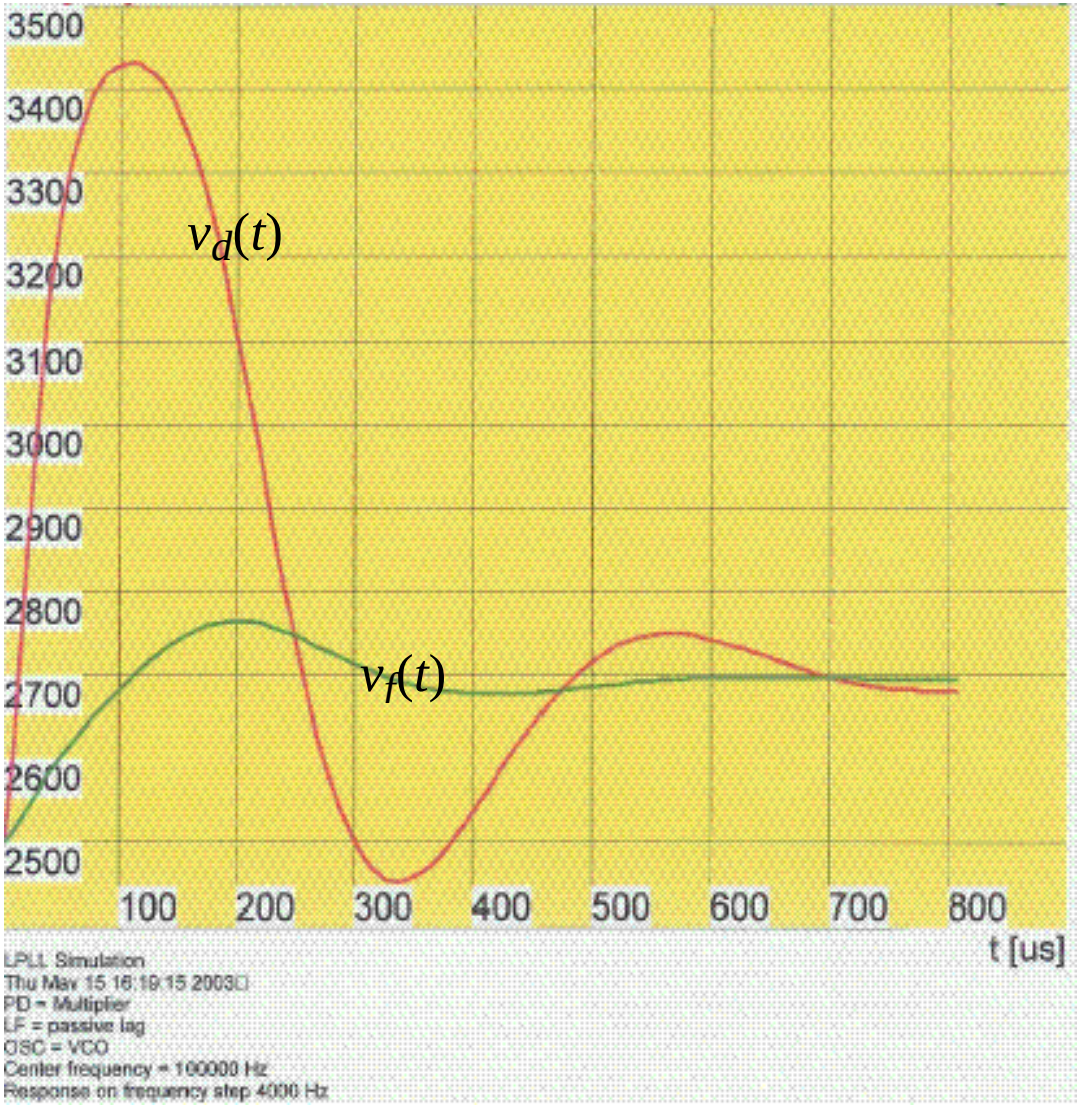
4.) Hold range: $\Delta\omega_H$ = 130,000 rads/sec. $\rightarrow$ Δf_L = 20,700 Hz

On the following pages, we attempt to verify these values by simulation.

Pull-out Range of the LPLL (2kHz Frequency Step)



Linearity of the LPLL (Frequency Step Doubled from 2kHz to 4kHz)

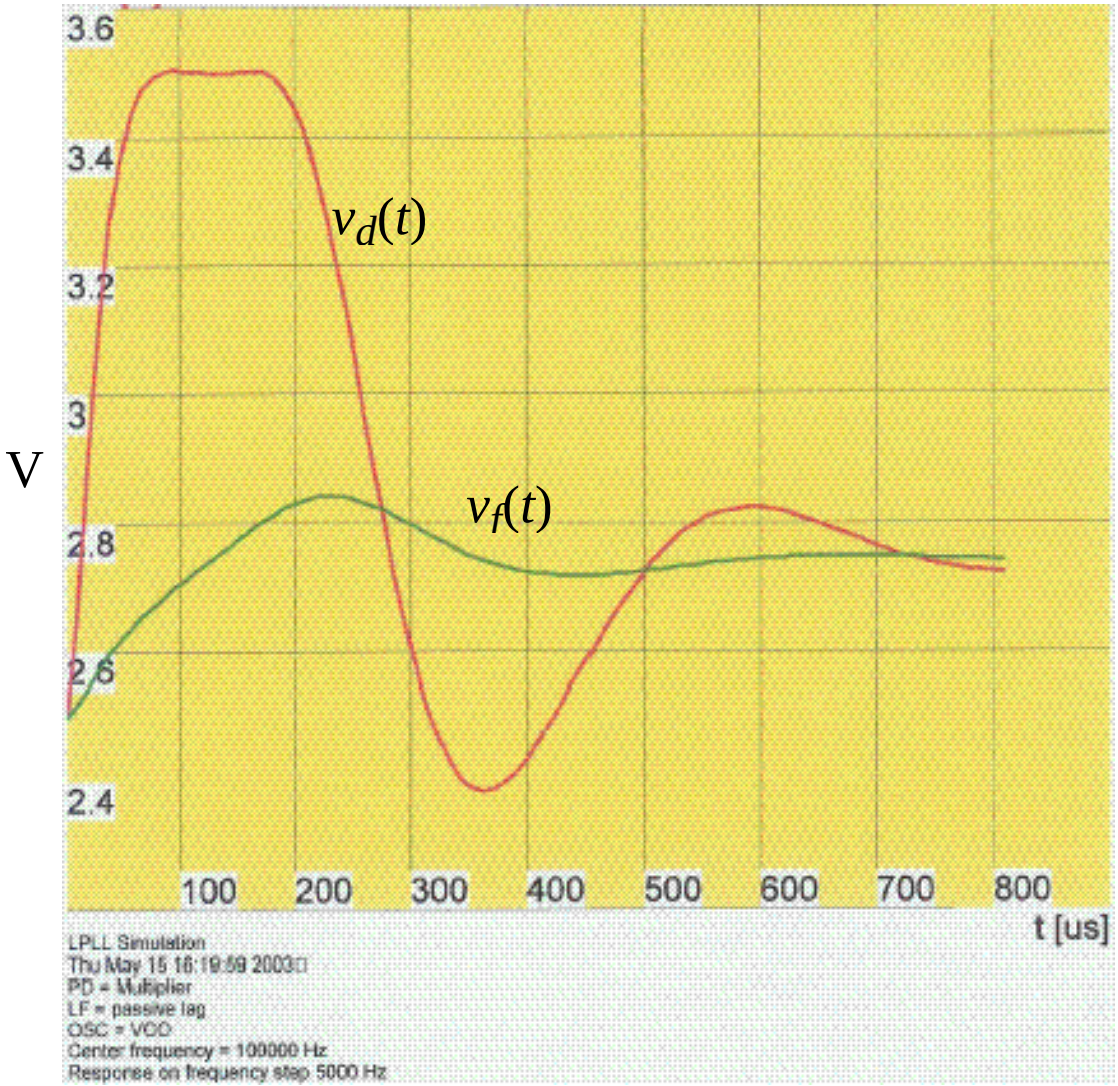


The LPLL is not linear because doubling the frequency step did not double the output.

The flat topped response for $v_d(t)$ indicates that the phase error is close to $\pi/2$.

Loop is still locked.

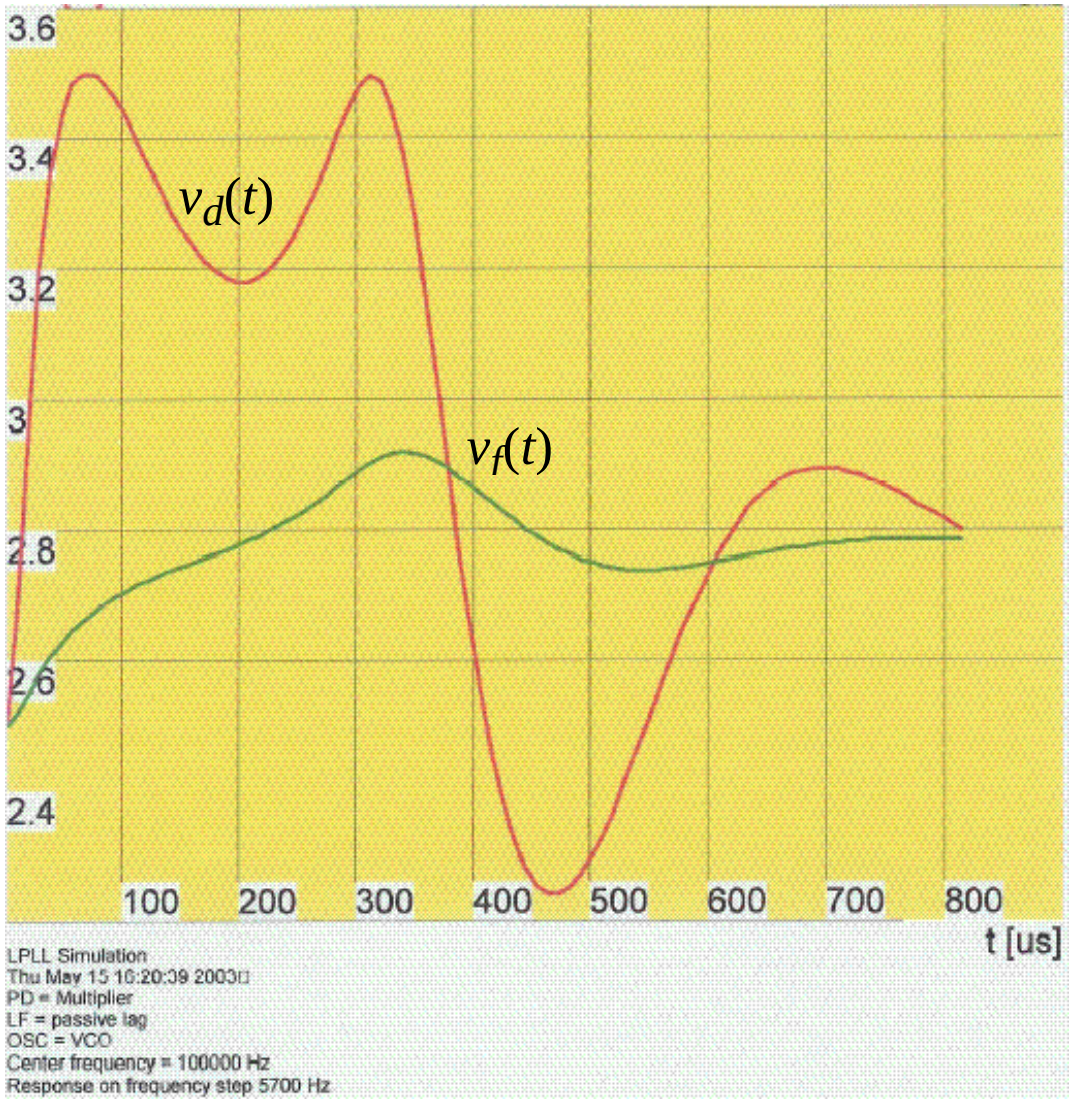
Pull-out Range of the LPLL (Frequency = 5kHz)



The dip in the response of the detector output implies that the phase error has exceeded $\pi/2$.

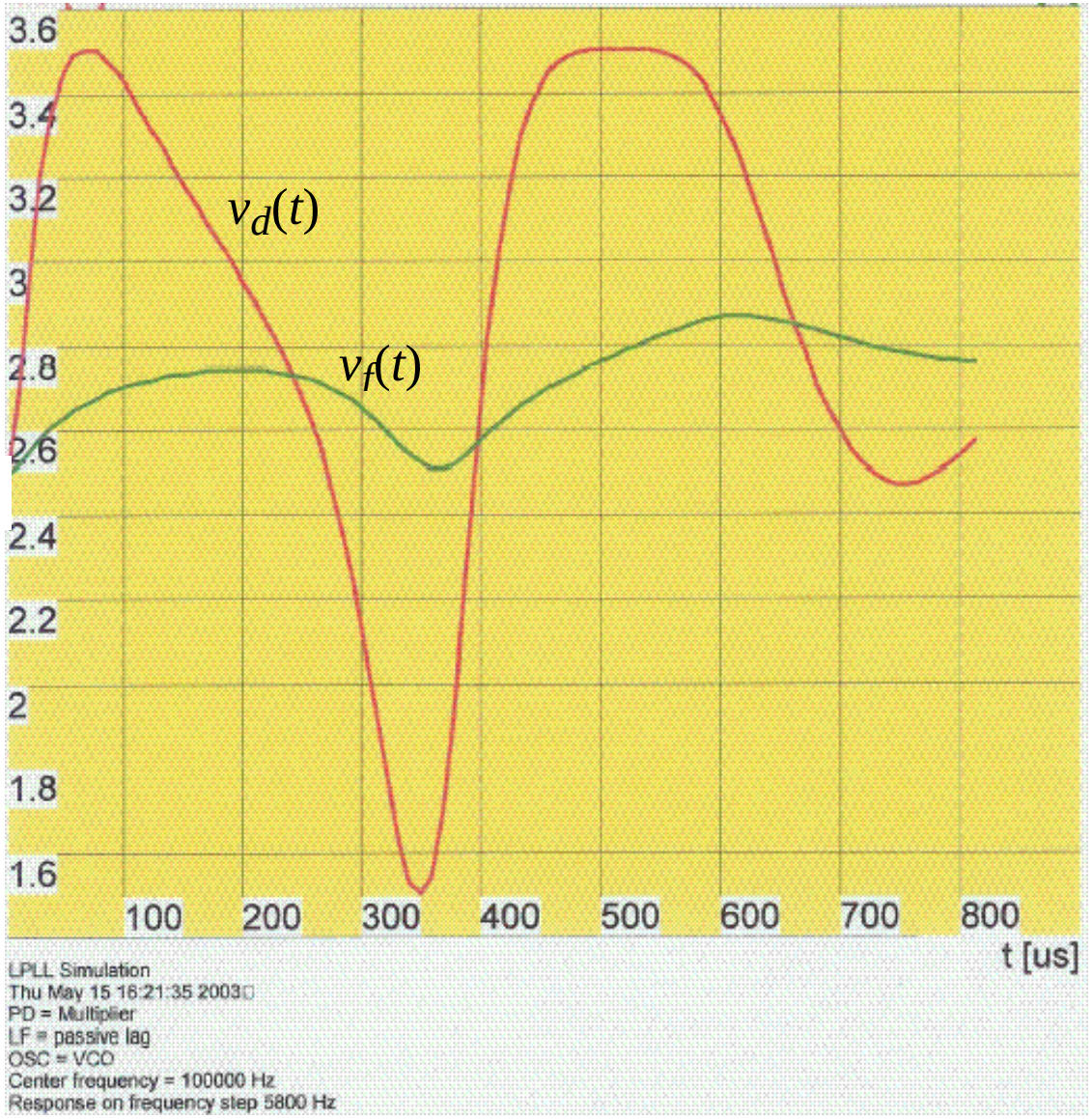
The loop is still locked.

Finding the Pull-out Range (Frequency step = 5700Hz)



The loop has not yet pulled out and is still locked.

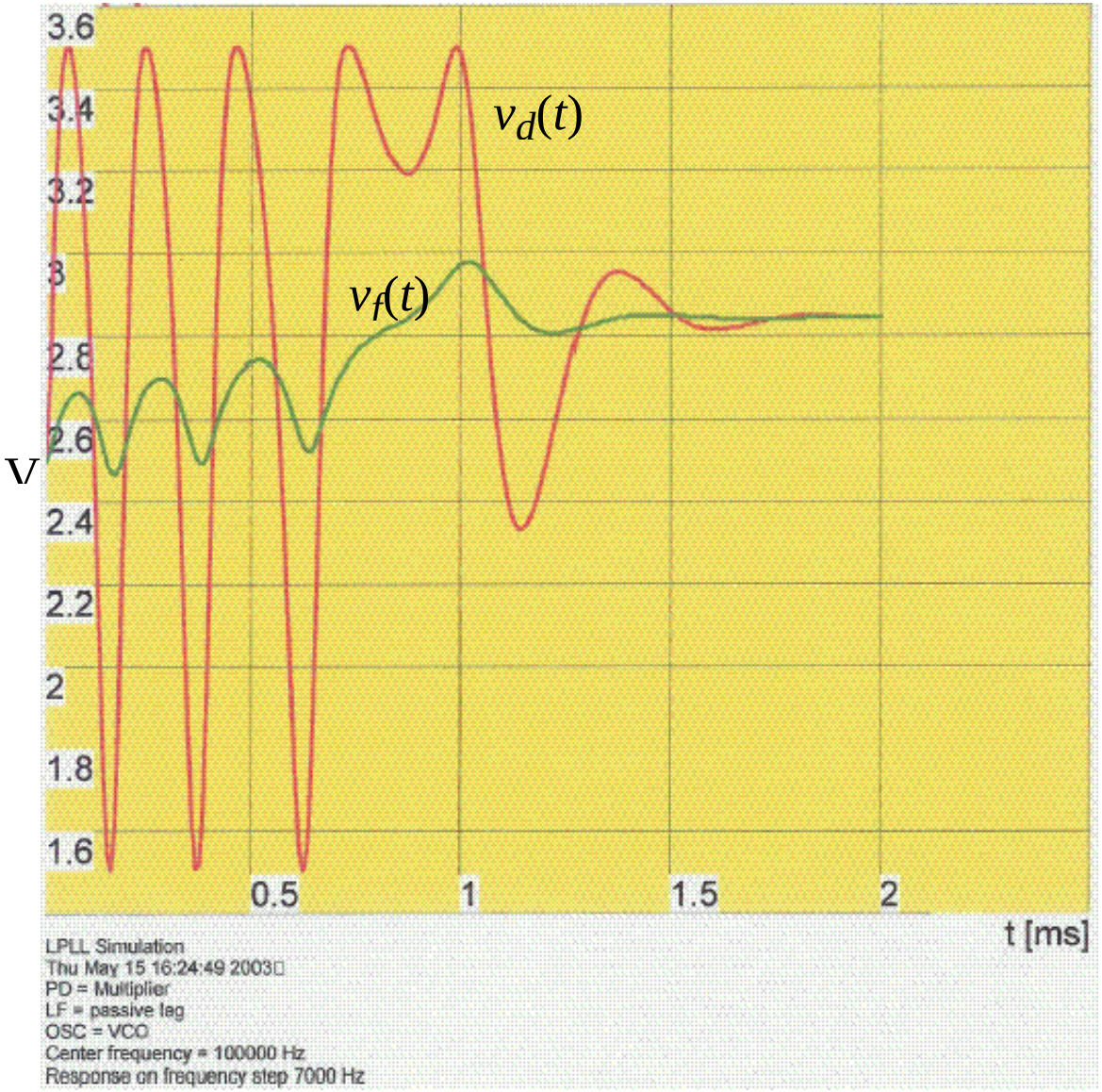
Finding the Pull-out Frequency (Frequency step = 5800Hz)



From this simulation, we see that the pull-out frequency is close to 5800Hz which is compared with the predicted value of 6358Hz (10% error).

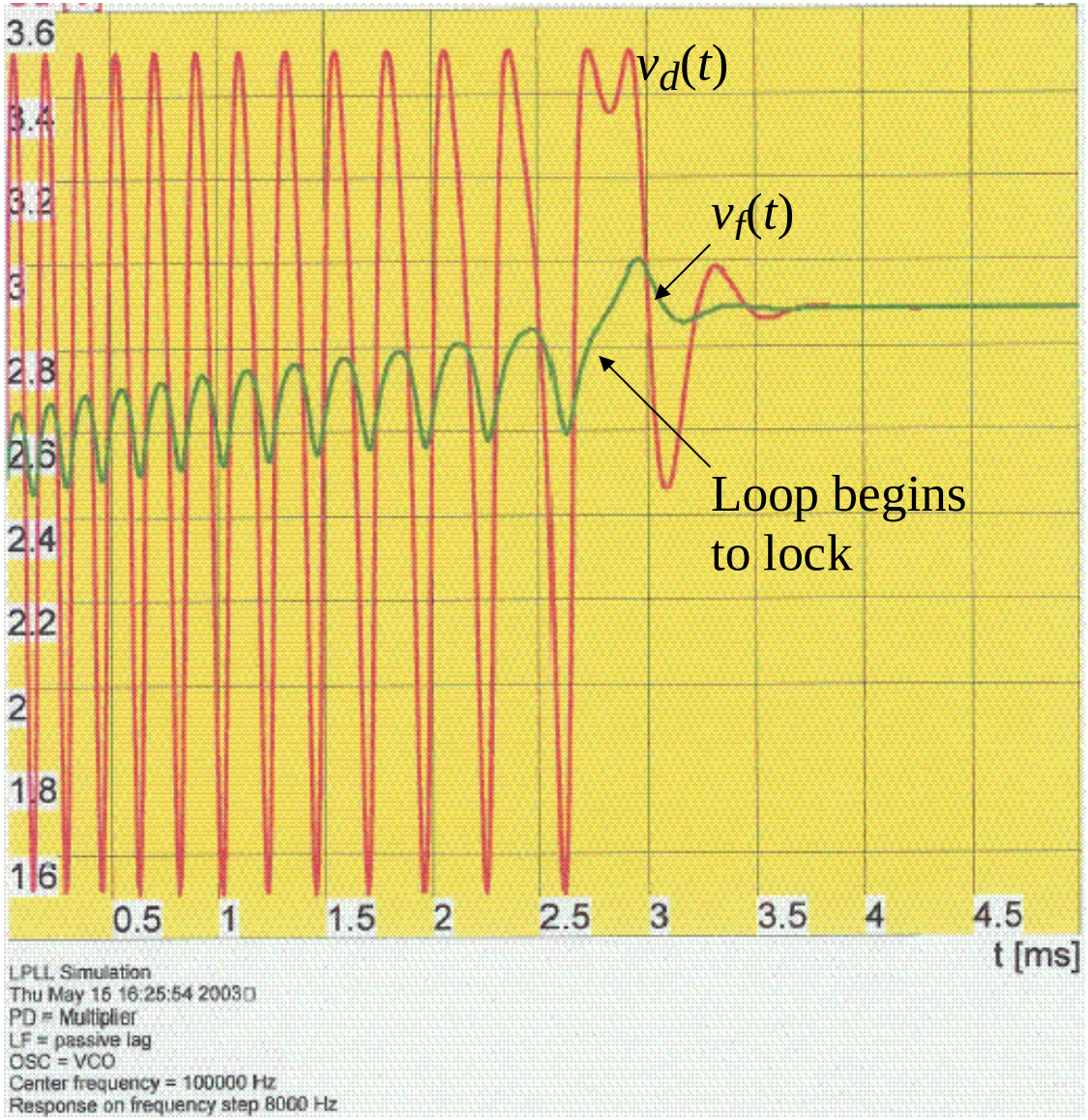
Because the frequency step applied to the LPLL is smaller than the pull-in range, the loop locks again after a short time.

Finding the Pull-in Frequency (Frequency step = 7000Hz)



The frequency step of 7000Hz causes the LPLL to pull-out again. However, the pull-in process takes longer than before.

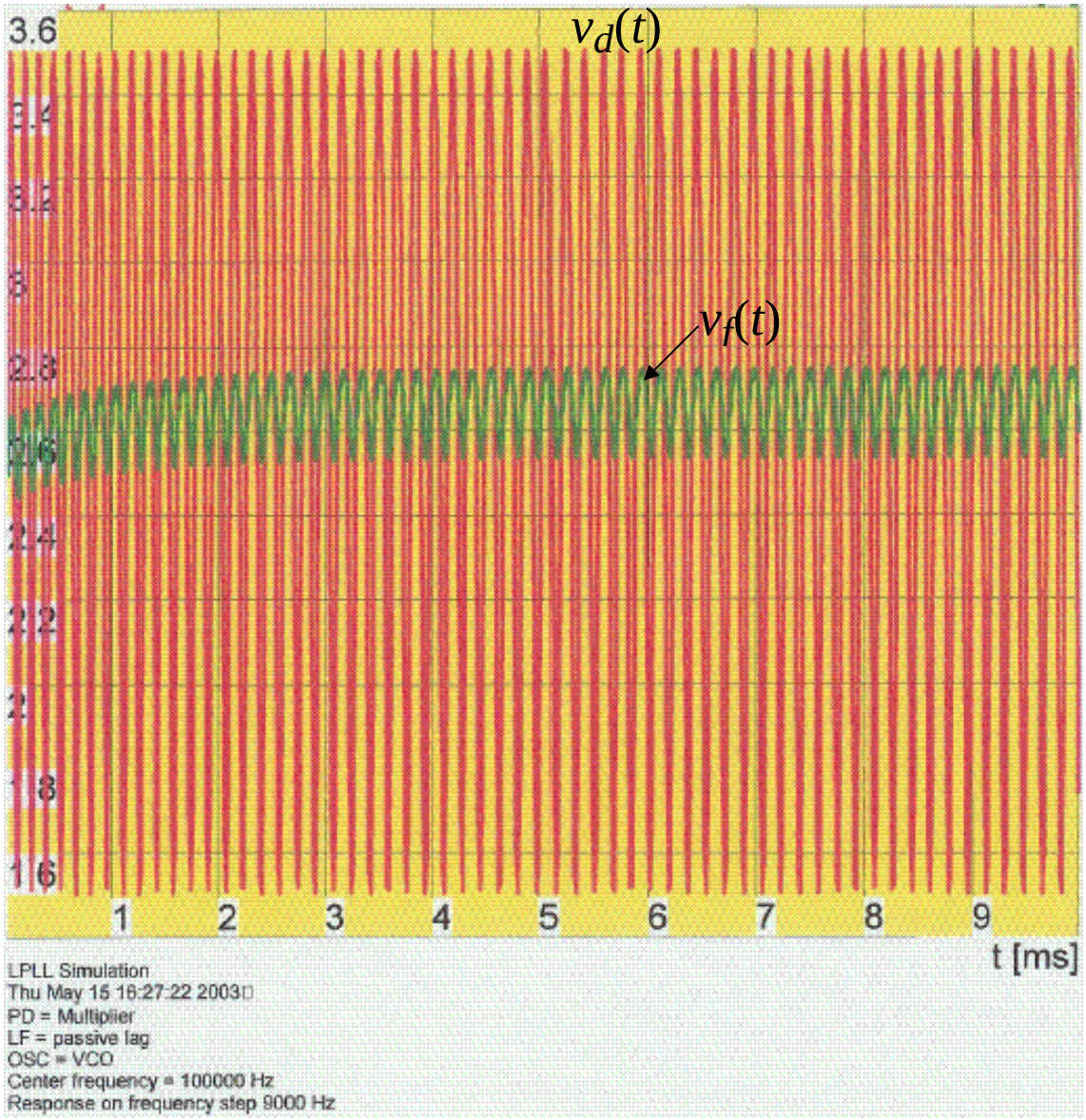
Finding the Pull-in Frequency (Frequency step = 8000Hz)



The frequency step of 8000Hz causes the LPLL to pull-out again. However, the pull-in process takes even longer than before.

We can estimate the lock range by observing that $v_f(t)$ gets slowly "pumped up". When it reached about 2.8V, the PLL became locked within one oscillation of $v_d(t)$. The value of $v_f(t)$ at lock is 2.9V. The 0.1V difference corresponds to a lock range of 2000Hz.

Finding the Pull-in Frequency (Frequency Step = 9000Hz)



The frequency step of 9000Hz causes the LPLL to pull-out and is no longer able to pull back in.

Further simulation showed that the LPLL cannot pull back in for a frequency step of 8500Hz.

$\therefore$ The pull-in frequency is near 8500Hz compared with a predicted value of 8534Hz.

SUMMARY

- LPLL design –Design the parameters K_o, K_d, ζ, and the filter $F(s)$ of the LPLL for a given performance specification
- PLL system simulation methods include:
  1.) Behavioral modeling of PSPICE (illustrated on the previous example)
  2.) PC-based simulator developed by R.M. Best