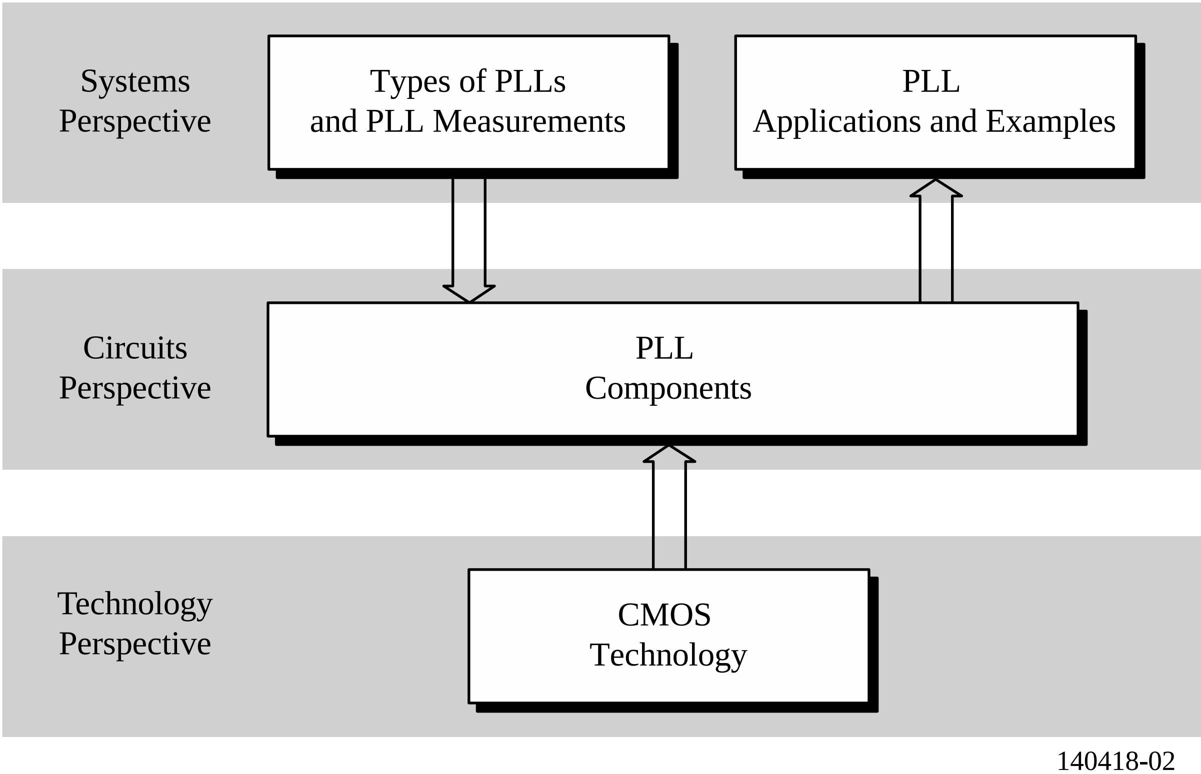
LECTURE 3 – CMOS PHASE LOCKED LOOPS

Topics

• The acquisition process – unlocked state

• Noise in linear PLLs

Organization:



THE ACQUISTION PROCESS – LPLL IN THE UNLOCKED STATE

Unlocked Operation

If the PLL is initially unlocked, the phase error, θ_e, can take on arbitrarily large values and as a result, the linear model is no longer valid.

The mathematics behind the unlocked state are beyond the scope of this presentation. In the section we will attempt to answer the following questions from an intuitive viewpoint:

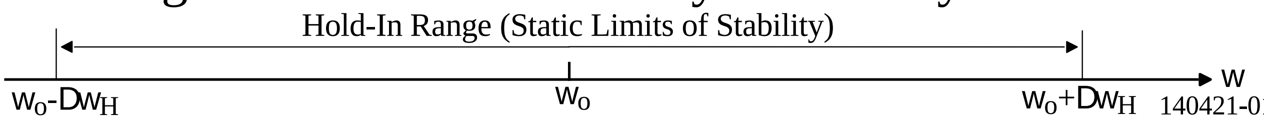
1.) Under what conditions will the LPLL become locked?

2.) How much time does the lock-in process require?

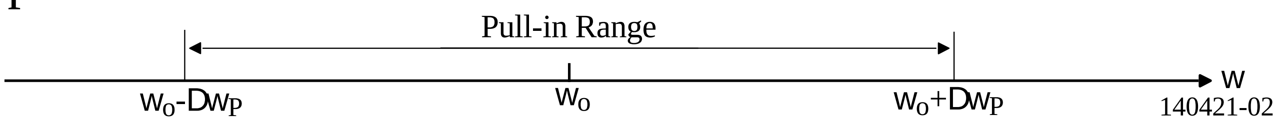
3.) Under what conditions will the LPLL lose lock?

Some Definitions of Key Performance Parameters

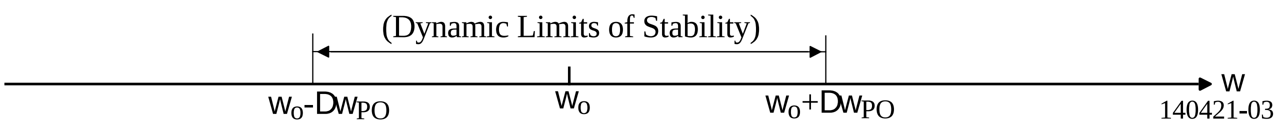
1.) The *hold range* ($\Delta\omega_H$) is the frequency range over which an LPLL can statically maintain phase tracking. A PLL is conditionally stable only within this range.



2.) The *pull-in range* ($\Delta\omega_P$) is the range within which an LPLL will always become locked, but the process can be rather slow.



3.) The *pull-out range* ($\Delta\omega_{PO}$) is the dynamic limit for stable operation of a PLL. If tracking is lost within this range, an LPLL normally will lock again, but this process can be slow.



4.) The *lock range* ($\Delta\omega_L$) is the frequency range within which a PLL locks within one single-beat note between reference frequency and output frequency. Normally, the operating frequency range of an LPLL is restricted to the lock range.

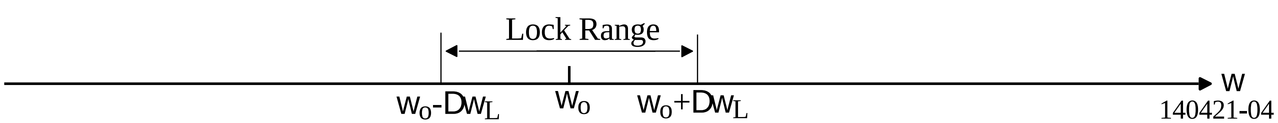
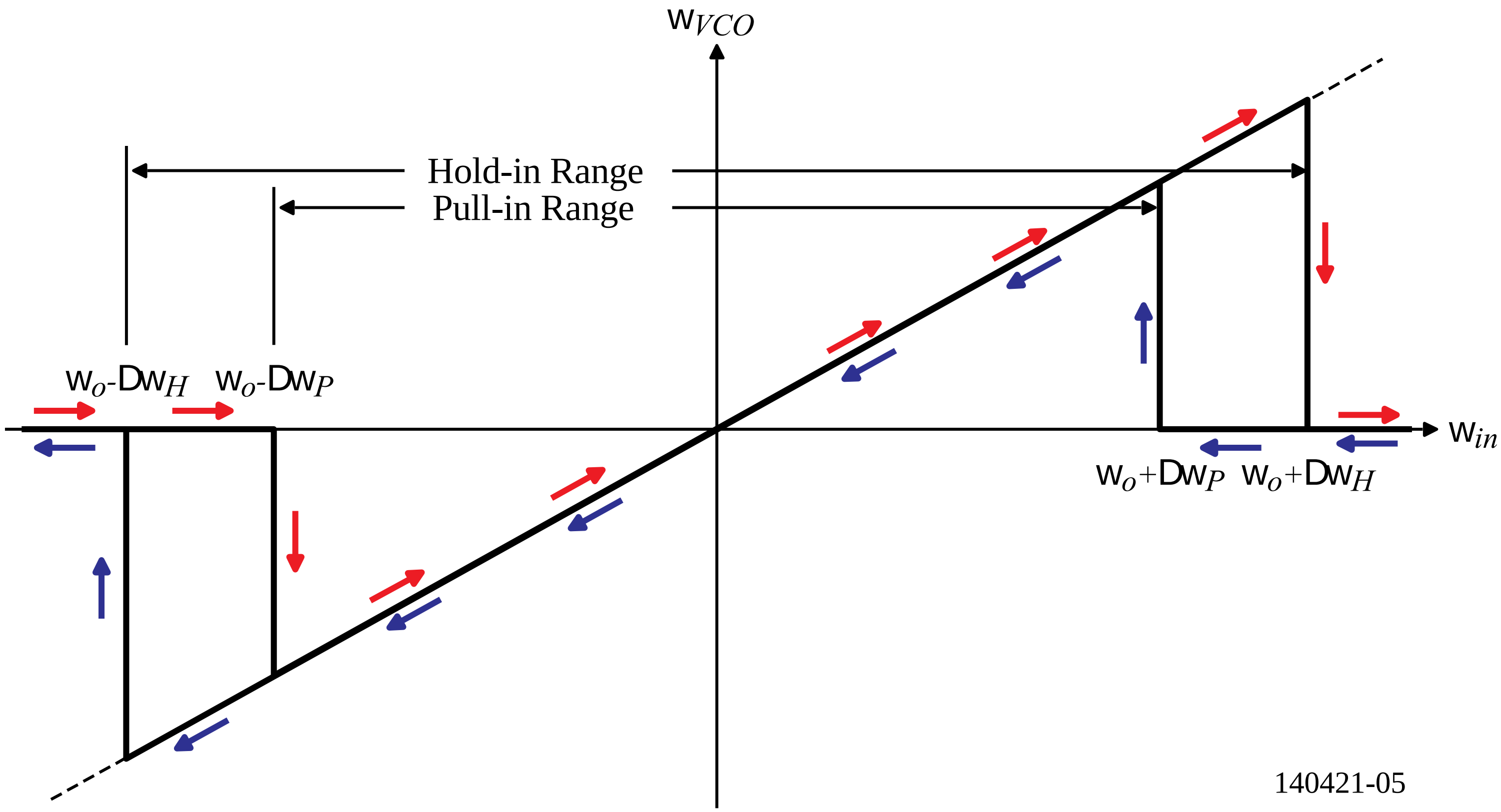


Illustration of Static Ranges

Assume the frequency of the VCO is varied very slowly from a value below ω_o-$\Delta\omega_H$ to a frequency above ω_o+$\Delta\omega_H$.



The following pages will attempt to relate the key parameters of hold range, pull-in range, pull-out range, and lock range to the time constants, τ_1 and τ_2 and the gain factors K_d, K_o, and K_a.

Hold Range ($\Delta\omega_H$)

The magnitude of the hold range is calculated by finding the frequency offset of the input that causes a phase error of $\pm\pi/2$.

Let,

$$\omega_1 = \omega_o \pm \Delta\omega_H \quad \rightarrow \quad \theta_1(t) = \Delta\omega_H \, t \rightarrow \quad \Theta_1(s) = \frac{\Delta\omega}{s^2}$$

$$\therefore \quad \Theta_e(s) = \Theta_1(s)\, H_e(s) = \frac{\Delta\omega}{s^2} \frac{s}{s + K_oK_dF(s)}$$

$$\lim_{t\to\infty} \theta_e(t) = \lim_{s\to 0} s\Theta_e(s) = \frac{\Delta\omega}{K_oK_dF(0)} \text{ (valid for small values of } \theta_e)$$

For large variations, we write

$$\lim_{t\to\infty} \sin\theta_e(t) = \frac{\Delta\omega_H}{K_oK_dF(0)} \quad \rightarrow \quad \Delta\omega_H = \pm K_oK_dF(0) \text{ when } \theta_e = \pm\pi/2$$

For the various filters-

1.) Passive lag filter: $\Delta\omega_H = \pm K_oK_d$

2.) Active lag filter: $\Delta\omega_H = \pm K_oK_dK_a$

3.) Active PI filter: $\Delta\omega_H = \pm\infty$

(If $\Delta\omega_H = \pm\infty$, the actual hold range may be limited by the frequency range of the VCO)

Lock Range ($\Delta\omega_L$)

Assume the loop is unlocked and the reference frequency is $\omega_1 = \omega_o + \Delta\omega$. Therefore,

$$v_1(t) = V_{10}\, sin(\omega_o t + \Delta\omega\, t)$$

The VCO output is assumed to be

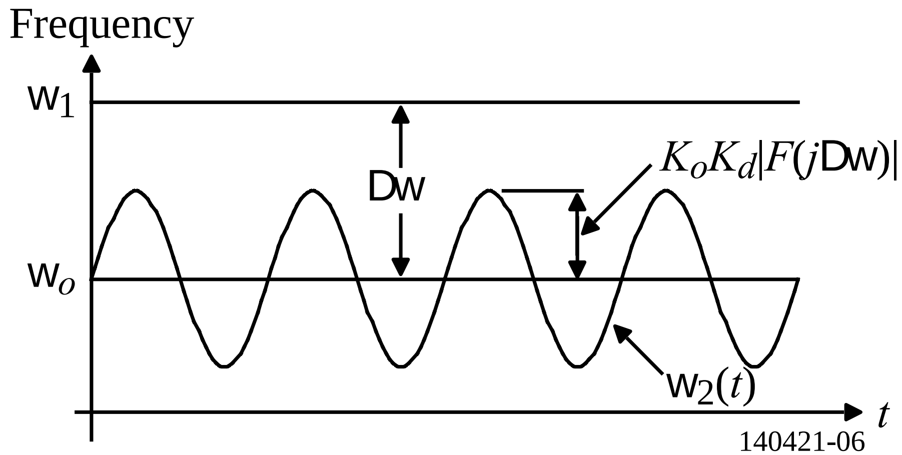
$$v_2(t) = V_{20}\, sgn(\omega_o t)$$

$\therefore$ $v_d(t) = K_d\, sin(\Delta\omega\, t)$ + higher frequency terms

Assuming the higher frequency terms are filtered out, the filter output is

$$v_f(t) \approx K_d|F(j\Delta\omega)|\, sin(\Delta\omega\, t)$$

This signal causes a frequency modulation of the VCO output frequency as shown.



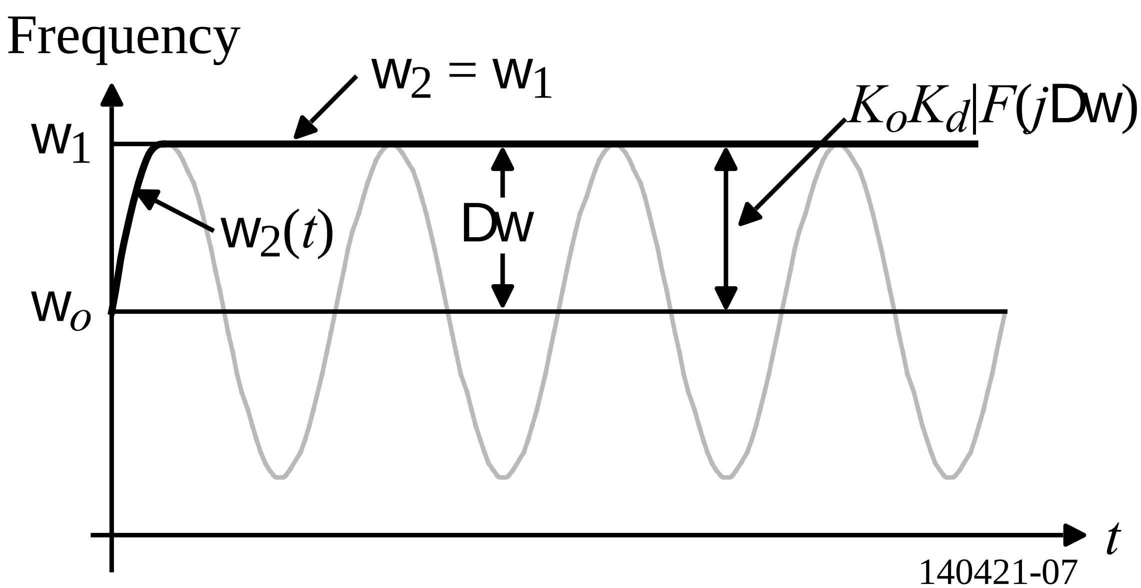
Note: No locking occurs in the above illustration because $\Delta\omega > K_oK_d\,|F(j\Delta\omega)|$.

Lock Range – Continued

Locking will take place if $K_oK_d\,|F(j\Delta\omega)| \geq \Delta\omega$. Therefore, the lock range can be expressed as,

$$\Delta\omega_L = \pm\, K_oK_d\,|F(j\Delta\omega)|$$

and is illustrated as,



Locks within one cycle or beat note.

Lock Range - Continued

If we assume that the lock range is greater than the filter frequencies, $1/\tau_1$ and $1/\tau_2$, the lock range for the various filters can be expressed as,

1.) Passive lag filter: $\Delta\omega_L = \pm K_oK_d\,|F(j\Delta\omega)| \approx \pm K_oK_d \dfrac{\tau_2}{\tau_1+\tau_2} \approx \pm K_oK_d \dfrac{\tau_2}{\tau_1}$

2.) Active lag filter: $\Delta\omega_L = \pm K_a\,|F(j\Delta\omega)| \approx \pm K_a \dfrac{\tau_2}{\tau_1}$

3.) Active PI filter: $\Delta\omega_L = \pm\,|F(j\Delta\omega)| \approx \pm \dfrac{\tau_2}{\tau_1}$

Previously, we found expressions for ω_n and ζ for each type of filter. Using these expressions and assuming that the loop gain is large, we find for all three filters that

$$\Delta\omega_L \approx \pm 2\zeta\omega_n$$

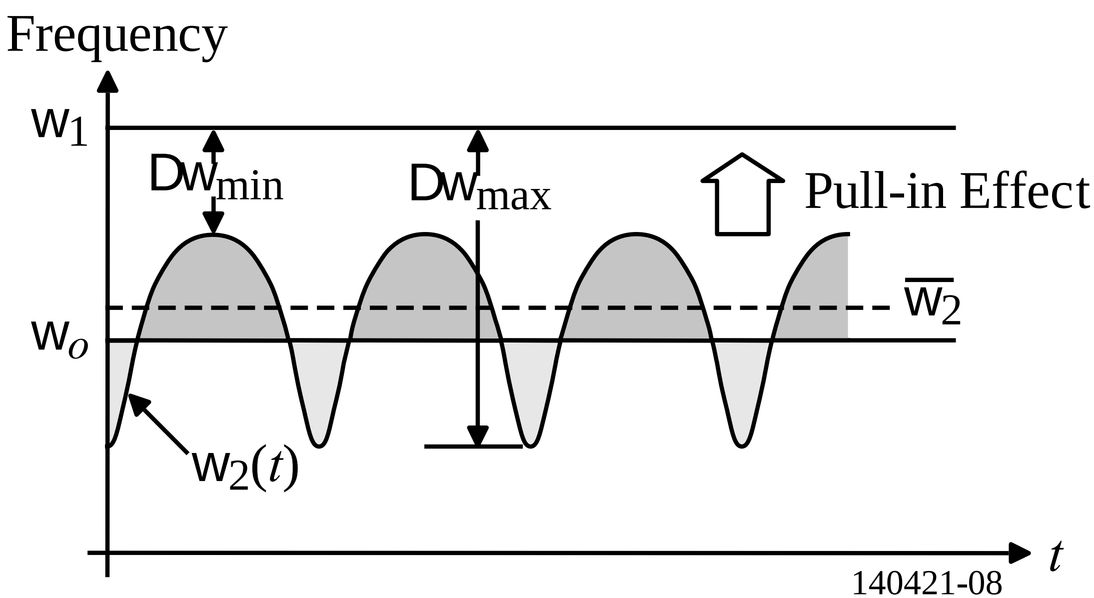
The lock-in time or settling time can be approximated as one cycle of oscillation,

$$T_L \approx \frac{1}{f_n} = \frac{2\pi}{\omega_n}$$

Pull-In Range ($\Delta\omega_P$)

Again assume the loop is unlocked and the reference frequency is $\omega_1 = \omega_o + \Delta\omega$ and the VCO initially operates at the center frequency of ω_o.

Let us re-examine the previous considerations:

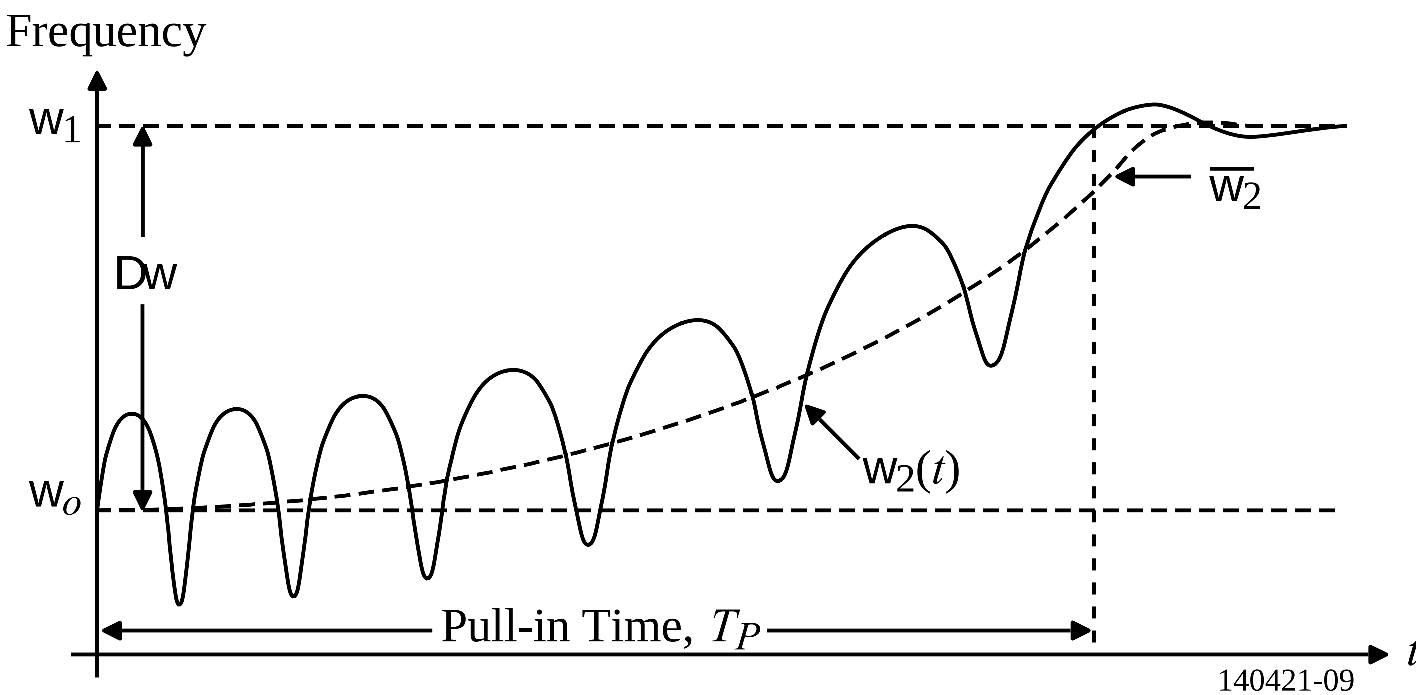


Since $\Delta\omega_{min}$ is less than $\Delta\omega_{max}$, the frequency of the positive going sinusoid is less than the frequency of the negative going sinusoid. As a consequence, the average value of the VCO output, $\overline{\omega_2}$, “pulls” toward ω_1.

The Pull-In Process

For an unlocked PLL with the frequency offset, $\Delta\omega$, less than the pull-in range, $\Delta\omega_P$, the VCO output frequency, ω_2 will approach the reference frequency, ω_1, over a time interval called the *pull-in time*, T_P.

Illustration:



Pull-In Range ($\Delta\omega_P$) for Various Types of Filters

The mathematical treatment of the pull-in process is beyond the scope of this presentation†. The results are summarized below.

Type of Filter	$\Delta\omega_P$ (Low Loop Gains)	$\Delta\omega_P$ (High Loop Gains)	Pull-In Time, T_P
Passive Lag	$\approx \frac{4}{\pi}\sqrt{2\zeta\omega_n K_o K_d - \omega_n^2}$	$\approx \frac{4\sqrt{2}}{\pi}\sqrt{\zeta\omega_n K_o K_d}$	$= \frac{\pi^2}{16}\frac{\Delta\omega_o^2}{\zeta\omega_n^3}$
Active Lag	$\approx \frac{4}{\pi}\sqrt{2\zeta\omega_n K_o K_d - \frac{\omega_n^2}{K_a}}$	$\approx \frac{4\sqrt{2}}{\pi}\sqrt{\zeta\omega_n K_o K_d}$	$= \frac{\pi^2}{16}\frac{\Delta\omega_o^2 K_a}{\zeta\omega_n^3}$
Active PI Lag	$\rightarrow \infty$	$\rightarrow \infty$	$= \frac{\pi^2}{16}\frac{\Delta\omega_o^2}{\zeta\omega_n^3}$

† R.M. Best, *Phase-Locked Loops – Design, Simulation, and Applications*, 4th ed., McGraw-Hill Book Co., 1999, Appendix A.

Example 3

A second-order PLL having a passive lag loop filter is assumed to operate at a center frequency, f_o, of 100kHz and has a natural frequency, f_n, of 3 Hz which is a very narrow band system. If ζ = 0.7 and the loop gain, $K_oK_d = 2\pi\cdot 1000$ sec.$^{-1}$, find the lock-in time, T_L, and the pull-in time, T_P, for an initial frequency offset of 30 Hz.

Solution

$$T_L \approx \frac{1}{f_n} = \frac{1}{3} = 0.333 \text{ secs.}$$

$$T_P = \frac{\pi^2}{16}\frac{\Delta\omega_o{}^2}{\zeta\omega_n{}^3} = \frac{4\pi^4}{16\cdot 8\pi^3}\frac{\Delta f_o{}^2}{\zeta f_n{}^3} = \frac{\pi\, 30^2}{32(0.7)3^3} = 4.675 \text{ secs.}$$

Pull-Out Range ($\Delta\omega_{PO}$)

The pull-out range is that *frequency step* which causes a lock-out if applied to the reference input of the PLL.

An exact calculation is not possible but simulations show that,

$$\Delta\omega_{PO} \approx 1.8\omega_n(\zeta + 1)$$

At any rate, the pull-out range for most systems is between the pull-in range and the lock-range,

$$\Delta\omega_L < \Delta\omega_{PO} < \Delta\omega_P$$

Steady-State Error of the PLL

The steady-state error is the deviation of the controlled variable from the set point after the transient response has died out. We have called this error, $\theta_e(\infty)$.

$$\theta_e(\infty) = \lim_{s\to 0} s\Theta_e(s) = \lim_{s\to 0} s\Theta_1(s)\frac{s}{s + K_oK_dF(s)}$$

Let us consider a generalized filter given as,

$$F(s) = \frac{P(s)}{Q(s)s^N}$$

where $P(s)$ and $Q(s)$ can be any polynomials in s, and N is the number of poles at $s = 0$.

$$\therefore \qquad \theta_e(\infty) = \lim_{s\to 0} \frac{s^2 s^N Q(s)\Theta_1(s)}{s\cdot s^N Q(s) + K_oK_dP(s)}$$

Comments:

- Note that for the active PI filter, $N = 1$.
- For $N > 1$, it becomes difficult to maintain stability.
- In most cases, $P(s)$ is a first-order polynomial and $Q(s)$ is a polynomial of order 0 or 1.

To find the steady-state error, the input, $\Theta(s)$ must be known. We will consider several inputs on the following slide.

Steady-State Error for Various Inputs

1.) A phase step, $\Delta\Phi$.

$$\Theta_1(s) = \frac{\Delta\Phi}{s}$$

$$\therefore \quad \theta_e(\infty) = \lim_{s\to 0} \frac{s^2 s^N Q(s)\Delta\Phi}{s[s\cdot s^N Q(s) + K_o K_d P(s)]} = 0 \text{ for any value of } N.$$

2.) A frequency step, $\Delta\omega$.

$$\Theta_1(s) = \frac{\Delta\omega}{s^2}$$

$$\therefore \quad \theta_e(\infty) = \lim_{s\to 0} \frac{s^2 s^N Q(s)\Delta\omega}{s^2[s\cdot s^N Q(s) + K_o K_d P(s)]} = 0 \text{ if } N \geq 1$$

(The LPLL must have one pole at $s = 0$ for the steady-state error to be zero.)

3.) A frequency ramp, $\Delta\dot{\omega}$.

$$\Theta_1(s) = \frac{\Delta\dot{\omega}}{s^3}$$

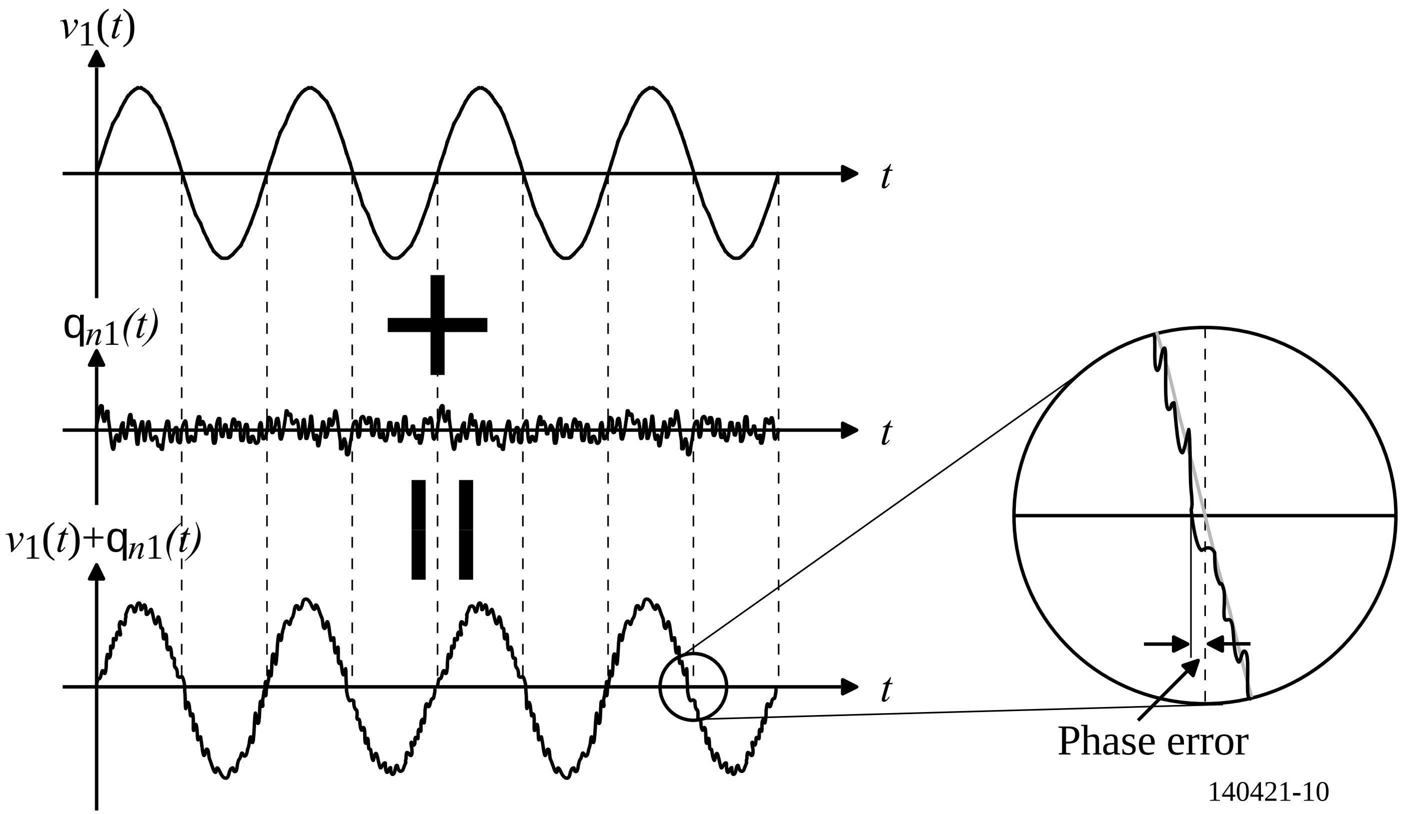
$$\therefore \quad \theta_e(\infty) = \lim_{s\to 0} \frac{s^2 s^N Q(s)\Delta\dot{\omega}}{s^3[s\cdot s^N Q(s) + K_o K_d P(s)]} = 0 \text{ if } N \geq 2$$

For $N = 2$ and $Q(s) =1$, the order of the LPLL becomes 3 permitting a phase shift of nearly 270° which must be compensated for by zeros to maintain stability.

NOISE IN LINEAR PLL SYSTEMS

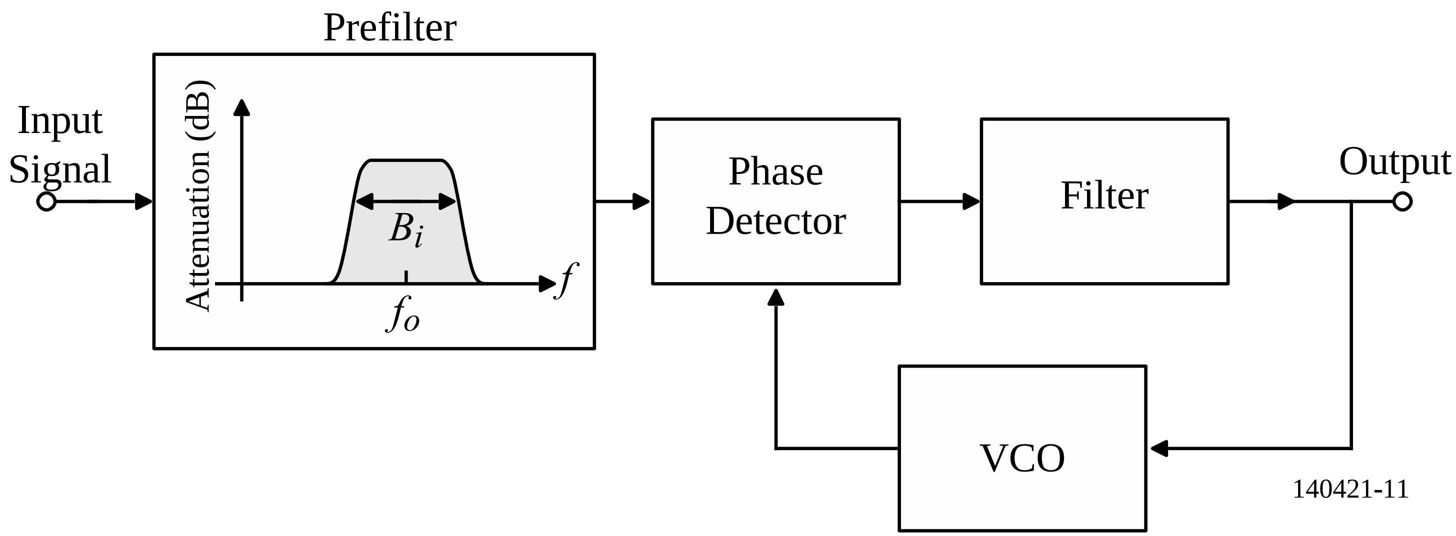
Phase Noise

Illustration:



PLL for Noise Analysis

Assume that the input is band limited as shown below.



B_i = Bandwidth of the prefilter (or system)

Some terminology:

- Power spectral density is the measure of power in a given frequency range (Watts/Hz) or (V^2/Hz). It is found by dividing the rms power by the bandwidth.
- Consider all noise signals as white noise which means the power spectrum is flat.
- P_s = input signal rms power ($V_1(\text{rms})^2/R_{in}$)
- P_n = rms power of the input noise

Power Spectra of a PLL

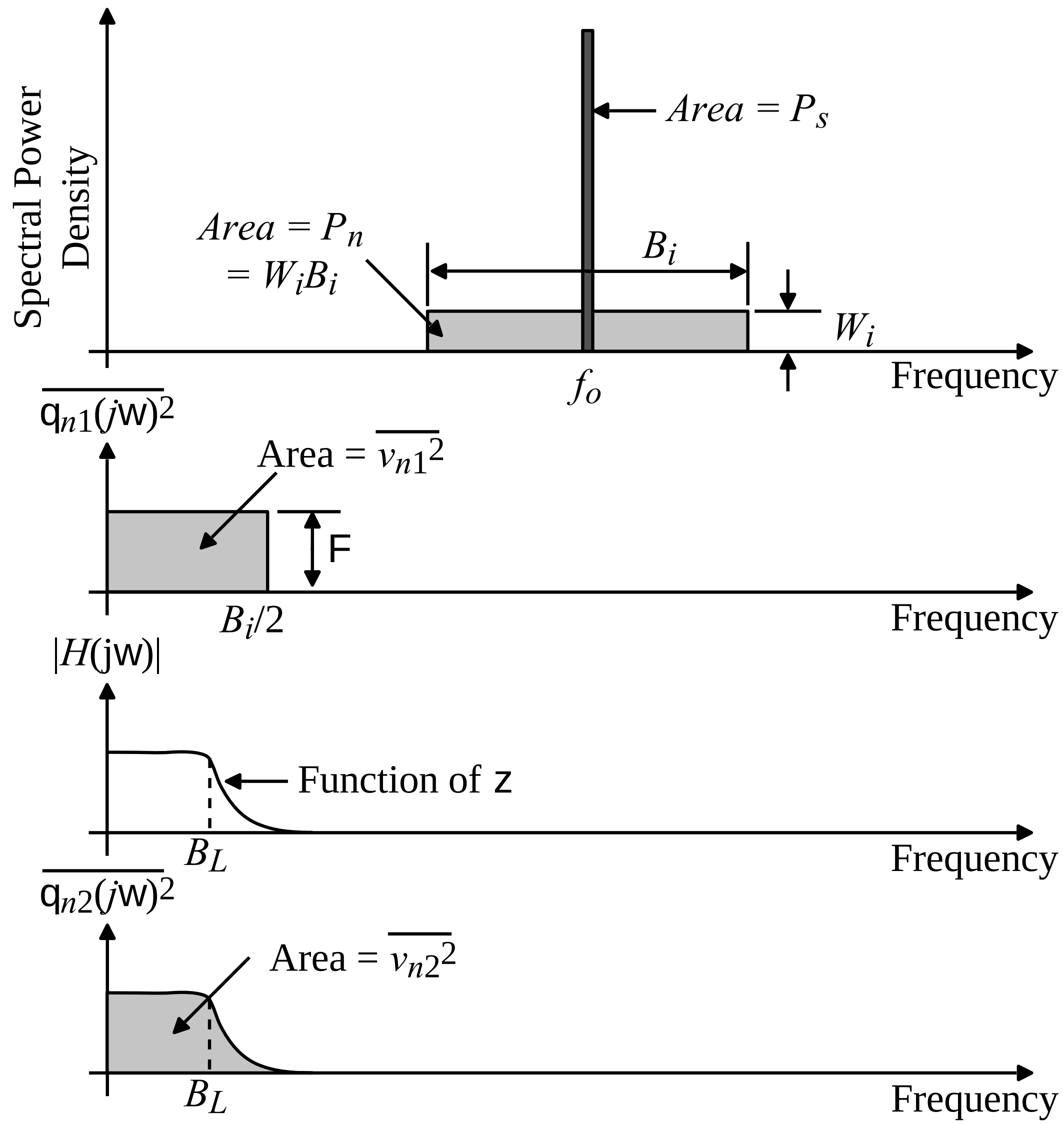
Illustration of how input noise becomes phase noise in the frequency spectrum:

Power spectra of the reference signal, $v_1(t)$, and the superimposed noise signal, $v_n(t)$.

Spectrum of the phase noise at the input of the PLL.

Frequency response of the phase-transfer function, $H(j\omega)$.

Spectrum of the phase noise at the output of the PLL.



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Noise Relationships for a PLL

Spectral density of the input noise signal:

$$W_i = \frac{P_n}{B_i} \text{ (W/Hz)}$$

Input rms phase noise jitter (or the square of the rms phase noise):

$$\theta_{n1}(t) \quad \rightarrow \quad \overline{\theta_{n1}^2} = \frac{P_n}{2P_s} \qquad \text{(Comes from the assumption of white noise)}$$

Signal-to-Noise Ratio (SNR):

$$SNR \text{ at the input} = (SNR)_i \equiv \frac{P_s}{P_n} \rightarrow \qquad \overline{\theta_{n1}^2} = \frac{P_n}{2P_s} = \frac{1}{2(SNR)_i} \text{ (radians}^2\text{)}$$

Input phase jitter (noise) spectrum:

$$\overline{\Theta_{n1}^2(j\omega)} = \Phi = \frac{\overline{\theta_{n1}^2}}{B_i/2} \text{ (radians}^2\text{/Hz)}$$

Output phase jitter (noise) spectrum:

$$\overline{\Theta_{n2}^2(j\omega)} = |H(j\omega)|^2 \, \overline{\Theta_{n1}^2(j\omega)} = |H(j\omega)|^2 \Phi$$

RMS Value of the Output Phase Noise

The output phase noise is found by integrating $\Theta_{n2}(j\omega)$ over the bandwidth of the PLL.

$$\overline{\theta_{n2}^2} = \int_0^{\infty} \overline{\Theta_{n2}^2(j2\pi f)}\, df$$

where $\overline{\theta_{n2}^2}$ is the area under the output phase noise plot in a previous slide.

$$\overline{\theta_{n2}^2} = \int_0^{\infty} \Phi\, |H(j\omega)|^2 df = \frac{\Phi}{2\pi}\int_0^{\infty} |H(j\omega)|^2 d\omega$$

The integral $\int_0^{\infty} |H(j2\pi f)|^2 df = B_L$ is called the noise bandwidth.

The solution of this integral is,

$$B_L = \frac{\omega_n}{2}\left(\zeta + \frac{1}{4\zeta}\right) \rightarrow \frac{dB_L}{d\zeta} = \frac{\omega_n}{2}\left(1 - \frac{1}{2\zeta}\right) = 0 \rightarrow \zeta = 0.5 \rightarrow B_L(\min) = 0.5\omega_n$$

$$\therefore \quad \overline{\theta_{n2}^2} = \Phi\, B_L = \frac{\overline{\theta_{n1}^2}}{B_i/2} B_L = \frac{P_n}{2P_s}\frac{2B_L}{B_i} = \frac{P_n}{P_s}\cdot\frac{B_L}{B_i} = \frac{B_L}{(SNR)_i B_i}$$

RMS Value of the Output Phase Noise – Continued

We noted previously that,

$$\overline{\theta_{n1}^2} = \frac{1}{2(SNR)_i} = \frac{P_n}{2P_s} \qquad \rightarrow \qquad (SNR)_i = \frac{P_s}{P_n}$$

A dual relationship holds for the output,

$$\overline{\theta_{n2}^2} = \frac{1}{2(SNR)_L} = \frac{P_n}{P_s} \cdot \frac{B_L}{B_i} \qquad \rightarrow \qquad (SNR)_L = \frac{P_s}{P_n} \frac{B_i}{2B_L}$$

where $(SNR)_L$ is the signal-to-noise ratio at the output.

$$\therefore \qquad (SNR)_L = (SNR)_i \frac{B_i}{2B_L}$$

This equation suggests that the PLL improves the *SNR* of the input signal by a factor of $B_i/2B_L$. Thus, the narrower the noise PLL bandwidth, B_L, the greater the improvement.

Some experimental observations:

- For $(SNR)_L = 1$, a lock-in process will not occur because the output phase noise is excessive (0.707 radians or 40.4°).
- At an $(SNR)_L = 2$, lock-in is eventually possible (0.5 radians or 28.6°).
- For $(SNR)_L = 4$, stable operation is generally possible.

Note: $(SNR)_L = 4$, $\overline{\theta_{n2}^2}$ becomes 0.125 radians^2. $\sqrt{\overline{\theta_{n2}^2}} = 0.353$ radians $\Rightarrow$ 20° and the limit of dynamic stability (180°) is rarely exceeded.

Summary of Noise Analysis of the LPLL

- Stable operation of the LPLL is possible if $(SNR)_L \geq 4$
- $(SNR)_L$ is calculated from

$$(SNR)_L = \frac{P_s}{P_n}\frac{B_i}{2B_L}$$

where P_s = signal power at the reference input

P_n = noise power at the reference point

B_i = bandwidth of the system at the input

B_L = noise bandwidth of the PLL

- The noise bandwidth, B_L, is a function of ω_n and ζ. For $\zeta = 0.7$, $B_L = 0.53\omega_n$
- The average time interval between two unlocking events gets longer as the $(SNR)_L$ increases.

Pull-In Techniques for Noisy Signals

1.) The sweep technique.

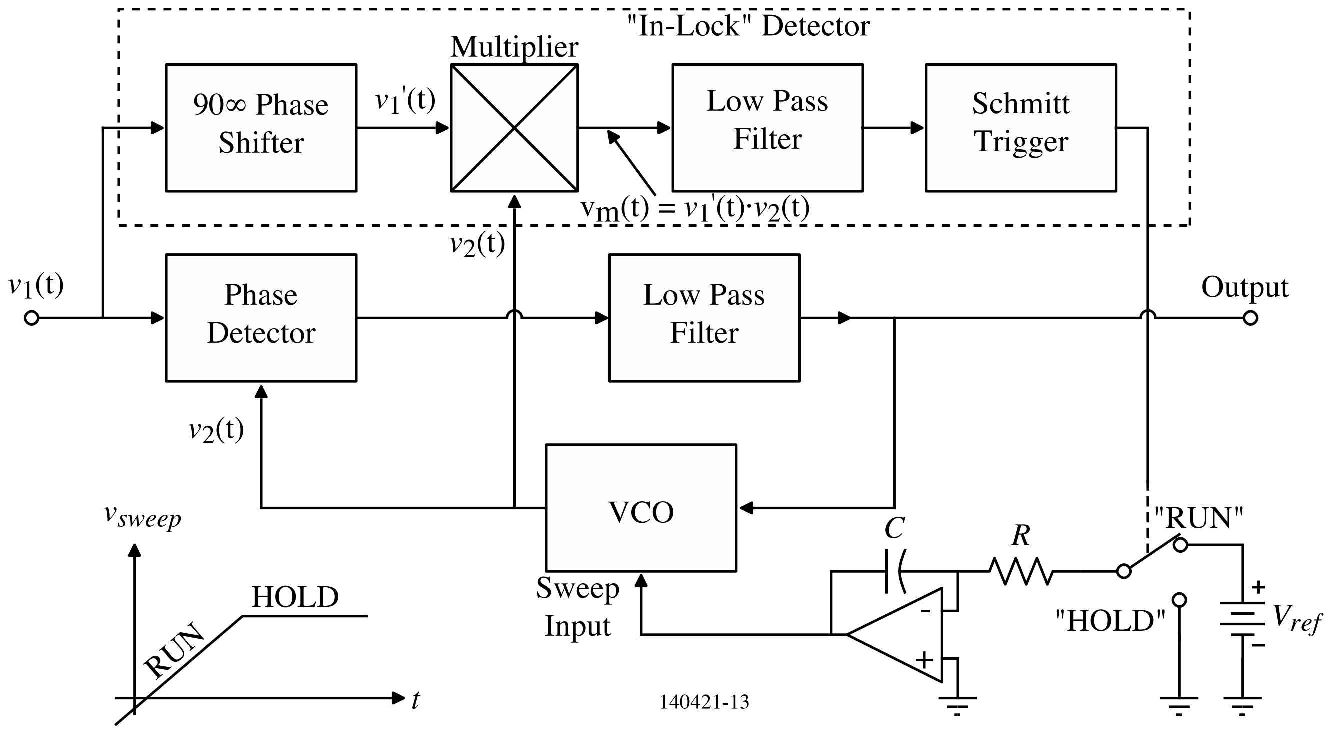
When the noise bandwidth is made small, the *SNR* of the loop is sufficiently large to provide stable operation. However, the lock range can become smaller than the frequency interval $\Delta\omega$ within which the input signal is expected to be. The following circuit solves this problem by providing a direct VCO sweep.

(1.) LPLL not locked.

(2.) RUN mode starts a positive sweep.

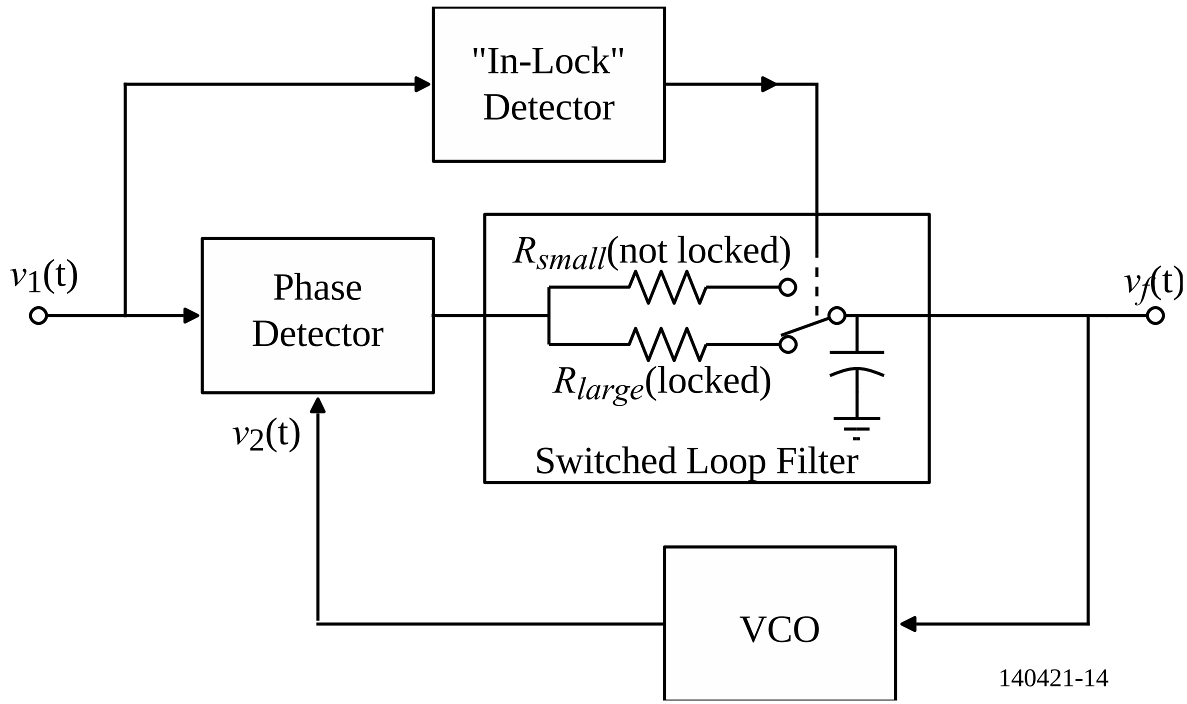
(3.) When the VCO frequency approaches the input frequency the loop locks.

(4.) The “In-Lock” detector switches the sweep switch to the “HOLD” position.



Pull-In Techniques for Noisy Signals

2.) Switched filter technique.



In the unlocked state, the filter bandwidth is large so that lock range exceeds the frequency range within which the input is expected.

In the locked state, the filter bandwidth is reduced in order to reduce the noise.

SUMMARY

- Acquisition process – the PLL in the unlocked state
- Influence of noise on the linear PLL
- Pull-in techniques for noisy signals