LECTURE 1 – CMOS PHASE LOCKED LOOPS
OVERVIEW

Objective
Understand the principles and applications of phase locked loops using integrated circuit technology with emphasis on CMOS technology.

Topics
• Background
• Fundamentals

Organization

![Diagram of PLL components and perspectives]

- Systems Perspective
  - Types of PLLs and PLL Measurements
  - PLL Applications and Examples

- Circuits Perspective
  - PLL Components

- Technology Perspective
  - CMOS Technology
**Suggested References**

Phase Locked Loops:

OPERATING PRINCIPLES OF PLLs

What is a PLL?

A PLL contains three basic components as shown below:

- Phase/frequency detector determines the difference between the phase and/or frequency of two signals.
- The loop filter removes the high-frequencies from the voltage-controlled oscillator (VCO) controlling voltage.
- The VCO produces and output frequency controlled by a voltage.
More Detailed PLL Block Diagram

- $v_{in}(t)$ – The input or reference signal
- $\omega_{in}$ – The radian frequency of the input signal
- $v_{osc}(t)$ – The output of the VCO
- $\omega_{osc}$ – The radian frequency of the VCO
- $v_{d}(t)$ – The detector output voltage = $K_{d}\theta_{e}$
- $\theta_{e}$ – Phase error between $v_{in}(t)$ and $v_{out}(t) = \theta_{in} - \theta_{osc}$
- $v_{c}(t)$ – The output voltage of the loop filter and the control voltage for the VCO
The Phase Detector and VCO in more Detail

Phase Detector:

\[ v_d(t) = K_d \theta_e = K_d (\theta_{in} - \theta_{osc}) \]

where

- \( K_d \) is the gain of the phase detector
- \( \theta_{in} \) = phase shift of the input voltage
- \( \theta_{osc} \) = phase shift of the VCO output voltage

The units of \( K_d \) are volts/radians or simply volts assuming all phase shifts are in radians and not degrees.

Voltage Controlled Oscillator:

\[ \omega_{osc} = \omega_o + K_o \cdot v_c(t) \]

where \( K_o \) is the VCO gain and \( \omega_o \) is the free-running radian frequency.

The units of \( K_o \) are rads/sec·V or simply (sec·V)^{-1} assuming all phase shifts are in radians and not degrees.
PLL Operation

Locked Operation:

• The loop is locked when the frequency of the VCO is exactly equal to the average frequency of the input signal.

• The PLL has the inherent ability to suppress noise superimposed on its input signal.

• To maintain the control voltage needed for locked conditions, it is generally necessary for the output of the phase/frequency detector to be nonzero.

Unlocked Operation:

• The VCO runs at a frequency called the free running frequency, $\omega_o$, which corresponds to zero control voltage.

• The capture process is the means by which the loop goes from unlocked, free-running state to that of the locked state.
Transient Response of the PLL

Assume the input frequency is increased by an amount $\Delta \omega$.

1.) $\omega_{in}$ increases by $\Delta \omega$ at $t_o$.

2.) The input signal leads the VCO and $v_d$ begins to increase.

3.) After a delay due to the loop filter, the VCO increases $\omega_{osc}$.

4.) As $\omega_{osc}$ increases, the phase error reduces.

5.) Depending on the loop filter, the final phase error will be reduced to zero or to a finite value.
## CLASSIFICATION OF PLL TYPES

### Types of PLLs

<table>
<thead>
<tr>
<th>PLL Type</th>
<th>Phase Detector</th>
<th>Loop Filter</th>
<th>Controlled Oscillator</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linear PLL (LPLL)</td>
<td>Analog multiplier</td>
<td>RC passive or active</td>
<td>Voltage</td>
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<tr>
<td>Digital PLL (DPLL)</td>
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</tr>
<tr>
<td>All digital PLL (ADPLL)</td>
<td>Digital detector</td>
<td>Digital filter</td>
<td>Digitally controlled</td>
</tr>
<tr>
<td>Software PLL (SPLL)</td>
<td>Software multiplier</td>
<td>Software filter</td>
<td>Software oscillator</td>
</tr>
</tbody>
</table>

The digital PLL (DPLL) has been the mainstay of most PLLs and is called the “classical” digital PLL.
The Linear PLL (LPLL)

- Uses a analog multiplier for the PDF
- Loop filter is active or passive analog
- VCO is analog
**The Digital PLL (DPLL)**

- Phase detector is digital
- Loop filter is passive of active analog
- VCO is analog
- Called the “Classical Digital PLL”
The All-Digital PLL (ADPLL)

- Phase detector is digital
- Loop filter is digital
- VCO is digital
- Compatible with modern CMOS technology
The Software PLL (SPLL)

- Phase detector is implemented in software
- Loop filter is implemented in software
- Oscillator is implemented in software driven by an external clock
- Requires analog to digital conversion at the input and digital to analog conversion at the output
- Software permits reconfiguring of the PLL
SYSTEMS PERSPECTIVE OF LINEAR PHASE LOCK LOOPS (LPLLs)

Introduction

Objective:
Understand the operating principles and classification of LPLLs.

Organization:
Outline
• LPLL Blocks
• Locked State
• Order of the LPLL System
• The Acquisition Process - Unlocked State
• Noise in the LPLL
• LPLL System Design
• Simulation of LPLLs
### LPLL BLOCKS

**Building Blocks of the LPLL**

- $v_1(t) = \text{Input signal, generally sinusoidal}$
- $v_2(t) = \text{VCO output signal, may be sinusoidal or square wave}$
- $v_d(t) = \text{Phase detector output signal}$
- $v_f(t) = \text{Loop filter output signal and controlling signal to the VCO}$
- $\omega_1 = \text{Frequency of the input signal}$
- $\omega_2 = \text{Frequency of the VCO}$
**Loop Filters**

In the PLL, there are many high frequencies including noise that must be removed by the use of a low pass filter in order to achieve optimum performance.

Types of Loop Filters:

1.) Passive lag filter (*lag-lead*)

\[ F(s) = \frac{1 + s \tau_2}{1 + s(\tau_1 + \tau_2)} \]

where \( \tau_1 = R_1 C \) and \( \tau_2 = R_2 C \)

Pole is at \( 1/(\tau_1 + \tau_2) \) and the zero at \( 1/\tau_2 \).

- Since the pole is smaller than the zero, the filter is lag-lead
- Passive filters should have no amplitude nonlinearity
Loop Filters - Continued

2.) Active Lag filter

\[ F(s) = K_a \frac{1 + s \tau_2}{1 + s \tau_1} \]

where \( \tau_1 = R_1 C_1 \), \( \tau_2 = R_2 C_2 \) and \( K_a = -\frac{C_1}{C_2} \)

- Easier to make lead-lag
- Can have gain (not necessarily desirable)
- Limited by the linearity and noise of the op amp
Loop Filters - Continued

3.) Active Proportional-Integral (PI) Filter

\[ F(s) = \frac{1 + s\tau_2}{s\tau_1} \quad \text{where} \quad \tau_1 = R_1C \quad \text{and} \quad \tau_2 = R_2C \]

- Has large open loop gain at low frequencies ⇒ Large hold range
- Limited by the linearity and noise of the op amp
- Gain limits at the op amp open loop gain

Stability:

To keep the loop stable, it is important to pick the loop filter so that it does not introduce more than a 90° phase shift in the loop.
**Phase Signals**

It is important to remember that frequency and phase are related as

\[ \frac{d\theta}{dt} = \omega \quad \rightarrow \quad \theta = \int \omega \cdot dt \]

Transfer functions:

\[ H(s) = \frac{V_2(s)}{V_1(s)} \]

where \( V_2(s) \) and \( V_1(s) \) are the Laplace transforms of \( v_2(t) \) and \( v_1(t) \).

To examine phase signals, let us assume that,

\[ v_1(t) = V_{10} \sin[\omega_1 t + \theta_1(t)] \quad \text{and} \quad v_2(t) = V_{20} \sin[\omega_2 t + \theta_2(t)] \]

For phase signals, the information is carried only in \( \theta(t) \).

Next, we consider some simple phase signals that are used to excite a PLL.
Phase Signals – Continued

1.) A step phase shift which is an example of phase modulation.

\[ \theta_1(t) = \Delta \Phi \ u(t) \]

2.) A step frequency change assuming that \( \omega_1(t) = \omega_0 \) for \( t < 0 \). We may express \( v_1(t) \) as,

\[
v_1(t) = V_{10} \sin[\omega_0 t + \Delta \omega \cdot t]
\]

\[
= V_{10} \sin[\omega_0 t + \theta_1(t)]
\]

\[ \therefore \quad \theta_1(t) = \Delta \omega \cdot t \]

(the phase becomes a ramp signal)
Phase Signals – Continued

3.) Frequency ramp

\[
\omega_1(t) = \omega_o + \Delta \omega \cdot t
\]

where \( \Delta \omega \) is the rate of change of the angular frequency.

\[
\therefore \quad v_1(t) = V_{10} \sin \left[ \int_{0}^{t} (\omega_o + \Delta \omega \tau) d\tau \right]
\]

\[
= V_{10} \sin \left( \omega_o t + \Delta \omega \frac{t^2}{2} \right)
\]

\[
\theta_1(t) = \Delta \omega \frac{t^2}{2}
\]
SUMMARY

- LPLL blocks are:
  1. Multiplying phase detector
  2. Low pass filter
  3. Voltage controlled oscillator
- Locked state: Input frequency = VCO frequency
  - The phase response is low pass
  - The phase error response is high pass