CHAPTER 4 – CMOS SUBCIRCUITS

Chapter Outline

Goal

To develop an understanding of the sub-blocks and subcircuits used in CMOS analog circuit design.

Design Hierarchy

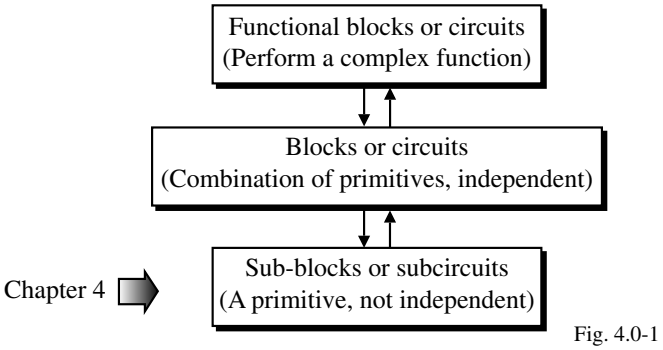

Fig. 4.0-1

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Illustration of Hierarchy in Analog Circuits for an Op Amp

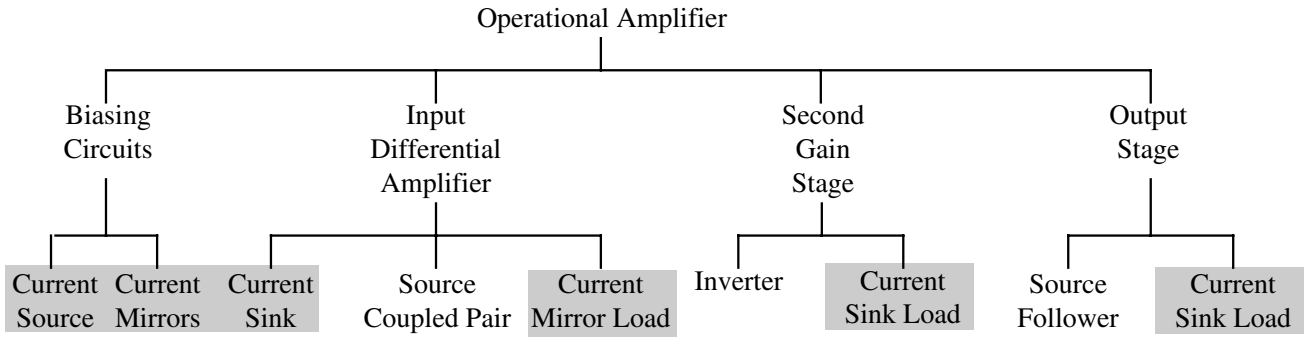

Fig. 4.0-2

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SECTION 4.1 - MOS SWITCH

Model for a Switch

- An ideal switch is a short-circuit when ON and an open-circuit when OFF.

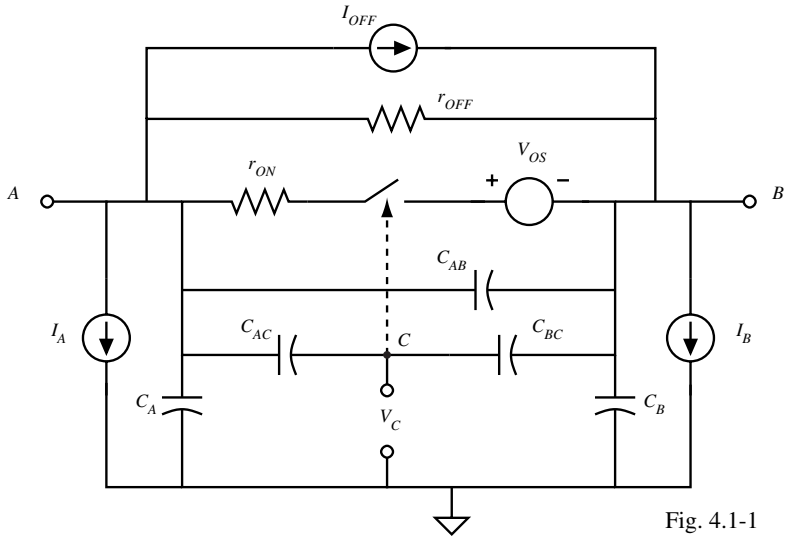

Fig. 4.1-1

- Actual switch:

V_C = controlling terminal for the switch (V_C high $\Rightarrow$ switch ON, V_C low $\Rightarrow$ switch OFF)

r_{on} = resistance of the switch when ON r_{off} = resistance of the switch when OFF

V_{OS} = offset voltage when the switch is ON I_{off} = offset current when the switch is OFF

I_A and I_B are leakage currents to ground C_A and C_B are capacitances to ground

C_{AC} and C_{BC} = parasitic capacitors between the control terminal and switch terminals

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MOS Transistor as a Switch

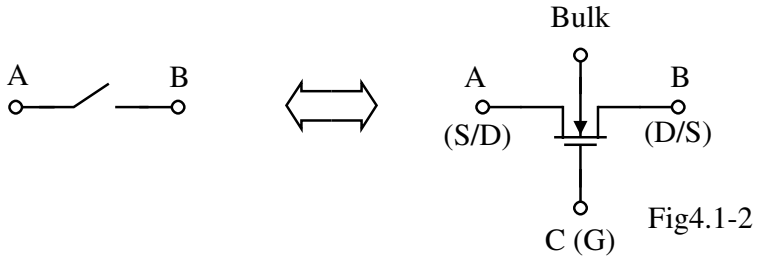

Fig4.1-2

On Characteristics of a MOS Switch

Assume operation in active region ($v_{DS} < v_{GS} - V_T$) and v_{DS} small.

$$i_D = \frac{\mu C_{ox} W}{L}\left[(v_{GS} - V_T) - \frac{v_{DS}}{2}\right]v_{DS} \approx \frac{\mu C_{ox} W}{L}(v_{GS} - V_T)v_{DS}$$

Thus,

$$R_{ON} \approx \frac{v_{DS}}{i_D} = \frac{1}{\frac{\mu C_{ox} W}{L}(v_{GS} - V_T)}$$

OFF Characteristics of a MOS Switch

If $v_{GS} < V_T$, then $i_D = I_{OFF} = 0$ when $v_{DS} \approx 0$V.

If $v_{DS} > 0$, then

$$R_{OFF} \approx \frac{1}{i_D \lambda} = \frac{1}{I_{OFF}\lambda} \approx \infty$$

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MOS Switch Voltage Ranges

If a MOS switch is used to connect two circuits that can have analog signal that vary from 0 to 1V, what must be the value of the bulk and gate voltages for the switch to work properly?

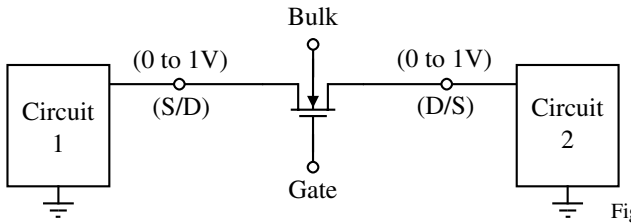

Fig.4.1-3

- To insure that the bulk-source and bulk-drain pn junctions are reverse biased, the bulk voltage must be less than the minimum analog signal for a NMOS switch.
- To insure that the switch is on, the gate voltage must be greater than the maximum analog signal plus the threshold for a NMOS switch.

Therefore:

$$V_{Bulk} \leq 0V$$

and $$V_{Gate}(\text{on}) > 1V + V_T$$

Also, $$V_{Gate}(\text{off}) \leq 0V$$

Unfortunately, the large value of reverse bias bulk voltage causes the threshold voltage to increase.

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Current-Voltage Characteristics of a NMOS Switch

The following simulated output characteristics correspond to triode operation of the MOSFET.

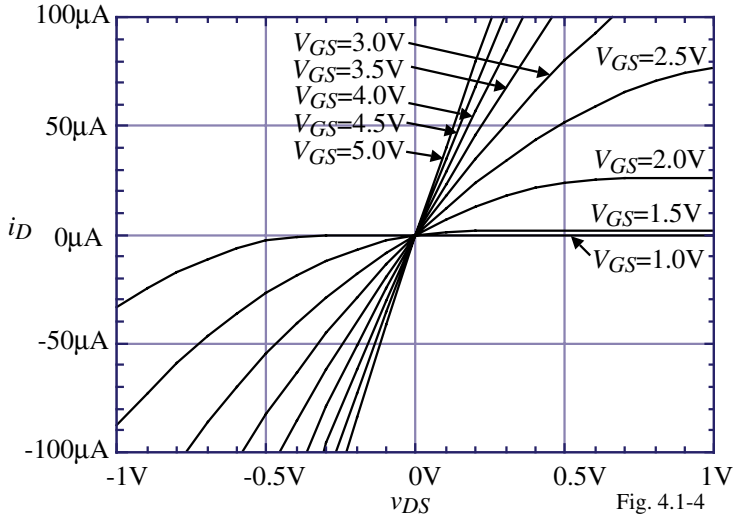

Fig. 4.1-4

SPICE Input File:

```
MOS Switch On Characteristics
M1 1 2 0 3 MNMOS W=1U L=1U
.MODEL MNMOS NMOS VTO=0.7, KP=110U,
+LAMBDA=0.04, GAMMA=0.4 PHI=0.7
VDS 1 0 DC 0.0
VGS 2 0 DC 0.0
VBS 3 0 DC -5.0
.DC VDS -1 1 0.1 VGS 1 5 0.5
.PRINT DC ID(M1)
.PROBE
.END
```

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MOS Switch ON Resistance as a Function of Gate-Source Voltage

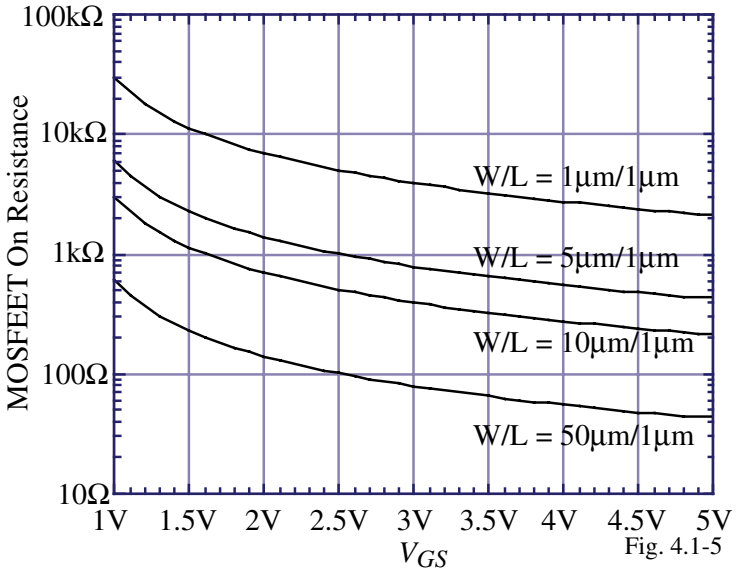

Fig. 4.1-5

SPICE Input File:

```
MOS Switch On Resistance as a f(W/L)
M1 1 2 0 0 MNMOS W=1U L=1U
M2 1 2 0 0 MNMOS W=5U L=1U
M3 1 2 0 0 MNMOS W=10U L=1U
M4 1 2 0 0 MNMOS W=50U L=1U
.MODEL MNMOS NMOS VTO=0.7, KP=110U,
+LAMBDA=0.04, GAMMA=0.4, PHI=0.7
VDS 1 0 DC 0.001V
VGS 2 0 DC 0.0
.DC VGS 1 5 0.1
.PRINT DC ID(M1) ID(M2) ID(M3)
ID(M4)
.PROBE
.END
```

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Influence of the ON Resistance on MOS Switches

Finite ON Resistance:

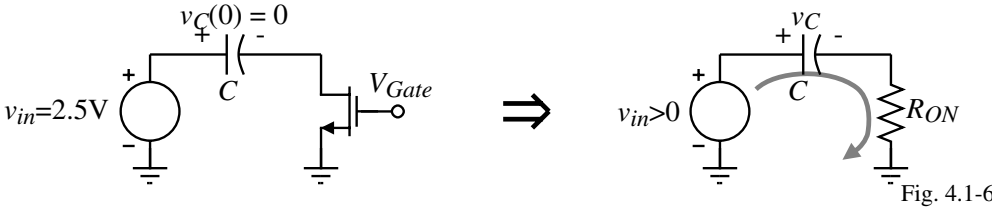

Fig. 4.1-6

Example

Initially assume the capacitor is uncharged. If V_{Gate}(ON) is 5V and is high for 0.1µs, find the W/L of the MOSFET switch that will charge a capacitance of 10pF in five time constants.

Solution

The time constant must be 100ns/5 = 20ns. Therefore R_{ON} must be less than 20ns/10pF = 2kΩ. The ON resistance of the MOSFET (for small v_{DS}) is

$$R_{ON} = \frac{1}{K_N'(W/L)(V_{GS}-V_T)} \Rightarrow \frac{W}{L} = \frac{1}{R_{ON}\cdot K_N'(V_{GS}-V_T)} = \frac{1}{2\text{k}\Omega\cdot 110\mu\text{A/V}^2\cdot 4.3} = 1.06$$

Comments:

- It is relatively easy to charge on-chip capacitors with minimum size switches.
- Switch resistance is really not constant during switching and the problem is more complex than above.

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Including the Influence of the Varying On Resistance

Gate-source Constant

$$g_{ON}(t) = \frac{K'W}{L}[(v_{GS}(t)-V_T) - 0.5v_{DS}(t)]$$

$$g_{ON}(\text{aver.}) = \frac{1}{r_{ON}(\text{aver.})} \approx \frac{g_{ON}(0) + g_{ON}(\infty)}{2}$$

$$= \frac{K'W}{2L}(V_{GS}-V_T) - \frac{K'WV_{DS}(0)}{4L} + \frac{K'W}{2L}(V_{GS}-V_T)$$

$$= \frac{K'W}{L}(V_{GS}-V_T) - \frac{K'WV_{DS}(0)}{4L}$$

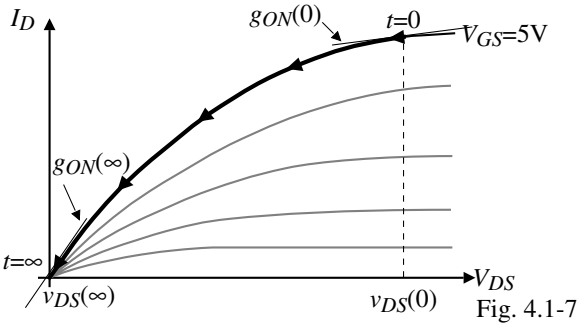
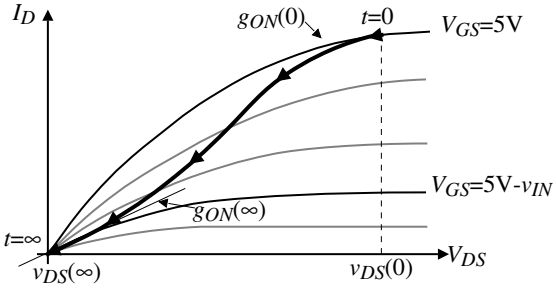


Fig. 4.1-7

Gate-source Varying



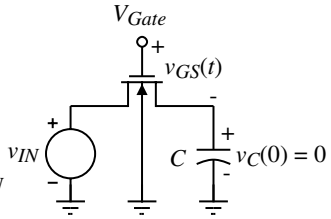


Fig. 4.1-8

$$g_{ON} = \frac{K'W}{2L}[V_{GS}(0)-V_T] - \frac{K'WV_{DS}(0)}{4L} + \frac{K'W}{2L}[V_{GS}(\infty)-v_{IN}-V_T]$$

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Example 4.1-1 - Switch ON Resistance

Assume that at $t = 0$, the gate of the switch shown is taken to 5V. Design the W/L value of the switch to discharge the C_1 capacitor to within 1% of its initial charge in 10ns. Use the MOSFET parameters of Table 3.1-2.

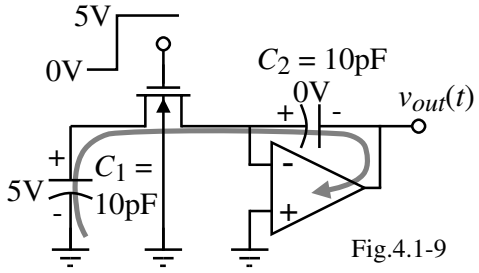

Fig.4.1-9

Solution

Note that the source of the NMOS is on the right and is always at ground potential so there is no bulk effect as long as the voltage across C_1 is positive. The voltage across C_1 can be expressed as

$$v_{C1}(t) = 5\exp\left(\frac{-t}{R_{ON}C_1}\right)$$

At 10ns, v_{C1} is 5/100 or 0.05V. Therefore,

$$0.05=5\exp\left(\frac{-10^{-8}}{R_{ON}10^{-11}}\right) = 5\exp\left(\frac{-10^3}{R_{ON}}\right) \Rightarrow \exp(G_{ON}10^3)=100 \Rightarrow G_{ON} = \frac{ln(100)}{10^3}=0.0046\text{S}$$

$$\therefore\ 0.0046 = \frac{K'W}{L}(V_{GS}-V_T) - \frac{K'WV_{DS}(0)}{4L} = \left(110\text{x}10^{-6}\cdot 4.3 - \frac{110\text{x}10^{-6}\cdot 5}{4}\right)\frac{W}{L} = 356\text{x}10^{-6}\frac{W}{L}$$

Thus, $\frac{W}{L} = \frac{0.0046}{356\text{x}10^{-6}} = 13.71 \approx 14$

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Influence of the OFF State on MOS Switches

The OFF state influence is primarily in any current that flows from the terminals of the switch to ground.

An example might be:

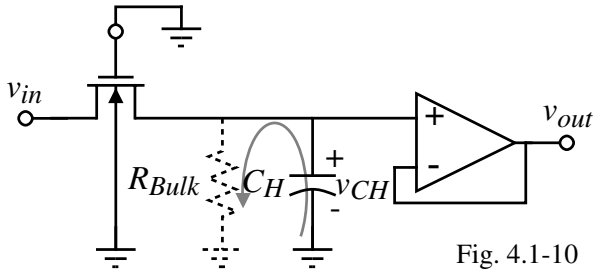

Fig. 4.1-10

Typically, no problems occur unless capacitance voltages are held for a long time. For example,

$$v_{out}(t) = v_{CH}\, e^{-t/(R_{Bulk}C_H)}$$

If $R_{Bulk} \approx 10^9\Omega$ and $C_H = 10\text{pF}$, the time constant is $10^9 \cdot 10^{-11} = 0.01\text{seconds}$

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Influence of Parasitic Capacitances

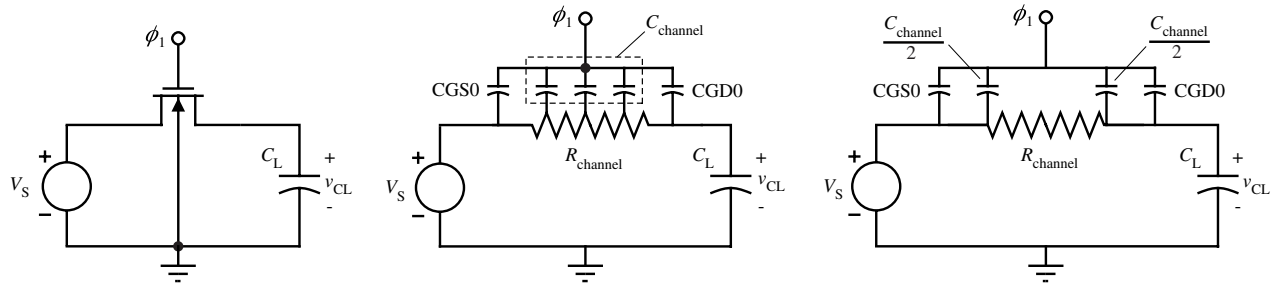
The parasitic capacitors have two influences:

- Parasitics to ground at the switch terminals (C_{BD} and C_{BS}) add to the value of the desired capacitors.

  This problem is solved by the use of stray-insensitive switched capacitor circuits
- Parasitics from gate to source and drain cause charge injection onto or off the desired capacitors.

  This problem can be minimized but not eliminated.

Model for studying charge injection:



A simple switch circuit useful for studying charge injection.

A distributed model of the transistor switch.

A lumped model of the transistor switch.

Fig. 4.1-11

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Charge Injection (Clock feedthrough, Charge feedthrough)

Charge injection is a complex analysis which is better suited for computer analysis. Here we will attempt to develop an understanding sufficient to show ways of reducing the effect of charge injection.

What is Charge Injection?

1.) When the voltages change across the gate-drain and gate-source capacitors, a current will flow because $i = C\frac{dv}{dt}$.

2.) When the switch is off, charge injection will appear on the external capacitors (C_L) connected to the switch terminals causing their voltages to change.

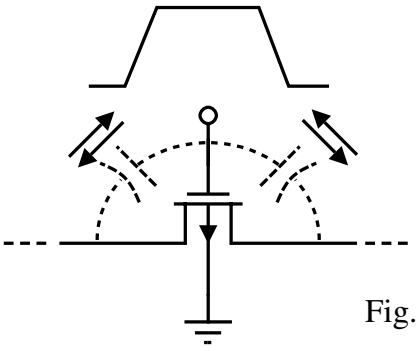

Fig. 4.1-12

There are two cases of charge injection depending upon the transition rate when the switch turns off.

1.) Slow transition time.

2.) Fast transition time.

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Slow Transition Time

Consider the following switch circuit:

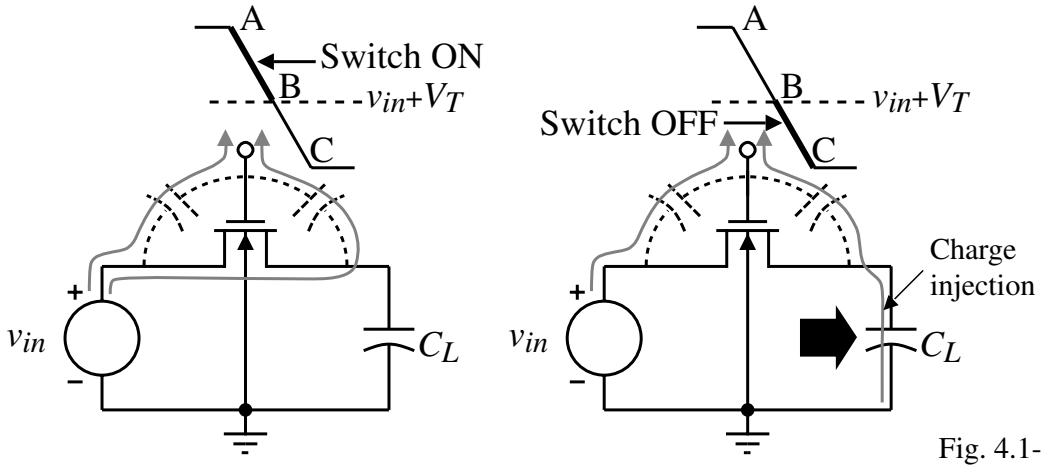

Fig. 4.1-13

1.) During the on-to-off transition time from A to B, the charge injection is absorbed by the low impedance source, v_{in}.

2.) The switch turns off when the gate voltage is $v_{in}+V_T$ (point B).

3.) From B to C the switch is off but the gate voltage is changing. As a result charge injection occurs to C_L.

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Fast Transition Time

For the fast transition time, the rate of transition is faster than the channel time constant so that some of the charge during the region from point A to point B is injected onto C_L even though the transistor switch has not yet turned off.

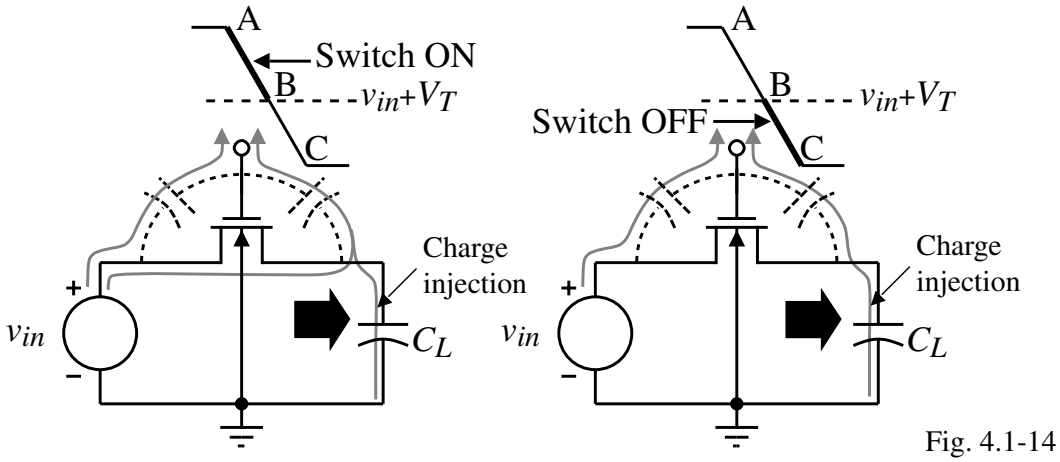

Fig. 4.1-14

A Quantized Model of Charge Injection[†]

Approximate the gate transition as a stair case and discretize in voltage as follows:

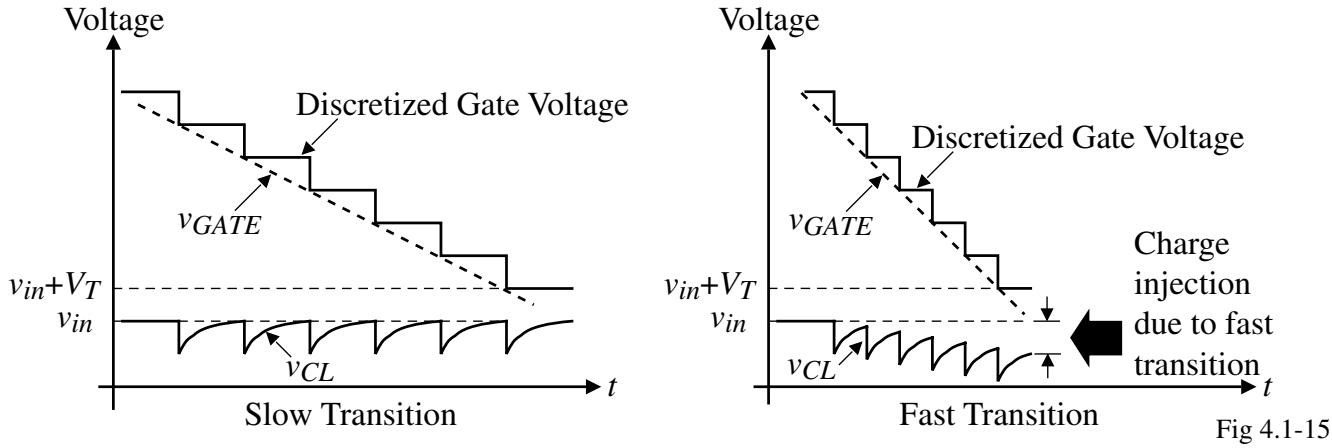

Fig 4.1-15

The time constant of the channel, $R_{channel} \cdot C_{channel}$, determines whether or not the capacitance, C_L, fully charges during each voltage step.

[†] B.J. Sheu and C. Hu, "Switched-Induced Error Voltage on A Switched Capacitor," *IEEE J. Solid-State Circuits*, Vol. SC-19, No. 4, pp. 519-525, August 1984.

Analytical Expressions to Approximate Charge Injection

Assume the gate voltage is making a transition from high, V_H, to low, V_L.

$\therefore \quad v_{Gate} = v_G(t) = V_H - Ut$

where U = magnitude of the slope of $v_G(t)$

Define $V_{HT} = V_H - V_S - V_T$ and $\beta = \frac{K'W}{L}$.

The error in voltage across C_L, V_{error}, is given below in two terms. The first term corrsponds to the feedthrough that occurs while the switch is still on and the second term corresponds to feedthrough when the switch is off.

1.) Slow transition occurs when $\frac{\beta V_{HT}^2}{2C_L} >> U$.

$$V_{error} = -\left(\frac{W\cdot CGD0 + \frac{C_{channel}}{2}}{C_L}\right)\sqrt{\frac{\pi U C_L}{2\beta}} - \frac{W\cdot CGD0}{C_L}(V_S+2V_T-V_L)$$

2.) Fast transition occurs when $\frac{\beta V_{HT}^2}{2C_L} << U$.

$$V_{error} = -\left(\frac{W\cdot CGD0 + \frac{C_{channel}}{2}}{C_L}\right)\left(V_{HT} - \frac{\beta V_{HT}^3}{6U\cdot C_L}\right) - \frac{W\cdot CGD0}{C_L}(V_S+2V_T-V_L)$$

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Expression for Feedthrough when the Switch is OFF

The model for this case is given as:

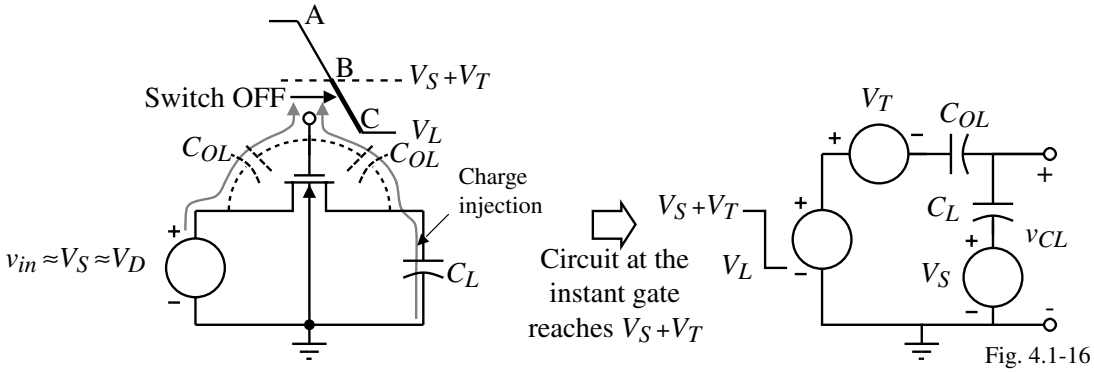

Fig. 4.1-16

The switch decrease from B to C is modeled as a negative step of magnitude $V_S+V_T-V_L$.

The output voltage on the capacitor after opening the switch is,

$$v_{CL} = \left(\frac{C_L}{C_{OL}+C_L}\right)V_S - \left(\frac{C_{OL}}{C_{OL}+C_L}\right)V_T - (V_S+V_T-V_L)\left(\frac{C_{OL}}{C_{OL}+C_L}\right) \approx V_S - (V_S+2V_T-V_L)\left(\frac{C_{OL}}{C_L}\right)$$

if $C_{OL} < C_L$.

Therefore, the error voltage is

$$V_{error} \approx -(V_S + 2V_T - V_L)\left(\frac{C_{OL}}{C_L}\right) = -(v_{in} + 2V_T - V_L)\left(\frac{C_{OL}}{C_L}\right)$$

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Example 4.1-2 - Calculation of Charge Feedthrough Error

Calculate the effect of charge feedthrough on the previous circuit where $V_S = 1V$, $C_L = 200fF$, $W/L = 0.8\mu m/0.8\mu m$, and V_G is given below for the two cases. Use model parameters from Tables 3.1-2 and 3.2-1. Neglect ΔL and ΔW effects.

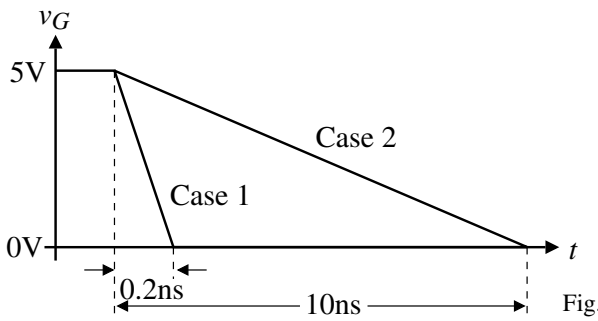

Fig. 4.1-17

Solution

Case 1:

The value of U is equal to 5V/0.2nS or $25x10^9$. Next we must test to see if the slow or fast transition time is appropriate. First calculate the value of V_T as

$$V_T = V_{T0} + \gamma\sqrt{2|\phi_F| - V_{BS}} - \gamma\sqrt{2|\phi_F|} = 0.7 + 0.4\sqrt{0.7+1} - 0.4\sqrt{0.7} = 0.887V$$

Therefore,

$$V_{HT} = V_H - V_S - V_T = 5-1-0.887 = 3.113V \Rightarrow \frac{\beta V_{HT}^2}{2C_L} = \frac{110x10^{-6}\cdot 3.113^2}{2\cdot 200fF} = 2.66x10^9 < 25x10^9$$

which corresponds to the fast transition case. Using the previous expression gives,

$$V_{error} = -\left(\frac{176x10^{-18}+0.5(1.58x10^{-15})}{200x10^{-15}}\right)\left(3.113-\frac{3.32x10^{-3}}{30x10^{-3}}\right) - \frac{176x10^{-18}}{200x10^{-15}}(1+1.774-0) = -16.94mV$$

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Example 4.1-2- Continued

Case 2:

In this case U is equal to 5V/10ns or $5x10^8$ which means that the slow transition case is valid ($5x10^8 < 2.66x10^9$).

Using the previous expression gives,

$$V_{error} = -\left(\frac{176x10^{-18}+0.5(1.58x10^{-15})}{200x10^{-15}}\right)\left(\sqrt{\frac{314x10^{-6}}{220x10^{-6}}}\right) - \frac{176x10^{-18}}{200x10^{-15}}(1+1.774-0) = -8.21mV$$

Comment:

These results are not expected to give precise answers regarding the amount of charge feedthrough one should expect in an actual circuit. Rather, they are a guide to understand the effects of various circuit elements and terminal conditions in order to minimize unwanted behavior by design techniques.

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Solutions to Charge Injection

1.) Use minimum size switches to reduce the overlap capacitances and/or increase C_L.

2.) Use a dummy compensating transistor.

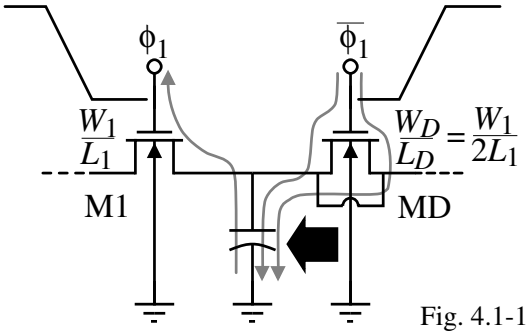

Fig. 4.1-19

- Requires complementary clocks
- Complete cancellation is difficult and may in fact may make the feedthrough worse

3.) Use complementary switches (transmission gates)

4.) Use differential implementation of switched capacitor circuits (probably the best solution)

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Input-Dependent Charge Injection

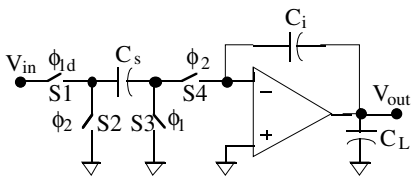
Examination of the error voltage reveals that,

Error voltage = Component independent of input + Component dependent on input

This only occurs for switches that are floating and is due to the fact that the input influences the voltage at which the transistor switches ($v_{in} \approx V_S \approx V_D$). Leads to spurious responses and other undesired results.

Solution:

Use delayed clocks to remove the input-dependence by breaking the current path for injection from the floating switches.



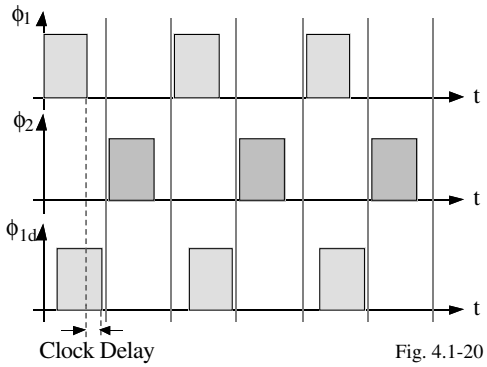


Fig. 4.1-20

Assume that C_s is charged to V_{in} (both ϕ_1 and ϕ_{1d} are high):

1.) ϕ_1 opens, no input-dependent feedthrough because switch terminals (S3) are at ground potential.

2.) ϕ_{1d} opens, no feedthrough occurs because there is no current path (except through small parasitic capacitors).

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CMOS Switches (Transmission Gate)

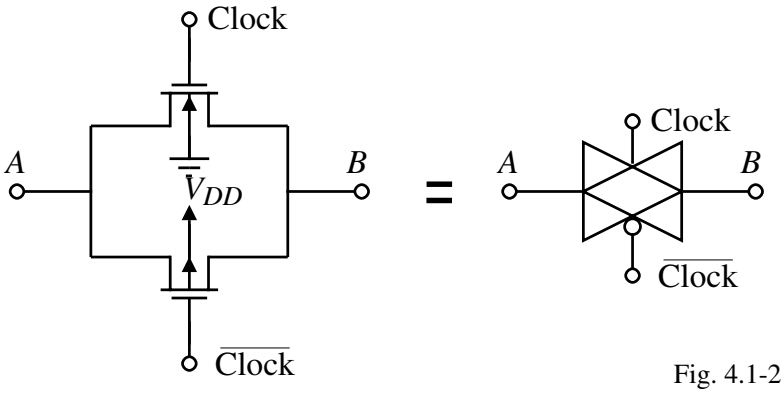

Fig. 4.1-21

Advantages:

- Feedthrough somewhat diminished
- Larger dynamic range
- Lower ON resistance

Disadvantages:

- Requires a complementary clock
- Requires more area

Example 4.1-3 - Charge Injection for a CMOS Switch

Calculate the effect of charge feedthrough on the circuit shown below. Assume that U = 5V/50ns = 10^8V/s, v_{in} = 2.5V and ignore the bulk effect. Use the model parameters from Tables 3.1-2 and 3.2-1.

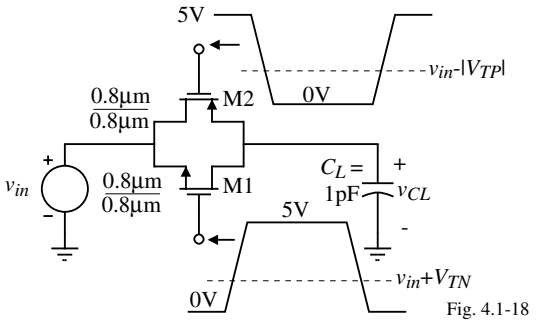

Fig. 4.1-18

Solution

First we must identify the transition behavior. For the NMOS transistor we have

$$\frac{\beta_N V_{HTN}^2}{2C_L} = \frac{110\text{x}10^{-6}\cdot(5\text{-}2.5\text{-}0.7)^2}{2\cdot 10^{-12}} = 1.78\text{x}10^8$$

For the PMOS transistor, noting that

$$V_{HTP} = V_S - |V_{TP}| - V_L = 2.5\text{-}0.7\text{-}0 = 1.8$$

we have $\frac{\beta_P V_{HTP}^2}{2C_L} = \frac{50\text{x}10^{-6}\cdot(1.8)^2}{2\cdot 10^{-12}} = 8.10\text{x}10^7$. Thus, the NMOS transistor is in the slow transition and the PMOS transistor is in the fast transition regimes.

Error due to NMOS:

$$V_{error}(\text{NMOS}) = -\left(\frac{176\text{x}10^{-18} + 0.5(1.58\text{x}10^{-15})}{10^{-12}}\right)\sqrt{\frac{\pi\cdot 10^8\cdot 10^{-12}}{2\cdot 110\text{x}10^{-6}}} - \frac{176\text{x}10^{-18}}{10^{-12}}(2.5+1.4-0)$$

$$= -1.840\text{mV}$$

Example 4.1-3 - Continued

Error due to PMOS:

$$V_{error}(\text{PMOS}) = \left(\frac{176\text{x}10^{-18}+0.5(1.58\text{x}10^{-15})}{10^{-12}}\right)\left(1.8-\frac{50\text{x}10^{-6}(1.8)^3}{6\cdot10^{8}\cdot10^{-12}}\right)+\frac{176\text{x}10^{-18}}{10^{-12}}(5+1.4-2.5)$$

$$= 1.956\text{mV}$$

Net error voltage due to charge injection is 116μV. This will vary with V_S.

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Dynamic Range of the CMOS Switch

The dynamic range of a switch is the range of voltages at the switch terminals ($V_A \approx V_B = V_{A,B}$) over which the ON resistance stays reasonably small.

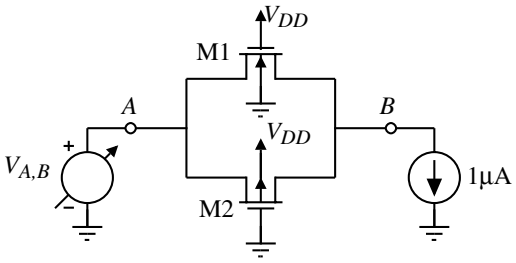

Fig. 4.1-22

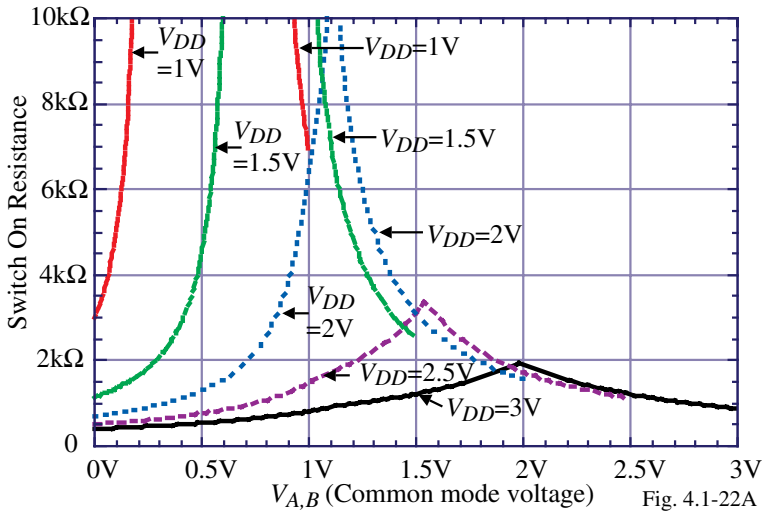

Fig. 4.1-22A

Spice File:

```
Simulation CMOS transmission switch resistance
M1 1 3 2 0 MNMOS L=1U W=10U
M2 1 0 2 3 MPMOS L=1U W=10U
.MODEL MNMOS NMOS VTO=0.7, KP=110U,
+LAMBDA=0.04, GAMMA=0.4, PHI=0.7
.MODEL MPMOS PMOS VTO=-0.7, KP=50U,
+ LAMBDA=0.05, GAMMA=0.5, PHI=0.8
VDD 3 0
VAB 1 0
IA 2 0 DC 1U
.DC VAB 0 3 0.02 VDD 1 3 0.5
.PRINT DC V(1,2)
.END
```

Result:

Low ON resistance over a wide voltage range is difficult as the power supply decreases.

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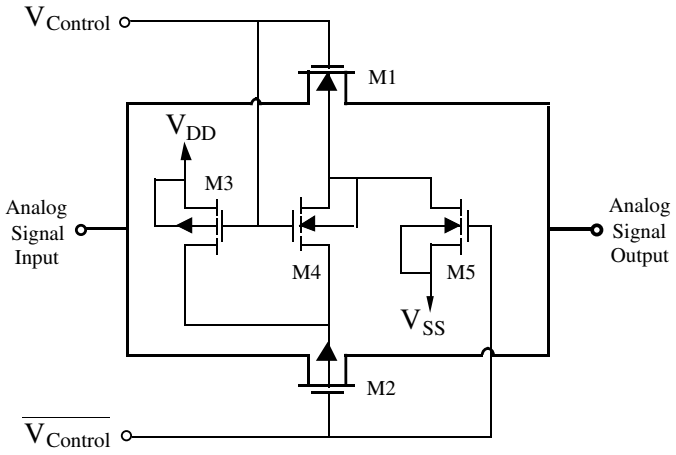
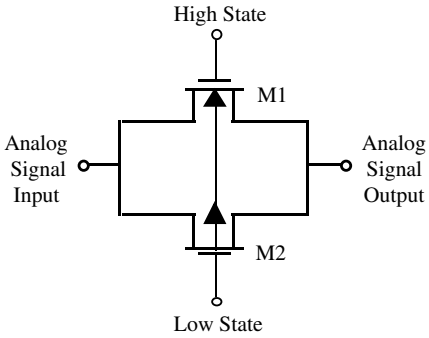
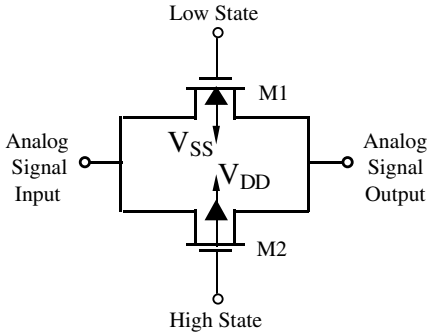
CMOS Switch with Twin-Well Switching



Circuit when $V_{Control}$ is in its high state.



Circuit when $V_{Control}$ is in its low state.



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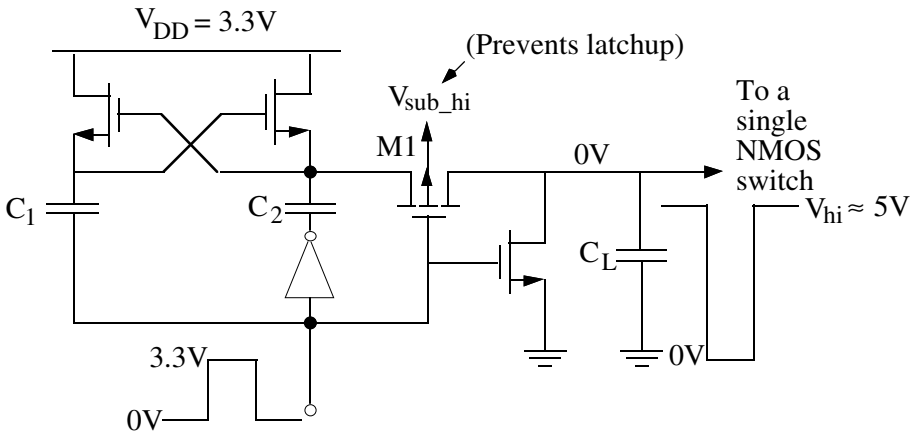
Charge Pumps for Switches with Low Power Supply Voltages

As power supply voltages decrease below 3V, it becomes difficult to keep the switch on at a low value of on-resistance over the range of the power supply. Consequently, charge pumps are used.

Charge pump circuit:



$$V_{hi} = 2V_{DD} \cdot \frac{C_2}{C_{gate,NMOS\ switch} + C_2 + C_L}$$

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Charge Pump - Continued

High voltage generator for the well of M1:

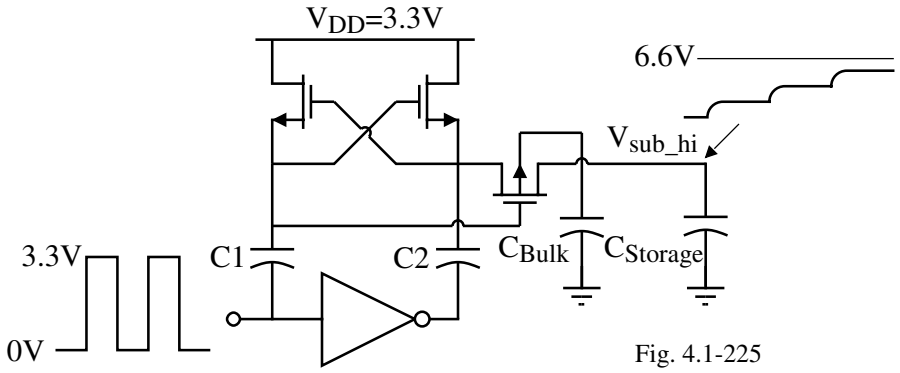

Fig. 4.1-225

Prevents latch-up of M1 by providing a high bulk bias (6.6V).

Use a separate clock driver for each switch to avoid crosstalk through the gate clock lines. Area for layout can be small.

Simulation of the Charge Pump Circuit†

Circuit:

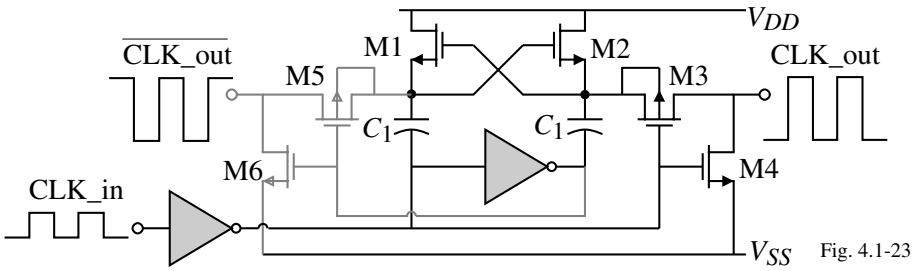

Fig. 4.1-23

Simulation:

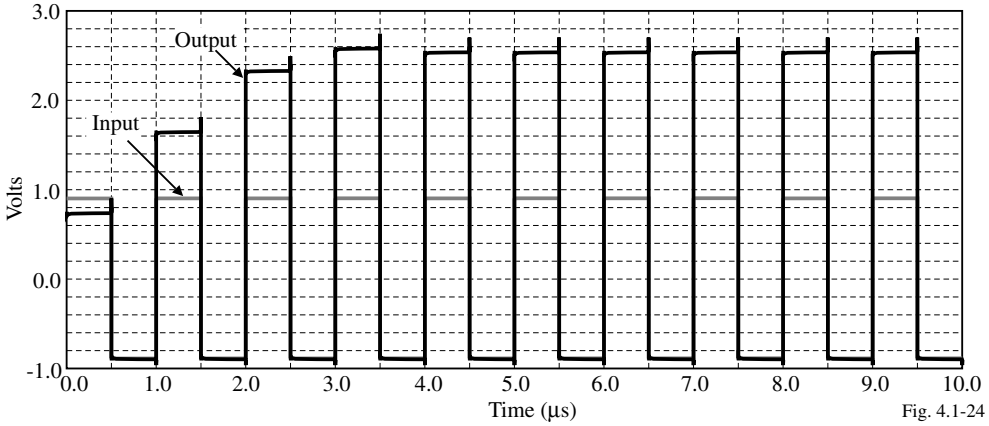

Fig. 4.1-24

† T.B. Cho and R.R. Gray, "A 10b, 20 Msample/s, 35mW Pipeline A/D Converter," *IEEE J. of Solid-State Circuits*, Vol. 30, No. 3m March 1995, pp. 166-172.

Summary of MOSFET Switches

- Symmetrical switching characteristics
- High OFF resistance
- Moderate ON resistance (OK for most applications)
- Clock feedthrough is proportional to size of switch (W) and inversely proportional to switching capacitors.
- Output offset due to clock feedthrough has 2 components:
  - Input dependent
  - Input independent
- Complementary switches help increase dynamic range.
- Fully differential operation should minimize the clock feedthrough.
- As power supply reduces, switches become more difficult to fully turn on.
- Switches contribute a kT/C noise which can get folded back into the baseband.

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SECTION 4.2 - MOS DIODE/ACTIVE RESISTOR

MOS Diode

When the MOSFET has the gate connected to the drain, it acts like a diode with characteristics similar to a pn-junction diode.

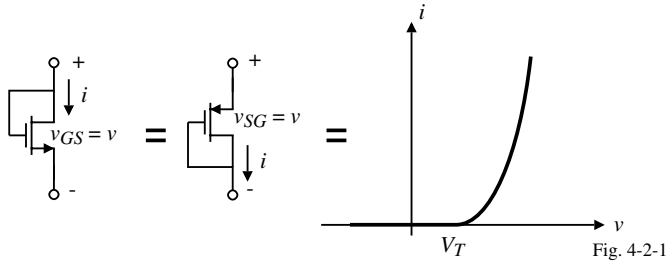

Fig. 4-2-1

Note that when the gate is connected to the drain of an enhancement MOSFET, the MOSFET is *always* in the saturation region.

$$v_{DS} \geq v_{GS} - V_T \quad \Rightarrow \quad v_D - v_S \geq v_G - v_S - V_T \Rightarrow \quad v_D - v_G \geq -V_T \quad \Rightarrow \quad v_{DG} \geq -V_T$$

Since V_T is always greater than zero for an enhancement device, then $v_{DG} = 0$ satisfies the conditions for saturation.

- Works for NMOS or PMOS
- Note that the drain could be V_T less than the gate and still be in saturation

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Large-Signal and Small-Signal Characteristics of the MOS Diode

Large-Signal Characteristics:

Ignore channel modulation-

$$i = i_D = \frac{K'W}{2L}(v_{GS} - V_T)^2 = \frac{\beta}{2}(v_{GS} - V_T)^2 \quad \text{and} \quad v = v_{GS} = v_{DS} = V_T + \sqrt{\frac{2i_D}{\beta}}$$

Small-Signal Characteristics:

The small signal model is a linearization of the large signal model at an operating point.

$$i_D = \frac{\beta}{2}(v_{GS}-V_T)^2(1+\lambda v_{DS}) \rightarrow \quad \imath_d + I_D = \frac{\beta}{2}[v_{gs}+(V_{GS}-V_T)]^2[1+\lambda(v_{ds}+V_{DS})]$$

$$i_d+I_D = \frac{\beta}{2}v_{gs}^2 + \boldsymbol{\beta(V_{GS}-V_T)v_{gs}} + \boldsymbol{\frac{\beta}{2}(V_{GS}-V_T)^2} + \frac{\beta}{2}v_{gs}^2\lambda v_{ds} + \beta(V_{GS}-V_T)v_{gs}\lambda v_{ds}$$

$$+\boldsymbol{\frac{\beta}{2}(V_{GS}-V_T)^2\lambda v_{ds}} + \frac{\beta}{2}v_{gs}^2\lambda V_{DS} + \beta(V_{GS}-V_T)v_{gs}\lambda V_{DS} + \boldsymbol{\frac{\beta}{2}(V_{GS}-V_T)^2\lambda V_{DS}}$$

Assume that $v_{gs} < V_{GS}-V_T$, $v_{ds} < V_{DS}$ and $\lambda \ll 1$. Therefore we write:

$$i_d+I_D \approx \beta(V_{GS}-V_T)v_{gs} + \frac{\beta}{2}(V_{GS}-V_T)^2\lambda v_{ds} + \frac{\beta}{2}(V_{GS}-V_T)^2(1+\lambda V_{DS})$$

$$\therefore\ i_d = \beta(V_{GS}-V_T)v_{gs}+\frac{\beta}{2}(V_{GS}-V_T)^2\lambda v_{ds} = g_m v_{gs}+g_{ds}v_{ds} \quad \text{and} \quad I_D = \frac{\beta}{2}(V_{GS}-V_T)^2(1+\lambda V_{DS})$$

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Application of the MOS Diode

DC resistor:

$$\text{DC resistance} = \frac{v}{i}\bigg|_Q = \frac{V}{I}$$

- Useful for biasing - creating current from voltage and vice versa

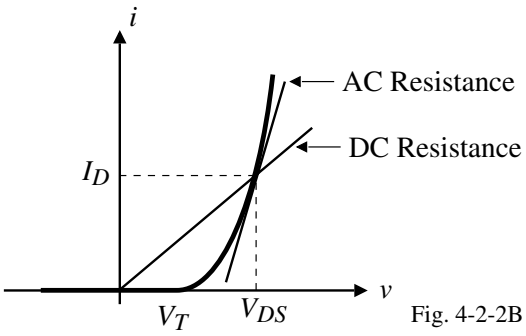

Fig. 4-2-2B

Small-Signal Load (AC resistance):

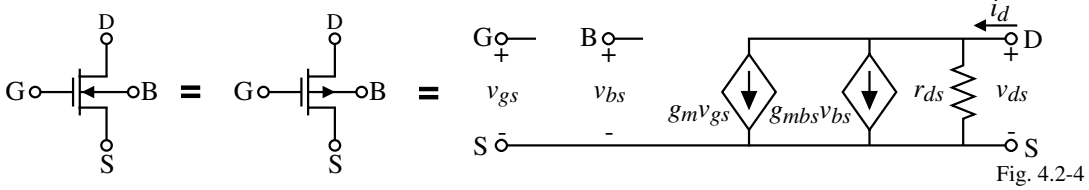

Fig. 4.2-4

$$\text{AC resistance} = \frac{v_{ds}}{i_d} = \frac{1}{g_m + g_{ds}} \approx \frac{1}{g_m}$$

where

$$g_m = \beta(V_{GS}-V_T) = \sqrt{2\beta I_D} \qquad \text{and } g_{ds} \approx \frac{\beta}{2}(V_{GS}-V_T)^2\lambda = I_D\lambda$$

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Influence of the Back Gate (Bulk)

It can be shown that the small signal model for the MOSFET with the bulk not connected to the source is,

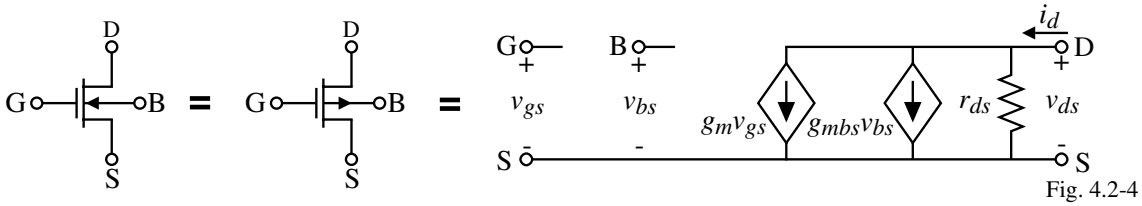

Fig. 4.2-4

where

$$g_{mbs} \text{ is defined as } \frac{\partial i_D}{\partial v_{BS}}\bigg|_Q = \left(\frac{\partial i_D}{\partial v_{GS}}\right)\left(\frac{\partial v_{GS}}{\partial v_{BS}}\right)\bigg|_Q = \left(-\frac{\partial i_D}{\partial v_T}\right)\left(\frac{\partial v_T}{\partial v_{BS}}\right)\bigg|_Q$$

$$g_{mbs} = \frac{g_m \gamma}{2\sqrt{2|\phi_F| - V_{BS}}} = \eta g_m$$

It is very useful to simplify the small signal model when possible. The following are reasonable guidelines for this simplification:

$$\boxed{g_m \approx 10 g_{mbs} \approx 100 g_{ds}}$$

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Example 4.2-1 - Small-Signal Load Resistance

Find the small signal resistance of the MOS diode shown using the parameters of Table 3.2-1. Assume that the *W/L* ratio is 10µm/1µm.

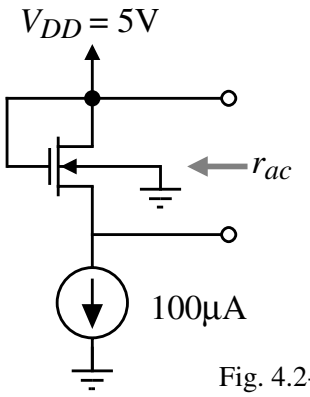

Fig. 4.2-5

Solution

If we are going to include the bulk effect, we must first find the dc value of the bulk-source voltage. Unfortunately, we do not know the threshold voltage because the bulk-source voltage is unknown. The best approach is to ignore the bulk-source voltage, find the gate-source voltage and then iterate if necessary.

$$\therefore \quad V_{GS} = \sqrt{\frac{2I}{\beta}} + V_{T0} = \sqrt{\frac{2 \cdot 100}{110 \cdot 10}} + 0.7 = 1.126V$$

Thus let us guess at a gate-source voltage of 1.3V (to account for the bulk effect) and calculate the resulting gate-source voltage.

$$V_T = V_{T0} + \gamma\sqrt{2|\phi_F| - (-3.7)} - \gamma\sqrt{2|\phi_F|} = 0.7 + 0.4\sqrt{0.7 + 3.7} - 0.4\sqrt{0.7} = 1.20V \Rightarrow V_{GS} = 1.63V$$

Now refine our guess at V_{GS} as 1.6V and repeat the above to get $V_T = 1.175V$ which gives $V_{GS} = 1.60V$.

Therefore, $V_{BS} = -3.4V$.

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Example 4.2-1 - Continued

The small signal model for this example is shown.

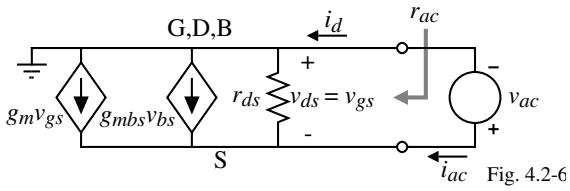

Fig. 4.2-6

The ac input resistance is found by,

$$i_{ac} = g_{ds}v_{ac} - g_m v_{gs} - g_{mbs}v_{bs}$$
$$= g_{ds}v_{ac} + g_m v_s + g_{mbs}v_s = v_{ac}(g_m+g_{mbs}+g_{ds})$$
$$\therefore \quad r_{ac} = \frac{v_{ac}}{i_{ac}} = \frac{1}{g_m+g_{mbs}+g_{ds}}$$

Now we must find the parameters which are,

$$g_m = \sqrt{2\beta I_D} = \sqrt{2\cdot 110\cdot 10\cdot 100}\ \mu S = 469\mu S, \quad g_{ds} = 0.04V^{-1}\cdot 100\mu A = 4\mu S,$$

and $$g_{mbs} = \frac{469\mu S\cdot 0.4}{2\sqrt{0.7+3.4}} = 0.0987\cdot 469\mu S = 46.33\mu S$$

Finally, $$r_{ac} = \frac{10^6}{469 + 46.33 + 4} = 1926\Omega$$

If we had used the previous approximations of $g_m \approx 10g_{mbs} \approx 100g_{ds}$, then we could have simply let

$$r_{ac} \approx 1/g_m = 1/469\mu S = 2132\Omega$$

Probably the most important result of this approximation is that we would not have to find V_{BS} which took a lot of effort for little return.

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Applications of the MOS Diode for Biasing

1.) Deriving a bias voltage from power supply.

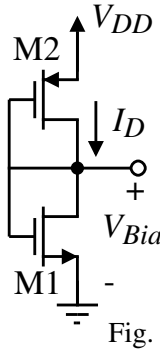

Fig. 4.2-7

$$I_{D1} = I_{D2} \quad \Rightarrow \quad \beta_N(V_{Bias}-V_{TN})^2 = \beta_P(V_{DD}-V_{Bias}-|V_{TP}|)^2$$

Solving for V_{Bias} gives

$$V_{Bias} = \frac{V_{TN} + \sqrt{\frac{\beta_P}{\beta_N}}(V_{DD}-|V_{TP}|)}{1+\sqrt{\frac{\beta_P}{\beta_N}}} \quad \text{and} \quad I_D = \beta_N(V_{Bias}-V_{TN})^2$$

Use the ratio of β_P/β_N to design V_{Bias} and the value of β_N to design the current I_D.

2.) Deriving a bias voltage from a bias current.

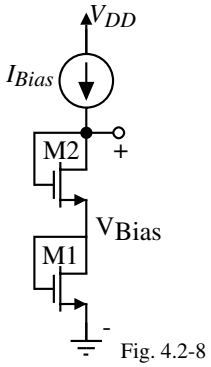

Fig. 4.2-8

$$V_{Bias} = V_{GS1} + V_{GS2}$$
$$= \sqrt{\frac{2I_{Bias}}{\beta_1}} + V_{T1} + \sqrt{\frac{2I_{Bias}}{\beta_2}} + V_{T2}$$

Design β_1 and β_2 to yield the desired value of V_{Bias}. Try to keep the values of W/L as close to unity as possible to minimize area.

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Use of the MOSFET to Implement a Floating Resistor

In many applications, it is useful to implement a resistance using a MOSFET. First, consider the simple, single MOSFET implementation.

$$R_{AB} = \frac{L}{K'W(V_{GS} - V_T)}$$

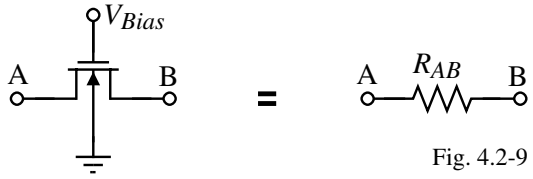


Fig. 4.2-9

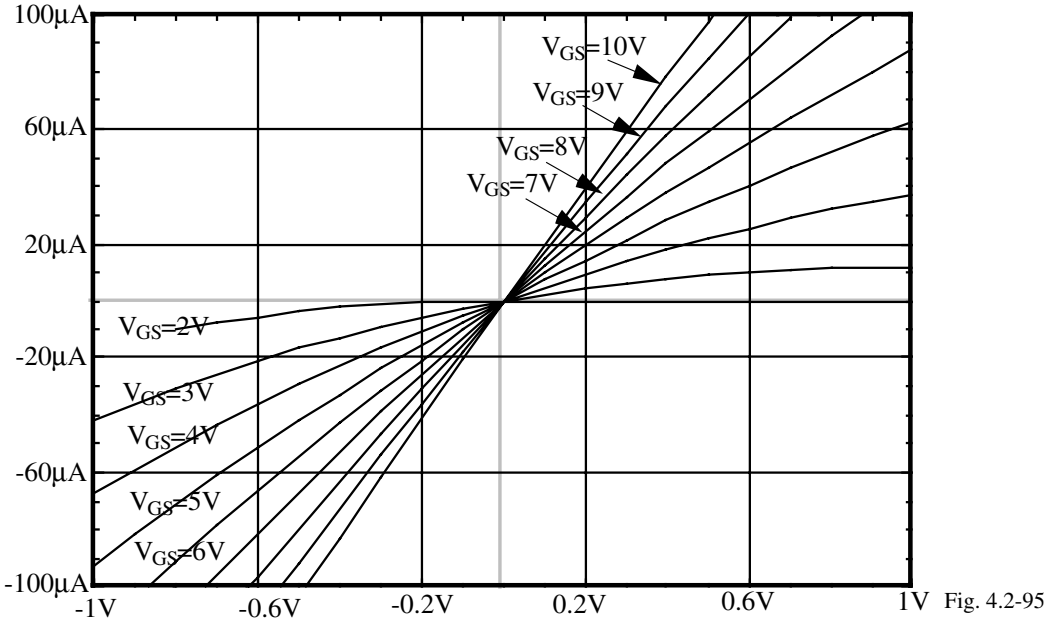


Fig. 4.2-95

Cancellation of Second-Order Voltage Dependence – Parallel MOSFETs

Circuit:

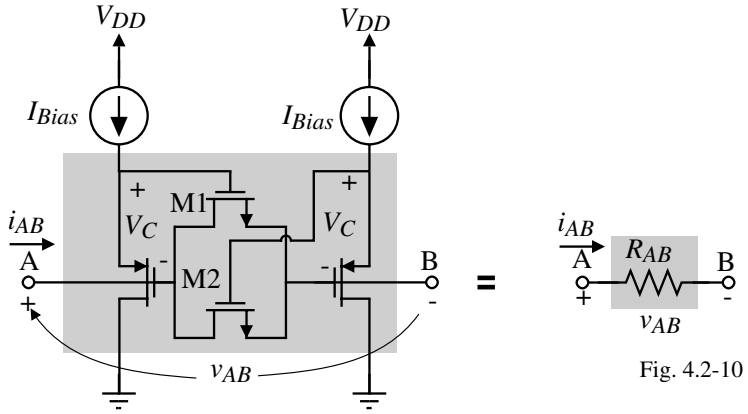


Fig. 4.2-10

Assume both devices are non-saturated

$$i_{D1} = ß_1\left[(v_{AB} + V_C - V_T)v_{AB} - \frac{v_{AB}^2}{2}\right]$$

$$i_{D2} = ß_2\left[(V_C - V_T)v_{AB} - \frac{v_{AB}^2}{2}\right]$$

$$i_{AB} = i_{D1} + i_{D2} = ß\left[v_{AB}^2 + (V_C - V_T)v_{AB} - \frac{v_{AB}^2}{2} + (V_C - V_T)v_{AB} - \frac{v_{AB}^2}{2}\right]$$

$$i_{AB} = 2ß(V_C - V_T)v_{AB}$$

$$\boxed{R_{AB} = \frac{1}{2ß(V_C - V_T)}}$$

Parallel MOSFET Performance

Voltage-Current Characteristic:

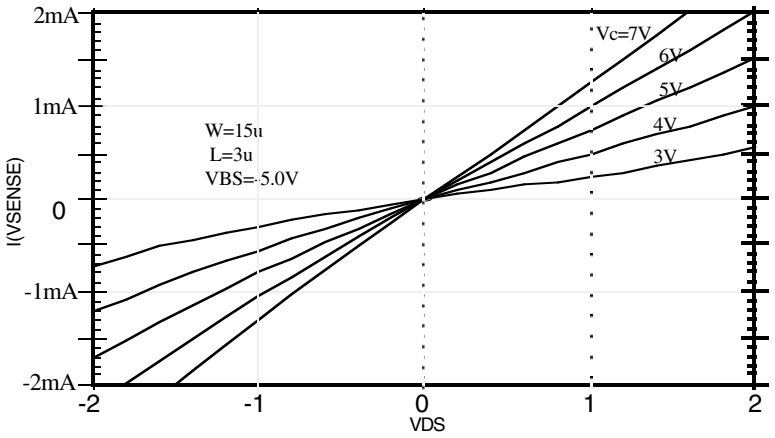


Fig. 4.1-11

SPICE Input File:

```
NMOS parallel transistor realization
M1 2 1 0 5 MNMOS W=15U L=3U
M2 2 4 0 5 MNMOS W=15U L=3U
.MODEL MNMOS NMOS VTO=0.75, KP=25U,
+LAMBDA=0.01, GAMMA=0.8 PHI=0.6
VC 1 2
E1 4 0 1 2 1.0
VSENSE 10 2 DC 0
VDS 10 0
VSS 5 0 DC -5
.DC VDS -2.0 2.0 .2 VC 3 7 1
.PRINT DC I(VSENSE)
.PROBE
.END
```

Still have the influence of the bulk on the threshold voltage.

Double MOSFET Differential Resistor

Cancels the bulk effect.

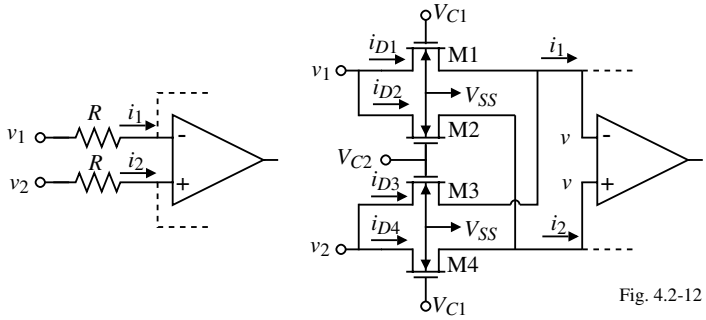


Fig. 4.2-12

$$i_{D1} = \beta\,[(V_{C1}\text{-}v\text{-}V_T)(v_1\text{-}v) - 0.5(v_1\text{-}v)^2] \qquad i_{D2} = \beta\,[(V_{C2}\text{-}v\text{-}V_T)(v_1\text{-}v) - 0.5(v_1\text{-}v)^2]$$

$$i_{D3} = \beta\,[(V_{C2}\text{-}v\text{-}V_T)(v_2\text{-}v) - 0.5(v_2\text{-}v)^2] \qquad i_{D4} = \beta\,[(V_{C1}\text{-}v\text{-}V_T)(v_2\text{-}v) - 0.5(v_2\text{-}v)^2]$$

$$i_1 = i_{D1}+i_{D3} = \beta\,[(V_{C1}\text{-}v\text{-}V_T)V_1\text{-}v) - 0.5(v_1\text{-}v)^2 + (V_{C2}\text{-}v\text{-}V_T)(v_2\text{-}v) - 0.5(v_2\text{-}v)^2]$$

$$i_2 = i_{D2}+i_{D4} = \beta\,[(V_{C2}\text{-}v\text{-}V_T)(v_1\text{-}v) - 0.5(v_1\text{-}v)^2 + (V_{C1}\text{-}v\text{-}V_T)(v_2\text{-}v) - 0.5(v_2\text{-}v)^2]$$

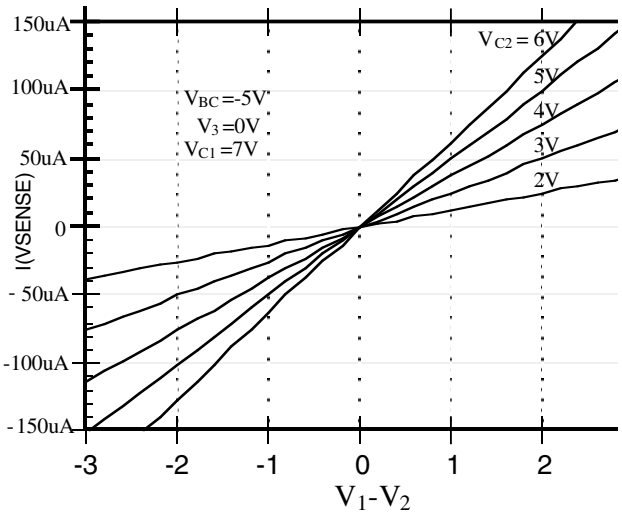
$$i_1 - i_2 = \beta\,[(V_{C1}\text{-}v\text{-}V_T)(v_1\text{-}v) + (V_{C2}\text{-}v\text{-}V_T)(v_2\text{-}v) + (V_{C2}\text{-}v\text{-}V_T)(v_1\text{-}v) + (V_{C1}\text{-}v\text{-}V_T)(v_2\text{-}v)]$$

$$= \beta\,[v_1(V_{C1}\text{-}V_{C2}) + v_2(V_{C2}\text{-}V_{C1})] = \beta\,(V_{C1}\text{-}V_{C2})(v_1\text{-}v_2)$$

Differential input resistance is

$$R_{in} = \frac{v_1\text{-}v_2}{i_1\text{-}i_2} = \frac{v_1\text{-}v_2}{\beta\,(V_{C1}\text{-}V_{C2})(v_1\text{-}v_2)} = \frac{1}{\beta\,(V_{C1}\text{-}V_{C2})}, v_1,v_2 \le \min\{(V_{C1}\text{-}V_T),(V_{C2}\text{-}V_T)\}$$

Double-MOSFET, Differential Resistor Performance



SPICE Input File:

```
Double MOSFET Differential Resistor Realization
M1 1 2 3 4 MNMOS1 W=3U L=3U
M2 1 5 8 4 MNMOS1 W=3U L=3U
M3 6 5 3 4 MNMOS1 W=3U L=3U
M4 6 2 8 4 MNMOS1 W=3U L=3U
VSENSE 3 8 DC 0
VC1 2 0 DC 7V
VC2 5 0
VSS 4 0 DC -5V
V12 1 6
.MODEL MNMOS1 NMOS VTO=0.75 KP=25U
+LAMBDA=0.01 GAMMA=0.8 PHI=0.6
.DC V12 -3 3 0.2 VC2 2 6 1
.PRINT DC I(VSENSE))
.PROBE
.END
```

Comments:

- Good linearity and tunability.
- Can be used as a multiplier.

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Summary of Active Resistor Realizations

AC Resistance Realization	Linearity	How Controlled	Restrictions
Single MOSFET	Poor	V_{GS} or W/L	$v_{BULK} < \text{Min}\ (v_S, v_D)$
Parallel MOSFET	Good	V_C or W/L	$v \leq (V_C - V_T)$
Double-MOSFET, differential resistor	Very Good	$V_{C1} - V_{C2}$ or W/L	$v_1, v_2 < \min(V_{C1}-V_T, V_{C2}-V_T)$ $v_{BULK} < \min(v_1, v_2)$ Transresistance only

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SECTION 4.3 - CURRENT SINKS AND SOURCES

Characterization of MOS Sinks and Sources

A sink/source is characterized by two quantities:

- r_{out} - a measure of the "flatness" of the current sink/source (its independence of voltage)
- V_{MIN} - the min. across the sink or source for which the current is no longer constant

CMOS Current Sink:

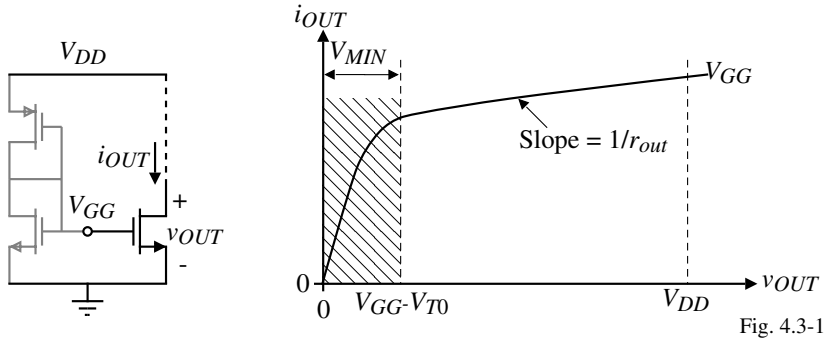

Fig. 4.3-1

$$r_{out} = \frac{1}{di_D/dv_{DS}} = \frac{1+\lambda V_{DS}}{\lambda I_D} \approx \frac{1}{\lambda I_D}$$

and

$$V_{MIN} = V_{DS}(\text{sat}) = V_{GS} - V_{T0} = V_{GG} - V_{T0}$$

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Simple MOS Current Source

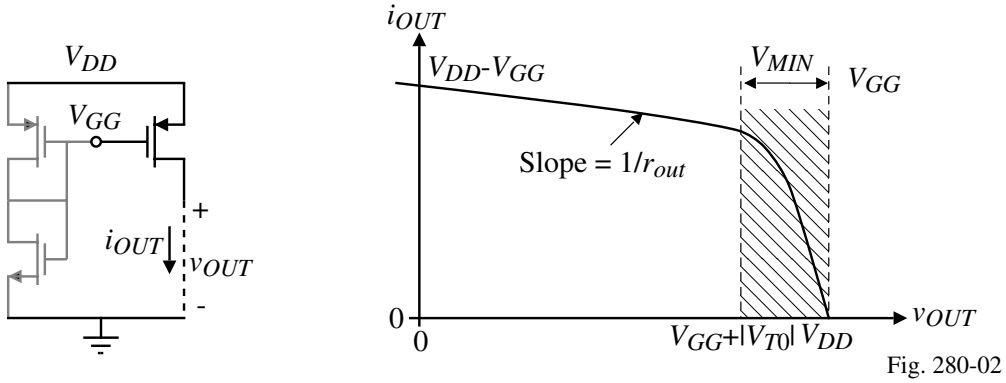

Fig. 280-02

This current source only works when $v_{OUT} \leq V_{GG} + |V_{T0}|$

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Gate-Source Voltage Components

It is important to note that the gate-source voltage consists of two parts as illustrated below:

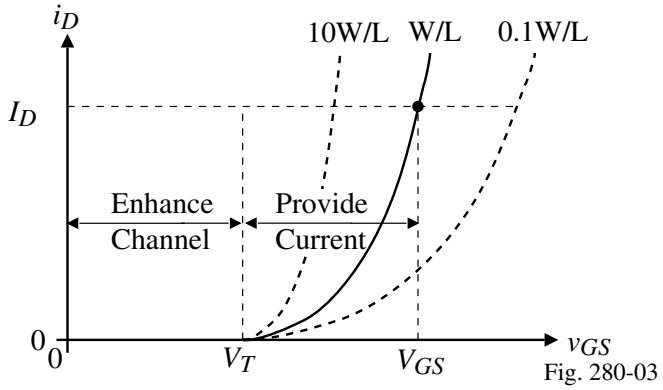

Fig. 280-03

$V_{GS} = V_{T0} + V_{ON}$ = Part to enhance the channel + Part to cause current flow

where

$V_{ON} = V_{DS}(\text{sat}) = V_{GS} - V_{T0}$

$\therefore$ $\boxed{V_{MIN} = V_{ON} = V_{DS}(\text{sat}) = \sqrt{\frac{2I_D}{K'(W/L)}}}$ for the simple current sink.

Note that V_{MIN} can be reduced by using large values of W/L.

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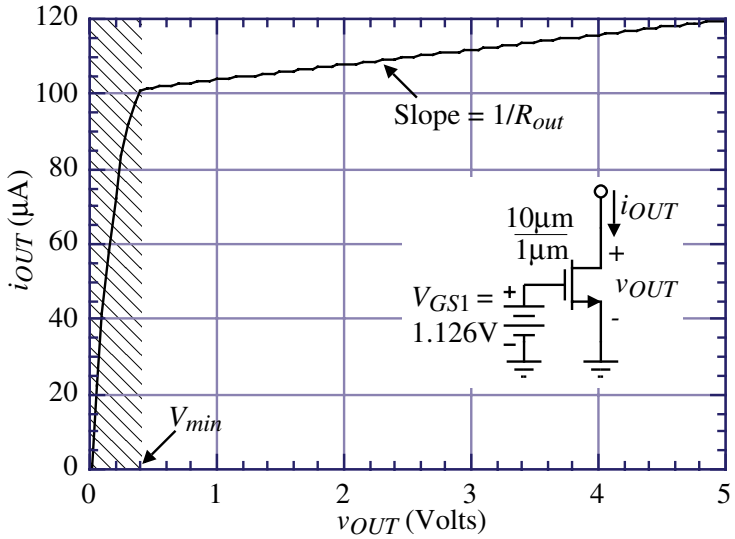
Simulation of a Simple MOS Current Sink



Comments:

V_{MIN} is too large - desire V_{MIN} to approach zero, at least approach $V_{CE}(\text{sat})$

Slope too high - desire the characteristic to be flat implying very large output resistance

($K_N' = 110\mu A/V^2$, $V_T = 0.7V$ and $\lambda = 0.04V^{-1}$) $\Rightarrow$ $r_{ds} = 250k\Omega$

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Increasing the Output Resistance of a Current Sink/Source

Principle:

In order to increase the output resistance, use negative series feedback because,

r_{out} (with feedback) = r_{out}(without feedback) x [1 + Loop gain]

Circuit:

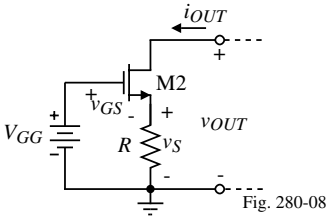

Fig. 280-08

How does it work?

1.) Assume i_{out} increases.
2.) As a result, v_S increases.
3.) Since the gate is held constant at V_{GG}, then v_{GS} decreases.
4.) The decrease in v_{GS} causes i_{OUT} to decrease opposing the original increase

Loop Gain?

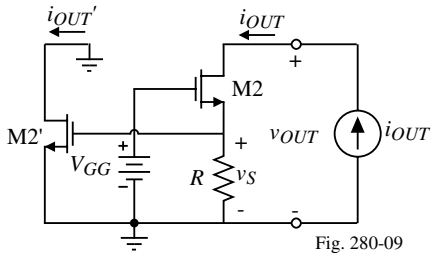

Fig. 280-09

$i_{OUT}' = g_m v_S = g_m R i_{OUT}$

$\therefore$ Loop gain $= \dfrac{i_{OUT}'}{i_{OUT}} = g_m R$

r_{out}(w.fb.) = r_{out}(w/o fb.)x [1+$g_m R$] = $r_{ds}(1+g_m R)$

If $g_m R >> 1$, then r_{out}(w. fb.) $\approx g_m r_{ds} R$

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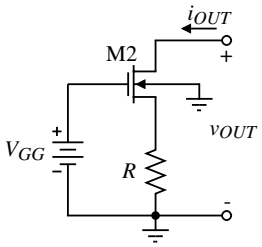
Increasing the Output Resistance of a Simple MOS Current Sink

Small signal model for calculating the output resistance for the cascode current sink:



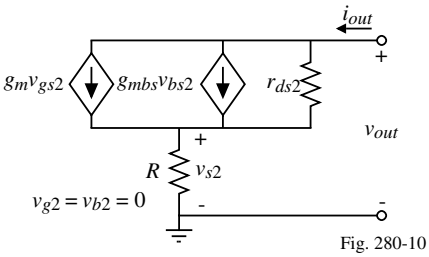


Fig. 280-10

Loop equation:

$v_{out} = (i_{out} - g_{m2}v_{gs2} - g_{mbs2}v_{bs2})r_{ds2} + i_{out}R$

$= i_{out}(r_{ds2}+R) - g_{m2}r_{ds2}v_{gs2} - g_{mbs2}r_{ds2}v_{bs2}$

But,

$v_{gs2} = 0 - v_{s2} = -i_{out}R$ and $v_{bs2} = 0 - v_{s2} = -i_{out}R$

Therefore,

$v_{out} = i_{out}[r_{ds2} + R + g_{m2}r_{ds2}R + g_{mbs2}r_{ds2}R]$

or

$$r_{out} = \frac{v_{out}}{i_{out}} = r_{ds2} + R + g_{m2}r_{ds2}R + g_{mbs2}r_{ds2}R \approx g_{m2}r_{ds2}R = \mu_2 R \qquad (\mu = g_m r_{ds})$$

A general principle emerges:

The output resistance of a cascode circuit $\approx R$ x (*Common source voltage gain of the cascoding transistor*)

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MOS Cascode Current Sink

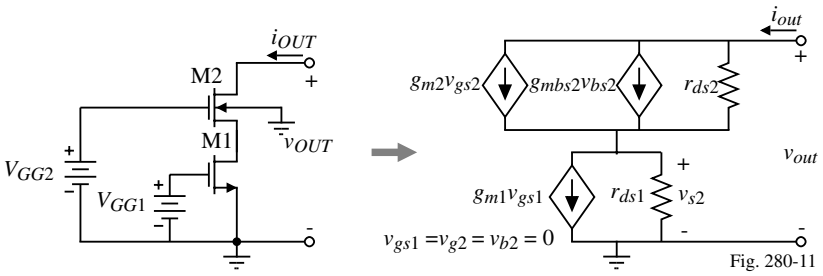

Fig. 280-11

Small signal output resistance:

Noting that $v_{gs1} = v_{g2} = v_{b2} = 0$ and writing a loop equation we get,

$$v_{out} = (i_{out} - g_{m2}v_{gs2} - g_{mbs2}v_{bs2})r_{ds2} + r_{ds1}i_{out}$$

However,

$$v_{gs2} = 0 - v_{s2} = -i_{out}r_{ds1} \quad \text{and} \quad v_{bs2} = 0 - v_{s2} = -i_{out}r_{ds1}$$

Therefore,

$$v_{out} = i_{out}[r_{ds1} + r_{ds2} + g_{m2}r_{ds1}r_{ds2} + g_{mbs2}r_{ds1}r_{ds2}]$$

or

$$r_{out} = \frac{v_{out}}{i_{out}} = r_{ds1} + r_{ds2} + g_{m2}r_{ds1}r_{ds2} + g_{mbs2}r_{ds1}r_{ds2} \approx g_{m2}r_{ds1}r_{ds2} = \mu_2 r_{ds1}$$

Comments:

1.) Same as before if $R = r_{ds1}$

2.) Bulk effects have little influence.

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Simulation of the Cascode CMOS Current Sink

Example

Use the model parameters K_N'=110μA/V^2, $V_T = 0.7$ and $\lambda_N = 0.04\text{V}^{-1}$ to calculate (a) the small-signal output resistance for the simple current sink if $I_{OUT} = 100\mu\text{A}$ and (b) the small-signal output resistance for the cascode current sink with $I_{OUT} = 100\mu\text{A}$. Assume that all W/L values are 1.

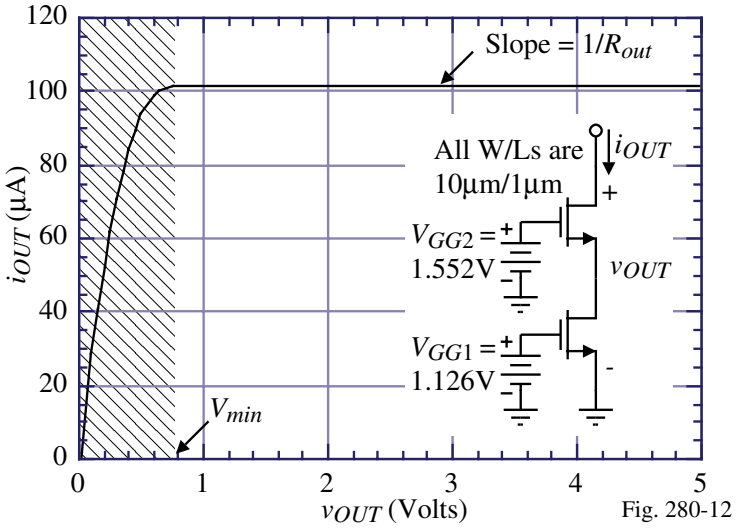

Fig. 280-12

Solution

(a) Using $\lambda = 0.04\ \text{V}^{-1}$ and $I_{OUT} = 100\mu\text{A}$ gives $r_{ds1} = 250\text{k}\Omega = r_{ds2}$. (b) Ignoring the bulk effect, we find that $g_{m1} = g_{m2} = 469\mu\text{S}$ which gives $r_{out} = (250\text{k}\Omega)(469\mu\text{S})(250\text{k}\Omega) = 29.32\text{M}\Omega$.

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Gate-Source Matching Principle

A. If the gate-source voltages of two or more transistors are equal and the transistors are matched and operating in the saturation region, then the currents are related by the W/L ratios of the individual transistors. The gate-source voltages may be directly connected or implied.

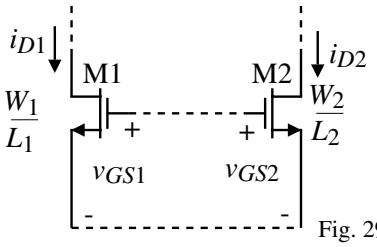

Fig. 290-02

$$i_{D1} = \frac{K'W_1}{2L_1}(v_{GS1}-V_{T1})^2 \rightarrow (v_{GS1}-V_{T1})^2 = \frac{2K'i_{D1}}{(W_1/L_1)}$$

$$i_{D2} = \frac{K'W_2}{2L_2}(v_{GS2}-V_{T2})^2 \rightarrow (v_{GS2}-V_{T2})^2 = \frac{2K'i_{D2}}{(W_2/L_2)}$$

If $v_{GS1} = v_{GS2}$, then $\boxed{\left(\frac{W_2}{L_2}\right) i_{D1} = \left(\frac{W_1}{L_1}\right) i_{D2}}$ or $\boxed{i_{D1} = \left(\frac{W_1/L_1}{W_2/L_2}\right) i_{D2}}$

B. If the drain currents of two or more transistors are equal and the transistors are matched and operating in the saturation region, then the gate-source voltages are related by the W/L ratios (ignoring bulk effects).

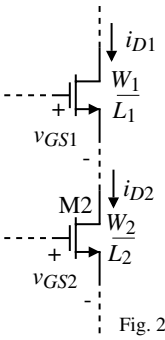

Fig. 290-03

If $i_{D1} = i_{D2}$, then $\boxed{v_{GS1} = V_{T1} + \sqrt{\frac{W_2/L_2}{W_1/L_1}}(v_{GS2} - V_{T2})}$

or

if $W_2/L_2 = W_1/L_1$, then $\boxed{v_{GS1} = v_{GS2}}$ (Note: V_{DS1}must equal V_{DS2} for ideal results)

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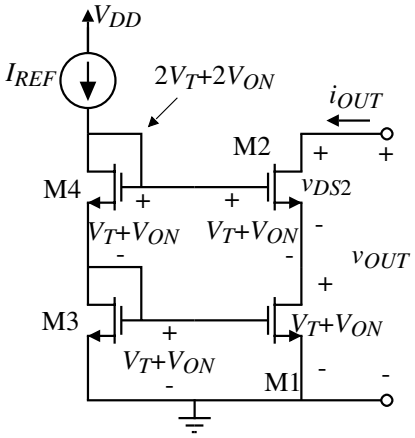
Practical Cascode Current Sink Implementation

Does not require any batteries and uses the gate-source matching principle.



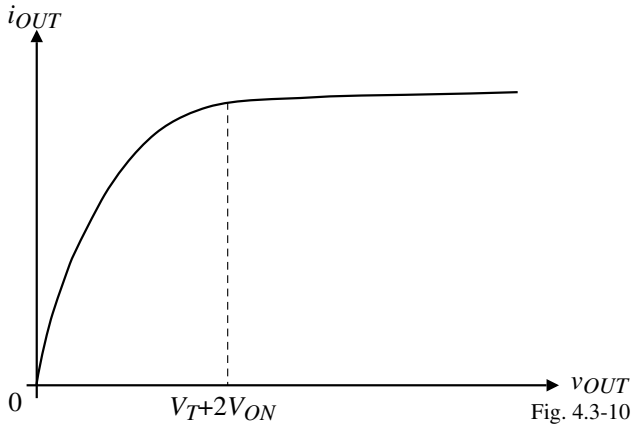


Fig. 4.3-10

However, V_{MIN} is now equal to $V_T + V_{ON} + v_{DS2}(\text{min}) = V_T + V_{ON} + V_{ON} = V_T + 2V_{ON}$

Assuming that $I_{OUT} = 100\mu A$ and $W_2/L_2 = W_1/L_1 = 10$ gives $V_{ON} = 0.426V$.

Thus $V_{MIN} = 0.7V + 2 \cdot 0.426V = 1.55V$ (this is way too much)

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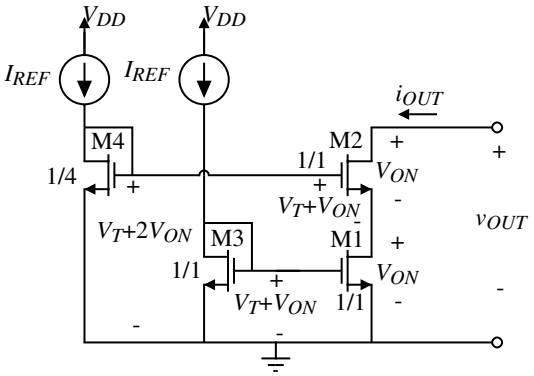
High-Swing Cascode Current Sink

Since $V_{ON} = \sqrt{\frac{2I_D}{K'(W/L)}}$, then if L/W is quadrupled, then V_{ON} is doubled.

$\therefore\ V_{MIN} = 2V_{ON}$.



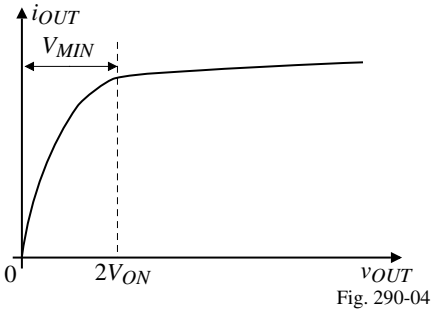


Fig. 290-04

Example

Use the cascode current sink configuration above to design a current sink of 100μA and a $V_{MIN} = 1$V. Assume the device parameters of Table 3.1-2.

Solution

With $V_{MIN} = 1$V, choose $V_{ON} = 0.5$V. Assuming M1 and M2 are identical gives

$$\frac{W}{L} = \frac{2 \cdot I_{OUT}}{K' \cdot V_{ON}^2} = \frac{2 \cdot 100\text{x}10^{-6}}{110\text{x}10^{-6}\text{x}0.25} = 7.27 \quad \Rightarrow \quad \frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{W_3}{L_3} = \underline{7.27} \text{ and } \frac{W_4}{L_4} = \underline{1.82}$$

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Improved High-Swing Cascode Current Sink

Because the drain-source voltages of the matching transistors, M1 and M3 are not equal, $i_{OUT} \neq I_{REF}$.

To circumvent this problem the cascode current sink shown is utilized:

Note that the drain-source voltage of M1 and M3 are identical causing i_{OUT} to be a replication of I_{REF}.

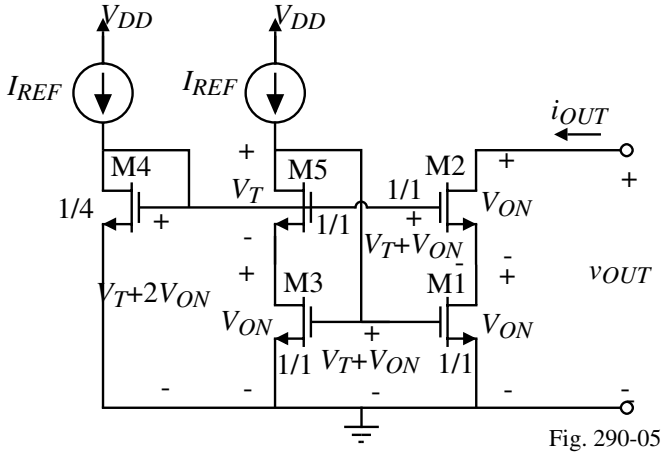

Fig. 290-05

Design Procedure

1.) Since $V_{MIN} = 2V_{ON} = 2V_{DS}(\text{sat})$, let $V_{ON} = 0.5V_{MIN}$.

2.) $V_{ON} = \sqrt{\frac{2I_{REF}}{K'(W/L)}} \quad \Rightarrow \quad \frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{W_3}{L_3} = \frac{W_5}{L_5} = \frac{2I_{REF}}{K'V_{ON}^2} = \frac{8I_{REF}}{K'V_{MIN}^2}$

3.) $\frac{W_4}{L_4} = \frac{2I_{REF}}{K'(V_{GS4}-V_T)^2} = \frac{2I_{REF}}{K'(2V_{ON})^2} = \frac{I_{REF}}{2K'V_{ON}^2}$

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Signal Flow in Transistors

The last example brings up an interesting and important point. This point is illustrated by the following question, "How does I_{REF} flow into the M3-M5 combination of transistors since there is no path to the gate of M5?"

Consider how signals flow in transistors:

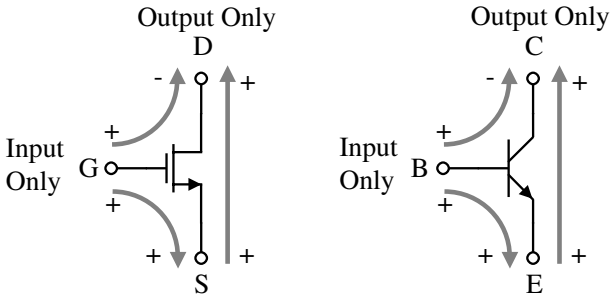

Fig. 4.3-12B

Answer to the above question:

As V_{DD} increases (i.e. the circuit begins to operate), I_{REF} cannot flow into the drain of M5, so it flows through the path indicated by the arrow to the gate of M3. It charges the stray capacitance and causes the gate-source voltage of M3 to increase to the exact value necessary to cause I_{REF} to flow through the M3-M5 combination.

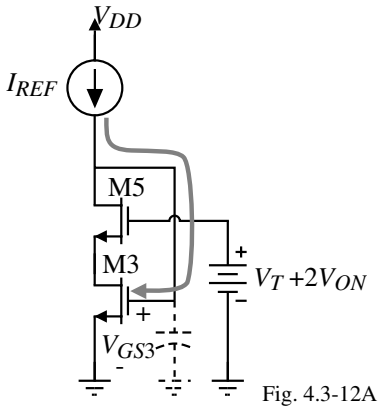

Fig. 4.3-12A

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Example 4.3-1 - Design of a Minimum V_{MIN} Current Sink

Assume $I_{REF} = 100\mu A$ and design a cascode current sink with a $V_{MIN} = 0.3V$ using the following parameters: VTO=0.7, KP=110U, LAMBDA=0.04, GAMMA=0.4, PHI=0.7

Solution

From the previous equations, we get

$$\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{W_3}{L_3} = \frac{W_5}{L_5} = \frac{8I_{REF}}{K'V_{MIN}^2} = \frac{8 \cdot 100}{110 \cdot (0.3V)^2} = 80.8 \text{ and}$$

$$\frac{W_4}{L_4} = \frac{I_{REF}}{2K'V_{ON}^2} = \frac{100}{2 \cdot 110 \cdot 0.15^2} = 20.2$$

Simulation Results:

```
Low Vmin Cascade Current Sink - Method No. 2
M1 5 1 0 0 MNMOS W=81U L=1U
M2 2 3 5 5 MNMOS W=81U L=1U
M3 4 1 0 0 MNMOS W=81U L=1U
M4 3 3 0 0 MNMOS W=20U L=1U
M5 1 3 4 4 MNMOS W=81U L=1U
.MODEL MNMOS NMOS VTO=0.7 KP=110U
+LAMBDA=0.04 GAMMA=0.4 PHI=0.7
VDD 6 0 DC 5V
IIN1 6 1 DC 100U
IIN2 6 3 DC 100U
VOUT 2 0 DC 5.0
.OP
.DC VOUT 5 0 0.05
.PRINT DC ID(M2)
.END
```

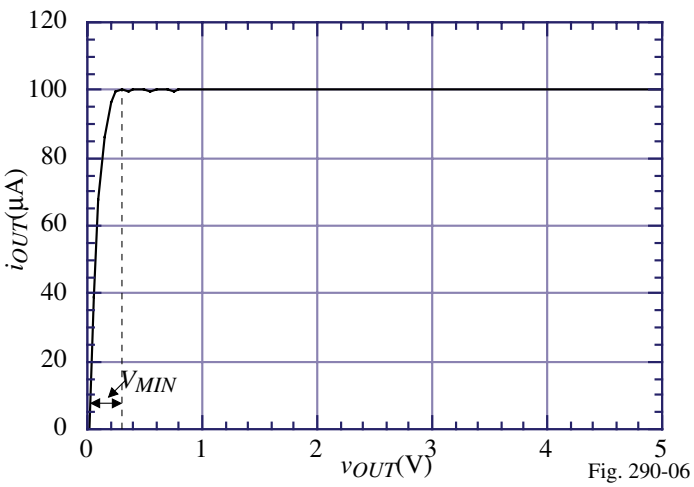

Fig. 290-06

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Self-Biased Cascode Current Sink†

The $V_T + 2V_{ON}$ bias voltage is developed through a series resistor.

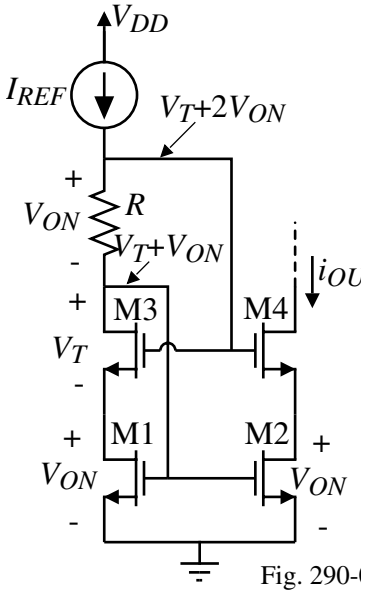

Fig. 290-

Design procedure:

Same as the previous except

$$R = \frac{V_{ON}}{I_{REF}} = \frac{V_{MIN}}{2I_{REF}}$$

For the previous example,

$$R = \frac{0.3\text{V}}{2 \cdot 100\mu\text{A}} = 1.5\text{k}\Omega$$

Observation:

Note that the last several slides have been devoted to just getting the MOS cascode current sink/source to have the same minimum voltage as the BJT!

† T.L. Brooks and A.L. Westwick, "A Low-Power Differential CMOS Bandgap Reference," *Proc. of IEEE Inter. Solid-State Circuits Conf.*, Feb. 1994, pp. 248-249.

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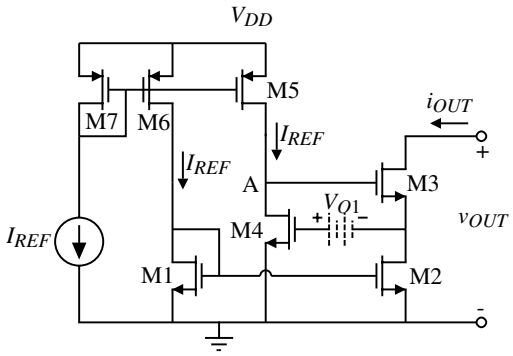
MOS Regulated Cascode Sink†



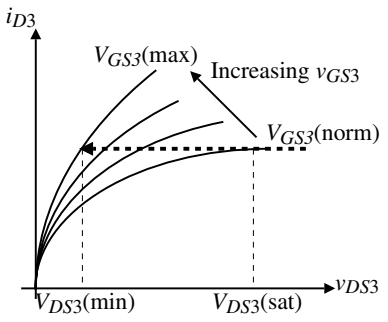


Fig. 290-08

Comments:

• Achieves very high output resistance by increasing the loop gain due to the M4-M5 inverting amplifier.

$$\text{Loop gain} = g_{m3}r_{ds2}\left(\frac{g_{m4}}{g_{ds4}+g_{ds5}}\right) \approx \frac{g_{m3}r_{ds2}g_{m4}r_{ds4}}{2} \text{ if } r_{ds4} \approx r_{ds5} \therefore r_{out} \approx \frac{r_{ds3}g_{m3}r_{ds2}g_{m4}r_{ds4}}{2}$$

• M3 maintains "constant" current even though it is no longer in the saturation region.

Assume an i_{OUT} increase $\rightarrow$ v_{S3} increase $\rightarrow$ v_{GS4} increase $\rightarrow$ v_{G3} decrease $\rightarrow$ Large decrease in v_{GS3} $\rightarrow$ Large decrease in i_{OUT}

† E. Sackinger and W. Guggenbuhl, "A Versatile Building Block: The CMOS Differential Difference Amplifier," *IEEE J. of Solid-State Circuits*, vol. SC-22, no. 2, pp. 287-294, April 1987.

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Regulated Cascode Current Sink - Continued

Small signal model:

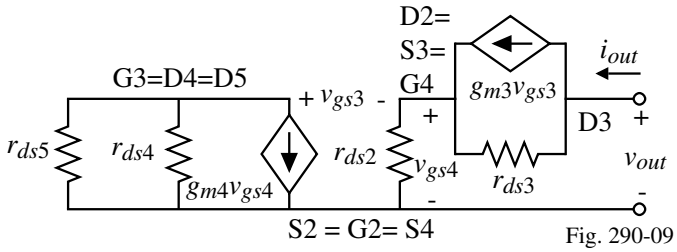

Fig. 290-09

Solving for the output resistance:

$$i_{out} = g_{m3}v_{gs3} + g_{ds3}(v_{out}-v_{gs4})$$

But

$$v_{gs4} = i_{out}r_{ds2}$$

and

$$v_{gs3} = v_{g3} - v_{s3} = -g_{m4}(r_{ds4}||r_{ds5})v_{gs4} - v_{gs4} = -r_{ds2}[1 + g_{m4}(r_{ds4}||r_{ds5})]i_{out}$$

$$\therefore \quad i_{out} = -g_{m3}r_{ds2}[1 + g_{m4}(r_{ds4}||r_{ds5})]i_{out} + g_{ds3}v_{out} - g_{ds3}r_{ds2}i_{out}$$

$$v_{out} = r_{ds3}[1 + g_{m3}r_{ds2} + g_{ds3}r_{ds2} + g_{m3}r_{ds2}g_{m4}(r_{ds4}||r_{ds5})]i_{out}$$

$$\therefore r_{out} = \frac{v_{out}}{i_{out}} = r_{ds3}[1 + g_{m3}r_{ds2} + g_{ds3}r_{ds2} + g_{m3}r_{ds2}g_{m4}(r_{ds4}||r_{ds5})]$$

$$\approx r_{ds3}g_{m3}r_{ds2}g_{m4}(r_{ds4}||r_{ds5})$$

If I_{REF} = 100μA, all W/Ls are 10μm/1μm we get r_{ds} = 0.25MΩ and g_m = 469μS which gives

$$r_{out} \approx (0.25\text{M}\Omega)(469\mu\text{S})(0.25\text{M}\Omega)(469\mu\text{S})(0.125\text{M}\Omega) = 1.72\text{G}\Omega$$

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Regulated Cascode Current Sink - Continued

V_{MIN}:

Without the use of the V_{O1} battery shown, V_{MIN} is pretty bad. It is,

$$V_{MIN} = V_{GS4} + V_{DS3}(\text{sat}) = V_T + 2V_{ON}$$

Minimizing V_{MIN}:

If $V_{O1} = V_T$, then $V_{MIN} = 2V_{ON}$. This is accomplished by the following circuit:

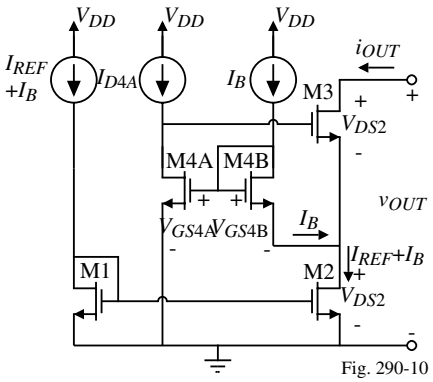

Fig. 290-10

If $V_{GS4A} - V_{GS4B} = V_{DS2}(\text{sat}) = V_{ON}$,
then $V_{MIN} = 2V_{ON}$

$$\therefore \sqrt{\frac{2I_{D4}}{K_N'(W_{4A}/L_{4A})}} - \sqrt{\frac{2I_B}{K_N'(W_{4B}/L_{4B})}} = \sqrt{\frac{2I_B+2I_{RE}}{K_N'(W_2/L}}$$

or

$$\sqrt{\frac{I_{D4}}{W_{4A}/L_{4A}}} - \sqrt{\frac{I_B}{W_{4B}/L_{4B}}} = \sqrt{\frac{I_B+I_{REF}}{W_2/L_2}}$$

A number of solutions exist. For example, let $I_B = I_{REF}$. This gives $I_{D4A} = 5.824I_{REF}$ assuming all W/L ratios are identical.

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Example 4.3-4 - Design of a Minimum V_{MIN} Regulated Cascode Current Sink

Design a regulated cascode current sink for 100μA and minimum voltage of $V_{MIN} = 0.3V$.

Solution

Let the W/L ratios of M1 through M5 be equal and let $I_B = 10\mu A$. Therefore,

$$V_{MIN} = 0.3V = V_{ON3} + V_{ON2} = \sqrt{\frac{2\cdot 100\mu A}{110\mu A/V^2(W/L)}} + \sqrt{\frac{2\cdot 110\mu A}{110\mu A/V^2(W/L)}}$$

$$= \sqrt{\frac{2\cdot 100\mu A}{110\mu A/V^2(W/L)}}\left(\sqrt{1} + \sqrt{1.1}\right)$$

Therefore,

$$0.3V = \sqrt{\frac{2\cdot 100\mu A}{110\mu A/V^2(W/L)}}(2.049)$$

$$\frac{W}{L} = \frac{2\cdot 100\mu A\cdot 2.049^2}{110\mu A/V^2 0.3^2} = 84.8 \approx 85.$$

With $I_B = 10\mu A$, then $I_{D4A} = \left(\sqrt{10} + \sqrt{110}\right)^2 = 186\mu A$

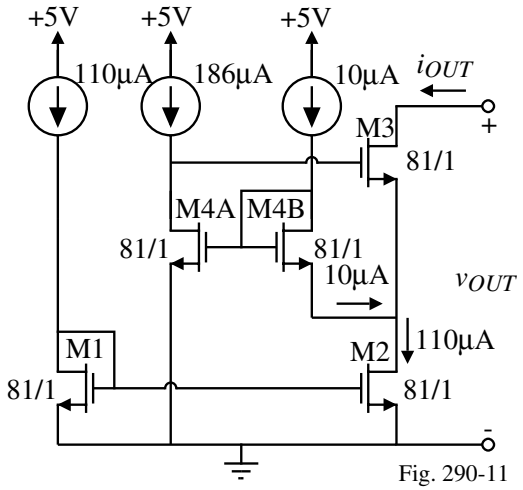

Fig. 290-11

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Comparison of the MOS Cascode Current Sink and Regulated Cascode Current Sink

Close examination in the knee area reveals interesting differences.

Simulation results:

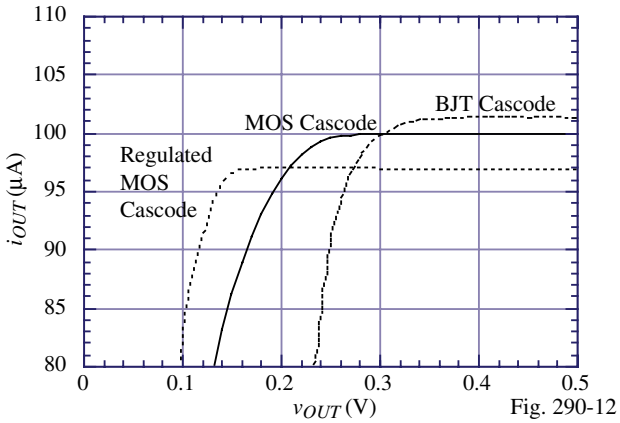

Fig. 290-12

Comments:

- The regulated cascode current is smaller than the cascode current because the drain-source voltages of M1 and M2 are not equal.
- The regulated cascode current sink has a smaller V_{MIN} due to the fact that M3 can have a drain-source voltage smaller than V_{DS}(sat).

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Summary of Current Sinks and Sources

Current Sink/Source	r_{OUT}	V_{MIN}
Simple MOS Current Sink	$r_{ds} = \frac{1}{\lambda I_D}$	$V_{DS}(\text{sat}) = V_{ON}$
Simple BJT Current Sink	$r_o = \frac{V_A}{I_C}$	$V_{CE}(\text{sat}) \approx 0.2\text{V}$
Cascode MOS	$\approx g_{m2} r_{ds2} r_{ds1}$	$V_T + 2V_{ON}$
Cascode BJT	$\approx \beta_F r_o$	$2V_{CE}(\text{sat})$
Minimum V_{MIN} Cascode Current Sink	$\approx g_{m2} r_{ds2} r_{ds1}$	$2V_{ON}$
Regulated Cascode Current Sink*	$\approx r_{ds3} g_{m3} r_{ds2} g_{m4} (r_{ds4} \| \| r_{ds5})$	$\approx V_T + V_{ON}$
Minimum V_{MIN} Regulated Cascode Current Sink*	$\approx r_{ds3} g_{m3} r_{ds2} g_{m4} (r_{ds4} \| \| r_{ds5})$	$\approx V_{ON}$

* Unfortunately, the regulated cascode current sink has a dominant pole in the feedback loop which can cause a pole-zero doublet which leads to a combination of fast and slow time constants. For this reason, the regulated cascode circuit should only be used in biasing applications unless the impact of this dynamic is understood.

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SECTION 4.4 - CURRENT MIRRORS

Characterization of Current Mirrors

A current mirror is basically nothing more than a current amplifier. The ideal characteristics of a current amplifier are:

- Output current linearly related to the input current, $i_{out} = A_i i_{in}$
- Input resistance is zero
- Output resistance is infinity

Also, the characteristic V_{MIN} applies not only to the output but also the input.

- V_{MIN}(in) is the range of v_{in} over which the input resistance is not small
- V_{MIN}(out) is the range of v_{out} over which the output resistance is not large

Graphically:

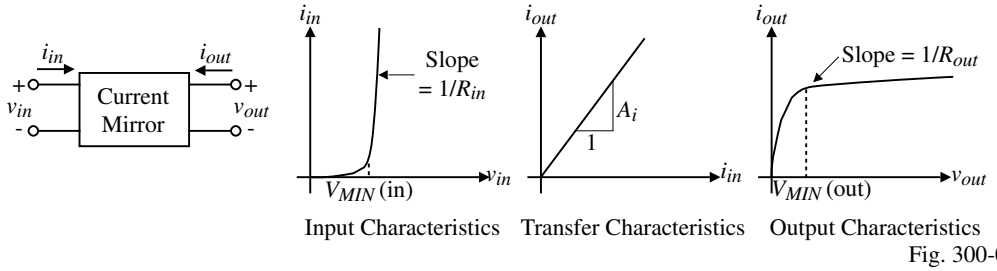

Fig. 300-01

Therefore, R_{out}, R_{in}, V_{MIN}(out), V_{MIN}(in), and A_i will characterize the current mirror.

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Simple MOS Current Mirror

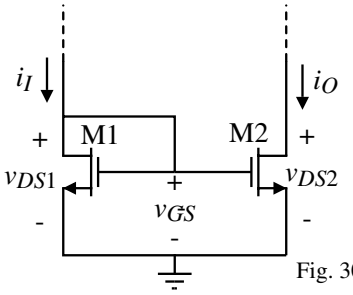

Fig. 300-02

Assume that $v_{DS2} > v_{GS} - V_{T2}$, then

$$\frac{i_O}{i_I} = \left(\frac{L_1 W_2}{W_1 L_2}\right)\left(\frac{V_{GS}-V_{T2}}{V_{GS}-V_{T1}}\right)^2\left[\frac{1 + \lambda v_{DS2}}{1 + \lambda v_{DS1}}\left(\frac{K_2'}{K_1'}\right)\right]$$

If the transistors are matched, then $K_1' = K_2'$ and $V_{T1} = V_{T2}$ to give,

$$\frac{i_O}{i_I} = \left(\frac{L_1 W_2}{W_1 L_2}\right)\left(\frac{1 + \lambda v_{DS2}}{1 + \lambda v_{DS1}}\right)$$

If $v_{DS1} = v_{DS2}$, then

$$\frac{i_O}{i_I} = \left(\frac{L_1 W_2}{W_1 L_2}\right)$$

Therefore the sources of error are 1.) $v_{DS1} \neq v_{DS2}$ and 2.) M1 and M2 are not matched.

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Influence of the Channel Modulation Parameter, λ

If the transistors are matched and the W/L ratios are equal, then

$$\frac{i_O}{i_I} = \frac{1 + \lambda v_{DS2}}{1 + \lambda v_{DS1}}$$

if the channel modulation parameter is the same for both transistors ($L_1 = L_2$).

Ratio error (%) versus drain voltage difference:

Note that one could use this effect to measure λ.

Measure V_{DS1},V_{DS2}, i_I and i_O and solve the above equation for the channel modulation parameter, λ.

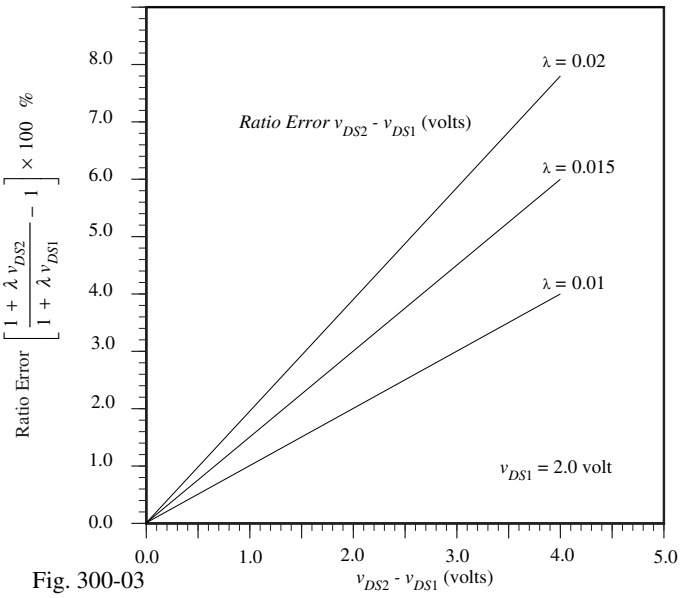

Fig. 300-03

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Influence of Mismatched Transistors

Assume that $v_{DS1} = v_{DS2}$ and that $K_1' \neq K_2'$ and $V_{T1} \neq V_{T2}$. Therefore we have

$$\frac{i_O}{i_I} = \frac{K_2'(v_{GS} - V_{T2})^2}{K_1'(v_{GS} - V_{T1})^2}$$

How do you analyze the mismatch? Use plus and minus worst case approach. Define

$\Delta K' = K'_2 - K'_1$ and $K' = 0.5(K_2' + K_1') \Rightarrow K_1' = K' - 0.5\Delta K'$ and $K_2' = K' + 0.5\Delta K'$

$\Delta V_T = V_{T2} - V_{T1}$ and $V_T = 0.5(V_{T1} + V_{T2}) \Rightarrow V_{T1} = V_T - 0.5\Delta V_T$ and $V_{T2} = V_T + 0.5\Delta V_T$

Substituting these terms into the above equation gives,

$$\frac{i_O}{i_I} = \frac{(K'+0.5\Delta K')(v_{GS} - V_T - 0.5\Delta V_T)^2}{(K'-0.5\Delta K')(v_{GS} - V_T + 0.5\Delta V_T)^2} = \frac{\left(1 + \frac{\Delta K'}{2K'}\right)\left(1 - \frac{\Delta V_T}{2(v_{GS}-V_T)}\right)^2}{\left(1 - \frac{\Delta K'}{2K'}\right)\left(1 + \frac{\Delta V_T}{2(v_{GS}-V_T)}\right)^2}$$

Assuming that the terms added to or subtracted from "1" are smaller than unity gives

$$\frac{i_O}{i_I} \approx \left(1 + \frac{\Delta K'}{2K'}\right)\left(1 + \frac{\Delta K'}{2K'}\right)\left(1 - \frac{\Delta V_T}{2(v_{GS}-V_T)}\right)^2\left(1 - \frac{\Delta V_T}{2(v_{GS}-V_T)}\right)^2 \approx 1 + \frac{\Delta K'}{K'} - \frac{2\Delta V_T}{(v_{GS}-V_T)}$$

Assume $\Delta K'/K' = \pm 5\%$ and $\Delta V_T/(v_{GS}-V_T) = \pm 10\%$.

$\therefore \quad i_O/i_I \approx 1 \pm 0.05 \pm(-0.20) = 1 \pm (0.25) \Rightarrow \pm 15\%$ error if tolerances are correlated.

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Illustration of the Offset Voltage Error Influence

Assume that $V_{T1} = 0.7\text{V}$ and $K'W/L = 110\mu\text{A/V}^2$.

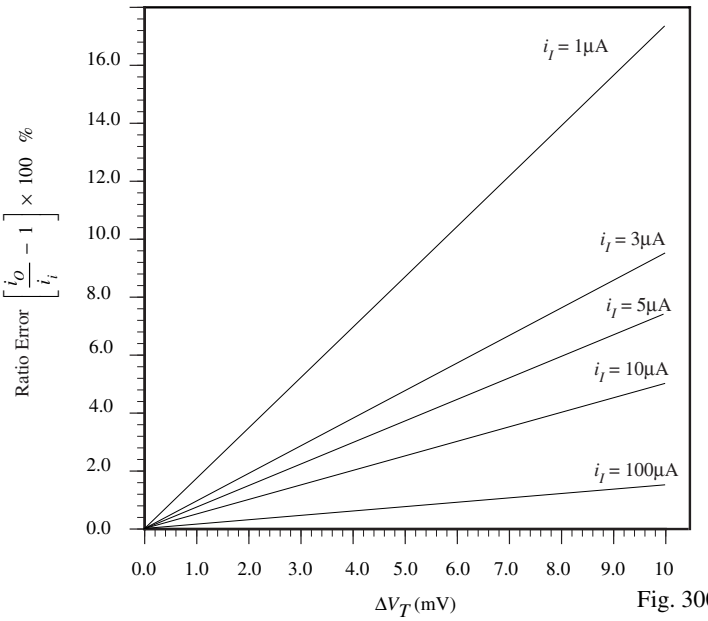

Fig. 300-4

Key: Make the part of V_{GS} causing the current to flow, V_{ON}, more significant than V_T.

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Influence of Error in Aspect Ratio of the Transistors

Example 1 - Aspect Ratio Errors in Current Mirrors

Figure 4.4-4 shows the layout of a one-to-four current amplifier. Assume that the lengths are identical ($L_1 = L_2$) and find the ratio error if $W_1 = 5 \pm 0.1$ μm. The actual widths of the two transistors are

$$W_1 = 5 \pm 0.1 \ \mu\text{m} \quad \text{and} \quad W_2 = 20 \pm 0.1 \ \mu\text{m}$$

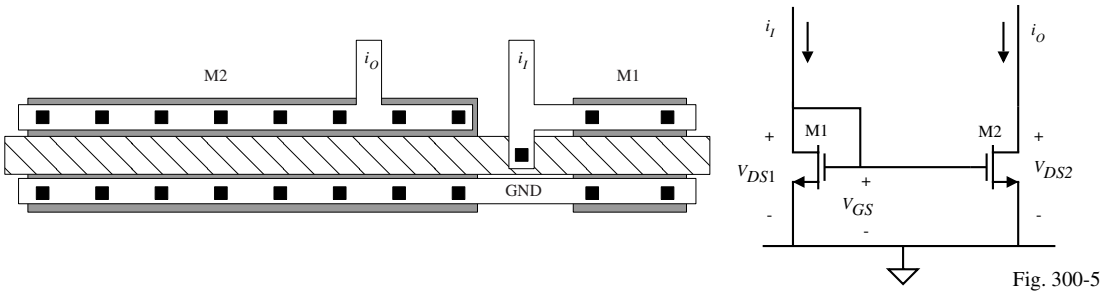

Fig. 300-5

Solution

We note that the tolerance is not multiplied by the nominal gain factor of 4. The ratio of W_2 to W_1 and consequently the gain of the current amplifier is

$$\frac{i_O}{i_I} = \frac{W_2}{W_1} = \frac{20 \pm 0.1}{5 \pm 0.1} = 4\left(\frac{1 \pm (0.1/20)}{1 \pm (0.1/5)}\right) \approx 4\left(1 \pm \frac{0.1}{20}\right)\left(1 - \frac{\pm 0.1}{5}\right) \approx 4\left(1 \pm \frac{0.1}{20} - \frac{\pm 0.4}{20}\right) = 4 - (\pm 0.03)$$

where we have assumed that the variations would both have the same sign (correlated). It is seen that this ratio error is 0.75% of the desired current ratio or gain.

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Influence of Error in Aspect Ratio of the Transistors-Continued

Example 2 - Reduction of the Aspect Ratio Errors in Current Mirrors

Use the layout technique illustrated in Fig. 4.4-5 and calculate the ratio error of a current amplifier having the specifications of the previous example.

Solutions

The actual widths of M1 and M2 are

$$W_1 = 5 \pm 0.1 \ \mu\text{m} \quad \text{and} \quad W_2 = 4(5 \pm 0.1) \ \mu\text{m}$$

The ratio of W_2 to W_1 and consequently the current gain is given below and is for all practical purposes independent of layout error.

$$\frac{i_O}{i_I} = \frac{4(5 \pm 0.1)}{5 \pm 0.1} = 4$$

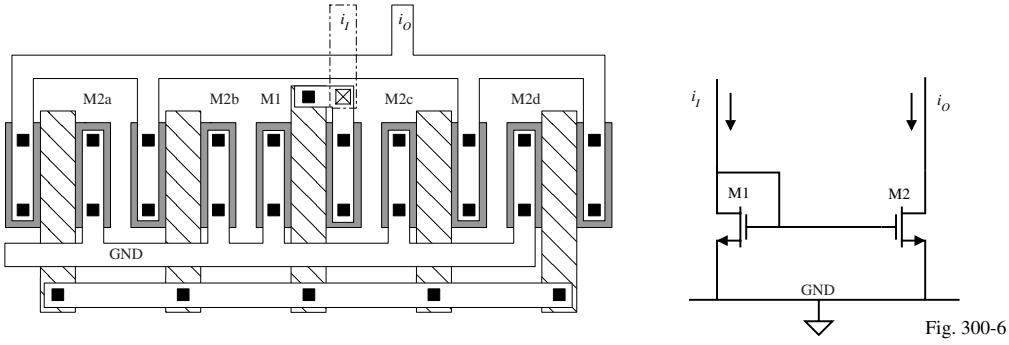

Fig. 300-6

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Summary of the Simple MOS Current Mirror/Amplifier

- Minimum input voltage is $V_{MIN}(\text{in}) = V_T + V_{ON}$

  Okay, but could be reduced to V_{ON}.

  Principle:

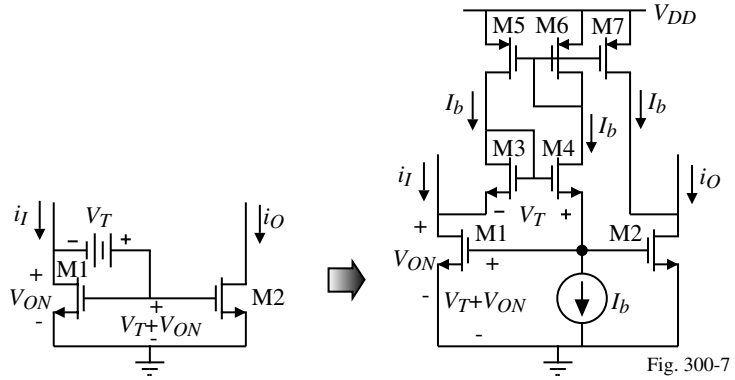

Fig. 300-7

  Will deal with later in low voltage op amps.

- Minimum output voltage is $V_{MIN}(\text{out}) = V_{ON}$
- Output resistance is $R_{out} = \dfrac{1}{\lambda I_D}$
- Input resistance is $R_{in} \approx \dfrac{1}{g_m}$
- Current gain accuracy is poor because $v_{DS1} \neq v_{DS2}$

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MOS Cascode Current Mirror

Improving the output resistance:

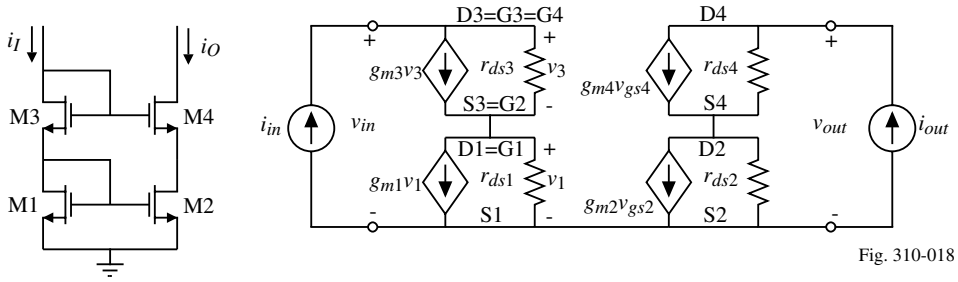

Fig. 310-018

- R_{out}:

  $v_{out} = r_{ds4}(i_{out} - g_{m4}v_{gs4}) + r_{ds2}(i_{out} - g_{m2}v_{gs2})$

  But, $i_{in} = 0$ so that $v_1 = v_3 = 0 \quad \Rightarrow \quad v_{gs4} = -v_{s4} = -i_{out}r_{ds2}$ and $v_{gs2} = 0$

  $\therefore \quad v_{out} = i_{out}[r_{ds4} + r_{ds2} + g_{m4}r_{ds2}r_{ds4}] \approx r_{ds2}g_{m4}r_{ds4}$

- R_{in}:

  $$R_{in} = \frac{1}{g_{m3}} \| r_{ds3} + \frac{1}{g_{m1}} \| r_{ds1} \approx \frac{1}{g_{m1}} + \frac{1}{g_{m3}} \approx \frac{2}{g_m}$$

- $V_{MIN}(\text{out}) = V_T + 2V_{ON}$
- $V_{MIN}(\text{in}) = 2(V_T + V_{ON})$
- Current gain match: Excellent since $v_{DS1} = v_{DS2}$

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Large Output Swing Cascode Current Mirror

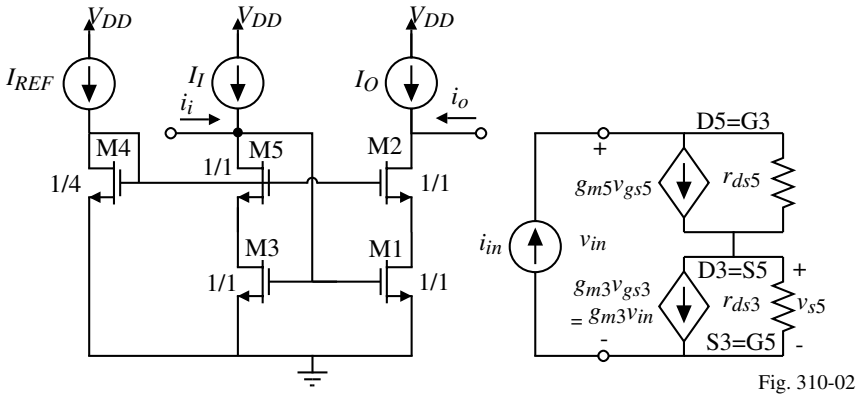


Fig. 310-02

- $R_{out} \approx g_{m2}r_{ds2}r_{ds1}$
- $R_{in} = ? v_{in} = r_{ds5}(i_{in}-g_{m5}v_{gs5})+v_{s5} = r_{ds5}(i_{in}+g_{m5}v_{s5})+v_{s5} = r_{ds5}i_{in}+(1+g_{m5}r_{ds5})v_{s5}$

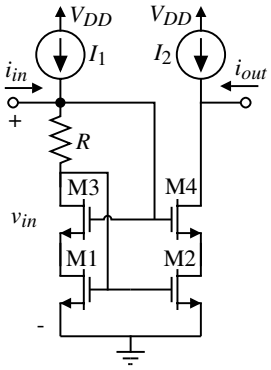
  But, $v_{s5} = r_{ds3}(i_{in} - g_{m3}v_{in})$

  $\therefore \quad v_{in} = r_{ds5}i_{in} + (1+g_{m5}r_{ds5})r_{ds3}i_{in} - g_{m3}r_{ds3}(1+g_{m5}r_{ds5})v_{in}$

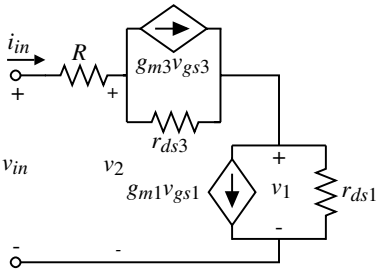
  $$R_{in} = \frac{v_{in}}{i_{in}} = \frac{r_{ds5} + r_{ds3} + r_{ds3}g_{m5}r_{ds5}}{g_{m3}r_{ds3}(1+g_{m5}r_{ds5})} \approx \frac{1}{g_{m3}}$$

- $V_{MIN}(\text{out}) = 2V_{ON}$
- $V_{MIN}(\text{in}) = V_T + V_{ON}$
- Current gain is excellent because $v_{DS1} = v_{DS3}$.

Self-Biased Cascode Current Mirror



Self-biased, cascode current mirror



Small-signal model to calculate R_{in}.

Fig. 310-03

- $R_{in} = ?$

$v_{in} = i_{in}R + r_{ds3}(i_{in}-g_{m3}v_{gs3})$
$\quad + r_{ds1}(i_{in}-g_{m1}v_{gs1})$

But,

$v_{gs1} = v_{in}-i_{in}R$

and

$v_{gs3} = v_{in}-r_{ds1}(i_{in}-g_{m1}v_{gs1}) = v_{in}-r_{ds1}i_{in}+g_{m1}r_{ds1}(v_{in}-i_{in}R)$

$\therefore \; v_{in} = i_{in}R+r_{ds3}i_{in}-g_{m3}r_{ds3}[v_{in}-r_{ds1}i_{in}+g_{m1}r_{ds1}(v_{in}-i_{in}R)]+r_{ds1}[i_{in}-g_{m1}(v_{in}+i_{in}R)]$

$v_{in}[1+g_{m3}r_{ds3}+g_{m1}r_{ds1}g_{m3}r_{ds3}+g_{m1}r_{ds1}]$
$\quad = i_{in}[R+r_{ds1}+r_{ds3}+g_{m3}r_{ds3}r_{ds1}+ g_{m1}r_{ds1}g_{m3}r_{ds3}R]$

$$R_{in} = \frac{R + r_{ds1} + r_{ds3} + g_{m3}r_{ds3}r_{ds1} + g_{m1}r_{ds1}g_{m3}r_{ds3}R}{1 + g_{m3}r_{ds3} + g_{m1}r_{ds1}g_{m3}r_{ds3} + g_{m1}r_{ds1}} \approx \frac{1}{g_{m1}} + R$$

- $R_{out} \approx g_{m4}r_{ds4}r_{ds2}$
- $V_{MIN}(\text{in}) = V_T + 2V_{ON}$ • $V_{MIN}(\text{out}) = 2V_{ON}$ • Current gain matching is excellent

Wilson MOS Current Mirror

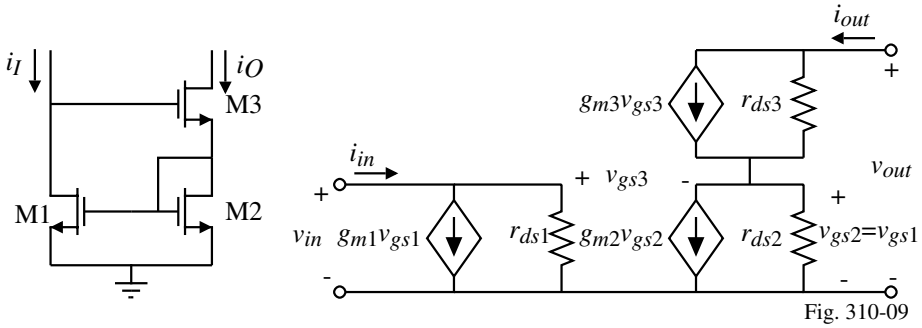


Fig. 310-09

Uses negative series feedback to achieve higher output resistance.

- $R_{out} = ?\ (i_{in}=0)$ $\quad v_{out} = r_{ds2}(i_{out} - g_{m3}v_{gs3}) + v_{gs2}$

$$v_{gs2} = \frac{i_{out}}{g_{m2}+g_{ds2}} = \frac{r_{ds2}i_{out}}{1+g_{m2}r_{ds2}} \quad \text{and} \quad v_{gs3} = -g_{m1}r_{ds1}v_{gs2} - v_{gs2} = -(1+g_{m1}r_{ds1})v_{gs2}$$

$$\therefore\ v_{out} = r_{ds2}i_{out} + g_{m3}r_{ds2}(1+g_{m1}r_{ds1})v_{gs2} = i_{out}\left[r_{ds3}+r_{ds2}\left(\frac{1+g_{m3}r_{ds2}+g_{m1}r_{ds1}g_{m3}r_{ds3}}{1+g_{m2}r_{ds2}}\right)\right]$$

$$R_{out} = r_{ds3}+r_{ds2}\left(\frac{1+g_{m3}r_{ds2}+g_{m1}r_{ds1}g_{m3}r_{ds3}}{1+g_{m2}r_{ds2}}\right) \approx \frac{g_{m1}r_{ds1}g_{m3}r_{ds3}}{g_{m2}}$$

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Wilson Current Mirror - Continued

- $R_{in} = ?\ \ (v_{out} = 0)$

$$i_{in} \approx g_{m1}v_{gs1} = \frac{g_{m1}g_{m3}v_{gs3}}{g_{m2}+g_{ds2}+g_{ds3}} \approx \frac{g_{m1}g_{m3}v_{gs3}}{g_{m2}}$$

$$v_{gs3} = v_{in} - v_{gs1} = v_{in} - \frac{g_{m1}g_{m3}v_{gs3}}{g_{m2}} \quad \Rightarrow \quad v_{gs3} = \frac{v_{in}}{1+\frac{g_{m1}g_{m3}}{g_{m2}}}$$

$$\therefore \quad i_{in} \approx \frac{g_{m1}g_{m3}\,v_{in}}{g_{m2}+g_{m3}} \quad \Rightarrow \quad R_{in} = \frac{g_{m2}+g_{m3}}{g_{m1}g_{m3}}$$

- $V_{MIN}(\text{in}) = 2(V_T+V_{ON})$
- $V_{MIN}(\text{out}) = V_T + 2V_{ON}$
- Current gain matching - poor, $v_{DS1} \neq v_{DS2}$

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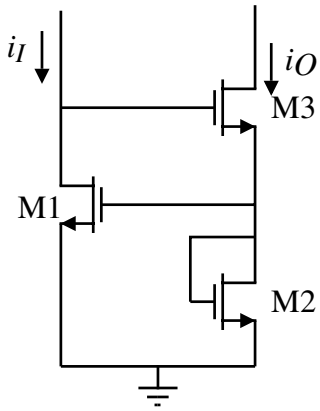
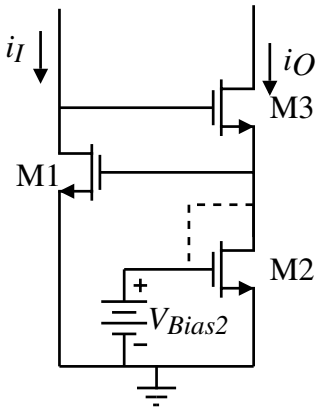
Evolution of the Regulated Cascode Current Mirror from the Wilson Current Mirror



Wilson Current Mirror Redrawn



Regulated Cascode Current Sink

Fig. 310-10

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MOS Regulated Cascode Current Mirror

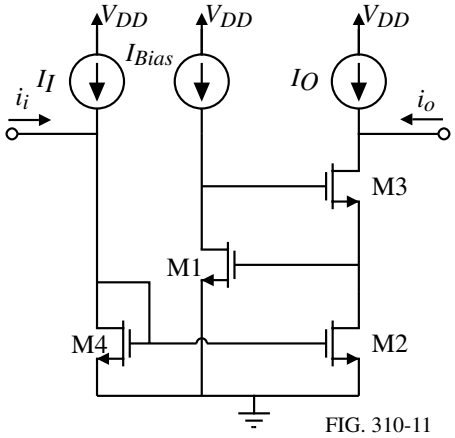

FIG. 310-11

- $R_{out} \approx g_m{}^2 r_{ds}{}^3$
- $R_{in} \approx \dfrac{1}{g_{m4}}$
- $V_{MIN}(\text{out}) = V_T + 2V_{ON}$ (Can be reduced to $2V_{ON}$)
- $V_{MIN}(\text{in}) = V_T + V_{ON}$ (Can be reduced to V_{ON})
- Current gain matching - good as long as $v_{DS4} = v_{DS2}$

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SUMMARY

Summary of MOS Current Mirrors

Current Mirror	Accuracy	Output Resistance	Input Resistance	Minimum Output Voltage	Minimum Input Voltage
Simple	Poor	r_{ds}	$\frac{1}{g_m}$	V_{ON}	V_T+V_{ON}
Cascode	Excellent	$g_m r_{ds}^2$	$\frac{2}{g_m}$	V_T+2V_{ON}	$2(V_T+V_{ON})$
Wide Output Swing Cascode	Excellent	$g_m r_{ds}^2$	$\frac{1}{g_m}$	$2V_{ON}$	V_T+V_{ON}
Self-biased Cascode	Excellent	$g_m r_{ds}^2$	$R+\frac{1}{g_m}$	$2V_{ON}$	V_T+2V_{ON}
Wilson	Poor	$g_m r_{ds}^2$	$\frac{2}{g_m}$	$2(V_T+V_{ON})$	V_T+2V_{ON}
Regulated Cascode	Good-Excellent	$g_m^2 r_{ds}^3$	$\frac{1}{g_m}$	V_T+2V_{ON} (min. is $2V_{ON}$)	V_T+V_{ON} (min. is V_{ON})

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SECTION 4.5 - CURRENT AND VOLTAGE REFERENCES

Characteristics of a Voltage or Current Reference

What is a Voltage or Current Reference?

A voltage or current reference is an independent voltage or current source that has a high degree of precision and stability.

Requirements of a Reference Circuit:

- Should be independent of power supply
- Should be independent of temperature
- Should be independent of processing variations
- Should be independent of noise and other interference

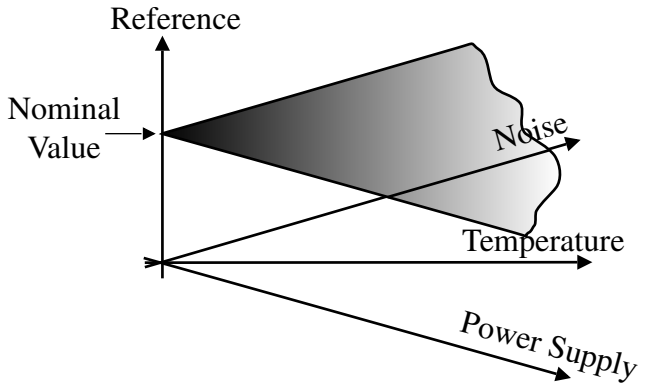

Fig. 4.5-1

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REFERENCES WITH POWER SUPPLY INDEPENDENCE

Power Supply Independence

How do you characterize power supply independence?

Use the concept of:

$$S_{V_{DD}}^{I_{REF}} = \frac{\partial I_{REF}/I_{REF}}{\partial V_{DD}/V_{DD}} = \frac{V_{DD}}{I_{REF}}\left(\frac{\partial I_{REF}}{\partial V_{DD}}\right)$$

Application of sensitivity to determining power supply dependence:

$$\frac{\partial I_{REF}}{I_{REF}} = \left(S_{V_{DD}}^{I_{REF}}\right)\frac{\partial V_{DD}}{V_{DD}}$$

Thus, the fractional change in the reference voltage is equal to the sensitivity times the fractional change in the power supply voltage.

For example, if the sensitivity is 1, then a 10% change in V_{DD} will cause a 10% change in I_{REF}.

Ideally, we want $S_{V_{DD}}^{I_{REF}}$ to be zero for power supply independence.

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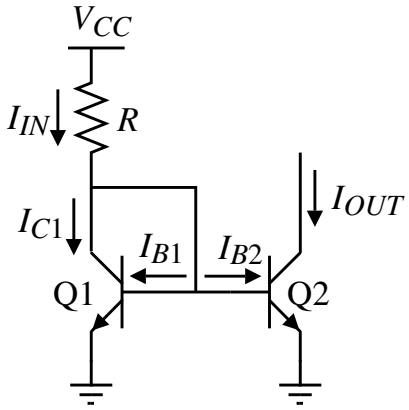
Simple Current Reference



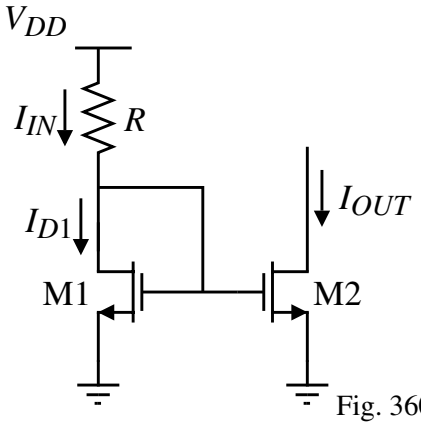


Fig. 360-02

$$I_{OUT} \approx \frac{V_{CC}\text{-}V_{BE}}{R}\left(\frac{1}{1+\frac{2}{\beta_F}}\right)$$

$$I_{OUT} \approx \frac{V_{DD}\text{-}V_{GS}}{R} = \frac{V_{DD} - \sqrt{\frac{2I_{IN}}{\beta_1}} - V_T}{R}$$

$$S_{V_{CC}}^{I_{REF}} = 1$$

$$S_{V_{DD}}^{I_{REF}} = 1$$

Temperature and process dependence?

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MOS Widlar Current Reference

Operation:

$$V_{GS1} - V_{GS2} - I_{OUT}R_2 = 0$$

$$I_{OUT}R_2 + V_{ON2} - V_{ON1} = 0$$

Assuming strong inversion and $\lambda \rightarrow 0$,

$$I_{OUT}R_2 + \sqrt{\frac{2I_{OUT}}{K'(W_2/L_2)}} - V_{ON1} = 0$$

Solving for $\sqrt{I_{OUT}}$ gives,

$$\sqrt{I_{OUT}} = \frac{-\sqrt{\frac{2}{K'(W_2/L_2)}} + \sqrt{\frac{2}{K'(W_2/L_2)} + 4R_2V_{ON1}}}{2R_2}$$

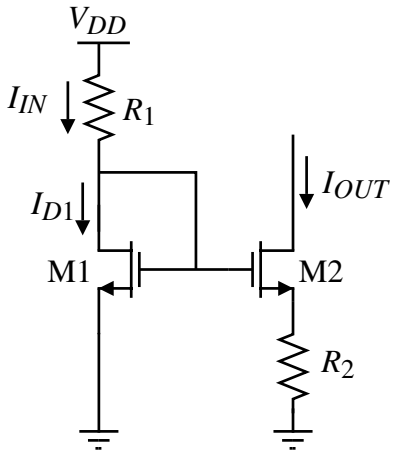

Fig. 360-04

where $V_{ON1} = \sqrt{\frac{2I_{IN}}{K'(W_1/L_1)}}$

Differentiating I_{OUT} with respect to V_{DD} gives,

$$\frac{1}{2\sqrt{I_{OUT}}}\frac{dI_{OUT}}{dV_{DD}} = \frac{1}{\sqrt{2/(K'W_2/L_2) + 4R_2V_{ON1}}}\frac{dV_{ON1}}{dV_{DD}}, \qquad \frac{dV_{ON1}}{dV_{DD}} = \frac{V_{ON1}}{2I_{IN}}\frac{dI_{IN}}{dV_{DD}}$$

$$\therefore \quad S_{V_{DD}}^{I_{REF}} = S_{V_{DD}}^{I_{OUT}} = \frac{V_{ON1}}{\sqrt{V_{ON2}^2 + 4I_{OUT}R_2V_{ON1}}} S_{V_{DD}}^{I_{IN}} \approx \frac{V_{ON1}}{\sqrt{4V_{ON1}^2}} S_{V_{DD}}^{I_{IN}} = 0.5S_{V_{DD}}^{I_{IN}}$$

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Example 4.5-1

For the MOS Widlar current reference, find I_{OUT} if $I_{IN} = 100\mu A$, $R_2 = 4k\Omega$, $K' = 200\mu A/V^2$, and $W_2/L_2 = W_1/L_1 = 25$. Assume the temperature is 27°C and that $n = 1.5$. Find the sensitivity of I_{OUT} with respect to V_{DD}.

Solution

$$V_{ON1} = \sqrt{\frac{2I_{IN}}{K'(W_1/L_1)}} = \sqrt{\frac{2\cdot 100}{200\cdot 25}} = 0.2V$$

$$\sqrt{I_{OUT}} = \frac{-\sqrt{\frac{2}{200\cdot 25}} + \sqrt{\frac{2}{200\cdot 25} + 4(0.004)0.2}}{20.004}\sqrt{\mu A} = 5\sqrt{\mu A} \quad \Rightarrow \quad I_{OUT} = 25\mu A$$

Note that $V_{ON2} = V_{ON1} - I_{OUT}R_2 = 0.2\text{-}(25)(0.004) = 0.1V > 2nV_t = 78mV$ so both transistors are in strong inversion.

For the sensitivity calculations, assume that $V_{DD} >> V_{GS1}$. Therefore $I_{IN} \approx V_{DD}/R_1$.

$$S_{V_{DD}}^{I_{REF}} = \frac{V_{ON1}}{\sqrt{4V_{ON2}^2}} S_{V_{DD}}^{I_{IN}} \approx \frac{V_{ON1}}{\sqrt{4V_{ON2}^2}} = 0.5$$

Therefore, a 10% variation in V_{DD} causes a 5% variation in I_{OUT}.

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MOS Peaking Current Reference

Strong Inversion Operation:

$$V_{GS1} - I_{IN}R - V_{GS2} = 0$$

$$V_{ON2} = V_{ON1} - I_{IN}R$$

$$I_{OUT} = \frac{K'(W_2/L_2)}{2} V_{ON2}^2$$

$$= \frac{K'(W_2/L_2)}{2} (V_{ON1} - I_{IN}R)^2$$

where

$$V_{ON1} = \sqrt{\frac{2I_{IN}}{K'(W_1/L_1)}}$$

Weak Inversion Operation:

$$V_{GS2} - V_T \approx nV_t \ln\left(\frac{I_{IN}}{(W_1/L_1)I_T}\right) - I_{IN}R$$

If the transistors are identical and $V_{DS2} > 3V_T$,

$$I_{OUT} = \frac{W_1}{L_1} I_T \exp\left(\frac{V_{GS2} - V_T}{nV_t}\right) \approx I_{IN} \exp\left(\frac{-I_{IN}R}{nV_t}\right)$$

Circuit:

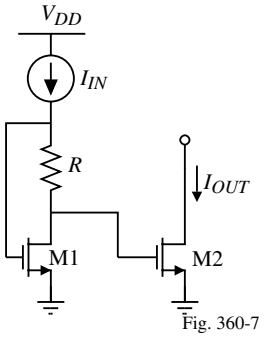

Fig. 360-7

Transfer Characteristics:

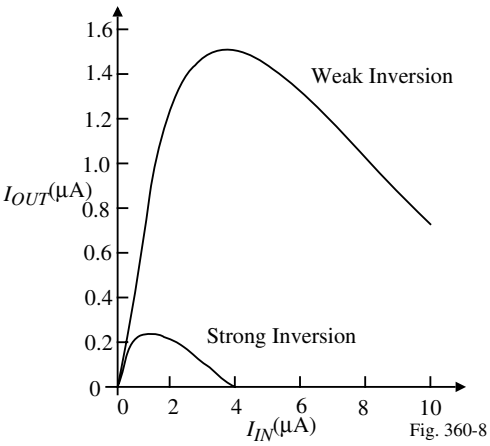

Fig. 360-8

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Threshold Referenced Current Reference

Circuit:

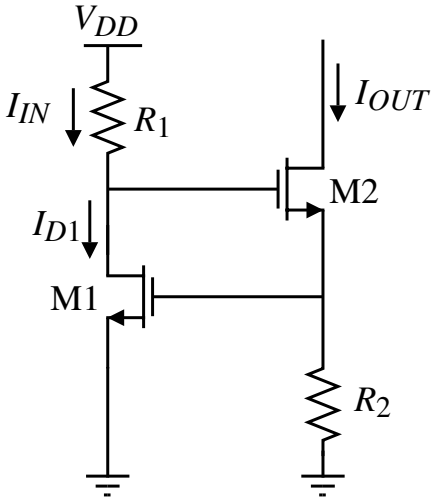

Fig. 360-10

Operation:

$$I_{OUT} = \frac{V_{GS1}}{R_2} = \frac{V_T + \sqrt{\frac{2I_{IN}}{K'(W_1/L_1)}}}{R_2}$$

$$\approx \frac{V_T}{R_2} \text{ if } V_T > V_{ON1}$$

The sensitivity of I_{OUT} with respect to V_{DD} is

$$S_{V_{DD}}^{I_{OUT}} = \left(\frac{V_{ON1}}{I_{OUT}R_2}\right) S_{V_{DD}}^{I_{IN}} = \left(\frac{V_{ON1}}{2V_{GS1}}\right) S_{V_{DD}}^{I_{IN}}$$

For example, if $V_T = 1\text{V}$, $V_{ON1} = 0.1\text{V}$ and $S_{V_{DD}}^{I_{IN}} \approx 1$, then

$$S_{V_{DD}}^{I_{OUT}} = \left(\frac{0.1}{2 \cdot 1.1}\right) = 0.045$$

Therefore, if V_{DD} changes by 10%, I_{REF} or I_{OUT} changes by 0.45%.

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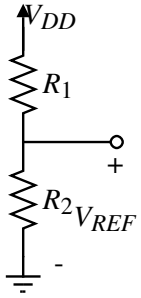
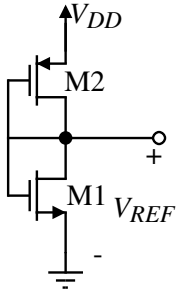
SIMPLE BIAS/REFERENCE CIRCUITS

Voltage References using Voltage Division



Resistor voltage divider.



Active device voltage divider. Fig. 370-01

$$V_{REF} = \frac{R_2}{R_1+R_2} V_{DD}$$

$$V_{REF} = \frac{V_{TN} + \sqrt{(\beta_P/\beta_N)}\,(V_{DD}-|V_{TP}|)}{1 + \sqrt{(\beta_P/\beta_N)}}$$

$$S_{V_{DD}}^{V_{REF}} = 1$$

$$S_{V_{DD}}^{V_{REF}} = \frac{V_{DD}}{V_{REF}}\left(\frac{\sqrt{(\beta_P/\beta_N)}}{1+\sqrt{(\beta_P/\beta_N)}}\right) = \frac{V_{DD}\sqrt{(\beta_P/\beta_N)}}{V_{TN} + \sqrt{(\beta_P/\beta_N)}\,(V_{DD}-|V_{TP}|)}$$

$$= \frac{V_{DD}\sqrt{(\beta_P/\beta_N)}}{V_{TN} + \sqrt{(\beta_P/\beta_N)}\,(V_{DD}-|V_{TP}|)}$$

Assume $\beta_N = \beta_P$ and $V_{TN} = |V_{TP}| \quad \Rightarrow \quad S_{V_{DD}}^{V_{REF}} = 1$

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References with Sensitivity Less than One

In order to get sensitivities less than one, the upper and lower circuits must be different with the lower circuit less dependent on V_{DD}.

In otherwords, the upper circuit should act like a current source and the lower circuit like a voltage source.

Principle:

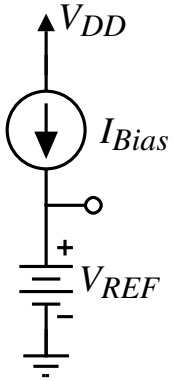

Fig. 370-02

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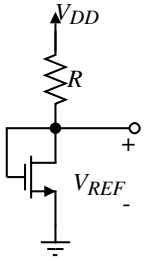
MOSFET-Resistance Voltage References



$$V_{REF} = V_{GS} = V_T + \sqrt{\frac{2(V_{DD}-V_{REF})}{\beta R}}$$

$$\text{or } V_{REF} = V_T - \frac{1}{\beta R} + \sqrt{\frac{2(V_{DD}-V_T)}{\beta R} + \frac{1}{(\beta R)^2}}$$

$$S_{V_{DD}}^{V_{REF}} = \left(\frac{1}{1 + \beta(V_{REF}-V_T)R}\right)\left(\frac{V_{DD}}{V_{REF}}\right)$$

Assume that V_{DD} = 5V, W/L = 2 and R = 100kΩ,

Thus, $V_{REF} \approx 1.281\text{V}$ and $S_{V_{REF}}^{V_{DD}} = 0.283$

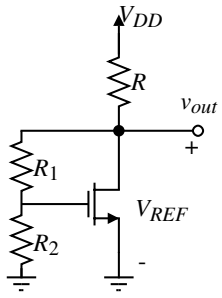


Fig. 370-03

This circuit allows V_{REF} to be larger.

If the current in R_1 (and R_2) is small compared to the current flowing through the transistor, then

$$V_{REF} \approx \left(\frac{R_1 + R_2}{R_2}\right) V_{GS}$$

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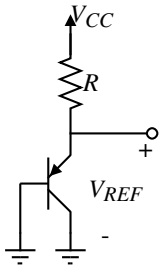
Bipolar-Resistance Voltage References



$$V_{REF} = V_{EB} = \frac{kT}{q}\ln\left(\frac{I}{I_S}\right)$$

$$I = \frac{V_{CC} - V_{EB}}{R} \cong \frac{V_{CC}}{R}$$

$$V_{REF} \cong \frac{kT}{q}\ln\left(\frac{V_{CC}}{RI_S}\right)$$

$$S_{V_{CC}}^{V_{REF}} = \frac{1}{\ln[V_{CC}/(RI_S)]} = \frac{1}{\ln(I/I_S)}$$

If V_{CC}=5V, R = 4.3kΩ and I_S = 1fA, then V_{REF} = 0.719V.

Also, $S_{V_{CC}}^{V_{REF}} = 0.0362$

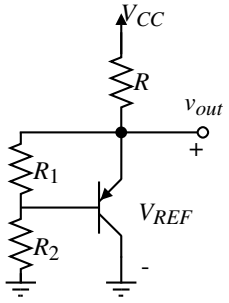


Fig. 370-04

If the current in R_1 (and R_2) is small compared to the current flowing through the transistor, then

$$V_{REF} \approx \left(\frac{R_1 + R_2}{R_2}\right) V_{EB}$$

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Example 1 - Design of a Higher-Voltage Bipolar Voltage Reference

Use the circuit on the previous slide to design a voltage reference having V_{REF} = 2.5V when V_{CC} = 5V. Assume I_s = 1fA and β_F = 100. Evaluate the sensitivity of V_{REF} with respect to V_{CC}.

Solution

Choose I (the current flowing through R) to be 100μA.

Therefore $R = \dfrac{V_{CC}\text{-}V_{REF}}{100\mu A} = \dfrac{2.5V}{100\mu A} = 25k\Omega$.

Choose I_1(the current flowing through R_1) to be 50μA. Therefore the current flowing in the emitter is 50μA. The value of $V_{EB} = V_t \ln\left(\dfrac{50\mu A}{1fA}\right) = 0.638V$.

$\therefore\ R_1 = \dfrac{0.638V}{50\mu A} = 12.76k\Omega$

With 50μA in the emitter, the base current is approximately 5μA.

Therefore, the current through R_2 is 55μA.

Since $V_{REF} = I_{R2}R_2 + 0.638V = 2.5V$, we get $R_2 = \left(\dfrac{2.5V\text{-}0.638V}{55\mu A}\right) = 33.85k\Omega$.

The sensitivity of V_{REF} with respect to V_{CC} is

$$S_{V_{CC}}^{V_{REF}} = \left(\frac{R_1+R_2}{R_1}\right)S_{V_{CC}}^{V_{EB}} = \left(\frac{12.76k\Omega+33.85k\Omega}{12.76k\Omega}\right)\left(\frac{1}{\ln(I_Q/I_s)}\right) = 3.652(0.0406) = 0.148$$

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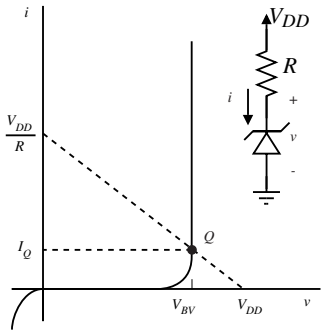
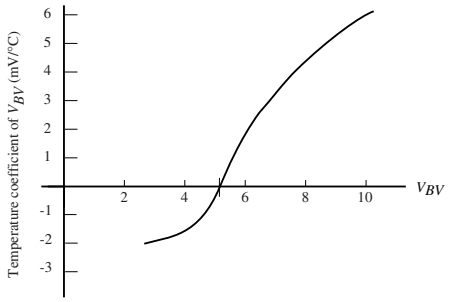
Breakdown Diode Voltage References

If the power supply voltage is high enough, i.e. $V_{DD} \approx 10V$, the breakdown diode can be used as a voltage reference.



V-I characteristics of a breakdown diode.



Variation of the temperature coefficient of the breakdown diode as a function of the breakdown voltage, BV.

Fig. 370-05

$$V_{REF} = V_{BV}$$

$$S_{V_{DD}}^{V_{REF}} = \left(\frac{\partial V_{REF}}{\partial V_{DD}}\right)\left(\frac{V_{DD}}{V_{REF}}\right) \cong \left(\frac{v_{ref}}{v_{dd}}\right)\left(\frac{V_{DD}}{V_{BV}}\right) = \left(\frac{r_Z}{r_Z+R}\right)\left(\frac{V_{DD}}{V_{BV}}\right)$$

where r_z is the small-signal impedance of the breakdown diode at I_Q (30 to 100Ω).

Typical sensitivities are 0.02 to 0.05.

Note that the temperature dependence could be zero if V_B was a variable.

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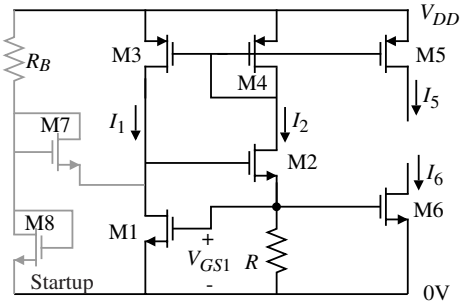
BOOTSTRAPPED BIAS/REFERENCE CIRCUITS

Bootstrapped Current Source

So far, none of the previous references except the base-emitter and threshold-referenced sources have shown very good independence from power supply. Let us now examine a technique which does achieve the desired independence.

Circuit:



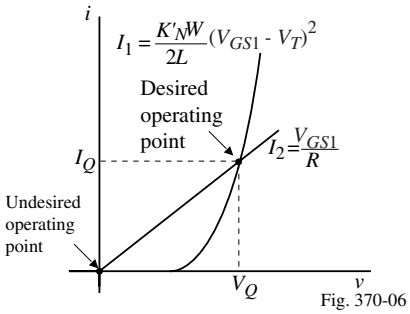


Fig. 370-06

Principle:

If M3 = M4, then $I_1 \approx I_2$. However, the M1-R loop gives $V_{GS1} = V_{T1} + \sqrt{\frac{2I_1}{K_N'(W_1/L_1)}}$

Solving these two equations gives $I_2 = \frac{V_{GS1}}{R} = \frac{V_{T1}}{R} + \left(\frac{1}{R}\right)\sqrt{\frac{2I_1}{K_N'(W_1/L_1)}}$

The output current, $I_{out} = I_1 = I_2$ can be solved as $I_{out} = \frac{V_{T1}}{R} + \frac{1}{\beta_1 R^2} + \frac{1}{R}\sqrt{\frac{2V_{T1}}{\beta_1 R} + \frac{1}{(\beta_1 R)^2}}$

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Simulation Results for the Bootstrapped Current Source

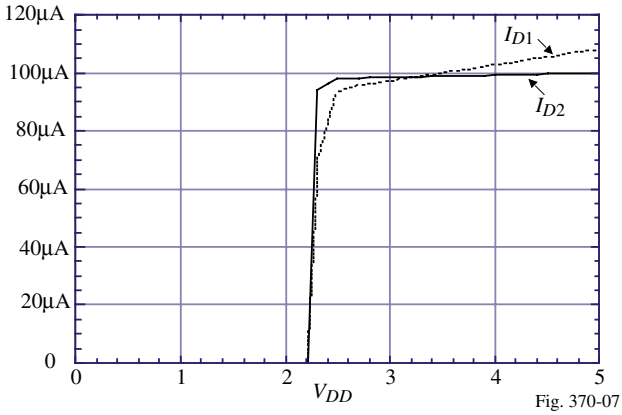

Fig. 370-07

The current I_{D2} appears to be okay, why is I_{D1} increasing?

Apparently, the channel modulation on the current mirror M3-M4 is large.

At V_{DD} = 5V, V_{SD3} = 2.83V and V_{SD4} = 1.09V which gives $I_{D3} = 1.067 I_{D4}$ $\approx$ 107µA

Need to cascode the upper current mirror.

SPICE Input File:

```
Simple, Bootstrap Current Reference
VDD 1 0 DC 5.0                      RB 1 6 100KILOHM
VSS 9 0 DC 0.0                      .OP
M1 5 7 9 9 N W=20U L=1U             .DC VDD 0 5 0.1
M2 3 5 7 9 N W=20U L=1U             .MODEL N NMOS VTO=0.7 KP=110U
M3 5 3 1 1 P W=25U L=1U             GAMMA=0.4 +PHI=0.7 LAMBDA=0.04
M4 3 3 1 1 P W=25U L=1U             .MODEL P PMOS VTO=-0.7 KP=50U
M5 9 3 1 1 P W=25U L=1U             GAMMA=0.57 +PHI=0.8 LAMBDA=0.05
R 7 9 10KILOHM                      .PRINT DC ID(M1) ID(M2) ID(M5)
M8 6 6 9 9 N W=1U L=1U              .PROBE
M7 6 6 5 9 N W=20U L=1U             .END
```

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Cascoded Bootstrapped Current Source

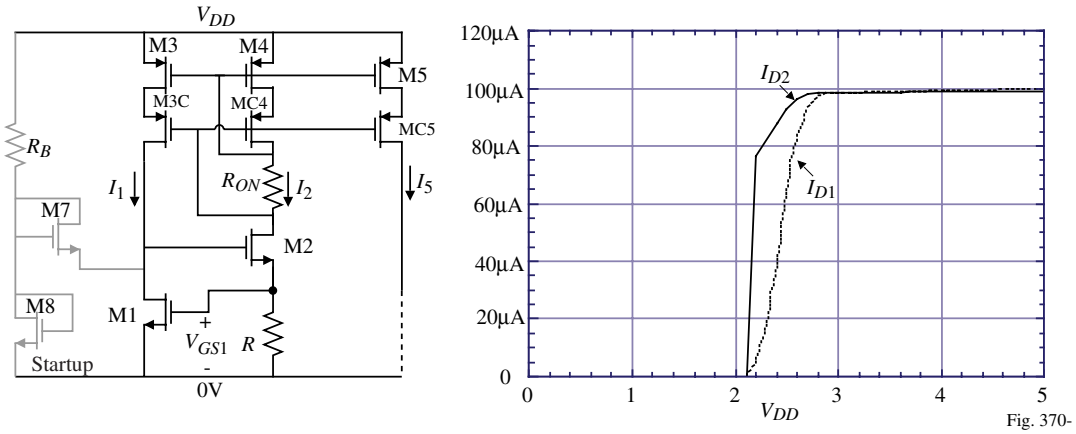

Fig. 370-

SPICE Input File:

```
Cascode, Bootstrap Current Reference
VDD 1 0 DC 5.0
VSS 9 0 DC 0.0
M1 5 7 9 9 N W=20U L=1U
M2 4 5 7 9 N W=20U L=1U
M3 2 3 1 1 P W=25U L=1U
M4 8 3 1 1 P W=25U L=1U
M3C 5 4 2 1 P W=25U L=1U
MC4 3 4 8 1 P W=25U L=1U
RON 3 4 4KILOHM
M5 9 3 1 1 P W=25U L=1U
R 7 9 10KILOHM
M8 6 6 9 9 N W=1U L=1U
M7 6 6 5 9 N W=20U L=1U
RB 1 6 100KILOHM
.OP
.DC VDD 0 5 0.1
.MODEL N NMOS VTO=0.7
KP=110U GAMMA=0.4 PHI=0.7
LAMBDA=0.04
.MODEL P PMOS VTO=-0.7
KP=50U GAMMA=0.57 PHI=0.8
LAMBDA=0.05
.PRINT DC ID(M1) ID(M2) ID(M5)
.PROBE
.END
```


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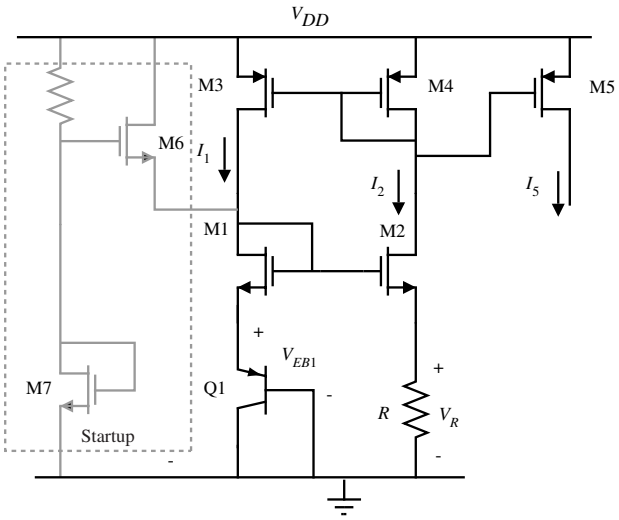
Base-Emitter Referenced Circuit



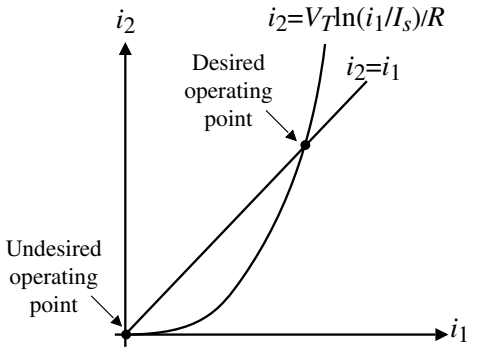


Fig. 370-09

$$I_{out} = I_2 = \frac{V_{EB1}}{R}$$

BJT can be a MOSFET in weak inversion.

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Low Voltage Bootstrap MOS Circuit

The previous bootstrap circuits required at least 2 volts across the power supply before operating.

A low-voltage bootstrap circuit:

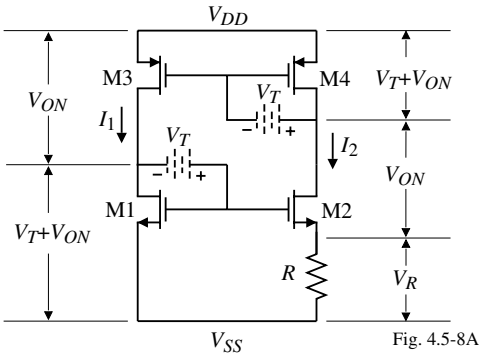

Fig. 4.5-8A

Without the batteries, V_T, the minimum power supply is $V_T+2V_{ON}+V_R$.

With the batteries, V_T, the minimum power supply is $2V_{ON}+V_R \approx 0.5V$

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Summary of Power-Supply Independent References

- Reasonably good, simple references are possible
- Best power supply sensitivity is approximately 0.01
  (10% change in power supply causes a 0.1% change in reference)
- Typical simple reference temperature dependence is ≈ 1000 ppm/°C
- Can obtain zero temperature coefficient over a limited range of operation

Type of Reference	$S^{V_{REF}}_{V_{PP}}$
Voltage division	1
MOSFET-R	<1
BJT-R	<<1
Threshold Referenced	<<1
Base-emitter Referenced	<<1

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REFERENCES WITH TEMPERATURE INDEPENDENCE

Characterization of Temperature Dependence

The objective is to minimize the fractional temperature coefficient defined as,

$$TC_F = \frac{1}{V_{REF}}\left(\frac{\partial V_{REF}}{\partial T}\right) = \frac{1}{T} S_T^{V_{REF}} \text{ parts per million per °C or ppm/°C}$$

Temperature dependence of PN junctions:

$$\left.\begin{aligned} i &\approx I_s \exp\left(\frac{v}{V_t}\right) \\ I_s &= KT^3 \exp\left(\frac{-V_{GO}}{V_t}\right) \end{aligned}\right\} \quad \frac{1}{I_s}\left(\frac{\partial I_s}{\partial T}\right) = \frac{\partial(\ln I_s)}{\partial T} = \frac{3}{T} + \frac{V_{GO}}{TV_t} \approx \frac{V_{GO}}{TV_t}$$

$$\frac{dv_{BE}}{dT} \approx \frac{V_{BE} - V_{GO}}{T} = -2\text{mV/°C at room temperature}$$

(V_{GO} = 1.205 V at room temperature and is called the bandgap voltage)

Temperature dependence of MOSFET in strong inversion:

$$\left.\begin{aligned} \frac{dv_{GS}}{dT} &= \frac{dV_T}{dT} + \sqrt{\frac{2L}{WC_{ox}}}\frac{d}{dT}\left(\sqrt{\frac{i_D}{\mu_o}}\right) \\ \mu_o &= KT^{-1.5} \\ V_T(T) &= V_T(T_o) - \alpha(T-T_o) \end{aligned}\right\} \quad \frac{dv_{GS}}{dT} \approx -\alpha \approx -2.3\frac{\text{mV}}{\text{°C}}$$

Resistors:

$(1/R)(dR/dT)$ ppm/°C

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Bipolar-Resistance Voltage References

From previous work we know that,

$$V_{REF} = \frac{kT}{q} ln\left(\frac{V_{DD} - V_{REF}}{RI_s}\right)$$

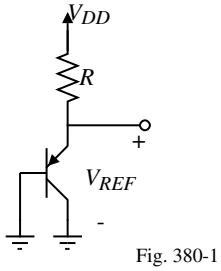

Fig. 380-1

However, not only is V_{REF} a function of T, but R and I_s are also functions of T.

$$\therefore \frac{dV_{REF}}{dT} = \frac{k}{q} ln\left(\frac{V_{DD}-V_{REF}}{RI_s}\right) + \frac{kT}{q}\left(\frac{RI_s}{V_{DD}-V_{REF}}\right)\left[\frac{-1}{RI_s}\frac{dV_{REF}}{dT} - \left(\frac{V_{DD}-V_{REF}}{RI_s}\right)\left(\frac{dR}{RdT} + \frac{dI_s}{I_s dT}\right)\right]$$

$$= \frac{V_{REF}}{T} - \frac{V_t}{V_{DD}-V_{REF}}\frac{dV_{REF}}{dT} - V_t\left(\frac{dR}{RdT} + \frac{dI_s}{I_s dT}\right) = \frac{V_{REF}-V_{GO}}{T} - \frac{V_t}{V_{DD}-V_{REF}}\frac{dV_{REF}}{dT} - \frac{3V_t}{T} - \frac{V_T}{R}\frac{dR}{dT}$$

$$\therefore \frac{dV_{REF}}{dT} = \frac{\frac{V_{REF}-V_{GO}}{T} - V_t\frac{dR}{RdT} - \frac{3V_t}{T}}{1 + \frac{V_t}{V_{DD}-V_{REF}}} \approx \frac{V_{REF}-V_{GO}}{T} - V_t\frac{dR}{RdT} - \frac{3V_t}{T}$$

$$TC_F = \frac{1}{V_{REF}}\frac{dV_{REF}}{dT} = \frac{V_{REF}-V_{GO}}{V_{REF}\cdot T} - \frac{V_t}{V_{REF}}\frac{dR}{RdT} - \frac{3V_t}{V_{REF}\cdot T}$$

If V_{REF} = 0.6V, V_t = 0.026V, and the R is polysilicon, then at 27°K the TC_F is

$$TC_F = \frac{0.6-1.205}{0.6\cdot 300} - \frac{0.026\cdot 0.0015}{0.6} - \frac{3\cdot 0.026}{0.6\cdot 300} = 33110^{-6} - 65x10^{-6} - 433x10^{-6} = -3859\text{ppm/°C}$$

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MOSFET Resistor Voltage Reference

From previous results we know that

$$V_{REF} = V_{GS} = V_T + \sqrt{\frac{2(V_{DD}-V_{REF})}{\beta R}}$$

or $$V_{REF} = V_T - \frac{1}{\beta R} + \sqrt{\frac{2(V_{DD}-V_T)}{\beta R} + \frac{1}{(\beta R)^2}}$$

Note that V_{REF}, V_T, β, and R are all functions of temperature.

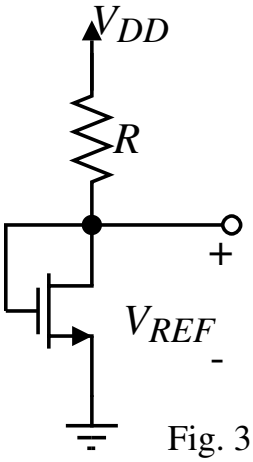

Fig. 380-02

It can be shown that the TC_F of this reference is

$$\frac{dV_{REF}}{dT} = \frac{-\alpha + \sqrt{\frac{V_{DD}-V_{REF}}{2\beta R}}\left(\frac{1.5}{T} - \frac{1}{R}\frac{dR}{dT}\right)}{1 + \frac{1}{\sqrt{2\beta R\,(V_{DD}-V_{REF})}}}$$

$$\therefore \quad TC_F = \frac{-\alpha + \sqrt{\frac{V_{DD}-V_{REF}}{2\beta R}}\left(\frac{1.5}{T} - \frac{1}{R}\frac{dR}{dT}\right)}{V_{REF}\left(1 + \frac{1}{\sqrt{2\beta R\,(V_{DD}-V_{REF})}}\right)}$$

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Example 4.5-1 - Calculation of MOSFET-Resistor Voltage Reference TC_F

Calculate the temperature coefficient of the MOSFET-Resistor voltage reference where W/L=2, V_{DD}=5V, R=100kΩ using the parameters of Table 3.1-2. The resistor, R, is polysilicon and has a temperature coefficient of 1500 ppm/°C.

Solution

First, calculate V_{REF}. Note that $\beta R = 220 \times 10^{-6} \times 10^5 = 22$ and $\frac{dR}{RdT} = 1500\text{ppm/°C}$

$$\therefore \quad V_{REF} = 0.7 - \frac{1}{22} + \sqrt{\frac{2(5-0.7)}{22} + \left(\frac{1}{22}\right)^2} = 1.281\text{V}$$

Now, $$\frac{dV_{REF}}{dT} = \frac{-2.3\times10^{-3} + \sqrt{\frac{5-1.281}{2(22)}}\left(\frac{1.5}{300} - 1500\times10^{-6}\right)}{1 + \frac{1}{\sqrt{2(22)\ (5-1.281)}}} = -1.189\text{x}10^{-3}\text{V/°C}$$

The fractional temperature coefficient is given by

$$TC_F = -1.189 \times 10^{-3}\left(\frac{1}{1.281}\right) = -928\ \text{ppm/°C}$$

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Bootstrapped Current Source/Sink

Gate-source referenced source:

The output current was given as, $I_{out} = \frac{V_{T1}}{R} + \frac{1}{\beta_1 R^2} + \frac{1}{R}\sqrt{\frac{2V_{T1}}{\beta_1 R} + \frac{1}{(\beta_1 R)^2}}$

Although we could grind out the derivative of I_{out} with respect to T, the temperature performance of this circuit is not that good to spend the time to do so. Therefore, let us assume that $V_{GS1} \approx V_{T1}$ which gives

$$I_{out} \approx \frac{V_{T1}}{R} \quad \Rightarrow \quad \frac{dI_{out}}{dT} = \frac{1}{R}\frac{dV_{T1}}{dT} - \frac{1}{R^2}\frac{dR}{dT}$$

In the resistor is polysilicon, then

$$TC_F = \frac{1}{I_{out}}\frac{dI_{out}}{dT} = \frac{1}{V_{T1}}\frac{dV_{T1}}{dT} - \frac{1}{R}\frac{dR}{dT} = \frac{-\alpha}{V_{T1}} - \frac{1}{R}\frac{dR}{dT} = \frac{-2.3\text{x}10^{-3}}{0.7} - 1.5\text{x}10^{-3} = -4786\text{ppm/°C}$$

Base-emitter referenced source:

The output current was given as, $I_{out} = I_2 = \frac{V_{BE1}}{R}$

The $TC_F = \frac{1}{V_{BE1}}\frac{dV_{BE1}}{dT} - \frac{1}{R}\frac{dR}{dT}$

If $V_{BE1} = 0.6$V and R is poly, then the $TC_F = \frac{1}{0.6}(-2\text{x}10^{-3}) - 1.5\text{x}10^{-3} = -4833\text{ppm/°C}$.

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Technique to Make g_m Dependent on a Resistor

Consider the following circuit with all transistors having a W/L = 10. This is a bootstrapped reference which creates a V_{bias} independent of V_{DD}. The two key equations are:

$$I_3 = I_4 \Rightarrow I_1 = I_2$$

and

$$V_{GS1} = V_{GS2} + I_2 R$$

Solving for I_2 gives:

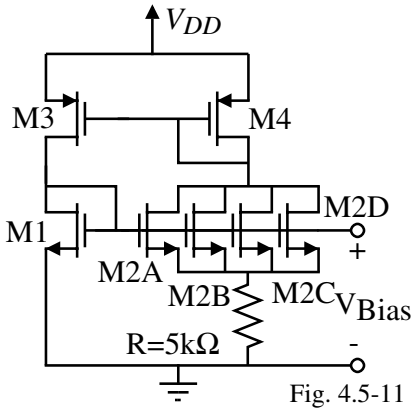

Fig. 4.5-11

$$I_2 = \frac{V_{GS1}-V_{GS2}}{R} = \frac{1}{R}\left(\sqrt{\frac{2I_1}{ß_1}} - \sqrt{\frac{2I_2}{ß_2}}\right) = \frac{\sqrt{2I_1}}{R\sqrt{ß_1}}\left(1 - \frac{1}{2}\right)$$

$$\therefore \quad \sqrt{I_2} = \frac{1}{R\sqrt{2ß_1}} \quad \Rightarrow \quad I_2 = I_1 = \frac{1}{2ß_1 R^2} = \frac{1}{2\cdot 110\text{x}10^{-6}\cdot 10\cdot 25\text{x}10^{6}} = 18.18\mu\text{A}$$

Now, V_{bias} can be written as

$$V_{bias} = V_{GS1} = \sqrt{\frac{2I_2}{ß_1}} + V_{TN} = \frac{1}{ß_1 R} + V_{TN} = \frac{1}{110\text{x}10^{-6}\cdot 10\cdot 5\text{x}10^{3}} + 0.7 = 0.1818 + 0.7 = 0.8818\text{V}$$

Any transistor with $V_{GS} = V_{bias}$ will have a current flow that is given by $1/2ßR^2$.

Therefore, $$g_m = \sqrt{2Iß} = \sqrt{\frac{2ß}{2ßR^2}} = \frac{1}{R} \quad \Rightarrow \quad \boxed{g_m = \frac{1}{R}}$$

(This means that the temperature dependence of g_m will be that of 1/R which can be used to achieve temperature controlled performance.)

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Summary of Reference Performance

Type of Reference	$S_{V_{DD}}^{V_{REF}}$	TC_F	Comments
MOSFET-R	<1	>1000ppm/°C	
BJT-R	<<1	>1000ppm/°C	
Breakdown Diode	<<1	Can be very small	BV too large
Bootstrap Gate-Source Referenced	Good if currents are matched	>1000ppm/°C	Requires start-up circuit
Bootstrap Base-emitter Referenced	Good if currents are matched	>1000ppm/°C	Requires start-up circuit

- A MOSFET can have zero temperature dependence of i_D for a certain v_{GS}
- If one is careful, very good independence of power supply can be achieved
- None of the above references have really good temperature independence

Consider the following example:

A 10 bit ADC has a reference voltage of 1V. The LSB is approximately 0.001V. Therefore, the voltage reference must be stable to within 0.1%. If a 100°C change in temperature is experienced, then the TC_F must be 0.001%/C or multiplying by 10^4 gives a TC_F = 10ppm/°C.

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SECTION 4.6 - BANDGAP REFERENCES

Temperature Stable References

- The previous reference circuits failed to provide small values of temperature coefficient although sufficient power supply independence was achieved.
- This lecture introduces the bandgap voltage concept combined with power supply independence to create a very stable voltage reference in regard to both temperature and power supply variations.

Bandgap Voltage Reference Principle

The principle of the bandgap voltage reference is to balance the negative temperature coefficient of a pn junction with the positive temperature coefficient of the thermal voltage, $V_t = kT/q$.

Concept:

Result: References with TC_F's approaching 10 ppm/°C.

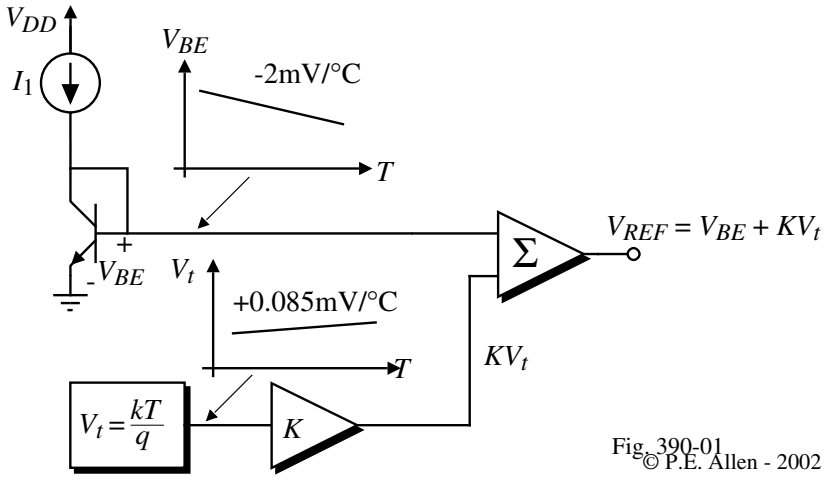

Fig. 390-01

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Derivation of the Temperature Coefficient of the Base-Emitter Voltage

For small TC_F's the dependence V_{BE} must be known more precisely than ≈ -2mV/°C.

1.) Start with the collector current density, J_C:

$$J_C = \frac{q\,\overline{D_n}\,n_{po}}{W_B}\exp\left(\frac{V_{BE}}{V_t}\right)$$

where, $J_C = I_C/\text{Area}$ = collector current density

$\overline{D_n}$ = average diffusion constant for electrons

W_B = base width

V_{BE} = base-emitter voltage

$V_t = kT/q$

k = Boltzmann's constant ($1.38\text{x}10^{-23}$J/°K)

T = Absolute temperature

$n_{po} = n_i^2/N_A$ = equilibrium concentration of electrons in the base

$n_i^2 = DT^3\exp\left(\frac{-V_{GO}}{V_t}\right)$ = intrinsic concentration of carriers

D = temperature independent constant

V_{GO} = bandgap voltage of silicon (1.205V)

N_A = acceptor impurity concentration

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Derivation of the Temperature Coefficient of the Base-Emitter Voltage - Continued

2.) Combine the above relationships into one:

$$J_C = \frac{q\,\overline{D_n}}{N_A W_B}\,DT^3\exp\left(\frac{V_{BE}-V_{GO}}{V_t}\right) = AT^{\gamma}\exp\left(\frac{V_{BE}-V_{GO}}{V_t}\right) \qquad \text{where,}\quad \gamma = 3$$

3.) The value of J_C at a reference temperature of $T = T_0$ is

$$J_{C0} = AT_0^{\gamma}\exp\left[\frac{q}{kT_0}(V_{BE}-V_{GO})\right]$$

while the value of J_C at a general temperature, T, is

$$J_C = AT^{\gamma}\exp\left[\frac{q}{kT}(V_{BE}-V_{GO})\right]$$

4.) The ratio of J_C/J_{C0} can be expressed as,

$$\frac{J_C}{J_{C0}} = \left(\frac{T}{T_0}\right)^{\gamma}\exp\left[\frac{q}{k}\left(\frac{V_{BE}-V_{G0}}{T}-\frac{V_{BE0}-V_{G0}}{T_0}\right)\right]$$

or

$$\ln\left(\frac{J_C}{J_{C0}}\right) = \gamma\ln\left(\frac{T}{T_0}\right) + \frac{q}{kT}\left[V_{BE}-V_{GO}-\frac{T}{T_0}(V_{BE0}-V_{GO})\right]$$

where V_{BE0} is the value of V_{BE} at $T = T_0$.

5.) Solving for V_{BE} from the above results gives,

$$\boxed{V_{BE}(T) = V_{GO}\left(1-\frac{T}{T_0}\right)+V_{BE0}\left(\frac{T}{T_0}\right)+\frac{\gamma kT}{q}\ln\left(\frac{T_0}{T}\right)+\frac{kT}{q}\ln\left(\frac{J_C}{J_{C0}}\right)}$$

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Derivation of the Temperature Coefficient of the Base-Emitter Voltage - Continued

6.) Next, assume $J_C \propto T^{\alpha}$ and find $\partial V_{BE}/\partial T$.

$$\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_{GO}}{\partial T}\left(1-\frac{T}{T_0}\right) - \frac{V_{GO}}{T_0} + \frac{V_{BE0}}{T_0} + \frac{\gamma kT}{q}\frac{\partial \ln(T_0/T)}{\partial T} + \ln\left(\frac{T_0}{T}\right)\frac{\partial(\gamma kT/q)}{\partial T} + \frac{kT}{q}\left(\frac{\partial \ln\left(\frac{J_C}{J_{C0}}\right)}{\partial T}\right) + \frac{k}{q}\ln\left(\frac{J_C}{J_{C0}}\right)$$

7.) Assume that $T = T_0$ which means $J_C = J_{C0}$. Since, $\partial V_{GO}/\partial T = 0$,

$$\left.\frac{\partial V_{BE}}{\partial T}\right|_{T=T_0} = -\frac{V_{GO}}{T_0} + \frac{V_{BE0}}{T_0} + \frac{\gamma kT}{q}\cdot\frac{\partial \ln(T_0/T)}{\partial T} + \frac{kT}{q}\left(\frac{\partial \ln(J_C/J_{C0})}{\partial T}\right)$$

8.) Note that,

$$\frac{\partial \ln(T_0/T)}{\partial T} = \frac{T}{T_0}\frac{\partial(T_0/T)}{\partial T} = \frac{T}{T_0}\left(\frac{-T_0}{T^2}\right) = \frac{-1}{T} \text{ and } \frac{\partial \ln(J_C/J_{C0})}{\partial T} = \frac{J_{C0}}{J_C}\frac{\partial(J_C/J_{C0})}{\partial T} = \frac{J_{C0}}{J_C}\left(\frac{\alpha}{T}\frac{J_C}{J_{C0}}\right) = \frac{\alpha}{T}$$

Therefore,

$$\left.\frac{\partial V_{BE}}{\partial T}\right|_{T=T_0} = -\frac{V_{GO}}{T_0} + \frac{V_{BE0}}{T_0} - \frac{\gamma k}{q} + \frac{\alpha k}{q} \quad \text{or} \quad \boxed{\left.\frac{\partial V_{BE}}{\partial T}\right|_{T=T_0} = \frac{V_{BE0} - V_{GO}}{T_0} + (\alpha - \gamma)\left(\frac{k}{q}\right)}$$

Typical values of α and γ are 1 and 3.2. If $V_{BE0} = 0.6V$, then at room temperature:

$$\left.\frac{\partial V_{BE}}{\partial T}\right|_{T=T_0} = \frac{0.6-1.205}{300} + (1-3.2)\left(\frac{0.026}{300}\right) = \frac{0.6-1.205-0.1092}{300} = -1.826\text{mV/°C}$$

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Derivation of the Temperature Coefficient of the Thermal Voltage (*kT/q*)

1.) Consider two identical pn junctions having different current densities,

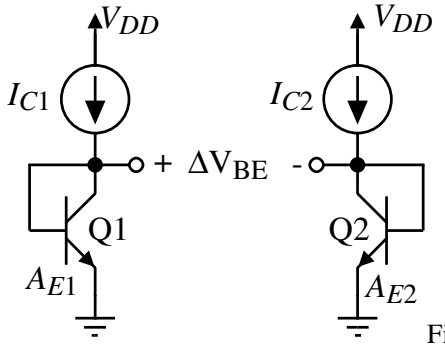

Fig. 390-02

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = \frac{kT}{q}\ln\left(\frac{J_{C1}}{J_{C2}}\right)$$

- Find $\partial(\Delta V_{BE})/\partial T$,

$$\boxed{\frac{\partial(\Delta V_{BE})}{\partial T} = \frac{V_t}{T}\ln\left(\frac{J_{C1}}{J_{C2}}\right) = \frac{k}{q}\ln\left(\frac{J_{C1}}{J_{C2}}\right)}$$

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Derivation of the Gain, K, for the Bandgap Voltage Reference

1.) In order to achieve a zero temperature coefficient at $T = T_0$, the following equation must be satisfied:

$$0 = \frac{\partial V_{BE}}{\partial T}\bigg|_{T=T_0} + K'' \frac{\partial(\Delta V_{BE})}{\partial T}$$ where K" is a constant that satisfies the equation.

2.) Therefore, we get

$$0 = K'' \left(\frac{V_{t0}}{T_0}\right) \ln\left(\frac{J_{C1}}{J_{C2}}\right) + \frac{V_{BE0} - V_{GO}}{T_0} + \frac{(\alpha - \gamma)V_{t0}}{T_0}$$

3.) Define $K = K'' \ln\left(\frac{J_{C1}}{J_{C2}}\right)$, therefore

$$0 = K\left(\frac{V_{t0}}{T_0}\right) + \frac{V_{BE0} - V_{GO}}{T_0} + \frac{(\alpha - \gamma)V_{t0}}{T_0}$$

4.) Solving for K gives $\boxed{K = \frac{V_{GO} - V_{BE0} - V_{t0}(\alpha-\gamma)}{V_{t0}}}$

Assuming that $J_{C1}/J_{C2} = A_{E1}/A_{E2} = 10$ and $V_{BE0} = 0.6V$ gives,

$$K = \frac{1.205 - 0.6 + (2.2)(0.026)}{0.026} = 25.469$$

5.) The output voltage of the bandgap voltage reference is found as,

$$V_{REF}\big|_{T=T_0} = V_{BE0} + KV_{t0} = V_{BE0} + V_{GO} - V_{BE0} + (\gamma-\alpha)V_{t0}$$ or $\boxed{V_{REF} = V_{GO} + (\gamma-\alpha)V_{t0}}$

For the previous values, $V_{REF} = 1.205 + 0.026(2.2) = 1.262V$.

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Variation of the Bandgap Reference Voltage with respect to Temperature

The previous derivation is only valid at a given temperature, T_0. As the temperature changes away from T_0, the value of $\partial V_{REF}/\partial T$ is no longer zero.

Illustration:

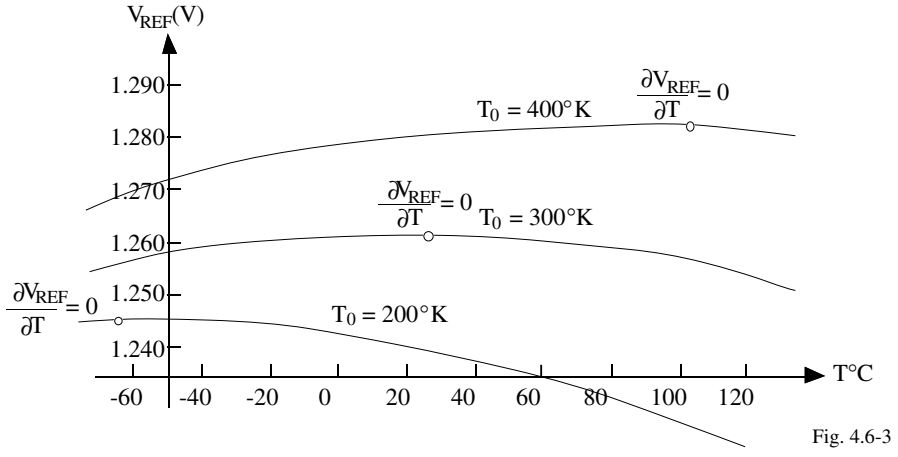

Fig. 4.6-3

Bandgap curvature correction will be necessary for low ppm/C bandgap references.

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Classical Widlar Bandgap Voltage Reference[†]

Operation:

$$V_{BE1} = V_{BE2} + I_2R_3$$

gives

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = I_2R_3$$

But,

$$\Delta V_{BE} = V_t \ln\left(\frac{I_1}{I_{s1}}\right) - V_t \ln\left(\frac{I_2}{I_{s2}}\right) = V_t \ln\left(\frac{I_1 I_{s2}}{I_2 I_{s1}}\right)$$

Assume $V_{BE1} \approx V_{BE3}$, we get $I_1R_1 = I_2R_2$

Therefore,

$$I_2 = \frac{\Delta V_{BE}}{R_3} = \frac{V_t}{R_3} \ln\left(\frac{I_1 I_{s2}}{I_2 I_{s1}}\right) = \frac{V_t}{R_3} \ln\left(\frac{R_2 I_{s2}}{R_1 I_{s1}}\right)$$

Now we can express V_{REF} as

$$V_{REF} = I_2R_2 + V_{BE3} = \frac{R_2}{R_3} V_t \ln\left(\frac{R_2 I_{s2}}{R_1 I_{s1}}\right) + V_{BE3} = KV_t + V_{BE}$$

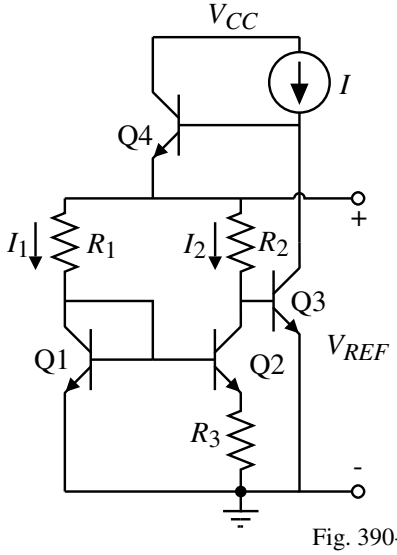

Fig. 390-04

Design R_1, R_2, I_{s1}, and I_{s2} to get the desired K.

Let K = 25 and $I_{s2} = 10I_{s1}$ and design R_1, R_2, and R_3. Choose $R_2 = 10R_1 = 10k\Omega$.
Therefore, ln(100) = 4.602. Therefore $R_2/R_3 = 25/4.602$ or $R_3 = R_2/5.4287 = 1.842k\Omega$.

[†] R.J. Widlar, "New Developments in IC Voltage Regulators," *IEEE J. of Solid-State Circuits*, Vol. SC-6, pp. 2-7, February 1971.

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A CMOS Bandgap Reference using PNP Lateral BJTs

Bootstrapped Voltage Reference using PNP Laterals-

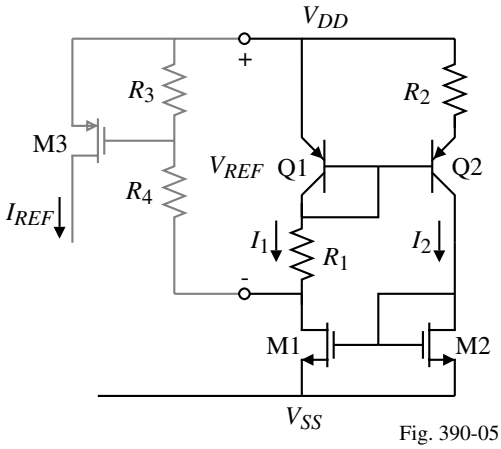

Fig. 390-05

$$I_2 = \frac{V_{BE1} - V_{BE2}}{R_2} = \frac{V_t}{R_2}\left[\ln\left(\frac{I_1}{I_{s1}}\right) - \ln\left(\frac{I_2}{I_{s2}}\right)\right] = \frac{V_t}{R_2} \ln\left(\frac{I_{s2}}{I_{s1}}\right) = \frac{V_t}{R_2} \ln\left(\frac{A_{E2}}{A_{E1}}\right)$$

if $I_1 = I_2$ which is forced by the current mirror consisting of M1 and M2.

$$\therefore \quad V_{REF} = V_{BE1} + I_1R_1 = V_{BE1} + \left(\frac{R_1}{R_2} \ln\left(\frac{A_{E2}}{A_{E1}}\right)\right) V_t = V_{BE1} + KV_t$$

While an op amp could be used to make $I_1 = I_2$ it suffers from offset and noise and leads to deterioration of the bandgap temperature performance.

V_{REF} is with respect to V_{DD} and therefore is susceptible to changes on V_{DD}.

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A CMOS Bandgap Reference using Substrate PNP BJTs

Operation:

The cascode mirror (M5-M8) keeps the currents in Q1, Q2, and Q3 identical.

Thus,

$$V_{BE1} = I_2R + V_{BE2}$$

or

$$I_2 = \frac{V_t}{R}\ln(n)$$

Therefore,

$$V_{REF} = V_{BE3} + I_2(kR) = V_{BE3} + kV_t\cdot\ln(n)$$

Use k and n to design the desired value of K (n is an integer greater than 1).

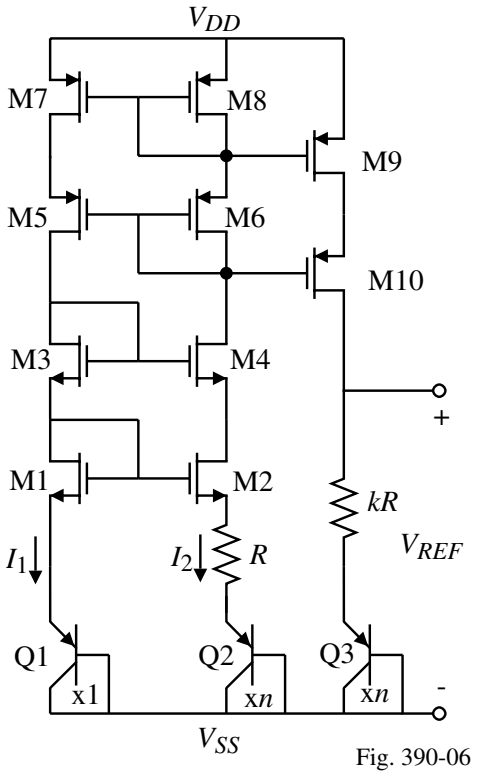

Fig. 390-06

Weak Inversion Bandgap Voltage Reference

Circuit:

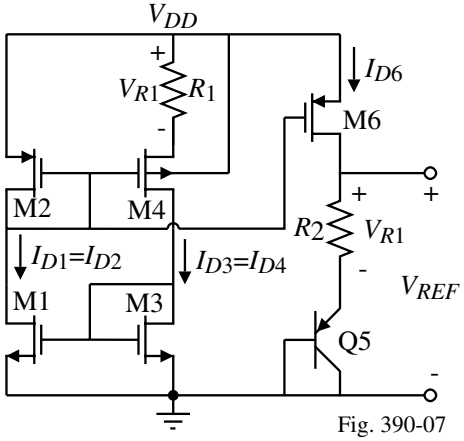

Fig. 390-07

Analysis:

For the p-channel transistors:

$$I_D = I_{DO}(W/L)\exp\left(\frac{V_{BG}}{nV_t}\right)\left[\exp\left(\frac{-V_{BS}}{V_t}\right) - \exp\left(\frac{-V_{BD}}{V_t}\right)\right]$$

where $V_t = kT/q$.

If $V_{BD} >> V_t$, then $I_D = I_{DO}(W/L)\exp\left(\frac{V_{BG}}{nV_t} - \frac{V_{BS}}{V_t}\right)$.

The various transistor currents can be expressed as:

$$I_{D1} = I_{D2} = I_{DO}(W_2/L_2)\exp\left(\frac{V_{BG2}}{nV_t}\right) \text{ and } I_{D3} = I_{D4} = I_{DO}(W_4/L_4)\exp\left(\frac{V_{BG4}}{nV_t} - \frac{V_{BS4}}{V_t}\right)$$

Note that $V_{BG2} = V_{BG4}$ and $V_{BS4} = V_{R1}$.

Therefore,

$$\frac{I_{D1}}{I_{D3}} = \frac{W_2/L_2}{W_4/L_4}\exp\left(\frac{V_{R1}}{V_t}\right)$$

where

$$V_{R1} = V_t\ln\left(\frac{W_1W_4L_2L_3}{L_1L_4W_2W_3}\right) \quad \text{and} \quad I_{R1} = \frac{V_{R1}}{R_1}$$

Weak Inversion Bandgap Voltage Reference - Continued

The reference voltage can be expressed as,

$$V_{REF} = R_2 I_6 + V_{BE5}$$

However,

$$I_6 = \frac{W_6 L_3}{L_6 W_3} \quad I_{R1} = \frac{W_6 L_3}{L_6 W_3}\frac{V_t}{R_1} \quad \ln\left(\frac{W_1 W_4 L_2 L_3}{L_1 L_4 W_2 W_3}\right) .$$

Substituting I_6 and the previously derived expression for $V_{BE}(T)$ in V_{REF} gives,

$$V_{REF} = \frac{W_6 L_3}{L_6 W_3}\frac{R_2}{R_1} V_t \ln\left(\frac{W_1 W_4 L_2 L_3}{L_1 L_4 W_2 W_3}\right) + V_{GO}\left(1 - \frac{T}{T_0}\right) + V_{BE0}\left(\frac{T}{T_0}\right) + 3V_t \ln\left(\frac{T_0}{T}\right)$$

To achieve $\partial V_{REF}/\partial T = 0$ at $T = T_0$, we get

$$\frac{\partial V_{REF}}{\partial T} = \left(\frac{k}{q}\right)\left(\frac{R_2}{R_1}\right)\left(\frac{W_6 L_3}{L_6 W_3}\right) \ln\left(\frac{W_1 W_4 L_2 L_3}{L_1 L_4 W_2 W_3}\right) - \frac{V_{GO}}{T_0} + \frac{V_{BE0}}{T_0} + \frac{3k}{q}$$

Therefore,

$$\boxed{\frac{R_2 W_6 L_3}{R_1 L_6 W_3} \ln\left(\frac{W_1 W_4 L_2 L_3}{L_1 L_4 W_2 W_3}\right) = \frac{q}{kT_0}(V_{GO} - V_{BE0}) - 3}$$

Under the above constraint, V_{REF} has an ≈ zero TC_F at $T = T_0$ and has a value of

$$V_{REF} = V_{GO} + \frac{3kT}{q}\left[1 + \ln\left(\frac{T_0}{T}\right)\right] = V_{GO} + \frac{3kT}{q}$$

Practical values of $\partial V_{REF}/\partial T$ for the weak inversion bandgap are less than 100 ppm/°C.

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Curvature Correction Techniques:

- Squared PTAT Correction:

  Temperature coefficient ≈ 1-20 ppm/°C

- V_{BE} loop

  M. Gunaway, *et. al.*, "A Curvature-Corrected Low-Voltage Bandgap Reference," *IEEE Journal of Solid-State Circuits*, vol. 28, no. 6, pp. 667-670, June 1993.

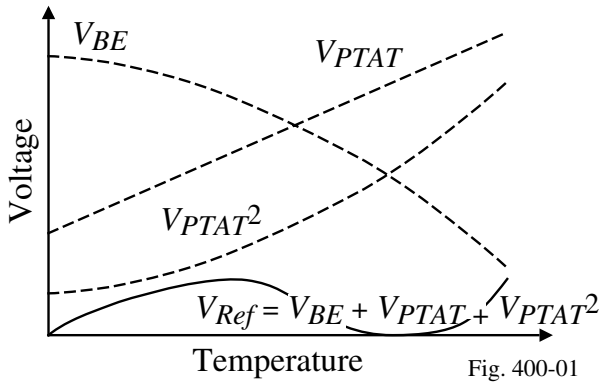

Fig. 400-01

- β compensation

  I. Lee *et. al.*, "Exponential Curvature-Compensated BiCMOS Bandgap References," *IEEE Journal of Solid-State Circuits*, vol. 29, no. 11, pp. 1396-1403, Nov. 1994.

- Nonlinear cancellation

  G.M. Meijer *et. al.*, "A New Curvature-Corrected Bandgap Reference," *IEEE Journal of Solid-State Circuits*, vol. 17, no. 6, pp. 1139-1143, December 1982.

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V_{BE} Loop Curvature Correction Technique

Circuit:

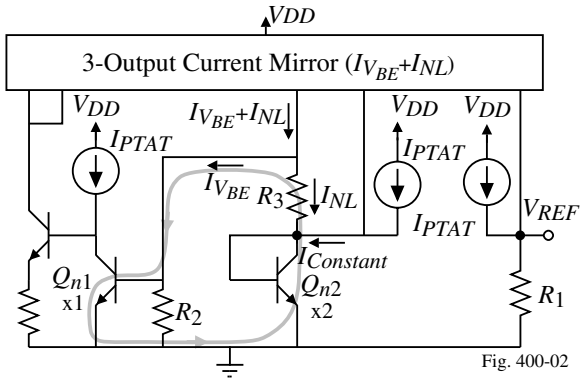

Fig. 400-02

Operation:

$$I_{NL} = \frac{V_{BE1}-V_{BE2}}{R_3} = \frac{V_t}{R_3} ln\left(\frac{I_{c1}A_2}{A_1 I_{c2}}\right)$$

$$= \frac{V_t}{R_3} ln\left(\frac{2I_{PTAT}}{I_{NL}+I_{Constant}}\right)$$

where

$$I_{constant} = I_{NL} + I_{PTAT} + I_{VBE}$$

$$\approx I_{NL} + \frac{V_t}{R_x} + \frac{V_{BE}}{R_2}$$

(a quasi-temperature independent current subject to the TC_F of the resistors)

where

$V_t = kT/q$

I_{c1} and I_{c2} are the collector currents of Q_{n1} and Q_{n2}, respectively

R_x = a resistor used to define I_{PTAT}

$$\therefore \quad V_{REF} = \left[\frac{V_{BE}}{R_2} + \frac{V_t}{R_3} ln\left(\frac{2I_{PTAT}}{I_{NL}+I_{constant}}\right) + I_{PTAT}\right] R_1$$

Temperature coefficient ≈ 3 ppm/°C with a total quiescent current of 95μA..

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β Compensation Curvature Correction Technique

Circuit:

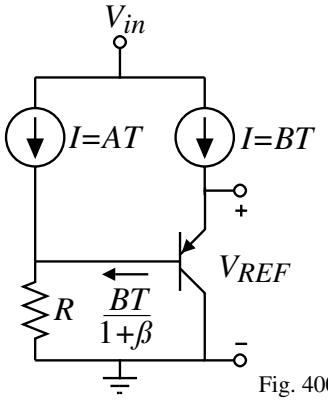

Fig. 400-0

Operation:

$$V_{REF} = V_{BE} + \left(AT + \frac{BT}{(1+\beta)}\right) R \approx V_{BE} + \left(AT + \frac{BT}{\beta}\right) R$$

where

A and B are constant

T = temperature

The temperature dependence of β is

$$\beta(T) \propto e^{-1/T} \Rightarrow \beta(T) = Ce^{-1/T}$$

$$\therefore \quad V_{REF} = V_{BE}(T) + \left(AT + \frac{BTe^{1/T}}{C}\right)$$

Not good for small values of V_{in}.

$$V_{in} \geq V_{REF} + V_{sat.} = V_{GO} + V_{sat.} = 1.4V$$

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Nonlinear Cancellation Curvature Correction Technique

Objective: Eliminate nonlinear term from the BE.

Result: 0.5 ppm/°C from -25°C to 85°C.

Operation: From above,

$$V_{REF} = V_{PTAT} + 4V_{BE}(I_{PTAT}) - 3V_{BE}(I_{Constant})$$

Note that, $I_{PTAT} \Rightarrow I_c \propto T^1 \Rightarrow \alpha = 1$

and $I_{constant} \Rightarrow I_c \propto T^0 \Rightarrow \alpha = 0,$

Previously we found,

$$V_{BE}(T) \approx V_{GO} - \frac{T}{T_0}[V_{GO} - V_{BE}(T_0)] - (\gamma - \alpha)V_t \ln\left(\frac{T}{T_0}\right)$$

so that

$$V_{BE}(I_{PTAT}) = V_{GO} - \frac{T}{T_0}[V_{GO} - V_{BE}(T_0)] - (\gamma - 1)V_t \ln\left(\frac{T}{T_0}\right)$$

and

$$V_{BE}(I_{Constant}) = V_{GO} - \frac{T}{T_0}[V_{GO} - V_{BE}(T_0)] - \gamma V_t \ln\left(\frac{T}{T_0}\right)$$

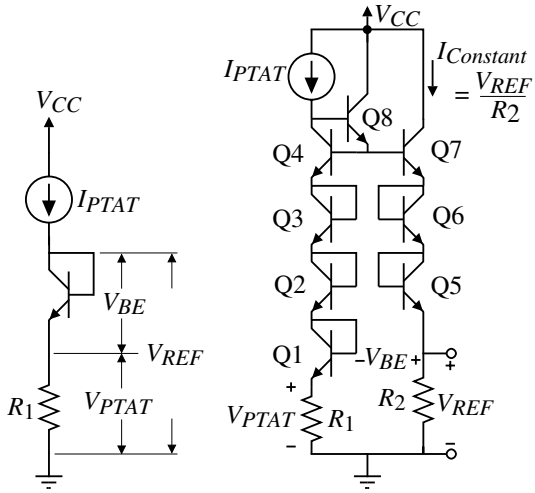

Fig. 400-04

Combining the above relationships gives,

$$V_{REF}(T) = V_{PTAT} + V_{GO} - (T/T_0)[V_{GO} - V_{BE}(T_0)] - [\gamma - 4]\, V_t \ln((T/T_0))$$

If $\gamma \approx 4$, then $\boxed{V_{REF}(T) \approx V_{PTAT} + V_{GO}(1 - (T/T_0)) + V_{BE}(T_0)(T/T_0)}$

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Other Characteristics of Bandgap Voltage References

Noise

Voltage references for high-resolution ADCs are particularly sensitive to noise.

Noise sources: Op amp, resistors, switches, etc.

PSRR

Maximize the PSRR of the op amp.

Offset Voltages

Becomes a problem when op amps are used.

$$V_{BE2} = V_{BE1} + V_{R1} + V_{OS}$$

$$\Delta V_{BE} = V_{BE2} - V_{BE1} = V_{R1} + V_{OS} = V_t \ln\left(\frac{i_{C2}A_{E1}}{i_{C1}A_{E2}}\right)$$

Since $i_{C2}R_3 = i_{C1}R_2 - V_{OS}$

then $\frac{i_{C2}}{i_{C1}} = \frac{R_2}{R_3} - \frac{V_{OS}}{i_{C1}R_3} = \frac{R_2}{R_3}\left(1 + \frac{V_{OS}}{i_{C1}R_2}\right)$

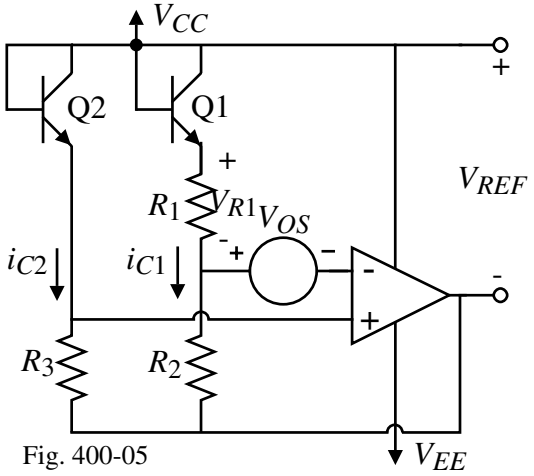

Fig. 400-05

Therefore,

$$V_{R1} = -V_{OS} + V_t \ln\left[\frac{R_2A_{E1}}{R_3A_{E2}}\left(1 + \frac{V_{OS}}{i_{C1}R_2}\right)\right]$$

$$V_{REF} = V_{BE2} - V_{OS} + i_{C1}R_2 = V_{BE2} - V_{OS} + \left(\frac{V_{R1}}{R_1}\right)R_2 = V_{BE2} - V_{OS} + \left(\frac{R_2}{R_1}\right)V_{R1}$$

$$\boxed{V_{REF} = V_{BE2} - V_{OS}\left(1 + \frac{R_2}{R_1}\right) + \frac{R_2}{R_1}V_t \ln\left[\frac{R_2A_{E1}}{R_3A_{E2}}\left(1 - \frac{V_{OS}}{i_{C1}R_2}\right)\right]}$$

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How do you get a Stable Reference Current from the Bandgap?

Assume that a temperature stable reference voltage is available (i.e. bandgap reference) and use the zero TC NMOS current sink.

The problem is that V_{REF} may not be equal to the value of V_{GS} that gives zero TC.

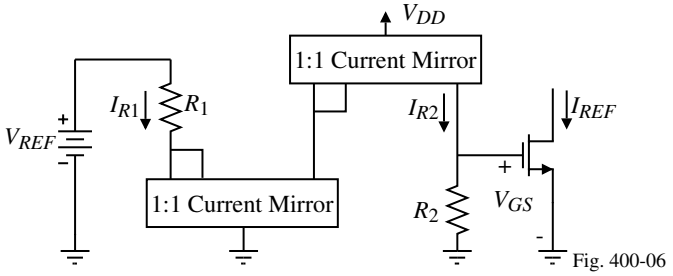

Fig. 400-06

$$V_{GS} = I_{R2}R_2 = R_2\left(\frac{V_{REF}}{R_1}\right) = \left(\frac{R_2}{R_1}\right)V_{REF}$$

$$\therefore \quad \frac{dV_{GS}}{dT} = \left(\frac{R_2}{R_1}\right)\frac{dV_{REF}}{dT} + \frac{V_{REF}}{R_1}\frac{dR_2}{dT} - \frac{R_2}{R_1^2}\frac{dR_1}{dT} = \frac{R_2}{R_1}\left[\frac{dV_{REF}}{dT} + \frac{dR_2}{dT} - \frac{dR_1}{dT}\right]$$

If the temperature coefficients of R_1 and R_2 are equal $\left(\frac{dR_1}{dT} = \frac{dR_2}{dT}\right)$, then

$\frac{dV_{GS}}{dT} = \frac{R_2}{R_1}\frac{dV_{REF}}{dT}$ and V_{GS} is proportional to the temperature dependence of V_{REF}.

If the MOSFET is biased at the zero TC point, then the current should have the same dependence on temperature as V_{REF}.

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Practical Aspects of Temperature-Independent and Supply-Independent Biasing

A temperature-independent and supply-independent current source and its distribution:

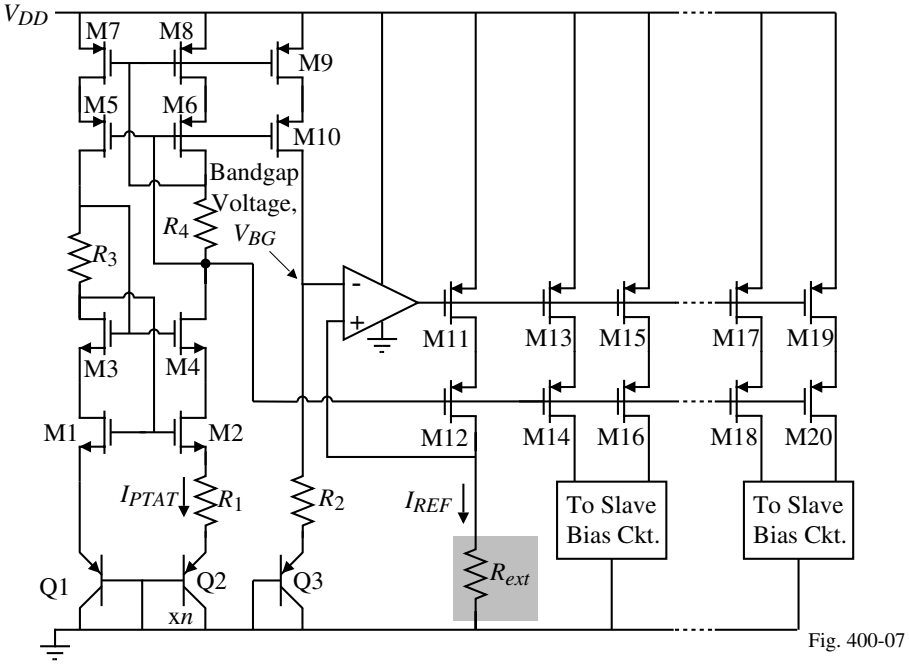

Fig. 400-07

Constant current:

$$I_{REF} = \frac{V_{BG}}{R_{ext}} \quad \text{where} \quad V_{BG} = V_{BE3} + I_{PTAT}R_2 = V_{BE3} + \frac{V_T}{R_1}\ln(n)\cdot R_2$$

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Practical Aspects of Bias Distribution Circuits - Continued

Distribution of the current avoids change in bias voltage due to *IR* drop in bias lines.

Slave bias circuit:

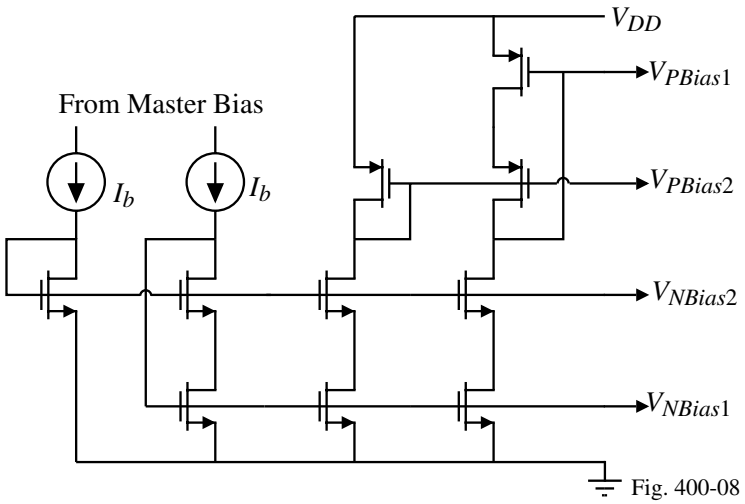

Fig. 400-08

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SUMMARY OF VOLTAGE AND CURRENT REFERENCES

- Reasonably good, simple references are possible
- Best power supply sensitivity is approximately 0.01
  (10% change in power supply causes a 0.1% change in reference)
- Typical simple reference temperature dependence is ≈ 1000 ppm/°C
- Can obtain zero temperature coefficient over a limited range of operation
- Bandgap voltage references can achieve temperature dependence less than 50 ppm/°C
- Correction of second-order effects in the bandgap voltage reference can achieve very stable (1 ppm/°C) voltage references.
- Watch out for second-order effects such as noise when using the bandgap voltage reference in sensitive applications.

We will examine bandgap voltage references once again when we consider low voltage circuits in Section 6 of Chapter 7.

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CHAPTER 4 - SUMMARY

- This chapter covered the analysis and design of sub-blocks or subcircuits including:
  - Switches
  - Current sinks and sources
  - Current and voltage references
  - MOS diode and floating resistor realizations
  - Current mirrors (amplifiers)
  - Bandgap reference
- Subcircuits represent primitives of circuit design and do not stand alone
- The current sink/source is an important subcircuit which is used for biases and ac loads
- A current sink/source is characterized by
  1.) The independence of the current on the voltage across it (r_{out})
  2.) The voltage range over which the current is not independent of the voltage (V_{MIN})
- A current mirror is characterized by
  1.) The independence of the output current on the voltage across it ($r_{out} \rightarrow$ large)
  2.) The output voltage range over which output current is dependent (V_{MIN}(out))
  3.) The independence of the input voltage on the input current ($r_{in} \rightarrow$ small)
  4.) The range of input voltage over which the input current is independent (V_{MIN}(in))
  5.) The accuracy of the current out as a function of the current in ratio.
- A voltage or current reference is independent of power supply and temperature
- The bandgap reference is the best realization of a voltage reference

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