CHAPTER 2 – CMOS TECHNOLOGY

Chapter Outline

2.1 Basic MOS Semiconductor Fabrication Processes
2.2 CMOS Technology
2.3 PN Junction
2.4 MOS Transistor
2.5 Passive Components
2.6 Other Considerations of CMOS Technology
2.7 Bipolar Transistor (optional)
2.8 BiCMOS Technology (optional)

Perspective

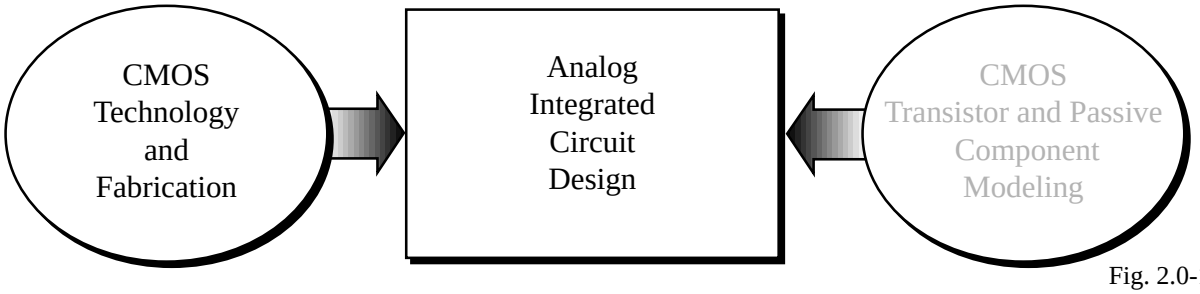


Fig. 2.0-1

Classification of Silicon Technology

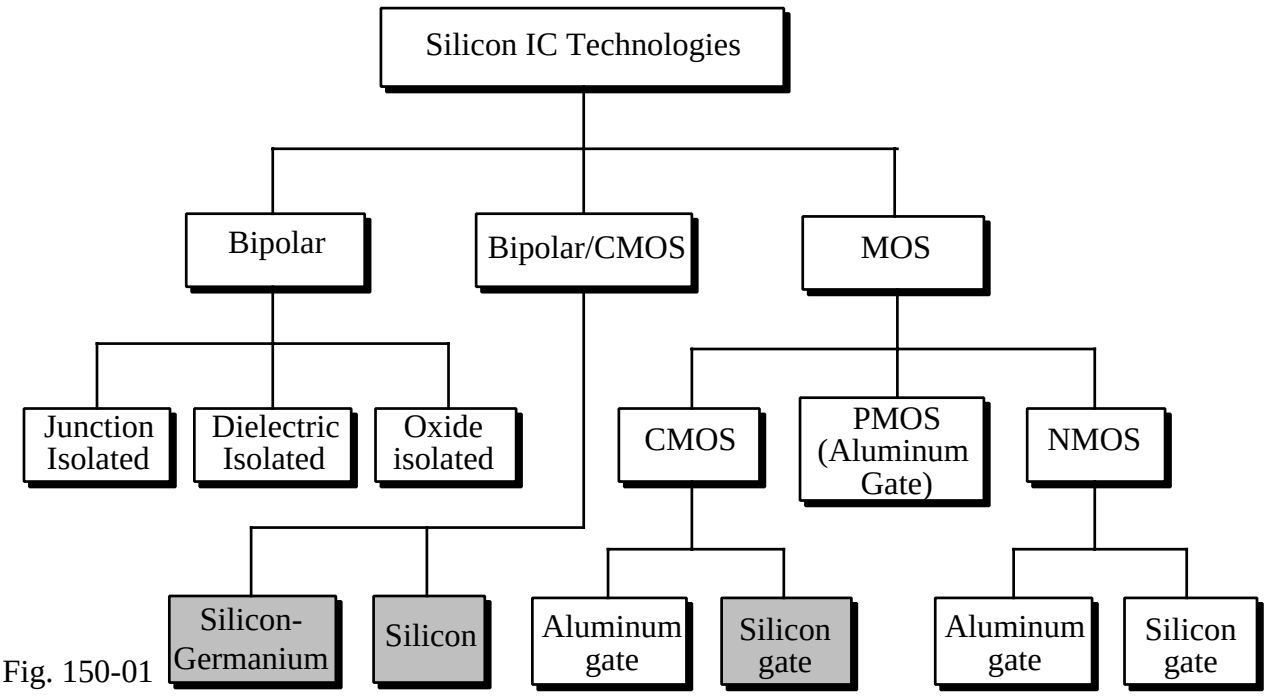


Fig. 150-01

Why CMOS Technology?

Comparison of BJT and MOSFET technology from an analog viewpoint:

Feature	BJT	MOSFET
Cutoff Frequency(f_T)	100 GHz	50 GHz (0.25µm)
Noise (thermal about the same)	Less 1/f	More 1/f
DC Range of Operation	9 decades of exponential current versus v_{BE}	2-3 decades of square law behavior
Small Signal Output Resistance	Slightly larger	Smaller for short channel
Switch Implementation	Poor	Good
Capacitor Implementation	Voltage dependent	Reasonably good

Therefore,

- Almost every comparison favors the BJT, *however* a similar comparison made from a digital viewpoint would come up on the side of CMOS.
- Therefore, since large-volume technology will be driven by digital demands, CMOS is an obvious result as the technology of availability.

Other factors:

- The potential for technology improvement for CMOS is greater than for BJT
- Performance generally increases with decreasing channel length

SECTION 2.1 - BASIC CMOS TECHNOLOGY

FUNDAMENTAL PROCESSING STEPS

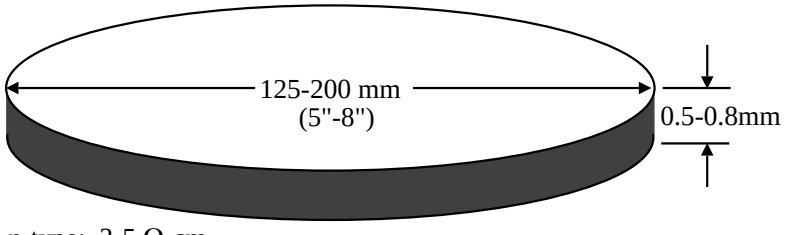
Basic steps

- Oxide growth
- Thermal diffusion
- Ion implantation
- Deposition
- Etching
- Epitaxy

Photolithography

Photolithography is the means by which the above steps are applied to selected areas of the silicon wafer.

Silicon wafer



n-type: 3-5 Ω-cm
p-type: 14-16 Ω-cm

Fig. 2.1-1r

Oxidation

Description:

Oxidation is the process by which a layer of silicon dioxide is grown on the surface of a silicon wafer.

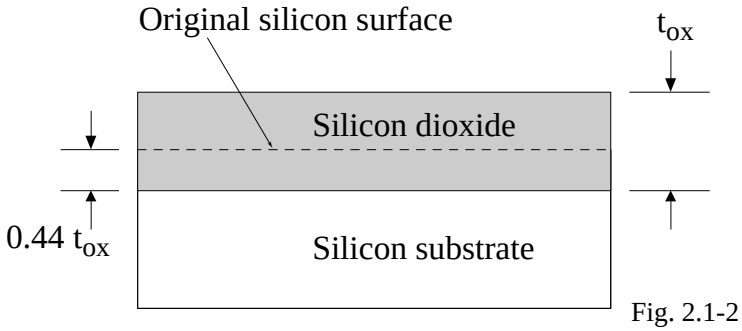


Fig. 2.1-2

Uses:

- Protect the underlying material from contamination
- Provide isolation between two layers.

Very thin oxides (100Å to 1000Å) are grown using dry oxidation techniques. Thicker oxides (>1000Å) are grown using wet oxidation techniques.

Diffusion

Diffusion is the movement of impurity atoms at the surface of the silicon into the bulk of the silicon.

Always in the direction from higher concentration to lower concentration.

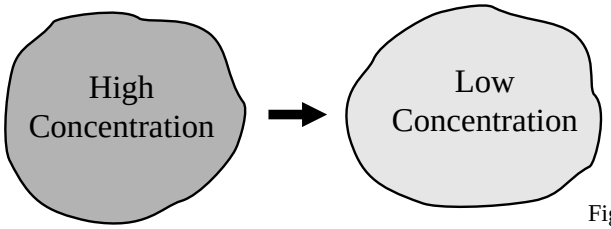
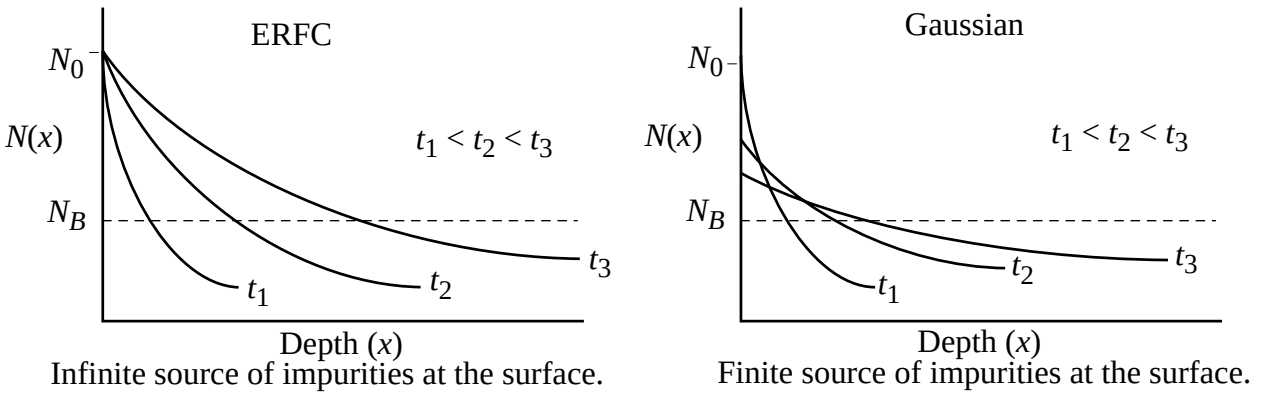


Fig. 150-04

Diffusion is typically done at high temperatures: 800 to 1400°C



Infinite source of impurities at the surface.

Finite source of impurities at the surface.

Fig. 150-05

Ion Implantation

Ion implantation is the process by which impurity ions are accelerated to a high velocity and physically lodged into the target material.

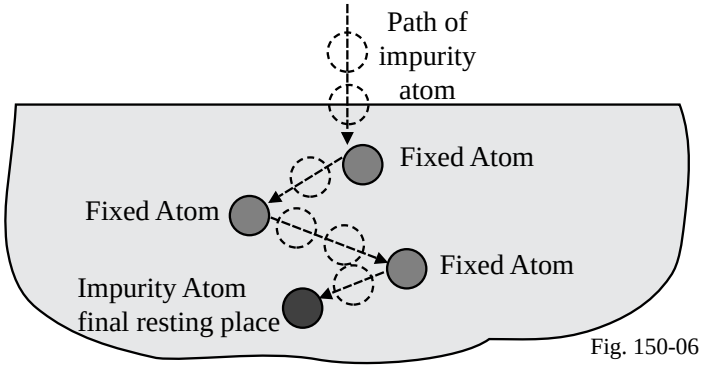


Fig. 150-06

- Annealing is required to activate the impurity atoms and repair the physical damage to the crystal lattice. This step is done at 500 to 800°C.
- Ion implantation is a lower temperature process compared to diffusion.
- Can implant through surface layers, thus it is useful for field-threshold adjustment.
- Can achieve unique doping profile such as buried concentration peak.

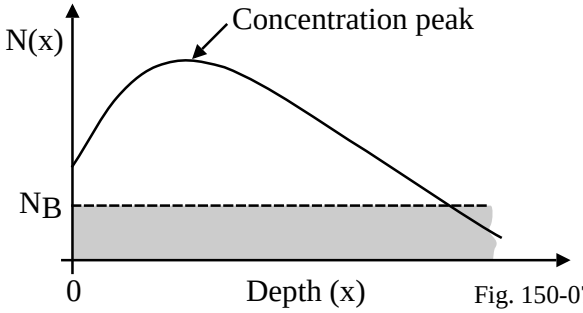


Fig. 150-07

Deposition

Deposition is the means by which various materials are deposited on the silicon wafer.

Examples:

- Silicon nitride (Si_3N_4)
- Silicon dioxide (SiO_2)
- Aluminum
- Polysilicon

There are various ways to deposit a material on a substrate:

- Chemical-vapor deposition (CVD)
- Low-pressure chemical-vapor deposition (LPCVD)
- Plasma-assisted chemical-vapor deposition (PECVD)
- Sputter deposition

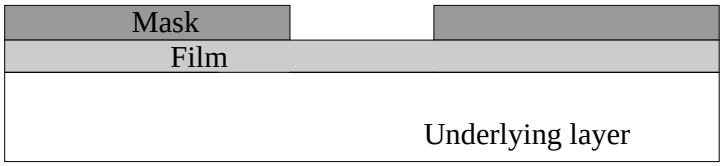
Material that is being deposited using these techniques covers the entire wafer.

Etching

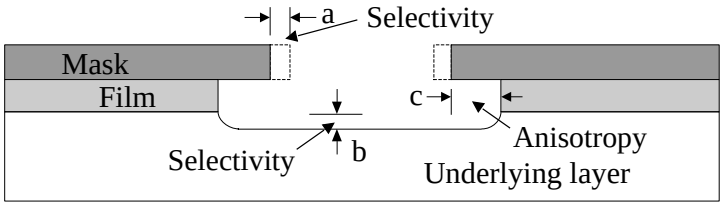
Etching is the process of selectively removing a layer of material.

When etching is performed, the etchant may remove portions or all of:

- The desired material
- The underlying layer
- The masking layer



(a) Portion of the top layer ready for etching.



(b) Horizontal etching and etching of underlying layer.

Fig. 150-08

Important considerations:

- *Anisotropy* of the etch is defined as,

  A = 1-(lateral etch rate/vertical etch rate)

- *Selectivity* of the etch (film to mask and film to substrate) is defined as,

$$S_{film\text{-}mask} = \frac{\text{film etch rate}}{\text{mask etch rate}}$$

A = 1 and $S_{film\text{-}mask} = \infty$ are desired.

There are basically two types of etches:

- Wet etch which uses chemicals
- Dry etch which uses chemically active ionized gases.

Epitaxy

Epitaxial growth consists of the formation of a layer of single-crystal silicon on the surface of the silicon material so that the crystal structure of the silicon is continuous across the interfaces.

- It is done externally to the material as opposed to diffusion which is internal
- The epitaxial layer (epi) can be doped differently, even oppositely, of the material on which it grown
- It accomplished at high temperatures using a chemical reaction at the surface
- The epi layer can be any thickness, typically 1-20 microns

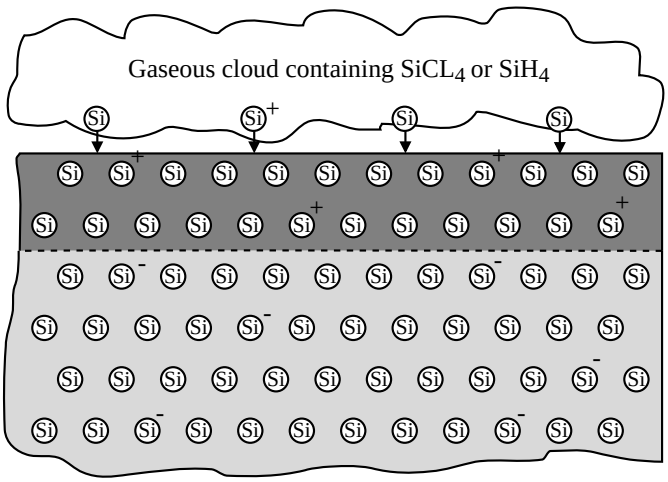


Fig. 150-09

Photolithography

Components

- Photoresist material
- Mask
- Material to be patterned (e.g., oxide)

Positive photoresist

Areas exposed to UV light are soluble in the developer

Negative photoresist

Areas not exposed to UV light are soluble in the developer

Steps

1. Apply photoresist
2. Soft bake (drives off solvents in the photoresist)
3. Expose the photoresist to UV light through a mask
4. Develop (remove unwanted photoresist using solvents)
5. Hard bake (≈ 100°C)
6. Remove photoresist (solvents)

Illustration of Photolithography - Exposure

The process of exposing selective areas to light through a photo-mask is called *printing*.

Types of printing include:

- Contact printing
- Proximity printing
- Projection printing

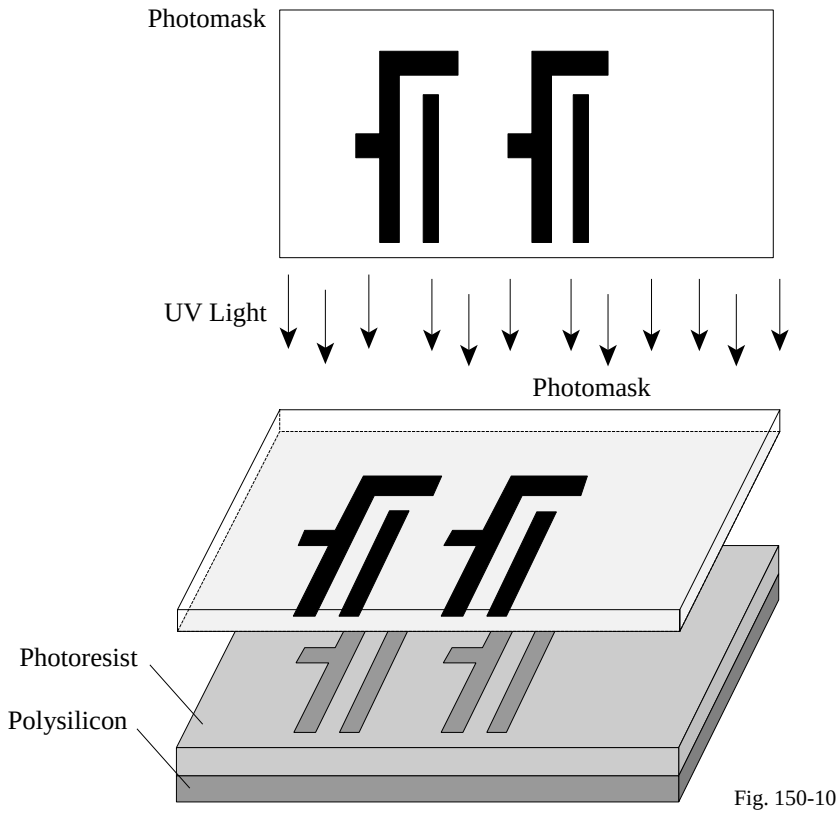


Fig. 150-10

Illustration of Photolithography - Positive Photoresist

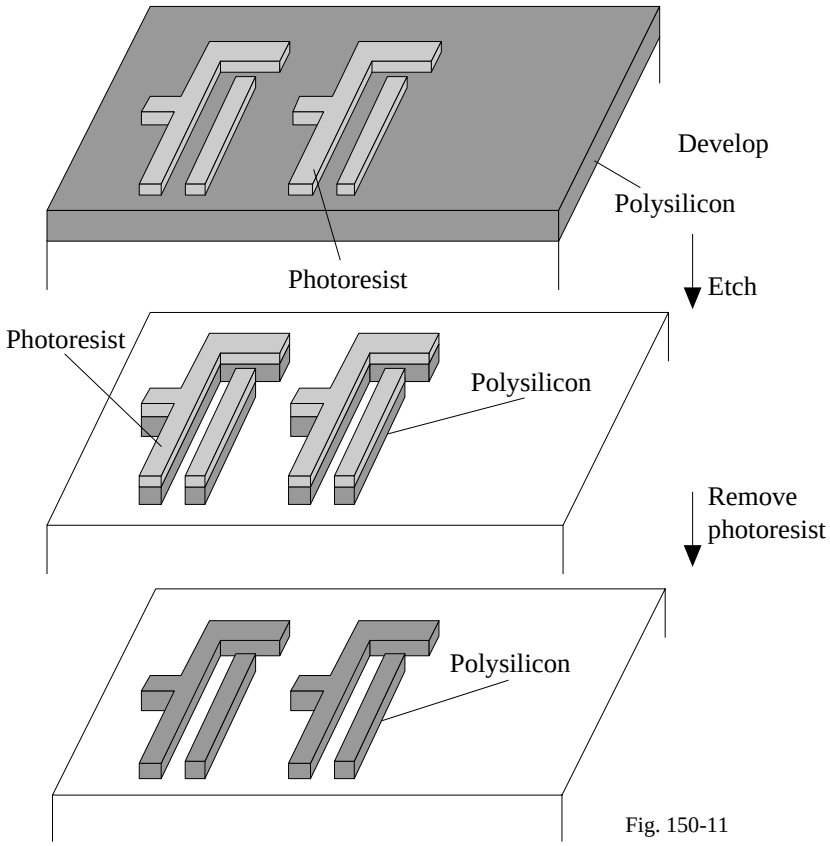


Fig. 150-11

Illustration of Photolithography - Negative Photoresist

(Not used much any more)

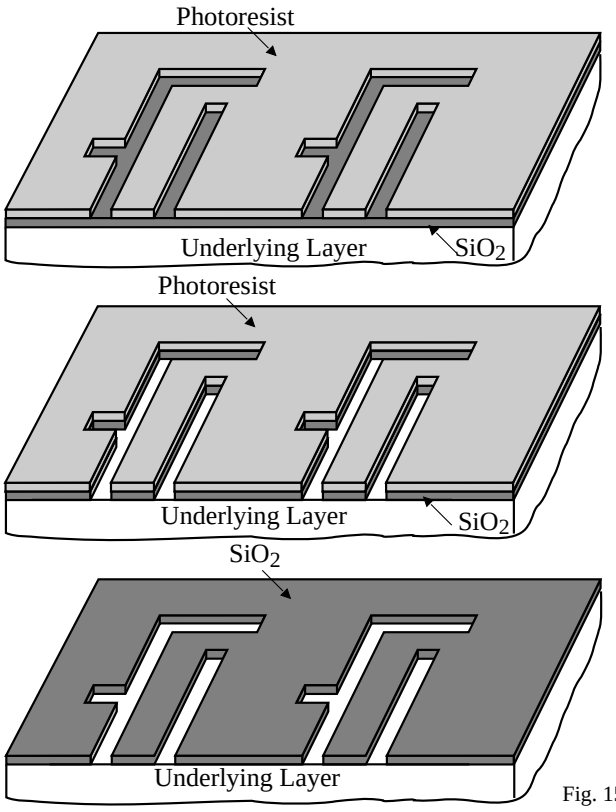


Fig. 150-12

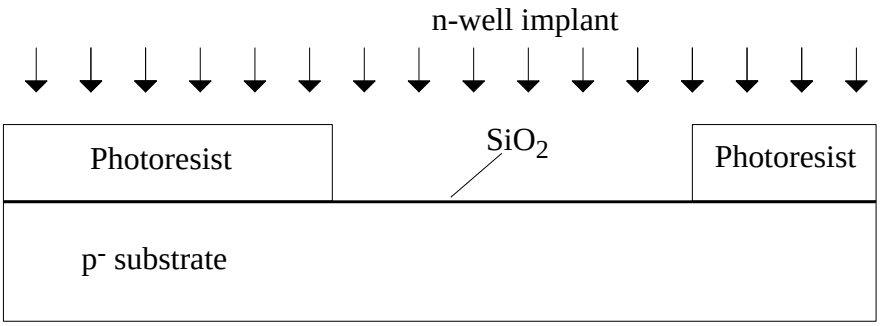
TYPICAL CMOS FABRICATION PROCESS

N-Well CMOS Fabrication Major Steps

1.) Implant and diffuse the n-well
2.) Deposition of silicon nitride
3.) n-type field (channel stop) implant
4.) p-type field (channel stop) implant
5.) Grow a thick field oxide (FOX)
6.) Grow a thin oxide and deposit polysilicon
7.) Remove poly and form LDD spacers
8.) Implantation of NMOS S/D and n-material contacts
9.) Remove spacers and implant NMOS LDDs
10.) Repeat steps 8.) and 9.) for PMOS
11.) Anneal to activate the implanted ions
12.) Deposit a thick oxide layer (BPSG - borophosphosilicate glass)
13.) Open contacts, deposit first level metal and etch unwanted metal
14.) Deposit another interlayer dielectric (CVD SiO_2), open vias, deposit 2nd level metal
15.) Etch unwanted metal, deposit a passivation layer and open over bonding pads

Major CMOS Process Steps

Step 1 - Implantation and diffusion of the n-wells



Step 2 - Growth of thin oxide and deposition of silicon nitride

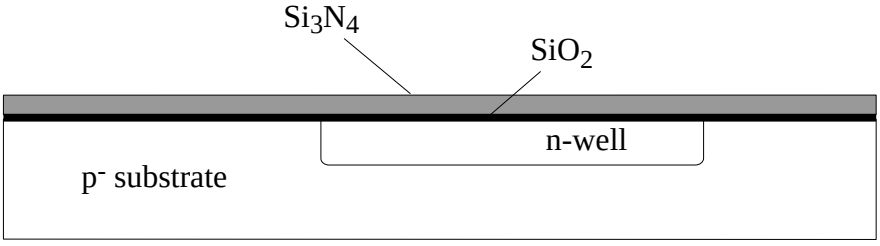
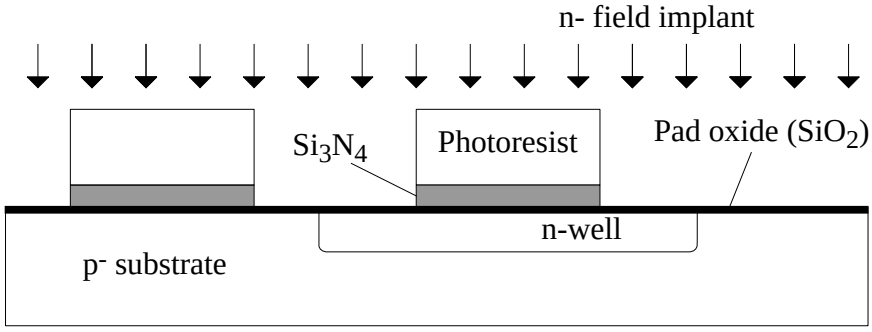


Fig. 180-01

Major CMOS Process Steps - Continued

Step 3.) Implantation of the n-type field channel stop



Step 4.) Implantation of the p-type field channel stop

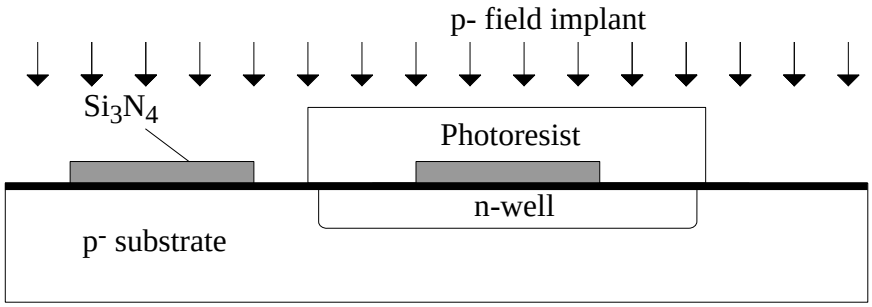
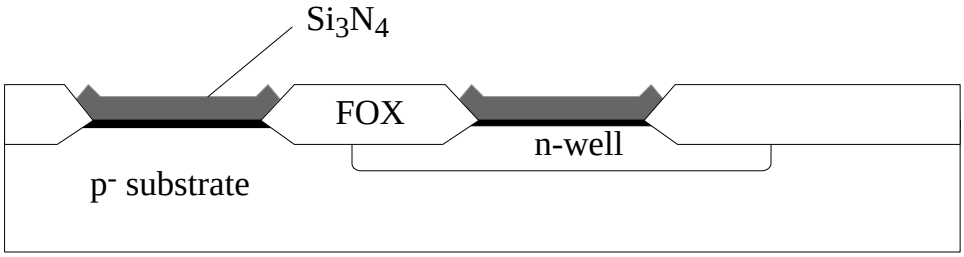


Fig. 180-02

Major CMOS Process Steps – Continued

Step 5.) Growth of the thick field oxide (LOCOS - *loc*alized *o*xidation of *s*ilicon)



Step 6.) Growth of the gate thin oxide and deposition of polysilicon

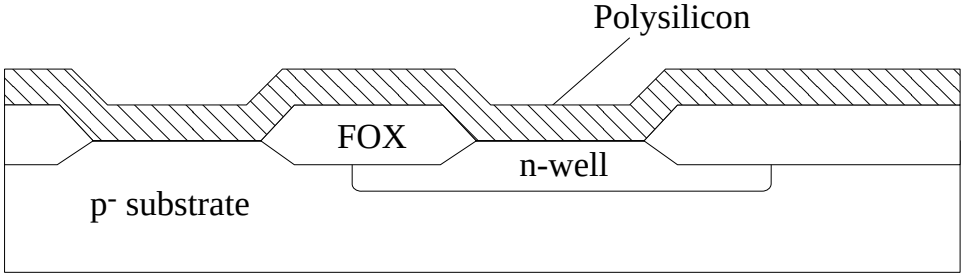
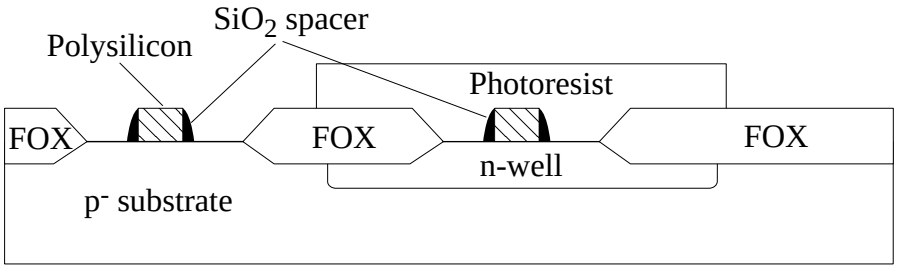


Fig. 180-03

Major CMOS Process Steps - Continued

Step 7.) Removal of polysilicon and formation of the sidewall spacers



Step 8.) Implantation of NMOS source and drain and contact to n-well (not shown)

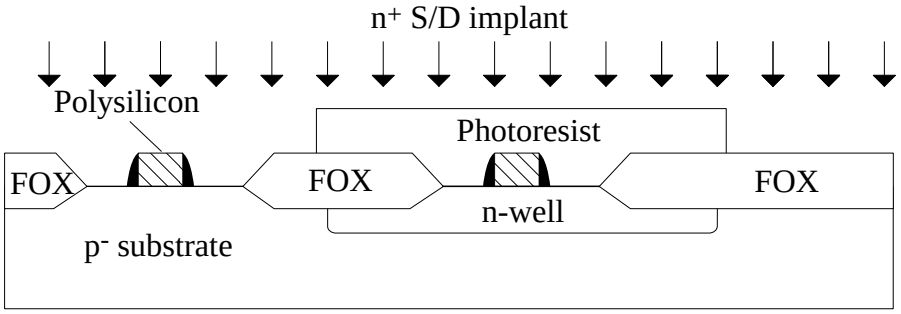
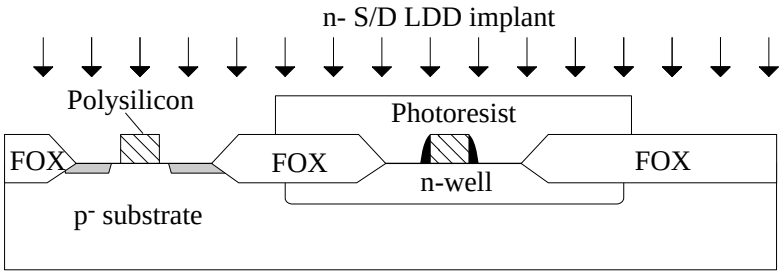


Fig. 180-04

Major CMOS Process Steps - Continued

Step 9.) Remove sidewall spacers and implant the NMOS lightly doped source/drains



Step 10.) Implant the PMOS source/drains and contacts to the p- substrate (not shown), remove the sidewall spacers and implant the PMOS lightly doped source/drains

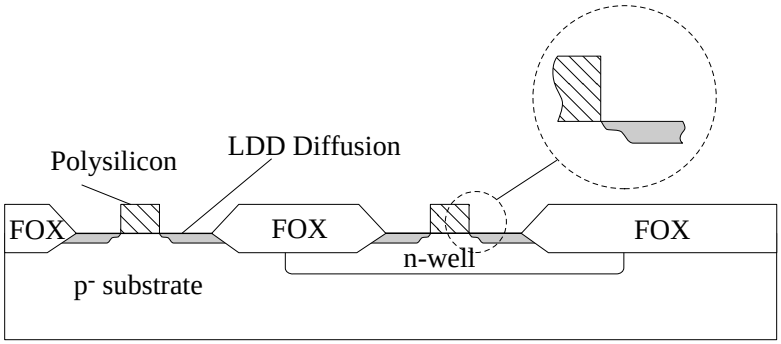
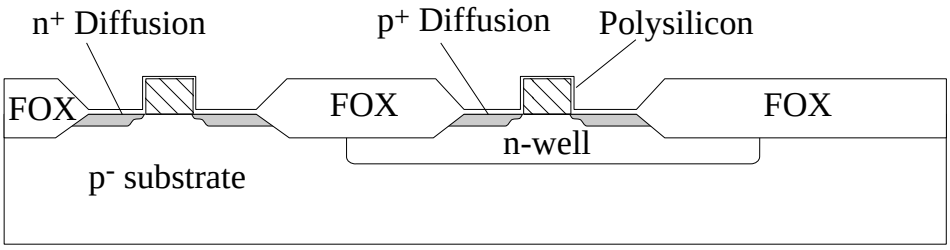


Fig. 180-05

Major CMOS Process Steps – Continued

Step 11.) Anneal to activate the implanted ions



Step 12.) Deposit a thick oxide layer (BPSG - borophosphosilicate glass)

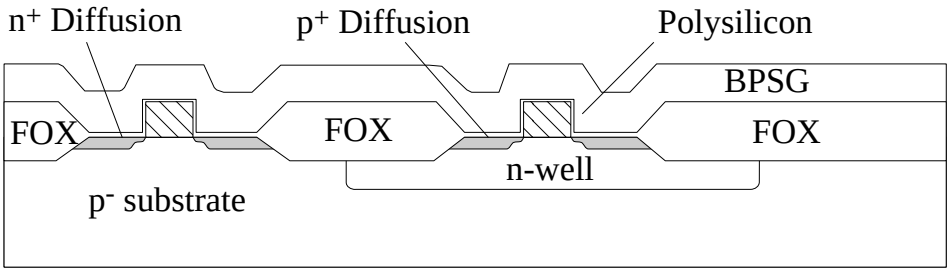
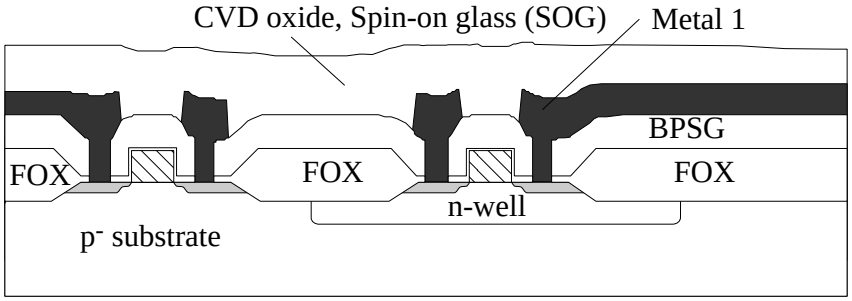


Fig. 180-06

Major CMOS Process Steps - Continued

Step 13.) Open contacts, deposit first level metal and etch unwanted metal



Step 14.) Deposit another interlayer dielectric (CVD SiO_2), open contacts, deposit second level metall

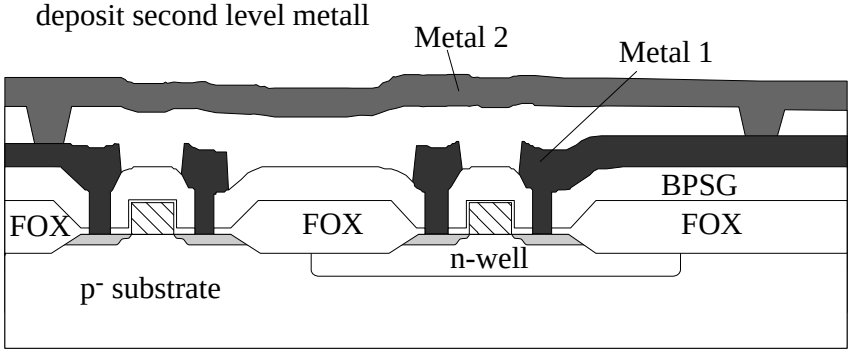


Fig. 180-07

Major CMOS Process Steps – Continued

Step 15.) Etch unwanted metal and deposit a passivation layer and open over bonding pads

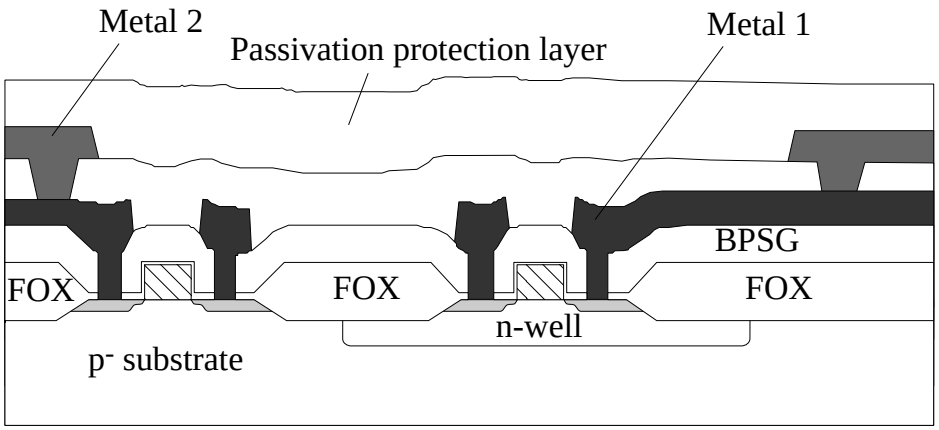


Fig. 180-08

p-well process is similar but starts with a p-well implant rather than an n-well implant.

Approximate Side View of CMOS Fabrication

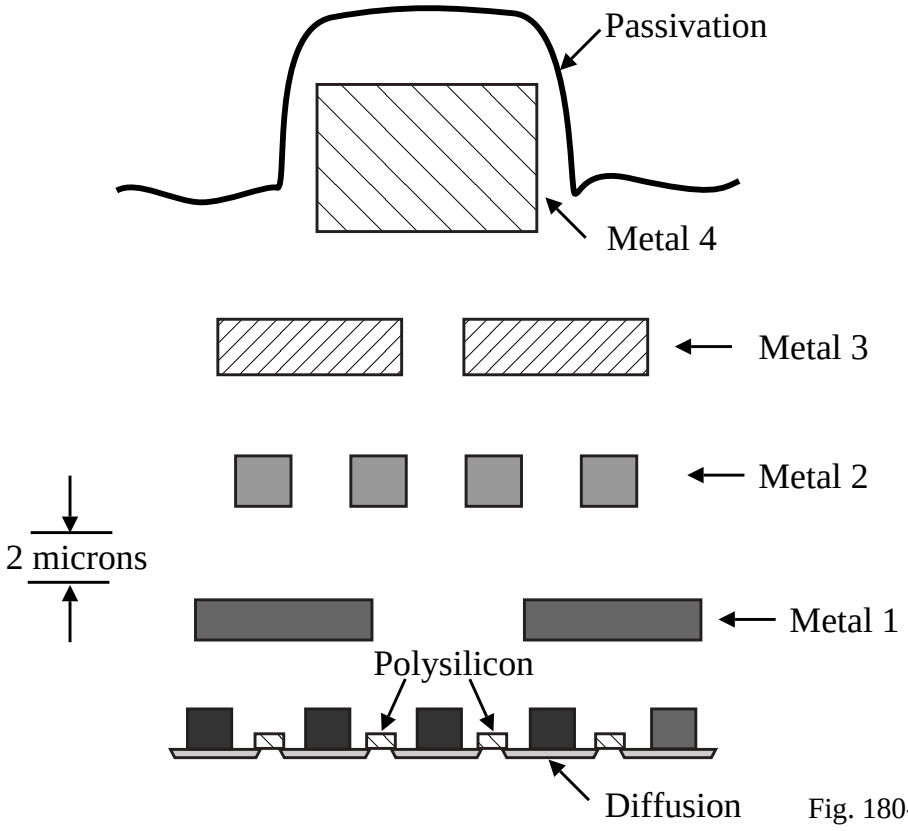
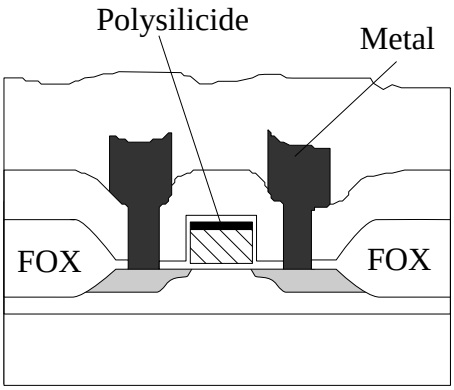


Fig. 180-09

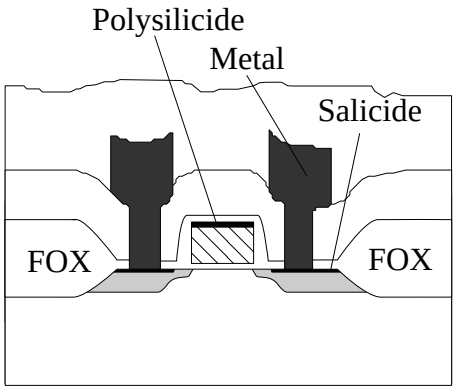
Silicide/Salicide Technology

Used to reduce interconnect resistivity by placing a low-resistance silicide such as $TiSi_2$, WSi_2, $TaSi_2$, etc. on top of polysilicon

Salicide technology (self-aligned silicide) provides low resistance source/drain connections as well as low-resistance polysilicon.



Polycide structure



Salicide structure

Fig 180-10

Scanning Electron Microscope of a MOSFET Cross-section

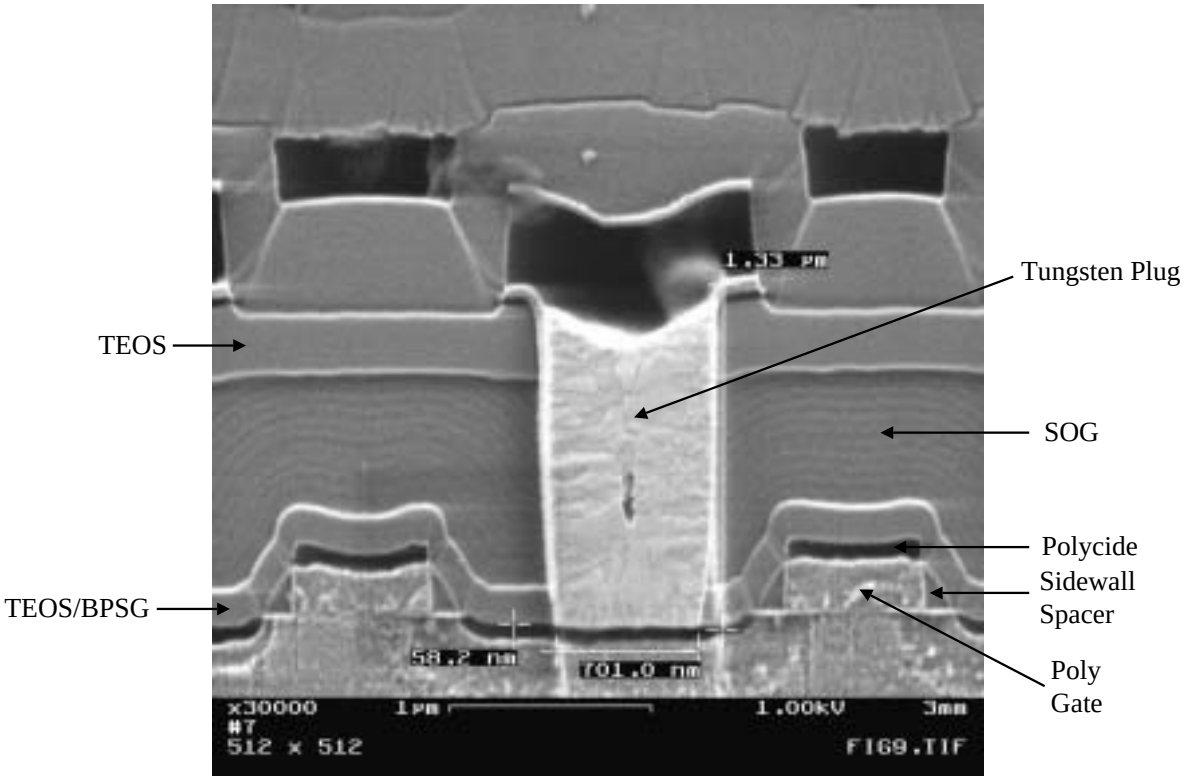


Fig. 2.8-20

Scanning Electron Microscope Showing Metal Levels and Interconnect

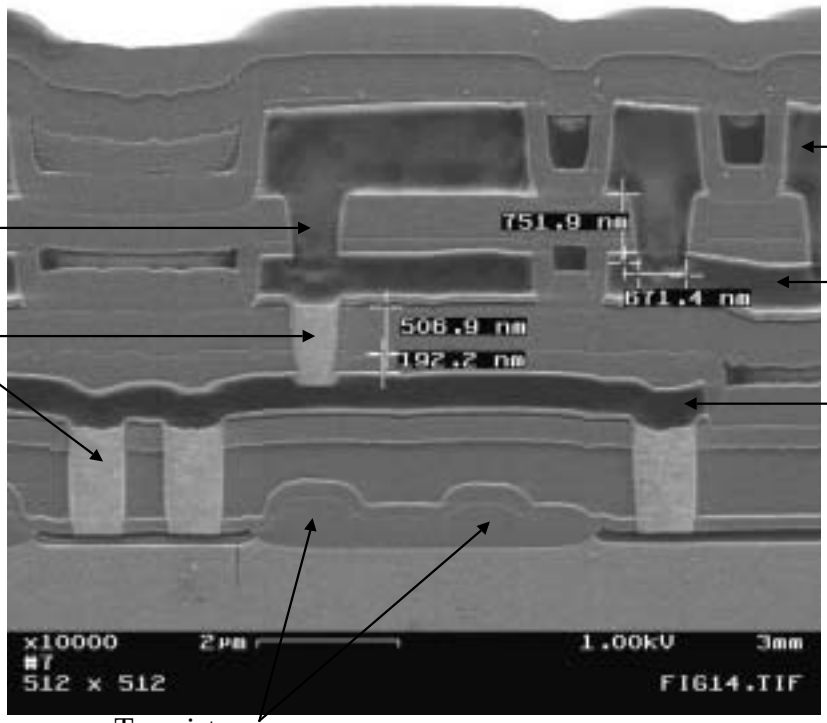


Fig.180-11

SUMMARY

- Fabrication is the means by which the circuit components, both active and passive, are built as an integrated circuit.
- Basic process steps include:
  1.) Oxide growth 2.) Thermal diffusion 3.) Ion implantation
  4.) Deposition 5.) Etching 6.) Epitaxy
- The complexity of a process can be measured in the terms of the number of masking steps or masks required to implement the process.
- Major CMOS Processing Steps:
  1.) Well definition
  2.) Definition of active areas and substrate/well contacts (SiNi3)
  3.) Thick field oxide (FOX)
  4.) Thin field oxide and polysilicon
  5.) Diffusion of the source and drains (includes the LDD)
  6.) Dielectric layer/Contacts
  7.) Metallization
  8.) Dielectric layer/Vias
  9.) Metallization
  10.) Passivation
  11.) Bond pad openings

SECTION 2.2 - THE *PN* JUNCTION

Abrupt Junction

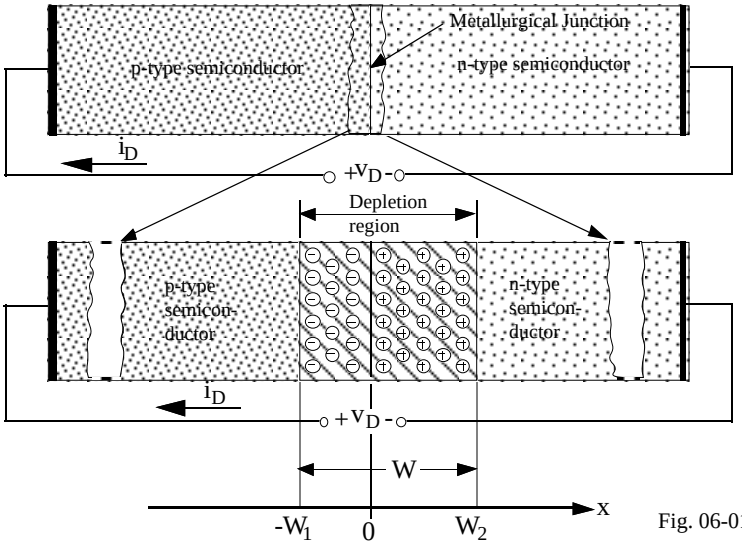


Fig. 06-01

1. Doped atoms near the metallurgical junction lose their free carriers by diffusion.
2. As these fixed atoms lose their free carriers, they build up an electric field, which opposes the diffusion mechanism.
3. Equilibrium conditions are reached when:

Current due to diffusion = Current due to electric field

Mathematical Characterization of the Abrupt *PN* Junction

Assume the pn junction is open-circuited.

Cross-section of an ideal pn junction:

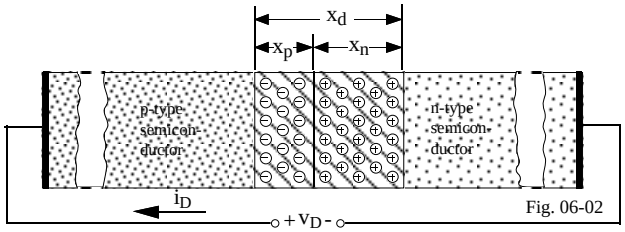


Fig. 06-02

Symbol for the *pn* junction:

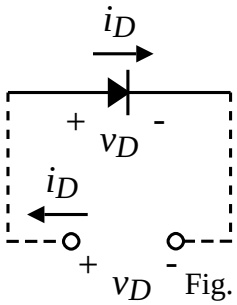


Fig. 06-03

Built-in potential, ψ_o:

$$\psi_o = V_t \ln\left(\frac{N_A N_D}{n_i^2}\right),$$

where $V_t = \frac{kT}{q}$ and

n_i^2 is the intrinsic concentration of silicon.

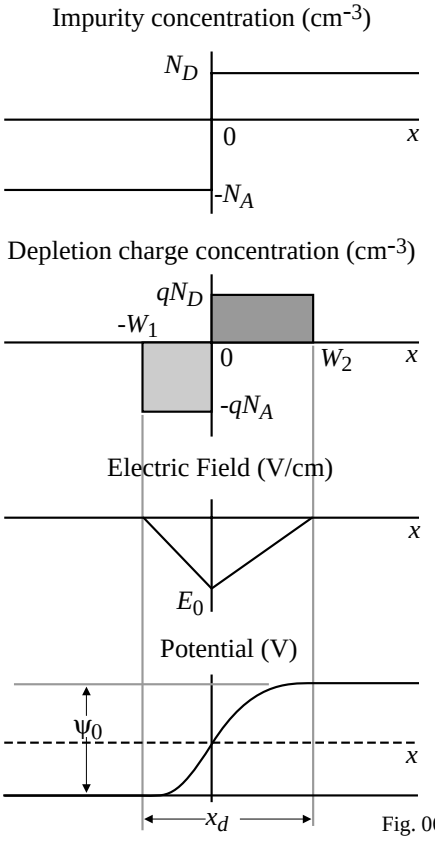


Fig. 06-04A

Physics of Abrupt *PN* Junctions

Apply a forward bias voltage, v_D, to the *pn* junction:

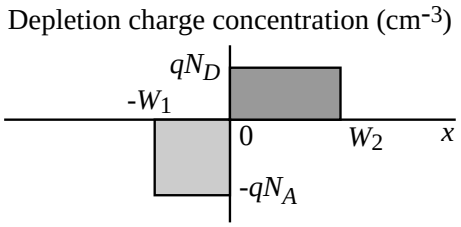
1.) The voltage across the junction is $\psi_o - v_D$.

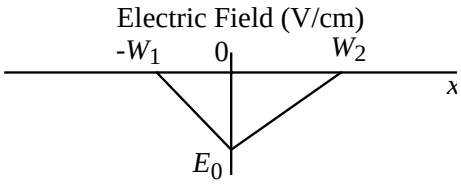
2.) Charge equality requires that $W_1N_A = W_2N_D$ where
W_1 (W_2) = depletion region width on the *p*-side(*n*-side)

3.) Poisson's equation in one dimension is

$$\frac{d^2v}{dx^2} = -\frac{\rho}{\varepsilon} = \frac{qN_A}{\varepsilon} \quad \text{for} \quad -W_1<x<0$$

where
ρ = charge density
q = charge of an electron (1.6×10^{-19} coulomb)
$\varepsilon = K_S\varepsilon_o$
K_S = dielectric constant of silicon
ε_o = permittivity of free space (8.86×10^{-14}F/cm)





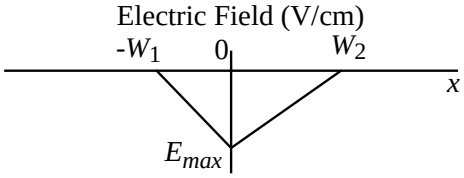
4.) Integrating Poisson's equation gives, $\frac{dv}{dx} = \frac{qN_A}{\varepsilon}x + C_1$

5.) The electric field, $\mathcal{E} = -\frac{dv}{dx} = -\left(\frac{qN_A}{\varepsilon}x + C_1\right)$

Physics of Abrupt *PN* Junctions - Continued

6.) Since there is zero electric field outside the depletion region, a boundary condition is

$\mathcal{E} = 0$ for $x = -W_1$

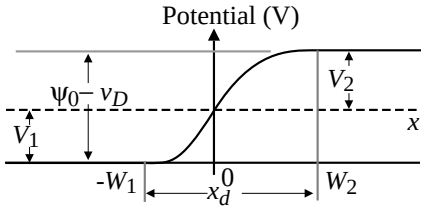


This gives,

$$\mathcal{E} = -\frac{dv}{dx} = -\frac{qN_A}{\varepsilon}(x + W_1) \quad \text{for} \quad -W_1 < x < 0$$

Note that the maximum electric field occurs at $x = 0$ which gives

$$\mathcal{E}_{max} = -\left(\frac{qN_AW_1}{\varepsilon}\right)$$



7.) Integration of the electric field gives,

$$v = \frac{qN_A}{\varepsilon}\left(\frac{x^2}{2} + W_1x\right) + C_2$$

8.) A second boundary condition is obtained by assuming that the potential of the neutral *p*-type region is zero. This boundary condition is,

$v = 0$ for $x = -W_1$

Substituting in the expression above gives,

$$v = \frac{qN_A}{\varepsilon}\left(\frac{x^2}{2} + W_1x + \frac{W_1^2}{2}\right)$$

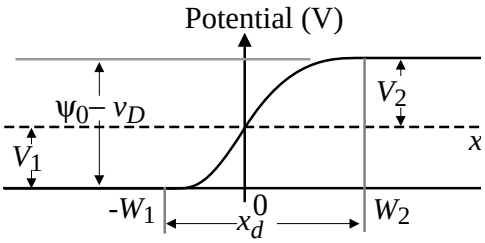
Physics of Abrupt *PN* Junctions - Continued

9.) At x =0, we define the potential $v = V_1$ which gives

$$V_1 = \frac{qN_A}{\varepsilon}\frac{W_1^2}{2}$$

If the potential difference from $x = 0$ to $x = W_2$ is V_2, then

$$V_2 = \frac{qN_D}{\varepsilon}\frac{W_2^2}{2}$$



10.) The total voltage across the *pn* junction is

$$\psi_o - v_D = V_1 + V_2 = \frac{q}{2\varepsilon}\left(N_A W_1^2 + N_D W_2^2\right)$$

11.) Substituting $W_1 N_A = W_2 N_D$ into the above expression gives

$$\psi_o - v_D = \frac{qN_A W_1^2}{2\varepsilon}\left[1 + \frac{N_D}{N_A}\left(\frac{W_2}{W_1}\right)^2\right] = \frac{qN_A W_1^2}{2\varepsilon}\left(1 + \frac{N_A}{N_D}\right)$$

12.) The depletion region width on the *p*-side of the *pn* junction is given as

$$W_1 = \sqrt{\frac{2\varepsilon(\psi_o - v_D)}{qN_A\left(1 + \frac{N_A}{N_D}\right)}} \qquad \text{and} \quad W_2 = \sqrt{\frac{2\varepsilon(\psi_o - v_D)}{qN_D\left(1 + \frac{N_D}{N_A}\right)}}$$

Summary of the Abrupt *PN* Junction Characterization

Barrier potential-

$$\psi_o = \frac{kT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right) = V_t \ln\left(\frac{N_A N_D}{n_i^2}\right)$$

Depletion region widths-

$$\left.\begin{aligned} W_1 &= \sqrt{\frac{2\varepsilon_{si}(\psi_o - v_D)N_D}{qN_A(N_A+N_D)}} \\ W_2 &= \sqrt{\frac{2\varepsilon_{si}(\psi_o - v_D)N_A}{qN_D(N_A+N_D)}} \end{aligned}\right\} \quad W \propto \sqrt{\frac{1}{N}}$$

Depletion capacitance-

$$C_j = \frac{\varepsilon_{si}A}{d} = \frac{\varepsilon_{si}A}{W_1+W_2} = \frac{\varepsilon_{si}A}{\sqrt{\frac{2\varepsilon_{si}(\psi_o - v_D)}{q(N_D+N_A)}}\left[\sqrt{\frac{N_D}{N_A}}+\sqrt{\frac{N_A}{N_D}}\right]}$$

$$= A\sqrt{\frac{\varepsilon_{si}qN_AN_D}{2(N_A+N_D)}}\frac{1}{\sqrt{\psi_o - v_D}} = \frac{C_{j0}}{\sqrt{1 - \frac{v_D}{\psi_o}}}$$

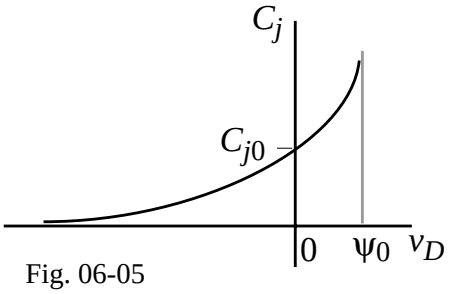


Fig. 06-05

Example 1

An abrupt silicon *pn* junction has the doping densities of $N_A = 10^{15}$ atoms/cm^3 and $N_D = 10^{16}$ atoms/cm^3. Calculate the junction built-in potential, the depletion-layer widths, the maximum field and the depletion capacitance with 10V reverse bias if $C_{j0} = 3$pF.

Solution

At room temperature, $kT/q = 26$mV and the intrinsic concentration is $n_i = 1.5\text{x}10^{10}$ cm^{-3}.

Therefore, the junction built-in potential is $\psi_o = 0.026 \ln\left(\frac{10^{15}\cdot 10^{16}}{2.25\text{x}10^{26}}\right) = \underline{0.637\text{V}}$

The depletion width on the p-side is,

$$W_1 = \sqrt{\frac{2\cdot 1.04\text{x}10^{-12}\cdot 10.64}{1.6\text{x}10^{-19}\cdot 10^{15}\cdot 1.1}} = 3.55\text{x}10^{-4}\text{ cm} = \underline{3.55\mu\text{m}}$$

The depletion width on the n-side is,

$$W_2 = \sqrt{\frac{2\cdot 1.04\text{x}10^{-12}\cdot 10.64}{1.6\text{x}10^{-19}\cdot 10^{16}\cdot 11}} = 0.35\text{x}10^{-4}\text{ cm} = \underline{0.35\mu\text{m}}$$

The maximum field occurs for $x = 0$ and is

$$E_{max} = -\frac{qN_A}{\varepsilon} W_1 = \left(\frac{-1.6\text{x}10^{-19}\cdot 10^{15}\cdot 3.5\text{x}10^{-4}}{1.04\text{x}10^{-12}}\right) = \underline{-5.38\text{x}10^4\text{ V/cm}}$$

The depletion capacitance can be found as $C_j = \frac{3\text{pF}}{\sqrt{1 + (10/0.637)}} = \underline{0.734\text{pF}}$

Reverse Breakdown and Leakage Current Characteristics of the *PN* Junction

Breakdown voltage

$$V_R = \frac{\varepsilon_{si}(N_A+N_D)}{2qN_AN_D} \quad E_{max}^2 \propto \frac{1}{N}$$

where E_{max}^2 is the maximum electric field before breakdown occurs (usually due to avalanche breakdown).

Reverse leakage current

The reverse current, I_R, increases by a multiplication factor M as the reverse voltage increases and is

$$I_{RA} = MI_R$$

where

$$M = \frac{1}{1 - \left(\frac{V_R}{BV}\right)^n}$$

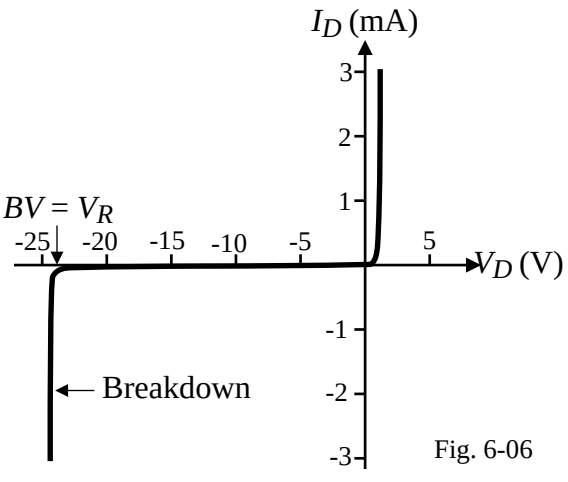


Fig. 6-06

Example 2

An abrupt *pn* junction has doping densities of $N_A = 3\text{x}10^{16}$ atoms/cm^3 and $N_D = 4\text{x}10^{19}$ atoms/cm^3. Calculate the breakdown voltage if $E_{crit} = 3\text{x}10^5$ V/cm.

Solution

$$V_R = \frac{\varepsilon_{si}(N_A+N_D)}{2qN_AN_D}E_{max}^2 \approx \frac{\varepsilon_{si}}{2qN_A}E_{max}^2 = \frac{1.04\text{x}10^{-12}\cdot 9\text{x}10^{10}}{2\cdot 1.6\text{x}10^{-19}\cdot 3\text{x}10^{16}} = \underline{9.7\text{V}}$$

Summary of a Graded *PN* Junction Characterization

Graded junction:

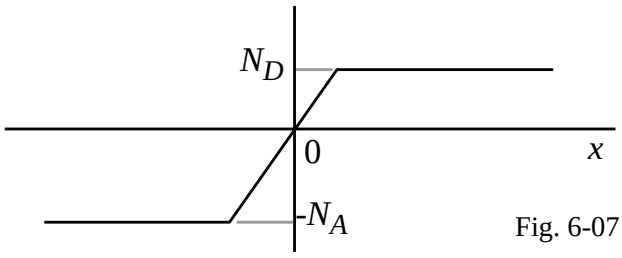


Fig. 6-07

The previous expressions become:

Depletion region widths-

$$\left.\begin{aligned} W_1 &= \left(\frac{2\varepsilon_{si}(\psi_o-v_D)N_D}{qN_A(N_A+N_D)}\right)^m \\ W_2 &= \left(\frac{2\varepsilon_{si}(\psi_o-v_D)N_A}{qN_D(N_A+N_D)}\right)^m \end{aligned}\right\} \quad W \propto \left(\frac{1}{N}\right)^m$$

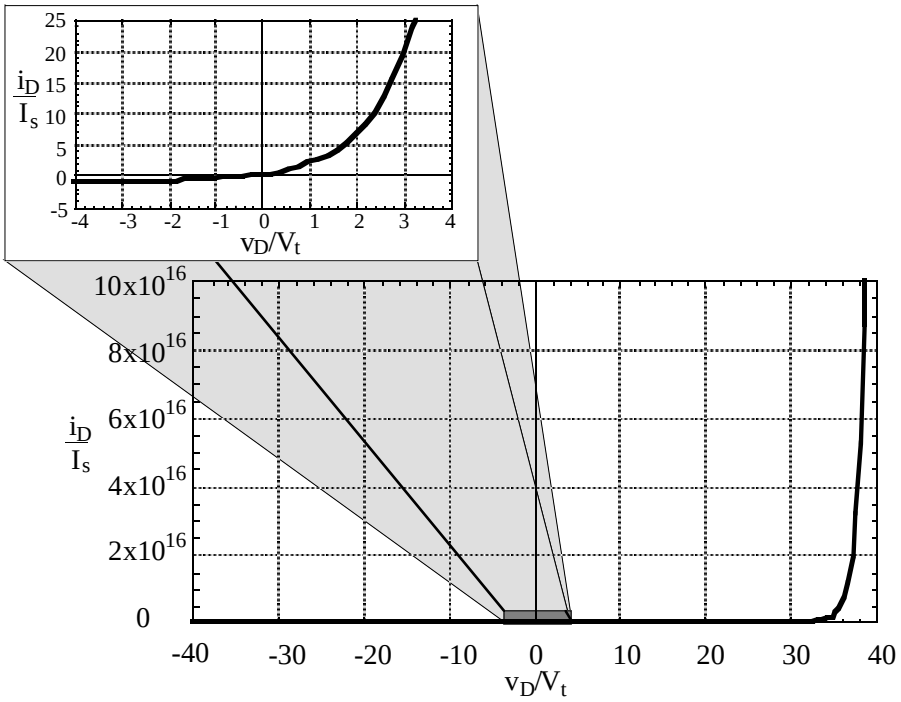
Depletion capacitance-

$$C_j = A\left(\frac{\varepsilon_{si}qN_AN_D}{2(N_A+N_D)}\right)^m \frac{1}{(\psi_o-v_D)^m} = \frac{C_{j0}}{\left(1-\frac{v_D}{\psi_o}\right)^m}$$

where $0.33 \le m \le 0.5$.

Forward Bias Current-Voltage Relationship of the *PN* Junction

$$i_D = I_s\left[\exp\left(\frac{v_D}{V_t}\right) - 1\right] \quad \text{where } I_s = qA\left[\frac{D_p p_{no}}{L_p} + \frac{D_n n_{po}}{L_n}\right] \approx \frac{qAD}{L}\frac{n_i^2}{N} = KT^3\exp\left(\frac{-V_{GO}}{V_t}\right)$$



Metal-Semiconductor Junctions

Ohmic Junctions: A pn junction formed by a highly doped semiconductor and metal.

Energy band diagram IV Characteristics

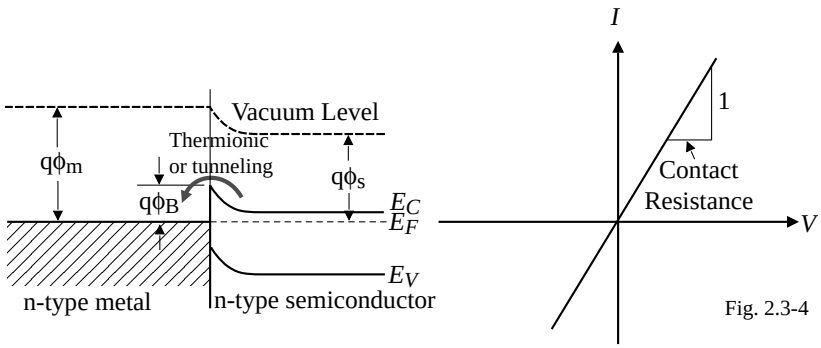


Fig. 2.3-4

Schottky Junctions: A pn junction formed by a lightly doped semiconductor and metal.

Energy band diagram IV Characteristics

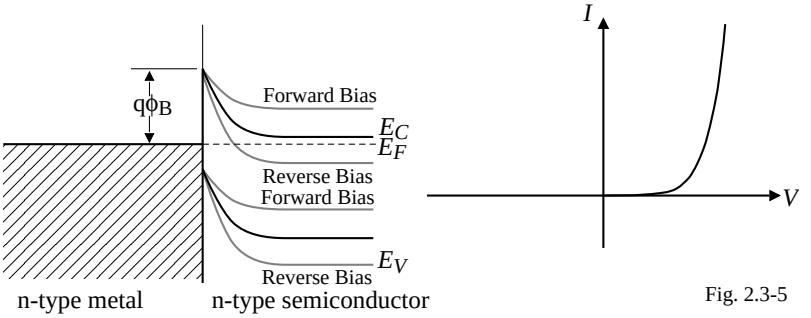


Fig. 2.3-5

SUMMARY

Characterized the reverse bias operation of the abrupt pn junction

- pn junction has a barrier potential ψ_o
- Depletion region widths are proportional to $N^{-0.5}$
- The pn junction depletion region acts like a voltage dependent capacitance

Applications of the reverse biased pn junction

- Isolate transistors from the material they are built in
- Variable capacitors - varactors

SECTION 2.3 - THE MOS TRANSISTOR

Physical Structure of the n-channel and p-channel transistor in an n-well technology

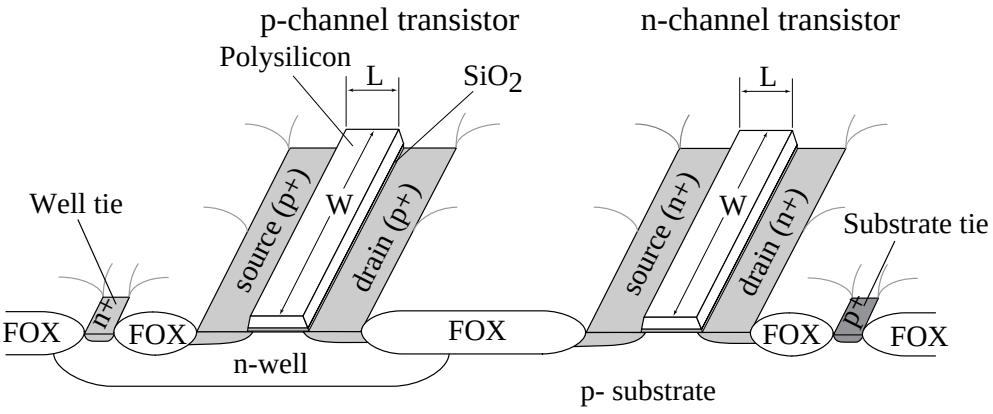


Fig. 2.4-1

How does the transistor work?

Consider the enhancement n-channel MOSFET:

When the gate is positive with respect to the substrate a depletion region is formed beneath the gate resulting in holes being pushed away from the Si-SiO_2 interface.

When the gate voltage is sufficiently large (0.5-0.7V), the region beneath the gate inverts and a n-channel is formed between the source and drain.

The MOSFET Threshold Voltage

When the gate voltage reaches a value called the *threshold voltage* (V_T), the substrate beneath the gate becomes inverted (it changes from p-type to n-type).

$$V_T = \phi_{MS} + \left(-2\phi_F - \frac{Q_b}{C_{ox}}\right) + \left(\frac{Q_{SS}}{C_{ox}}\right)$$

where

$\phi_{MS} = \phi_F$(substrate) - ϕ_F(gate)

ϕ_F = Equilibrium electrostatic potential (Femi potential)

$$\phi_F(\text{PMOS}) = \frac{kT}{q} ln(N_D/n_i) = V_t\, ln(N_D/n_i)$$

$$\phi_F(\text{NMOS}) = \frac{kT}{q} ln(n_i/N_A) = V_t\, ln(n_i/N_A)$$

$$Q_b \approx \sqrt{2q\mathrm{N}_A\varepsilon_{si}(|-2\phi_F+v_{SB}|)}$$

Q_{SS} = undesired positive charge present between the oxide and the bulk silicon

Rewriting the threshold voltage expression gives,

$$V_T = \phi_{MS} - 2\phi_F - \frac{Q_{b0}}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} - \frac{Q_b - Q_{b0}}{C_{ox}} = V_{T0} + \gamma\left(\sqrt{|-2\phi_F + v_{SB}|} - \sqrt{|-2\phi_F|}\right)$$

where

$$V_{T0} = \phi_{MS} - 2\phi_F - \frac{Q_{b0}}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} \quad \text{and} \quad \gamma = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}}$$

Signs for the Quantities in the Threshold Voltage Expression

Parameter	N-Channel	P-Channel
Substrate	p-type	n-type
ϕ_{MS}		
Metal	–	–
n^+ Si Gate	–	–
p^+ Si Gate	+	+
ϕ_F	–	+
Q_{b0},Q_b	–	+
Q_{ss}	+	+
V_{SB}	+	–
γ	+	–

Example 2.3-1 - Calculation of the Threshold Voltage

Find the threshold voltage and body factor γ for an n-channel transistor with an n^+ silicon gate if t_{ox} = 200Å, $N_A = 3 \times 10^{16}$ cm^{-3}, gate doping, $N_D = 4 \times 10^{19}$ cm^{-3}, and if the positively-charged ions at the oxide-silicon interface per area is 10^{10} cm^{-2}.

Solution

The intrinsic concentration is 1.45x10^{10} atoms/cm^3. From above, ϕ_F(substrate) is given as

$$\phi_F(\text{substrate}) = -0.0259 \ln\left[\frac{1.45\times10^{10}}{3\times10^{16}}\right] = -0.377 \text{ V}$$

The equilibrium electrostatic potential for the n^+ polysilicon gate is found from as

$$\phi_F(\text{gate}) = 0.0259 \ln\left[\frac{4\times10^{19}}{1.45\times10^{10}}\right] = 0.563 \text{ V}$$

Therefore, the potential ϕ_{MS} is found to be

$$\phi_F(\text{substrate}) - \phi_F(\text{gate}) = -0.940 \text{ V}.$$

The oxide capacitance is given as

$$C_{ox} = \varepsilon_{ox}/t_{ox} = \frac{3.9 \times 8.854 \times 10^{-14}}{200 \times 10^{-8}} = 1.727\times10^{-7} \text{ F/cm}^2$$

The fixed charge in the depletion region, Q_{b0}, is given as

$$Q_{b0} = -[2\times1.6\times10^{-19}\times11.7\times8.854\times10^{-14}\times2\times0.377\times3\times10^{16}]^{1/2} = -8.66\times10^{-8} \text{ C/cm}^2.$$

Example 2.3-1 - Continued

Dividing Q_{b0} by C_{ox} gives -0.501 V. Finally, Q_{ss}/C_{ox} is given as

$$\frac{Qss}{C_{ox}} = \frac{10^{10}\times1.60\times10^{-19}}{1.727\times10^{-7}} = 9.3\times10^{-3} \text{ V}$$

Substituting these values for V_{T0} gives

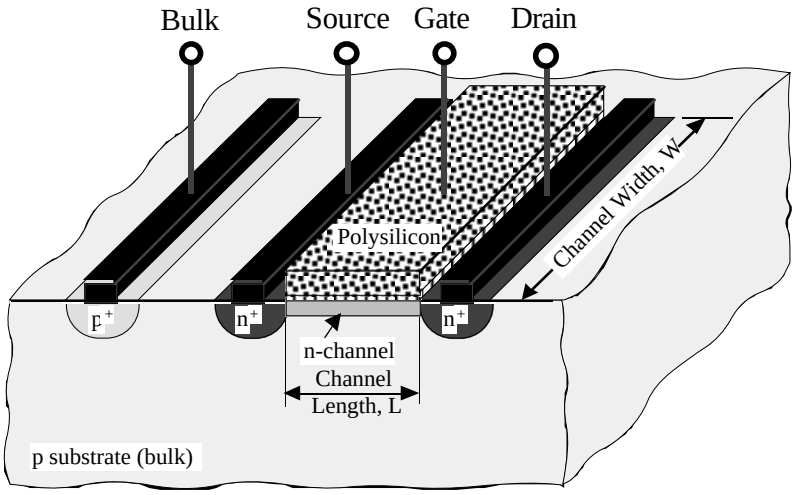
$$V_{T0} = -0.940 + 0.754 + 0.501 - 9.3 \text{ x } 10^{-3} = \underline{0.306} \text{ V}$$

The body factor is found as

$$\gamma = \frac{\left[2\times1.6\times10^{-19}\times11.7\times8.854\times10^{-14}\times3\times10^{16}\right]^{1/2}}{1.727\times10^{-7}} = \underline{0.577} \text{ V}^{1/2}$$

Depletion Mode MOSFET

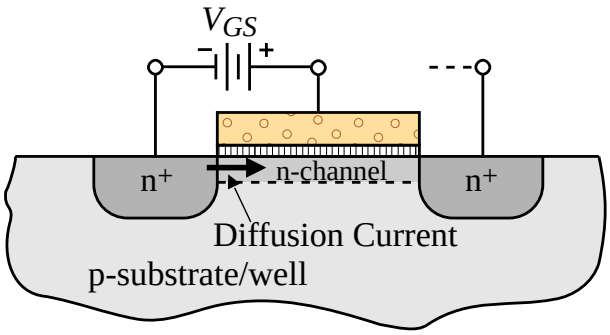
The channel is diffused into the substrate so that a channel exists between the source and drain with no external gate potential.



The threshold voltage for a depletion mode NMOS transistor will be negative (a negative gate potential is necessary to attract enough holes underneath the gate to cause this region to invert to p-type material).

Weak Inversion Operation

Weak inversion operation occurs when the applied gate voltage is below V_T and pertains to when the surface of the substrate beneath the gate is weakly inverted.



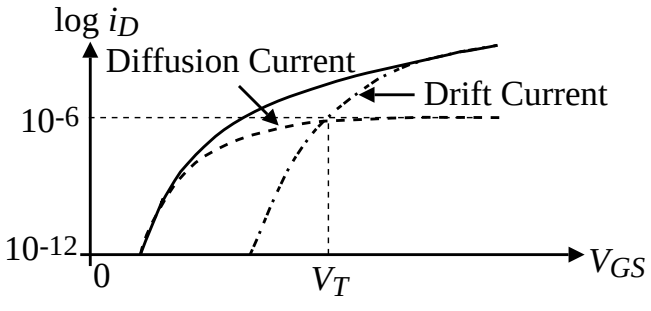
Regions of operation according to the surface potential, ϕ_S.

$\phi_S < \phi_F$: Substrate not inverted

$\phi_F < \phi_S < 2\phi_F$: Channel is weakly inverted (diffusion current)

$2\phi_F < \phi_S$: Strong inversion (drift current)

Drift current versus diffusion current in a MOSFET:



SECTION 2.4 - PASSIVE COMPONENTS

CAPACITORS

Types of Capacitors Considered

- pn junction capacitors
- Standard MOS capacitors
- Accumulation mode MOS capacitors
- Poly-poly capacitors
- Metal-metal capacitors

Characterization of Capacitors

Assume C is the desired capacitance:

1.) Dissipation (quality factor) of a capacitor is

$$Q = \omega C R_p$$

where R_p is the equivalent resistance in parallel with the capacitor, C.

2.) C_{max}/C_{min} ratio is the ratio of the largest value of capacitance to the smallest when the capacitor is used as a variable capacitor called *varactor*.

3.) Variation of capacitance with the control voltage.

4.) Parasitic capacitors from both terminal of the desired capacitor to ac ground.

Desirable Characteristics of Varactors

1.) A high quality factor

2.) A control voltage range compatible with supply voltage

3.) Good tunability over the available control voltage range

4.) Small silicon area (reduces cost)

5.) Reasonably uniform capacitance variation over the available control voltage range

6.) A high C_{max}/C_{min} ratio

Some References for Further Information

1.) P. Andreani and S. Mattisson, "On the Use of MOS Varactors in RF VCO's," *IEEE J. of Solid-State Circuits*, vol. 35, no. 6, June 2000, pp. 905-910.

2.) A-S Porret, T. Melly, C. Enz, and E. Vittoz, "Design of High-*Q* Varactors for Low-Power Wireless Applications Using a Standard CMOS Process," *IEEE J. of Solid-State Circuits*, vol. 35, no. 3, March 2000, pp. 337-345.

3.) E. Pedersen, "RF CMOS Varactors for 2GHz Applications," *Analog Integrated Circuits and Signal Processing*, vol. 26, pp. 27-36, Jan. 2001

PN Junction Capacitors

Generally made by diffusion into the well.

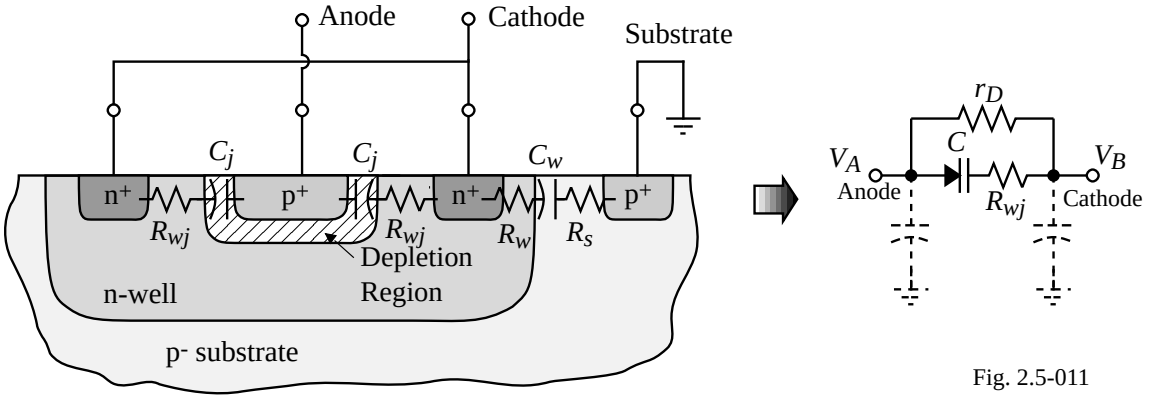


Fig. 2.5-011

Layout:

Minimize the distance between the p^+ and n^+ diffusions.

Two different versions have been tested.

1.) Large islands – 9μm on a side

2.) Small islands – 1.2μm on a side

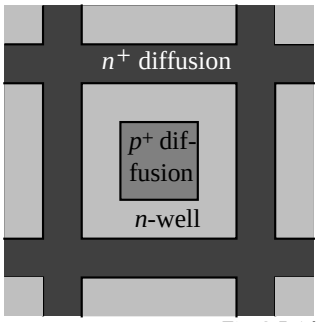


Fig. 2.5-1A

PN-Junction Capacitors – Continued

The anode should be the floating node and the cathode must be connected to ac ground.

Experimental data (Q at 2GHz, 0.5μm CMOS):

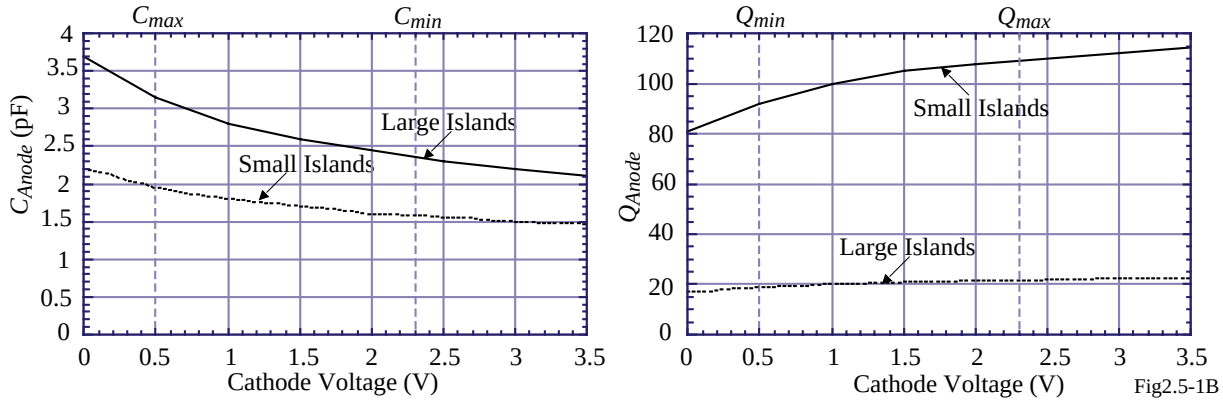


Fig2.5-1B

Summary:

Terminal Under Test	Small Islands (598 1.2μm x1.2μm)			Large Islands (42 9μm x 9μm)		
	C_{max}/C_{min}	Q_{min}	Q_{max}	C_{max}/C_{min}	Q_{min}	Q_{max}
Anode	1.23	94.5	109	1.32	19	22.6
Cathode	1.21	8.4	9.2	1.29	8.6	9.5

Electrons as majority carriers lead to higher Q because of their higher mobility.

The resistance, R_{wj}, is reduced in small islands compared with large islands ⇒ higher Q.

Single-Ended and Differential PN Junction Capacitors

Differential configurations can reduce the bulk resistances and increase the effective *Q*.

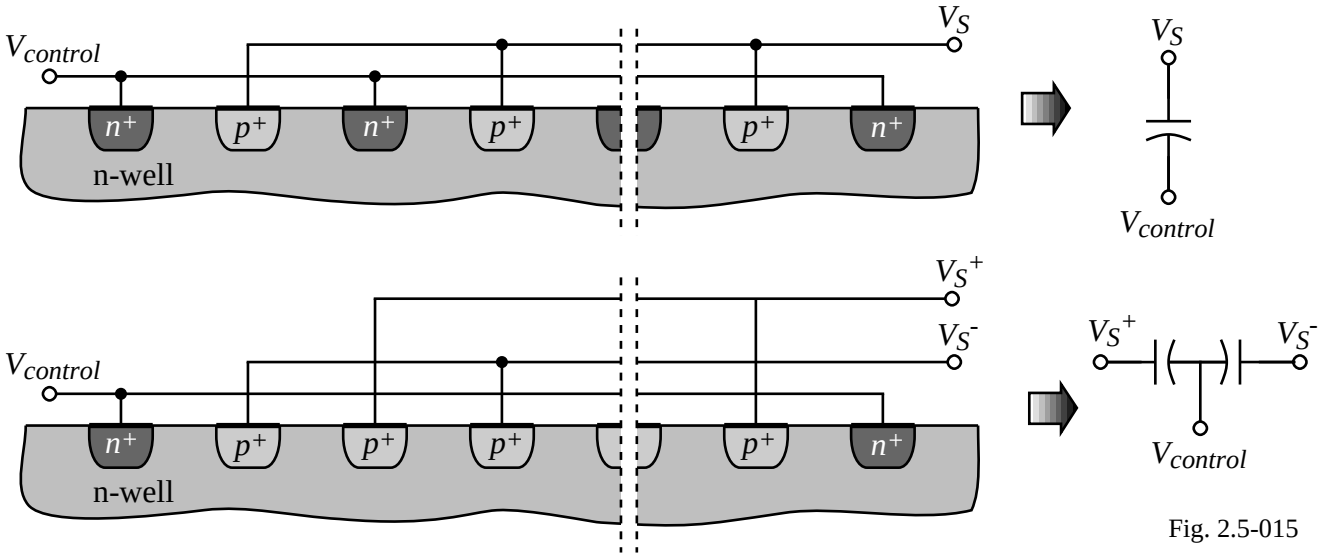


Fig. 2.5-015

An examination of the electric field lines shows that because the symmetry inherent in the differential configuration, the path to the small-signal ground can be shortened if devices with opposite polarity alternate.

Standard MOS Capacitor (D = S = B)

Conditions:

- D = S = B
- Operates from accumulation to inversion
- Nonmonotonic
- Nonlinear

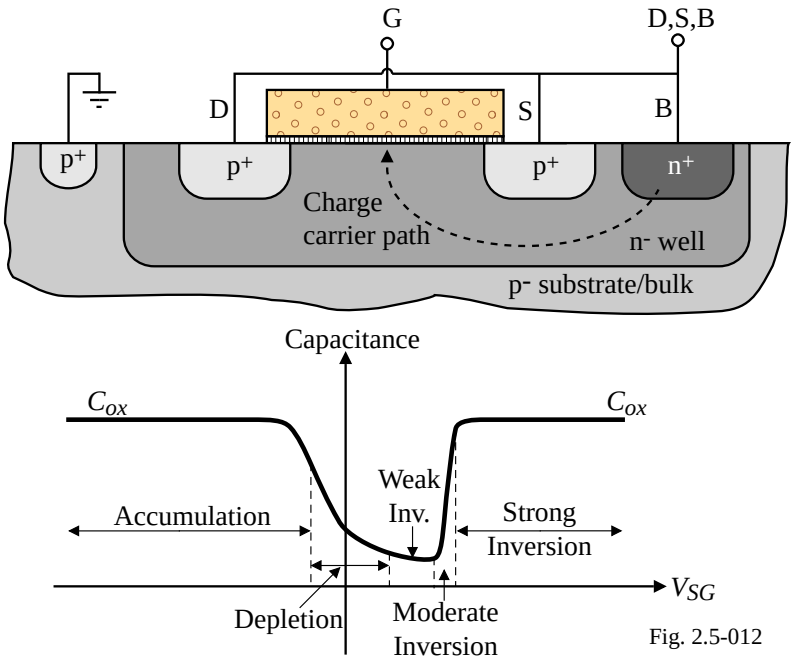


Fig. 2.5-012

Inversion Mode MOS Capacitors

Conditions:

- D = S, B = V_{DD}
- Accumulation region removed by connecting bulk to V_{DD}
- Channel resistance:

$$R_{on} = \frac{L}{12K_P'(V_{BG}-|V_T|)}$$

- LDD transistors will give lower Q because of the increased series resistance

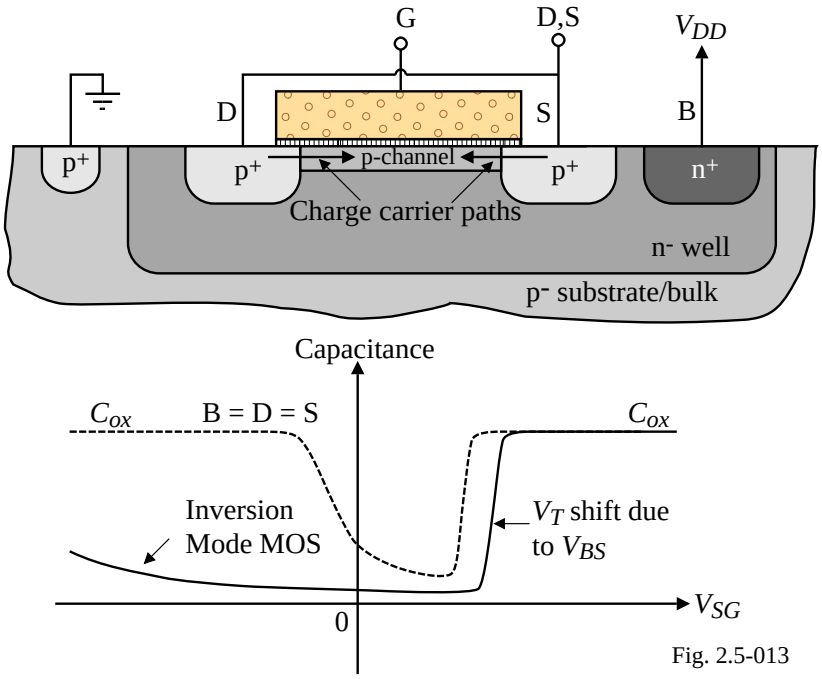
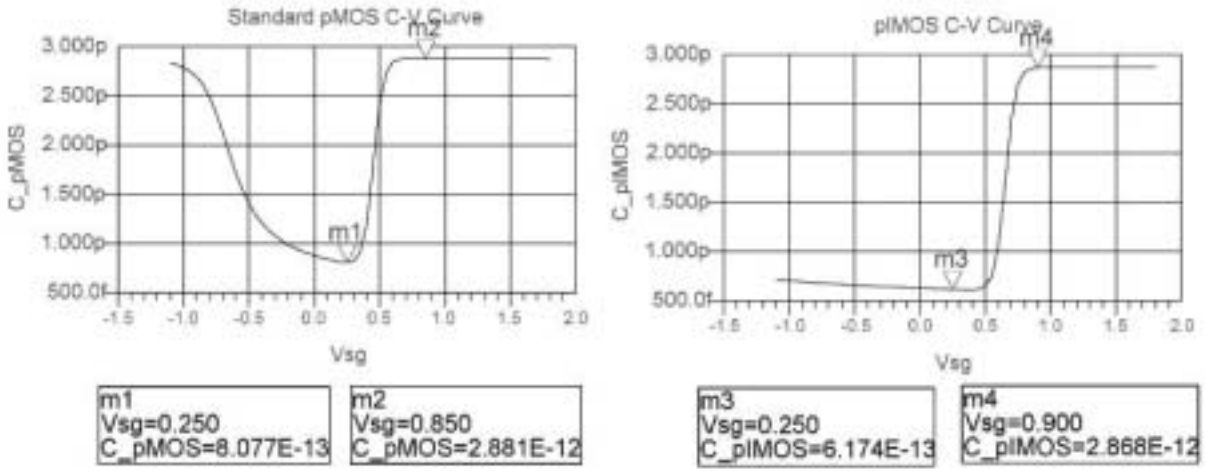


Fig. 2.5-013

Experimental Results for Standard and Inversion Mode 0.25µm CMOS Varactors

n-well:



Inversion Mode MOS Capacitors – Continued

Bulk tuning of the polysilicon-oxide-channel capacitor (0.35µm CMOS)

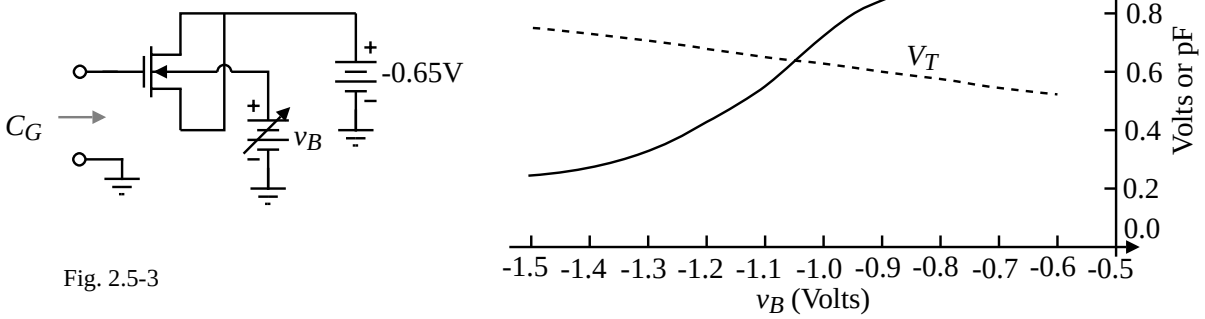


Fig. 2.5-3

$C_{max}/C_{min} \approx 4$

Inversion Mode NMOS Varactor – Continued

More Detail - Includes the LDD transistor

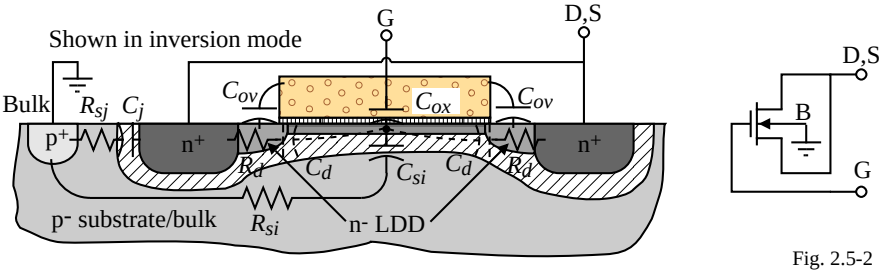


Fig. 2.5-2

Best results are obtained when the drain-source are on ac ground.

Experimental Results (Q at 2GHz, 0.5µm CMOS):

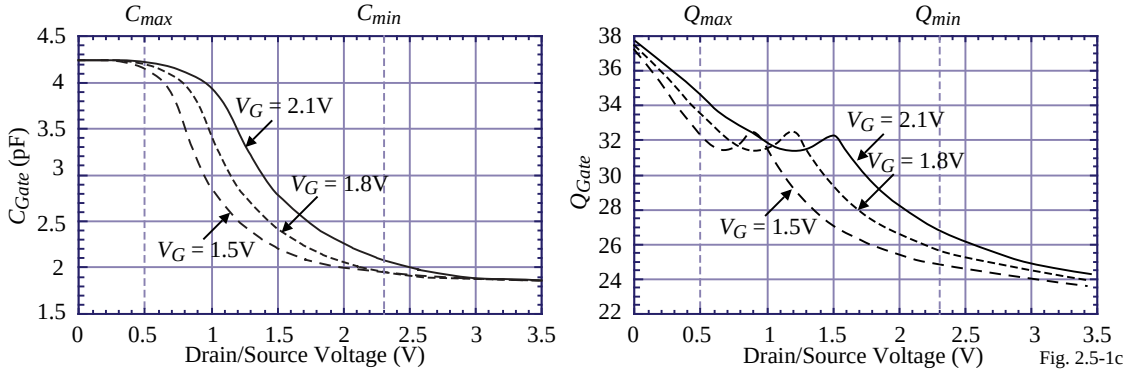


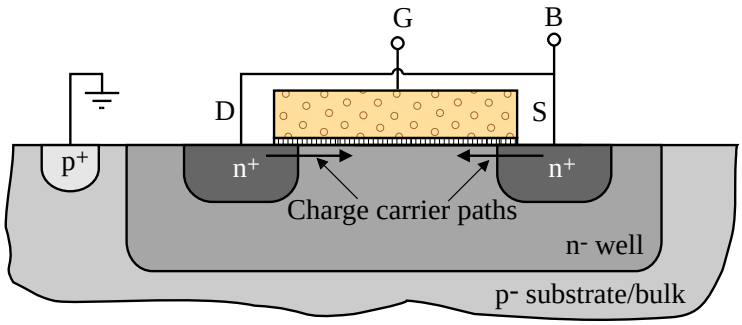
Fig. 2.5-1c

V_G =1.8V: C_{max}/C_{min} ratio = 2.15 (1.91), Q_{max} = 34.3 (5.4), and Q_{min} = 25.8(4.9)

Accumulation Mode MOS Capacitors

Conditions:

- Remove p^+ drain and source and put n^+ bulk contacts instead
- Generally not supported (yet) in most silicon foundries



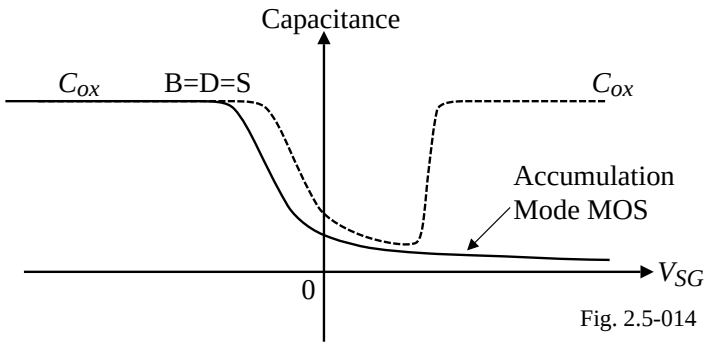
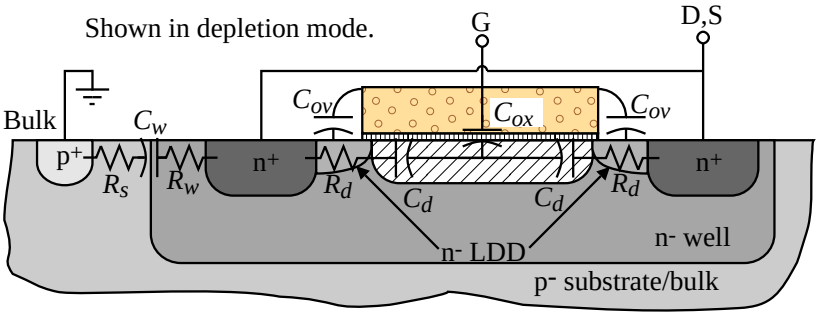


Fig. 2.5-014

Accumulation-Mode Capacitor – More Detail



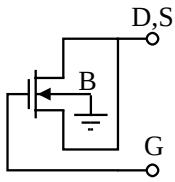


Fig. 2.5-5

Best results are obtained when the drain-source are on ac ground.

Experimental Results (Q at 2GHz, 0.5µm CMOS):

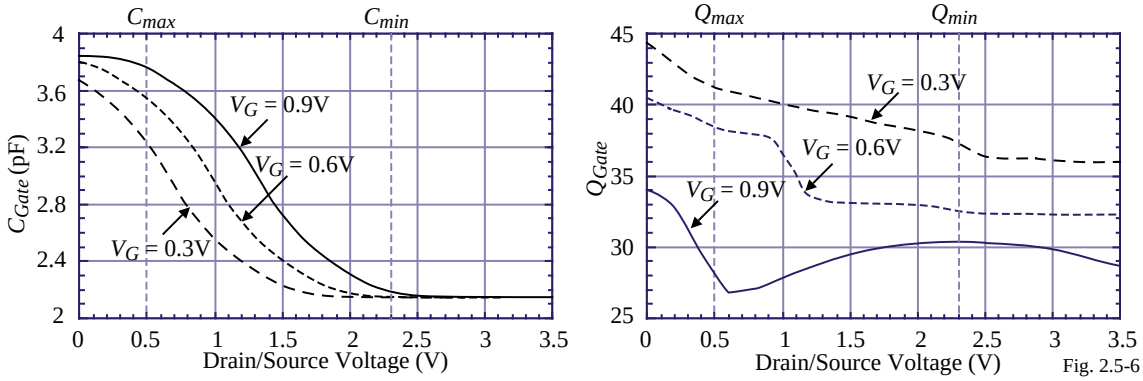
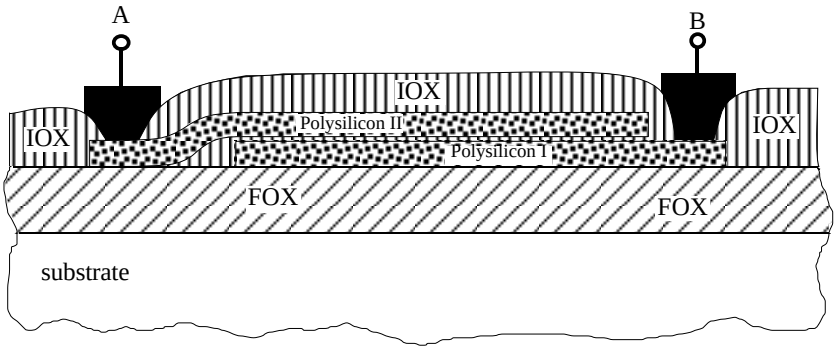


Fig. 2.5-6

V_G = 0.6V: C_{max}/C_{min} ratio = 1.69 (1.61), Q_{max} = 38.3 (15.0), and Q_{min} = 33.2(13.6)

MOS Capacitors - Continued

Polysilicon-Oxide-Polysilicon (Poly-Poly):

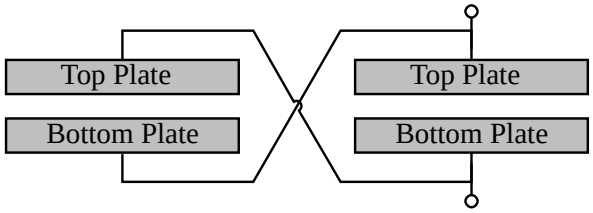


Best possible capacitor for analog circuits

Less parasitics

Voltage independent

Possible approach for increasing the voltage linearity:



Implementation of Capacitors using Available Interconnect Layers

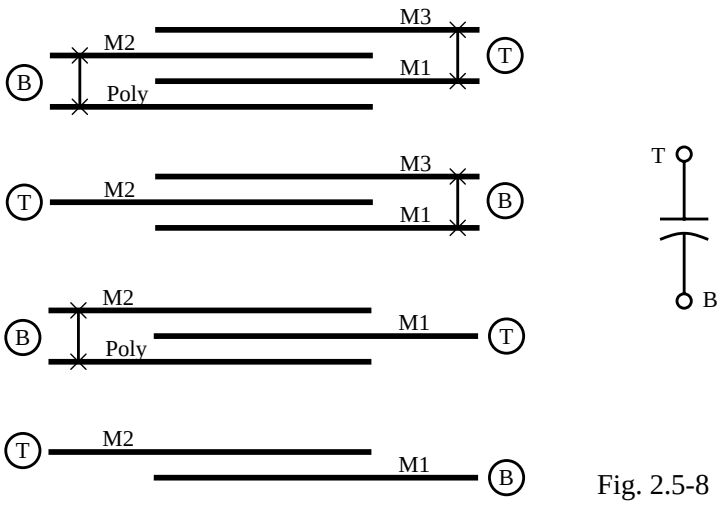
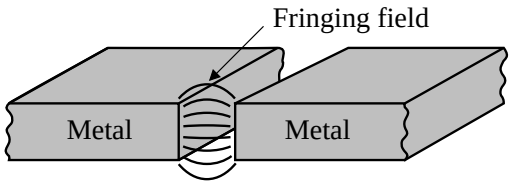


Fig. 2.5-8

Horizontal Metal Capacitors

Capacitance between conductors on the same level and use lateral flux..



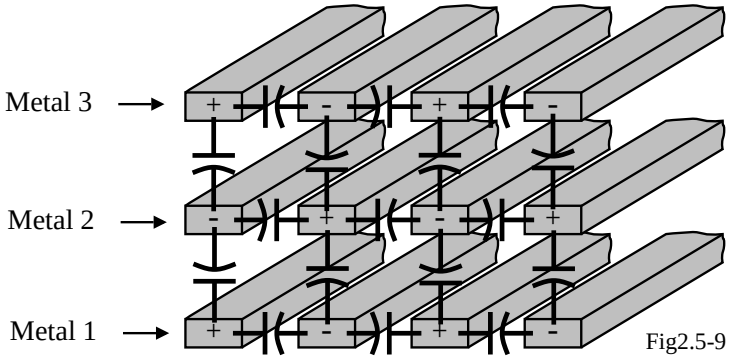


Fig2.5-9

These capacitors are sometimes called fractal capacitors because the fractal patterns are structures that enclose a finite area with an infinite perimeter.

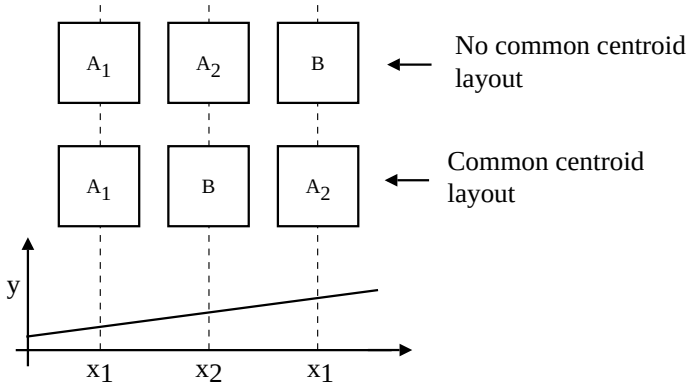
The capacitor/area can be increased by a factor of 10 over vertical flux capacitors.

Capacitor Errors

1.) Oxide gradients
2.) Edge effects
3.) Parasitics
4.) Voltage dependence
5.) Temperature dependence

Capacitor Errors - Oxide Gradients

Error due to a variation in oxide thickness across the wafer.



Only good for one-dimensional errors.

An alternate approach is to layout numerous repetitions and connect them randomly to achieve a statistical error balanced over the entire area of interest.

A	B	C	A	B	C	A	B	C
C	A	B	C	A	B	C	A	B
B	C	A	B	C	A	B	C	A

0.2% matching of poly resistors was achieved using an array of 50 unit resistors.

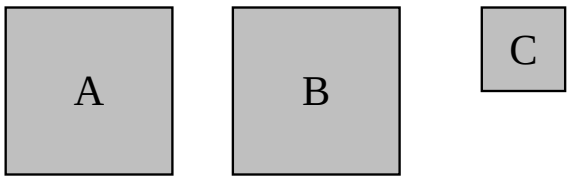
Capacitor Errors - Edge Effects

There will always be a randomness on the definition of the edge.

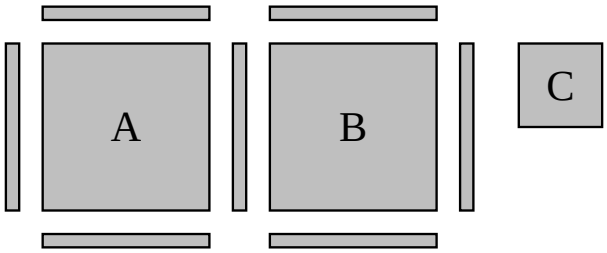
However, etching can be influenced by the presence of adjacent structures.

For example,

Matching of A and B are disturbed by the presence of C.



Improved matching achieve by matching the surroundings of A and B.



Capacitor Errors - Area/Periphery Ratio

The best match between two structures occurs when their area-to-periphery ratios are identical.

Let $C'_1 = C_1 \pm \Delta C_1$ and $C'_2 = C_2 \pm \Delta C_2$

where

C' = the actual capacitance

C = the desired capacitance (which is proportional to *area*)

ΔC = edge uncertainty (which is proportional to the *periphery*)

Solve for the ratio of C'_2/C'_1,

$$\frac{C'_2}{C'_1} = \frac{C_2 \pm \Delta C_2}{C_1 \pm \Delta C_1} = \frac{C_2}{C_1}\left(\frac{1 \pm \frac{\Delta C_2}{C_2}}{1 \pm \frac{\Delta C_1}{C_1}}\right) \approx \frac{C_2}{C_1}\left(1 \pm \frac{\Delta C_2}{C_2}\right)\left(1 \mp \frac{\Delta C_1}{C_1}\right) \approx \frac{C_2}{C_1}\left(1 \pm \frac{\Delta C_2}{C_2} \mp \frac{\Delta C_1}{C_1}\right)$$

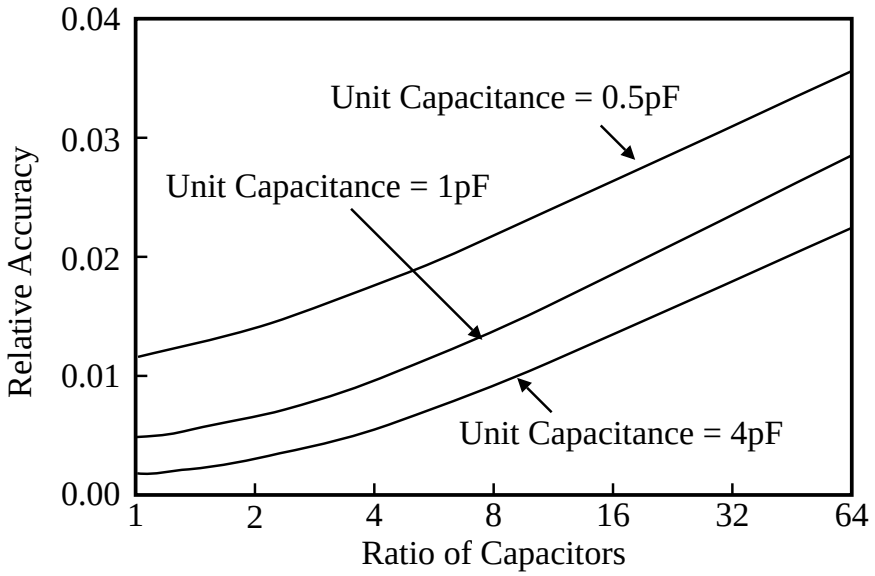
If $\frac{\Delta C_2}{C_2} = \frac{\Delta C_1}{C_1}$, then $\boxed{\frac{C'_2}{C'_1} = \frac{C_2}{C_1}}$

Therefore, the best matching results are obtained when the area/periphery ratio of C_2 is equal to the area/periphery ratio of C_1.

Capacitor Errors - Relative Accuracy

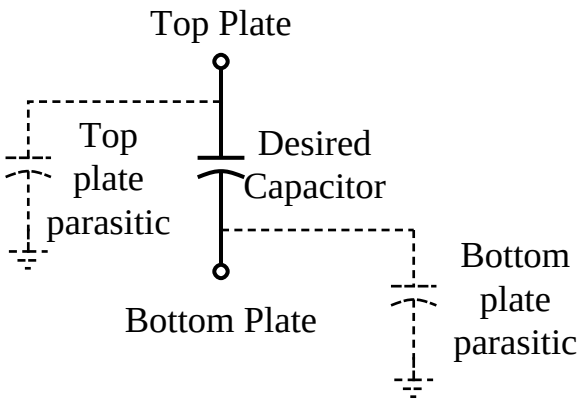
Capacitor relative accuracy is proportional to the area of the capacitors and inversely proportional to the difference in values between the two capacitors.

For example,



Capacitor Errors - Parasitics

Parasitics are normally from the top and bottom plate to ac ground which is typically the substrate.

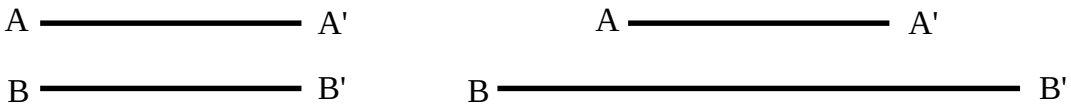


Top plate parasitic is 0.01 to 0.001 of $C_{desired}$

Bottom plate parasitic is 0.05 to 0.2 $C_{desired}$

Other Considerations on Capacitor Accuracy

Decreasing Sensitivity to Edge Variation:



Sensitive to edge variation in both upper andlower plates

Sensitive to edge varation in upper plate only.

Fig. 2.6-13

A structure that minimizes the ratio of perimeter to area (circle is best).

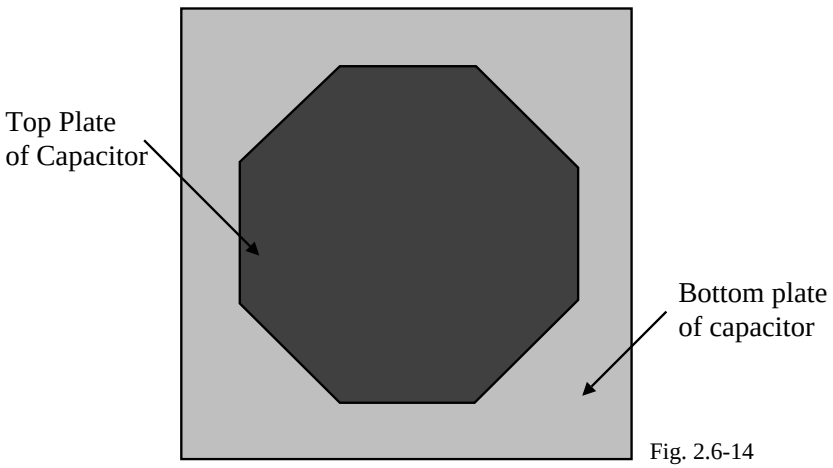


Fig. 2.6-14

Definition of Temperature and Voltage Coefficients

In general a variable y which is a function of x, $y = f(x)$, can be expressed as a Taylor series,

$$y(x = x_0) \approx y(x_0) + a_1(x - x_0) + a_2(x - x_0)^2 + a_1(x - x_0)^3 + \cdots$$

where the coefficients, a_i, are defined as,

$$a_1 = \frac{df(x)}{dx}\Big|_{x=x_0}, \; a_2 = \frac{1}{2}\frac{d^2f(x)}{dx^2}\Big|_{x=x_0}, \ldots.$$

The coefficients, a_i, are called the first-order, second-order, …. temperature or voltage coefficients depending on whether x is temperature or voltage.

Generally, only the first-order coefficients are of interest.

In the characterization of temperature dependence, it is common practice to use a term called *fractional temperature coefficient*, TC_F, which is defined as,

$$TC_F(T=T_0) = \frac{1}{f(T=T_0)}\frac{df(T)}{dT}\Big|_{T=T_0} \text{ parts per million/°C (ppm/°C)}$$

or more simply,

$$TC_F = \frac{1}{f(T)}\frac{df(T)}{dT} \text{ parts per million/°C (ppm/°C)}$$

A similar definition holds for fractional voltage coefficient.

Capacitor Errors - Temperature and Voltage Dependence

Polysilicon-Oxide-Semiconductor Capacitors

- Absolute accuracy ≈ ±10%
- Relative accuracy ≈ ±0.2%
- Temperature coefficient ≈ +25 ppm/C°
- Voltage coefficient ≈ -50ppm/V

Polysilicon-Oxide-Polysilicon Capacitors

- Absolute accuracy ≈ ±10%
- Relative accuracy ≈ ±0.2%
- Temperature coefficient ≈ +25 ppm/C°
- Voltage coefficient ≈ -20ppm/V

Accuracies depend upon the size of the capacitors.

RESISTORS

MOS Resistors - Source/Drain Resistor

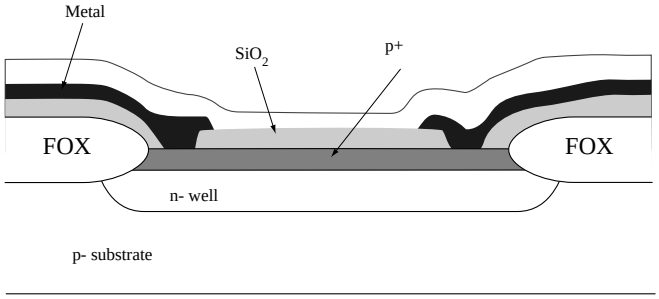


Fig. 2.5-16

Diffusion:

10-100 ohms/square
Absolute accuracy = ±35%
Relative accuracy=2% (5µm), 0.2% (50µm)
Temperature coefficient = +1500 ppm/°C
Voltage coefficient ≈ 200 ppm/V

Ion Implanted:

500-2000 ohms/square
Absolute accuracy = ±15%
Relative accuracy=2% (5µm), 0.15% (50µm
Temperature coefficient = +400 ppm/°C
Voltage coefficient ≈ 800 ppm/V

Comments:

- Parasitic capacitance to substrate is voltage dependent.
- Piezoresistance effects occur due to chip strain from mounting.

Polysilicon Resistor

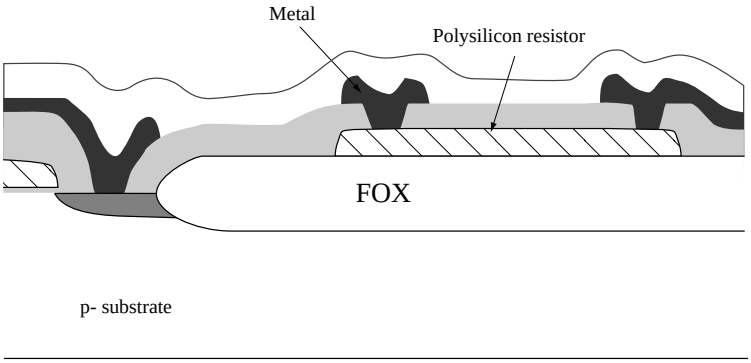


Fig. 2.5-17

30-100 ohms/square (unshielded)
100-500 ohms/square (shielded)
Absolute accuracy = ±30%
Relative accuracy = 2% (5 µm)
Temperature coefficient = 500-1000 ppm/°C
Voltage coefficient ≈ 100 ppm/V
Comments:

- Used for fuzzes and laser trimming
- Good general resistor with low parasitics

N-well Resistor

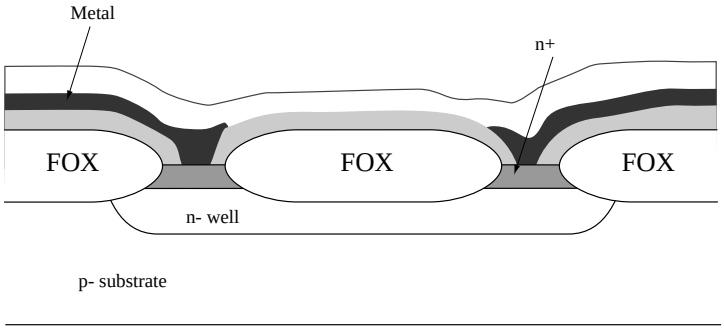


Fig. 2.5-18

1000-5000 ohms/square

Absolute accuracy = ±40%

Relative accuracy ≈ 5%

Temperature coefficient = 4000 ppm/°C

Voltage coefficient is large ≈ 8000 ppm/V

Comments:

- Good when large values of resistance are needed.
- Parasitics are large and resistance is voltage dependent

MOS Passive RC Component Performance Summary

Component Type	Range of Values	Absolute Accuracy	Relative Accuracy	Temperature Coefficient	Voltage Coefficient
Poly-oxide-semi-conductor Capacitor	0.35-0.5 fF/μm²	10%	0.1%	20ppm/°C	±20ppm/V
Poly-Poly Capacitor	0.3-0.4 fF/μm²	20%	0.1%	25ppm/°C	±50ppm/V
Diffused Resistor	10-100 Ω/sq.	35%	2%	1500ppm/°C	200ppm/V
Ion Implanted Resistor	0.5-2 kΩ/sq.	15%	2%	400ppm/°C	800ppm/V
Poly Resistor	30-200 Ω/sq.	30%	2%	1500ppm/°C	100ppm/V
n-well Resistor	1-10 kΩ/sq.	40%	5%	8000ppm/°C	10kppm/V

Future Technology Impact on Passive RC Components

What will be the impact of scaling down in CMOS technology?

- Resistors – probably little impact
- Capacitors – a different story

The capacitance can be divided into gate capacitance and overlap capacitance.

Gate capacitance varies with external voltage changes

Overlap capacitances are constant with respect to external voltage changes

$\therefore$ As the channel length decreases, the gate capacitance becomes less of the total capacitance and consequently the C_{max}/C_{min} will decrease. However, the Q of the capacitor will increase because the physical dimensions are getting smaller.

Best capacitor for future scaled CMOS?

The standard mode CMOS depeletion capacitor because C_{max}/C_{min} is larger than that for the accumulation mode and Q should be sufficient.

INDUCTORS

Inductors

What is the range of values for on-chip inductors?

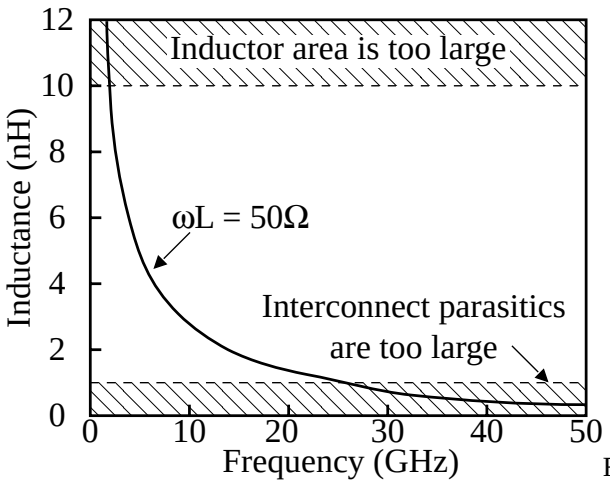


Fig. 6-5

Consider an inductor used to resonate with 5pF at 1000MHz.

$$L = \frac{1}{4\pi^2 f_o^2 C} = \frac{1}{(2\pi\cdot 10^9)^2\cdot 5\text{x}10^{-12}} = 5\text{nH}$$

Note: Off-chip connections will result in inductance as well.

Candidates for inductors in CMOS technology are:

1.) Bond wires
2.) Spiral inductors
3.) Multi-level spiral
4.) Solenoid

Bond wire Inductors:

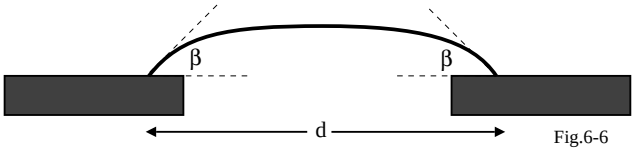


Fig.6-6

- Function of the pad distance d and the bond angle β
- Typical value is 1nH/mm which gives 2nH to 5nH in typical packages
- Series loss is 0.2 Ω/mm for 1 mil diameter aluminum wire
- $Q \approx 60$ at 2 GHz

Planar Spiral Inductors

Spiral Inductors on a Lossy Substrate:

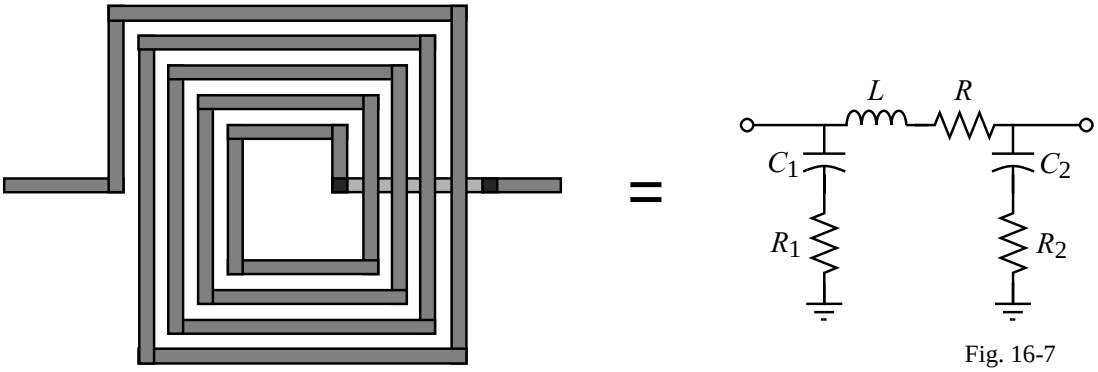


Fig. 16-7

- Design Parameters:

  Inductance, $L = \Sigma(L_{self} + L_{mutual})$

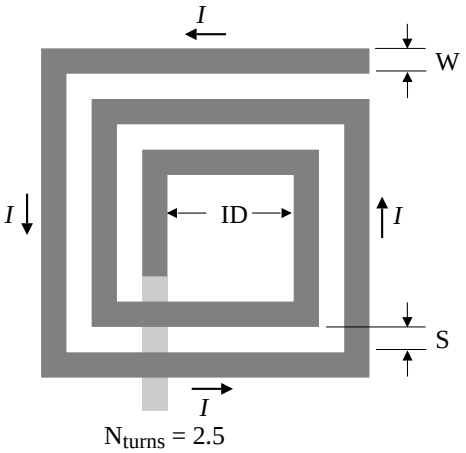
  Quality factor, $Q = \dfrac{\omega L}{R}$

  Self-resonant frequency: $f_{self} = \dfrac{1}{\sqrt{LC}}$

- Trade-off exists between the Q and self-resonant frequency
- Typical values are L = 1-8nH and Q = 3-6 at 2GHz

Planar Spiral Inductors - Continued

Inductor Design



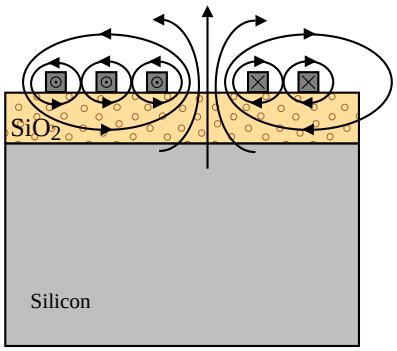


Fig. 6-9

Typically: $3 < N_{turns} < 5$ and $S = S_{min}$ for the given current

Select the OD, N_{turns}, and W so that ID allows sufficient magnetic flux to flow through the center.

Loss Mechanisms:

- Skin effect
- Capacitive substrate losses
- Eddy currents in the silicon

Planar Spiral Inductors - Continued

Influence of a Lossy Substrate

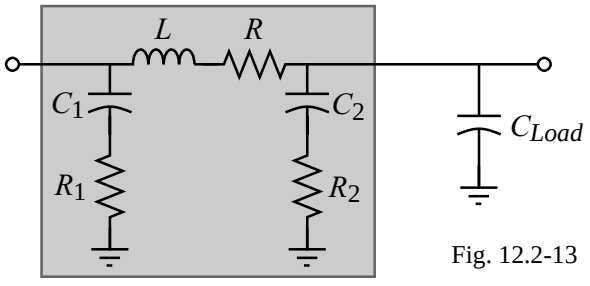


Fig. 12.2-13

where:

L is the desired inductance

R is the series resistance

C_1 and C_2 are the capacitance from the inductor to the ground plane

R_1 and R_2 are the eddy current losses in the silicon

Guidelines for using spiral inductors on chip:

- Lossy substrate degrades Q at frequencies close to f_{self}
- To achieve an inductor, one must select frequencies less than f_{self}
- The Q of the capacitors associated with the inductor should be very high

Planar Spiral Inductors - Continued

Comments concerning implementation:

1.) Put a metal ground shield between the inductor and the silicon to reduce the capacitance.

- Should be patterned so flux goes through but electric field is grounded
- Metal strips should be orthogonal to the spiral to avoid induced loop current
- The resistance of the shield should be low to terminate the electric field

2.) Avoid contact resistance wherever possible to keep the series resistance low.

3.) Use the metal with the lowest resistance and furtherest away from the substrate.

4.) Parallel metal strips if other metal levels are available to reduce the resistance.

Example:

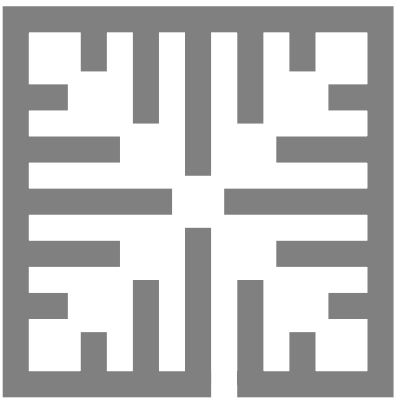


Fig. 6-10

Multi-Level Spiral Inductors

Use of more than one level of metal to make the inductor.

- Can get more inductance per area
- Can increase the interwire capacitance so the different levels are often offset to get minimum overlap.
- Multi-level spiral inductors suffer from contact resistance (must have many parallel contacts to reduce the contact resistance).
- Metal especially designed for inductors is top level approximately 4μm thick.

Solenoid Inductors

Example:

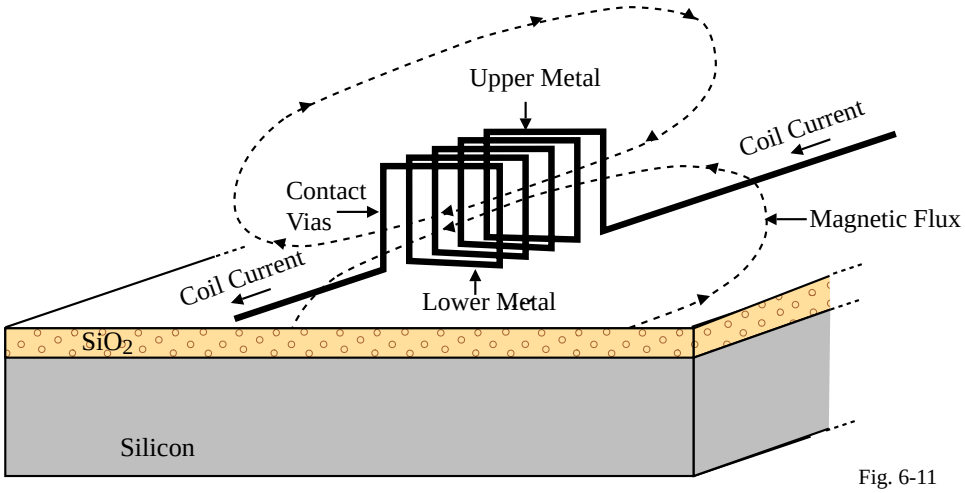


Fig. 6-11

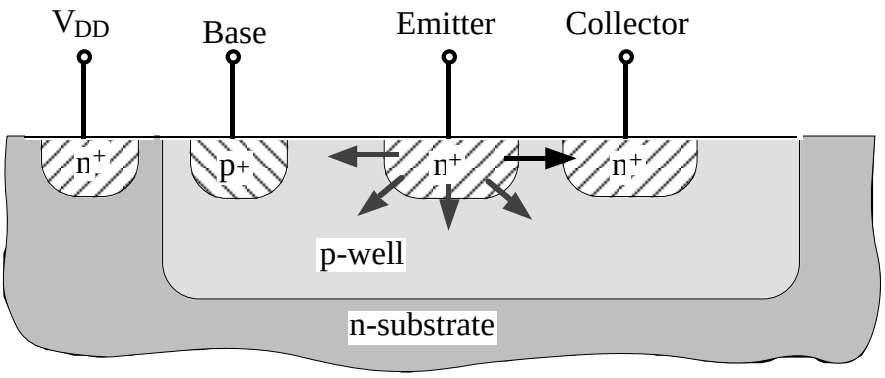
Comments:

- Magnetic flux is small due to planar structure
- Capacitive coupling to substrate is still present
- Potentially best with a ferromagnetic core

SECTION 2.5 - OTHER CONSIDERATIONS OF CMOS TECHNOLOGY

Lateral Bipolar Junction Transistor

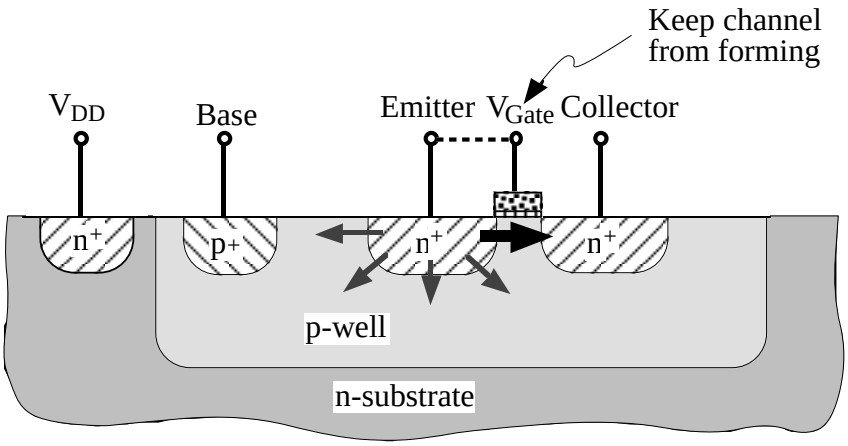
P-Well Process, NPN Lateral:



Lateral Bipolar Junction Transistor - Continued

Field-aided Lateral-

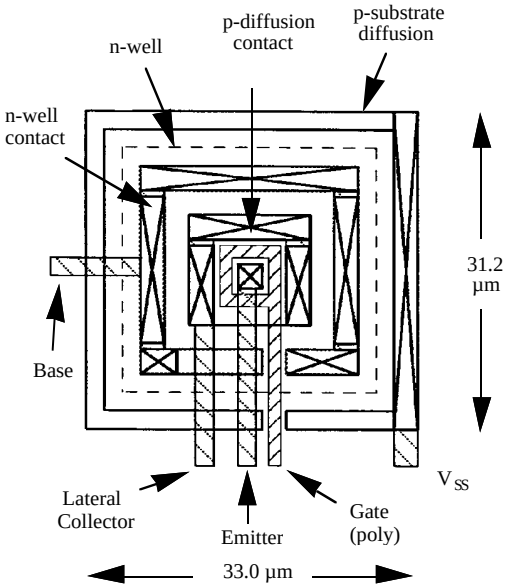
$ß_F \approx 50$ to 100 depending on the process



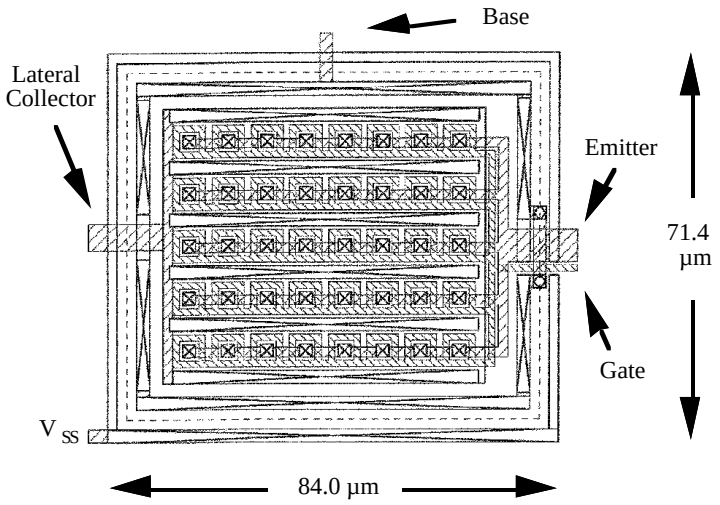
- Good geometry matching
- Low 1/f noise (if channel doesn't form)
- Acts like a photodetector with good efficiency

Geometry of the Lateral PNP BJT

Minimum Size layout of a single emitter dot lateral PNP BJT:

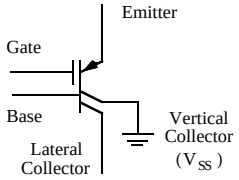


40 emitter dot LPNP transistor (total device area is 0.006mm^2 in a 1.2µm CMOS process):

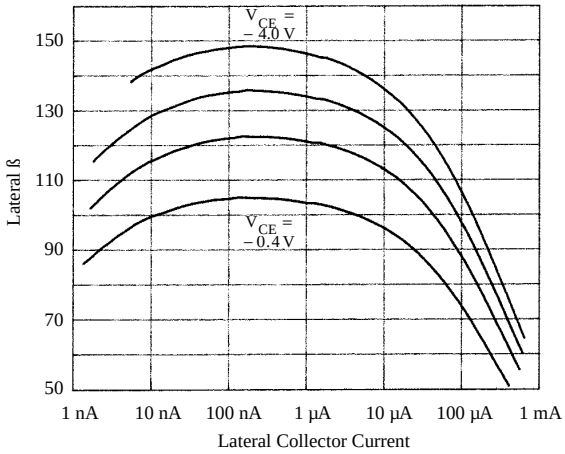


Performance of the Lateral PNP BJT

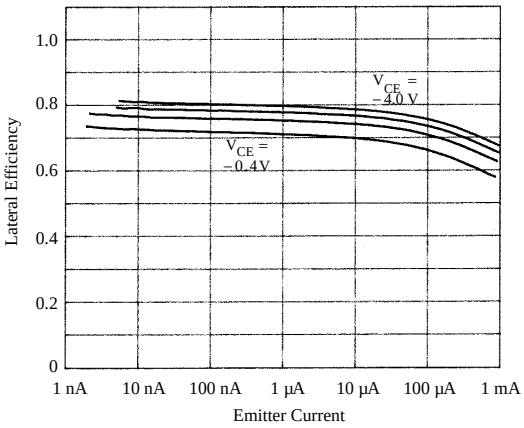
Schematic:



$ß_L$ vs I_{CL} for the 40 emitter dot LPNP BJT:



Lateral efficiency versus I_E for the 40 emitter dot LPNP BJT:



Performance of the Lateral PNP BJT - Continued

Typical Performance for the 40 emitter dot LPNP BJT:

Transistor area	0.006 mm^2
Lateral ß	90
Lateral efficiency	0.70
Base resistance	150 Ω
E_n @ 5 Hz	2.46 nV / $\sqrt{Hz}$
E_n (midband)	1.92 nV / $\sqrt{Hz}$
f_c (E_n)	3.2 Hz
I_n @ 5 Hz	3.53 pA / $\sqrt{Hz}$
I_n (midband)	0.61 pA / $\sqrt{Hz}$
f_c (In)	162 Hz
f_T	85 MHz
Early voltage	16 V

High Voltage MOS Transistor

The well can be substituted for the drain giving a lower conductivity drain and therefore higher breakdown voltage.

NMOS in n-well example:

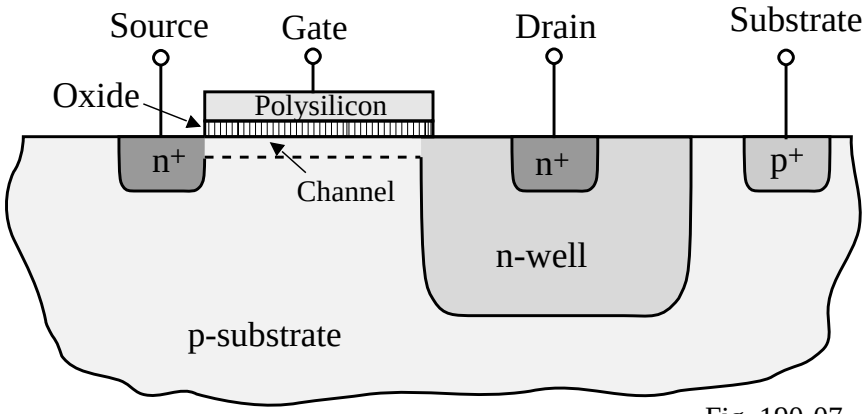


Fig. 190-07

Drain-substrate/channel can be as large as 20V or more.

Need to make the channel longer to avoid breakdowns via the channel.

Latch-up in CMOS Technology

Latch-up Mechanisms:

1. SCR regenerative switching action.
2. Secondary breakdown.
3. Sustaining voltage breakdown.

Parasitic lateral PNP and vertical NPN BJTs in a p-well CMOS technology:

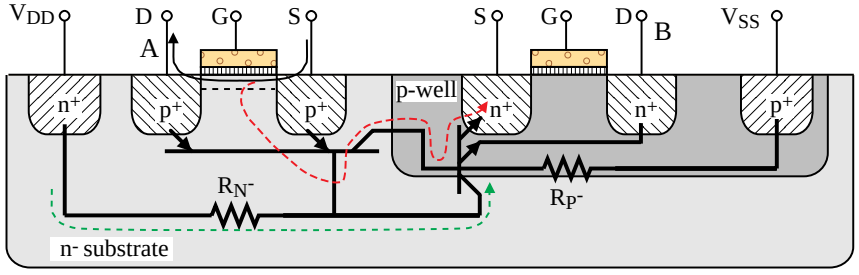


Fig. 190-08

Equivalent circuit of the SCR formed from the parasitic BJTs:

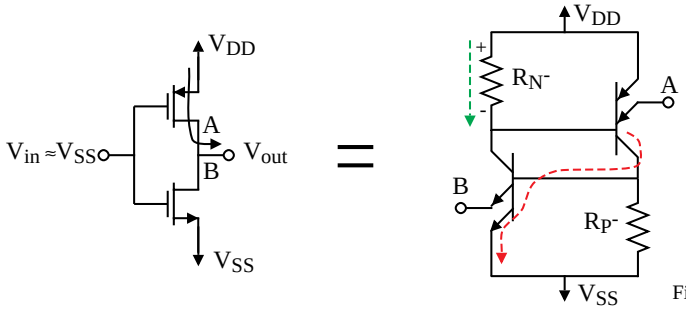


Fig. 190-09

Preventing Latch-Up in a P-Well Technology

1.) Keep the source/drain of the MOS device not in the well as far away from the well as possible. This will lower the value of the BJT betas.

2.) Reduce the values of R_{N^-} and R_{P^-}. This requires more current before latch-up can occur.

3.) Make a p^- diffusion around the p-well. This shorts the collector of Q1 to ground.

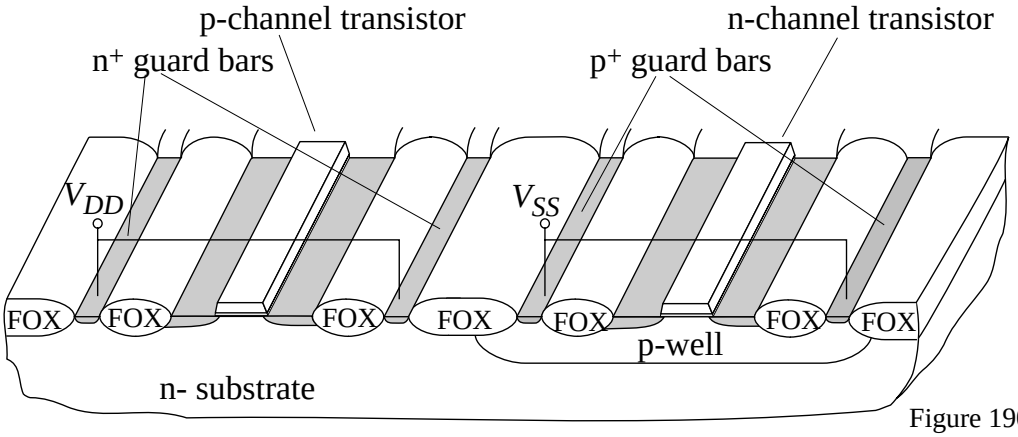


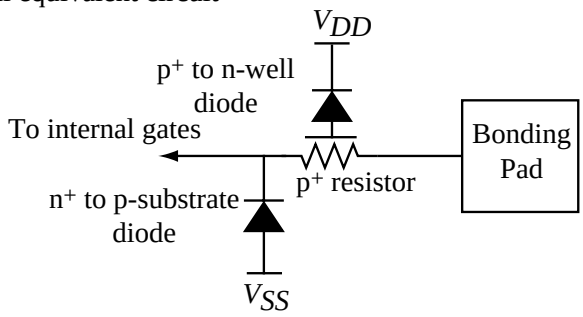
Figure 190-10

For more information see R. Troutman, "CMOS Latchup", Kluwer Academic Publishers.

Electrostatic Discharge Protection (ESD)

Objective: To prevent large external voltages from destroying the gate oxide.

Electrical equivalent circuit



Implementation in CMOS technology

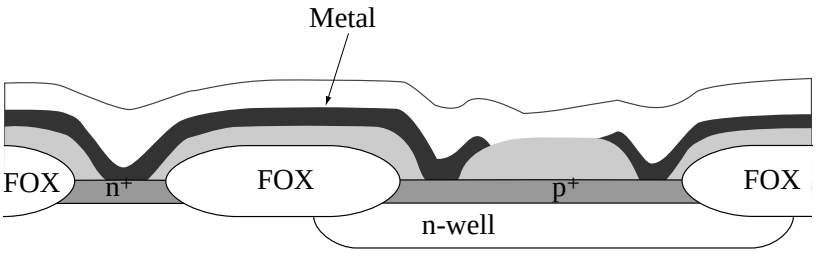


Fig. 190-11

Temperature Characteristics of Transistors

Fractional Temperature Coefficient

$$TC_F = \frac{1}{x}\cdot\frac{\partial x}{\partial T}$$ Typically in ppm/°C

MOS Transistor

$V_T = V(T_0) + \alpha(T-T_0) + \cdots,$ where $\alpha \approx -2.3\text{mV/°C}$ (200°K to 400°K)

$\mu = K_\mu T^{-1.5}$

BJT Transistor

Reverse Current, I_S:

$$\frac{1}{I_S}\cdot\frac{\partial I_S}{\partial T} = \frac{3}{T} + \frac{1}{T}\frac{V_{G0}}{kT/q}$$

Empirically, I_S doubles approximately every 5°C increase

Forward Voltage, v_D:

$$\frac{\partial v_D}{\partial T} = -\frac{V_{G0} - v_D}{T} - \frac{3kT/q}{T} \approx -2\text{mV/°C at } v_D = 0.6\text{V}$$

Noise in Transistors

Shot Noise

$$\overline{i^2} = 2qI_D\Delta f \text{ (amperes}^2\text{)}$$

where

q = charge of an electron
I_D = dc value of i_D
Δf = bandwidth in Hz

Noise current spectral density = $\frac{\overline{i^2}}{\Delta f}$ (amperes^2/Hz)

Thermal Noise

Resistor:

$$\overline{v^2} = 4kTR\Delta f \text{ (volts}^2\text{)}$$

MOSFET:

$$\overline{i_D^2} = \frac{8kTg_m\Delta f}{3}$$ (ignoring bottom gate)

where

k = Boltzmann's constant
R = resistor or equivalent resistor in which the thermal noise is occurring.
g_m = transconductance of the MOSFET

Noise in Transistors - Continued

Flicker (1/f) Noise

$$\overline{i_D^2} = K_f\left(\frac{I^a}{f^b}\right)\Delta f$$

where

K_f = constant (10^{-28} Farad·amperes)

a = constant (0.5 to 2)

b = constant (≈1)

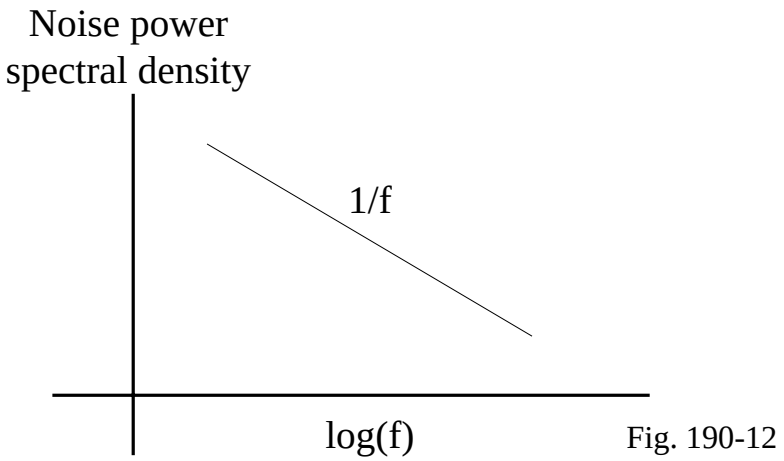


Fig. 190-12

SECTION 2.6 – INTEGRATED CIRCUIT LAYOUT

Matching Concepts

1.) Unit matching principle – Always implement two unequal components by an integer number of unit components.

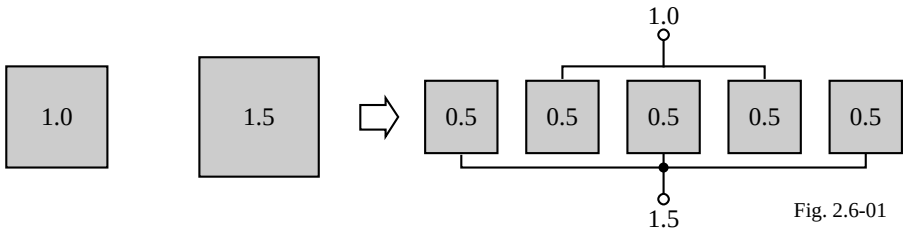


Fig. 2.6-01

2.) Common-centroid layout (illustrated above).

3.) Elimination of mismatch due to surrounding material

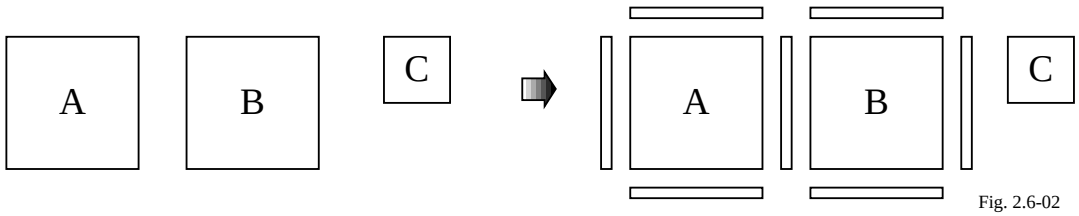


Fig. 2.6-02

4.) Minimize the ratio of the perimeter to the area (a circle is optimum).

5.) For parallel plates make one larger than the other to eliminate alignment problems.

Matching Concepts - Continued

6.) Maintain a constant area-to-perimeter ratio between matching elements.

Yiannoulos path – A serpentine structure that maintains a constant area-to-perimeter ratio and allows efficient use of area.

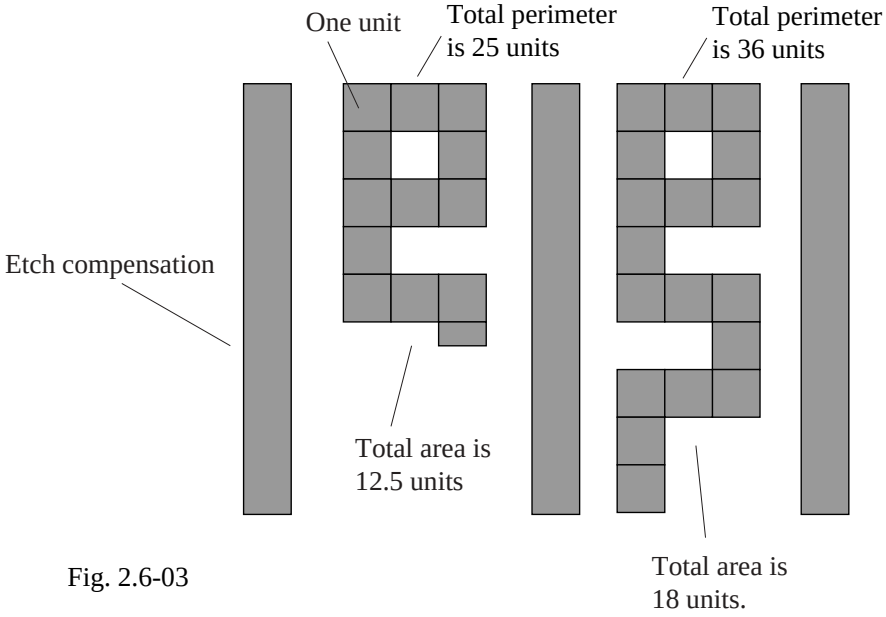


Fig. 2.6-03

Both structures have a periphery/area ratio of 2.

MOS Transistor Layout

Example of the layout of a single MOS transistor:

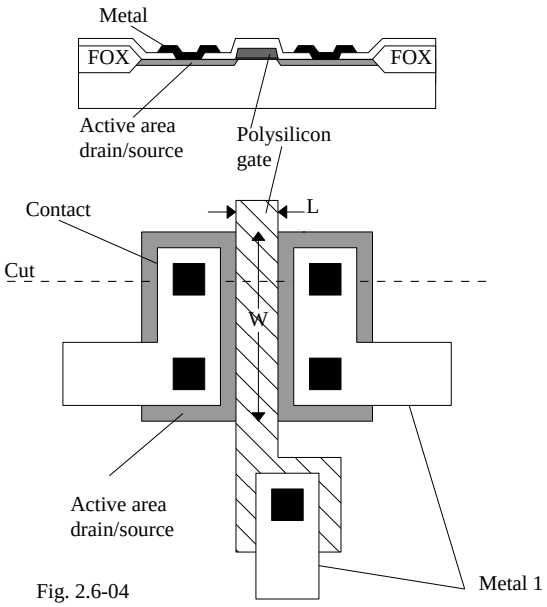


Fig. 2.6-04

Comments:

- Make sure to contact the source and drain with multiple contacts to evenly distribute the current flow under the gate.
- Minimize the area of the source and drain to reduce bulk-source/drain capacitance.

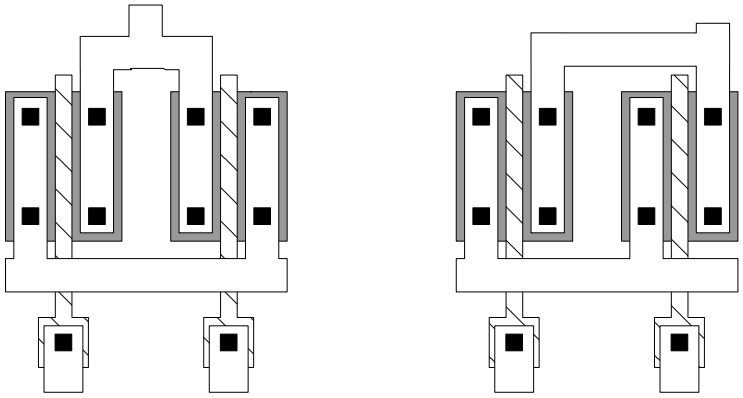
MOS Transistor Layout - Continued

For best matching, the transistor “stripes” should be oriented in the same direction (not orthogonal).

Photolithographic invariance (PLI) are transistors that exhibit identical orientation.

Examples of the layout of matched MOS transistors:

1.) Examples of mirror symmetry and photolithographic invariance.



Mirror Symmetry Photolithographic Invariance

Fig. 2.6-05

MOS Transistor Layout - Continued

2.) Two transistors sharing a common source and laid out to achieve both photolithographic invariance and common centroid.

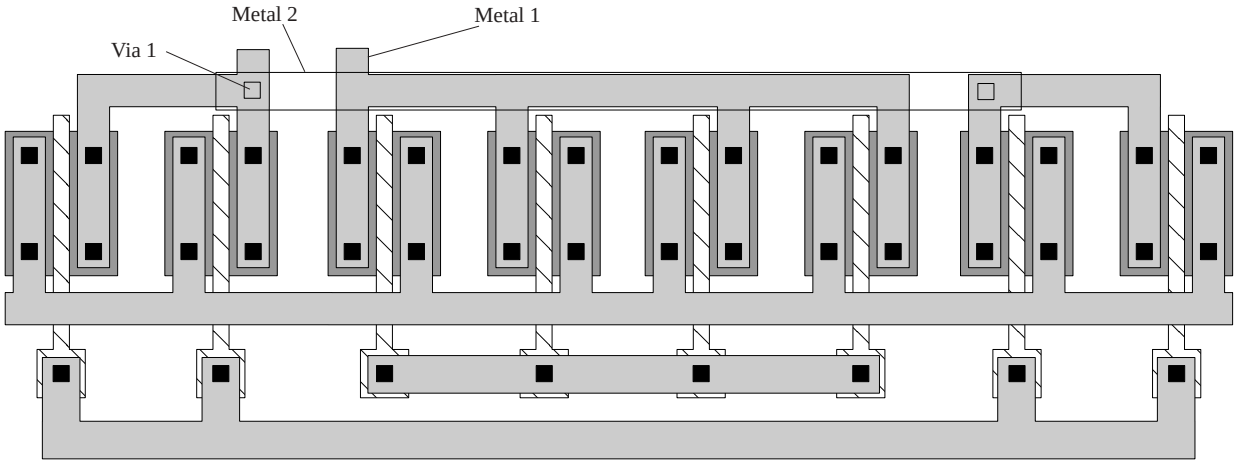


Fig. 2.6-06

MOS Transistor Layout - Continued

3.) Compact layout of the previous example.

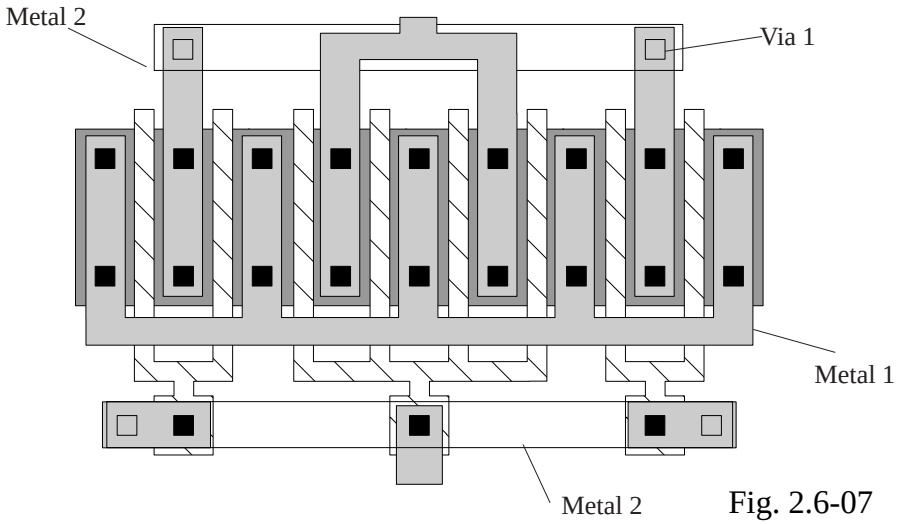


Fig. 2.6-07

Resistor Layout

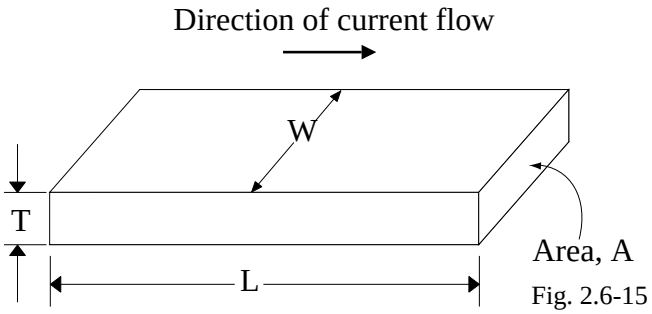


Fig. 2.6-15

Resistance of a conductive sheet is expressed in terms of

$$R = \frac{\rho L}{A} = \frac{\rho L}{WT} \quad (\Omega)$$

where

ρ = resistivity in Ω-m

Ohms/square:

$$R = \left(\frac{\rho}{T}\right)\frac{L}{W} = \rho_S \frac{L}{W} \quad (\Omega)$$

where

ρ_S is a sheet resistivity and has the units of ohms/square

Example of Resistor Layouts

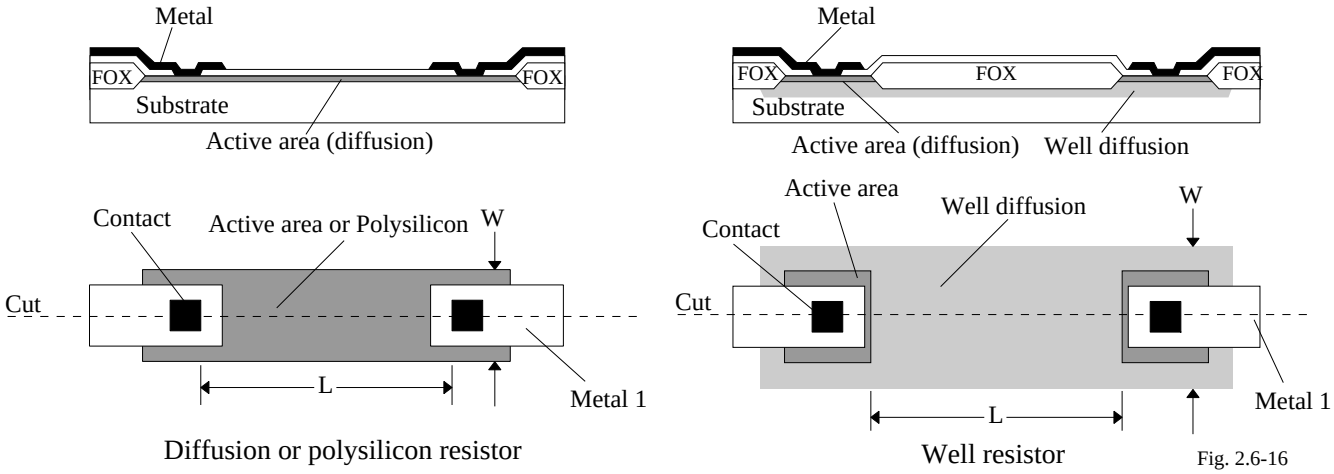


Fig. 2.6-16

Corner corrections:

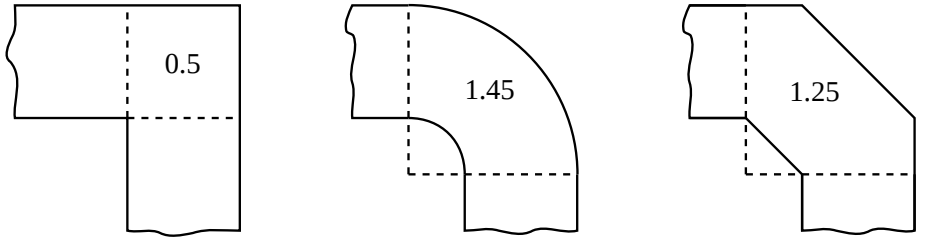


Fig. 2.6-16B

Example 2.6-1 Resistance Calculation

Given a polysilicon resistor like that drawn above with W=0.8μm and L=20μm, calculate ρ_S (in Ω/❑), the number of squares of resistance, and the resistance value. Assume that ρ for polysilicon is 9×10^{-4} Ω-cm and polysilicon is 3000 Å thick. Ignore any contact resistance.

Solution

First calculate ρ_S.

$$\rho_S = \frac{\rho}{T} = \frac{9 \times 10\text{-}4\ \Omega\text{-cm}}{3000 \times 10\text{-}8\ \text{cm}} = 30\ \Omega/❑$$

The number of squares of resistance, N, is

$$N = \frac{L}{W} = \frac{20\mu\text{m}}{0.8\mu\text{m}} = 25$$

giving the total resistance as

$$R = \rho_S \times N = 30 \times 25 = 750\ \Omega$$

Capacitor Layout

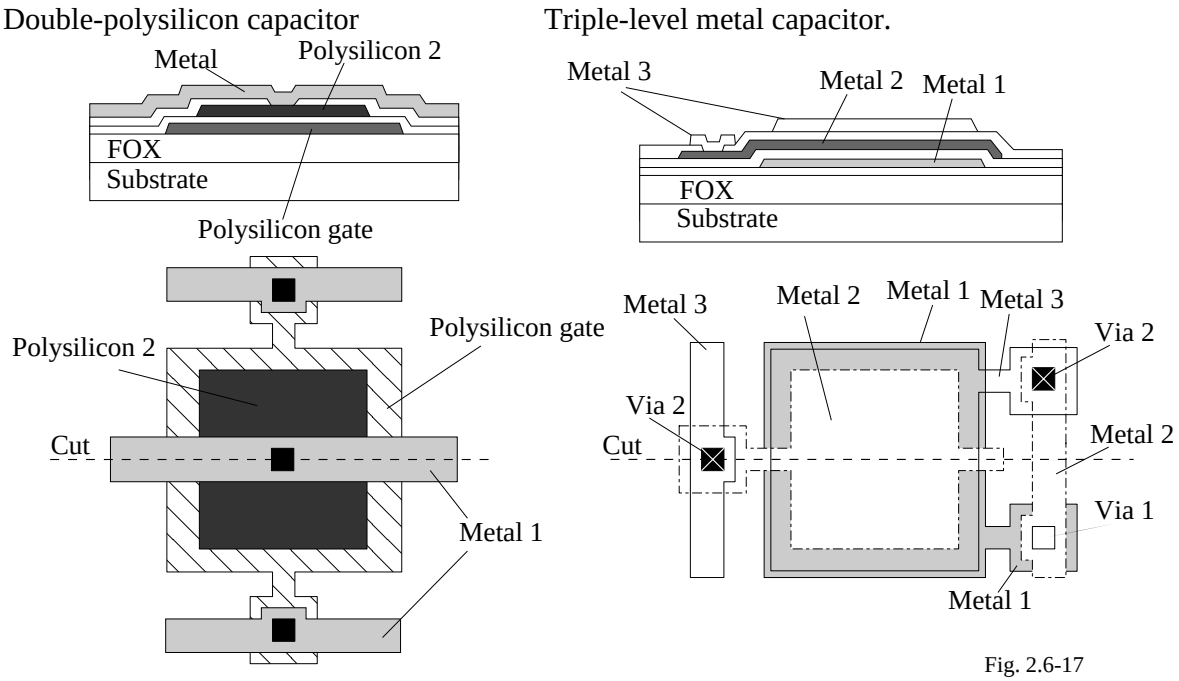


Fig. 2.6-17

Design Rules

Design rules are geometrical constraints which guarantee the proper operation of a circuit implemented by a given CMOS process.

These rules are necessary to avoid problems such as device misalignment, metal fracturing, lack of continuity, etc.

Design rules are expressed in terms of minimum dimensions such as minimum values of:

- Widths
- Separations
- Extensions
- Overlaps

• Design rules typically use a minimum feature dimension called “lambda”. Lambda is usually equal to the minimum channel length.

• Minimum resolution of the design rules is typically half lambda.

• In most processes, lambda can be scaled or reduced as the process matures.

SECTION 2.7 - BIPOLAR TRANSISTOR (OPTIONAL)

Major Processing Steps for a Junction Isolated BJT Technology

Start with a *p* substrate.

1. Implantation of the buried n^+ layer
2. Growth of the epitaxial layer
3. p^+ isolation diffusion
4. Base *p*-type diffusion
5. Emitter n^+ diffusion
6. p^+ ohmic contact
7. Contact etching
8. Metal deposition and etching
9. Passivation and bond pad opening

Implantation of the Buried Layer (Mask Step 1)

Objective of the buried layer is to reduce the collector resistance.

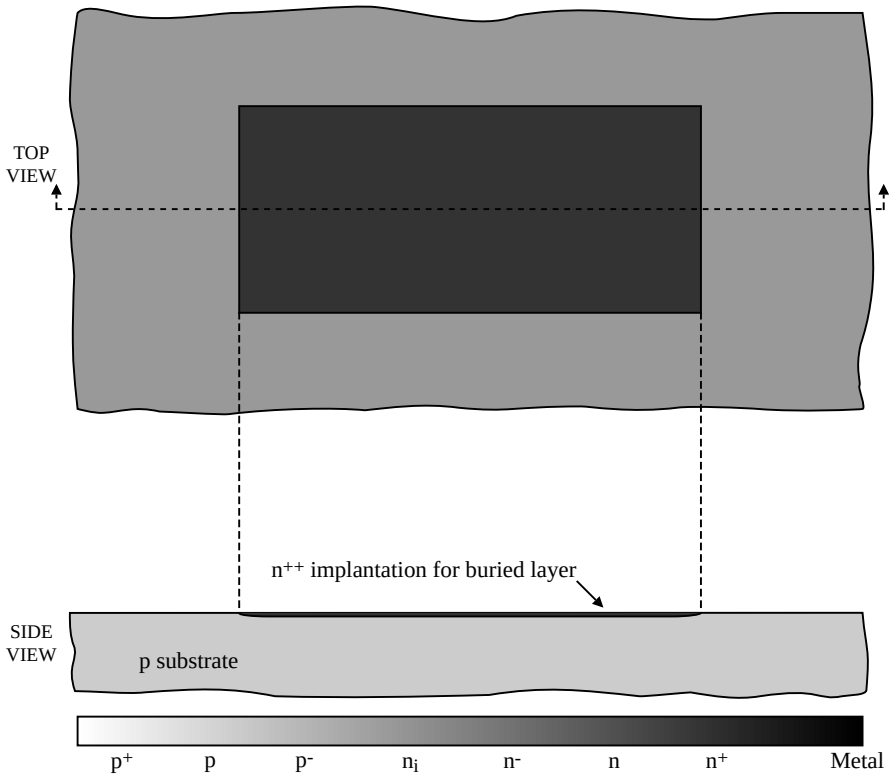


Fig.2.7-1

Epitaxial Layer (No Mask Required)

The objective is to provide the proper *n*-type doping in which to build the *npn* BJT.

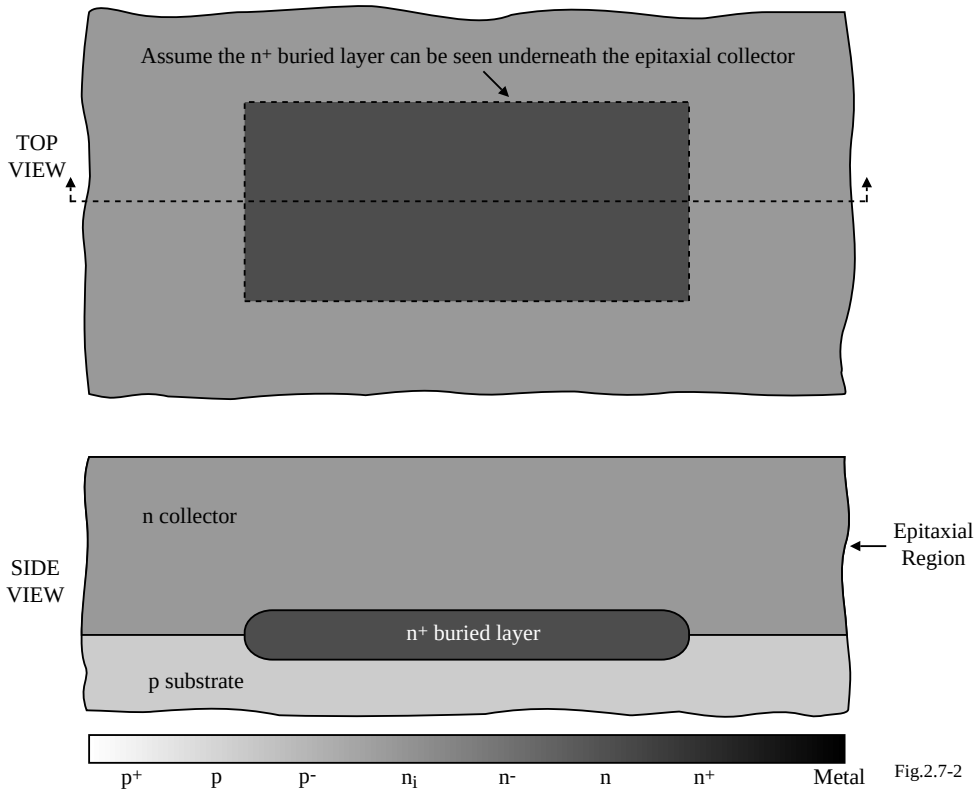


Fig.2.7-2

p^+ isolation diffusion (Mask Step 2)

The objective of this step is to surround (isolate) the *npn* BJT by a p^+ diffusion. These regions also permit contact to the substrate from the surface.

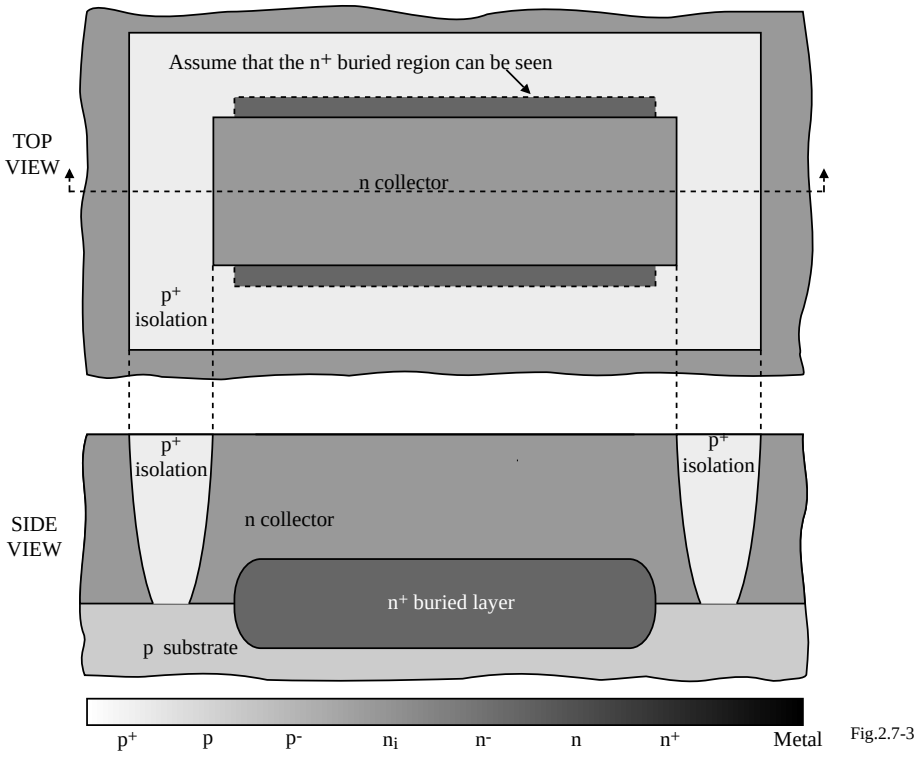


Fig.2.7-3

Base *p*-type diffusion (Mask Step 3)

The step provides the *p*-type base for the *npn* BJT.

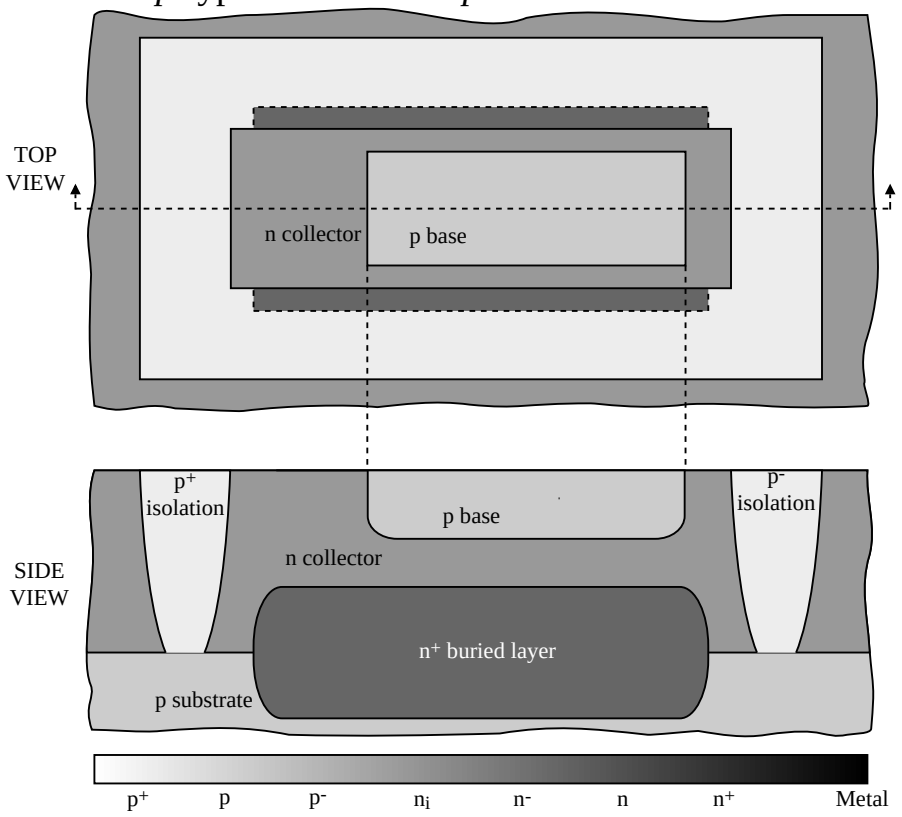


Fig.2.7-4

Emitter n^+ diffusion (Mask Step 4)

This step implements the n^+ emitter of the *npn* BJT and the collector ohmic contact.

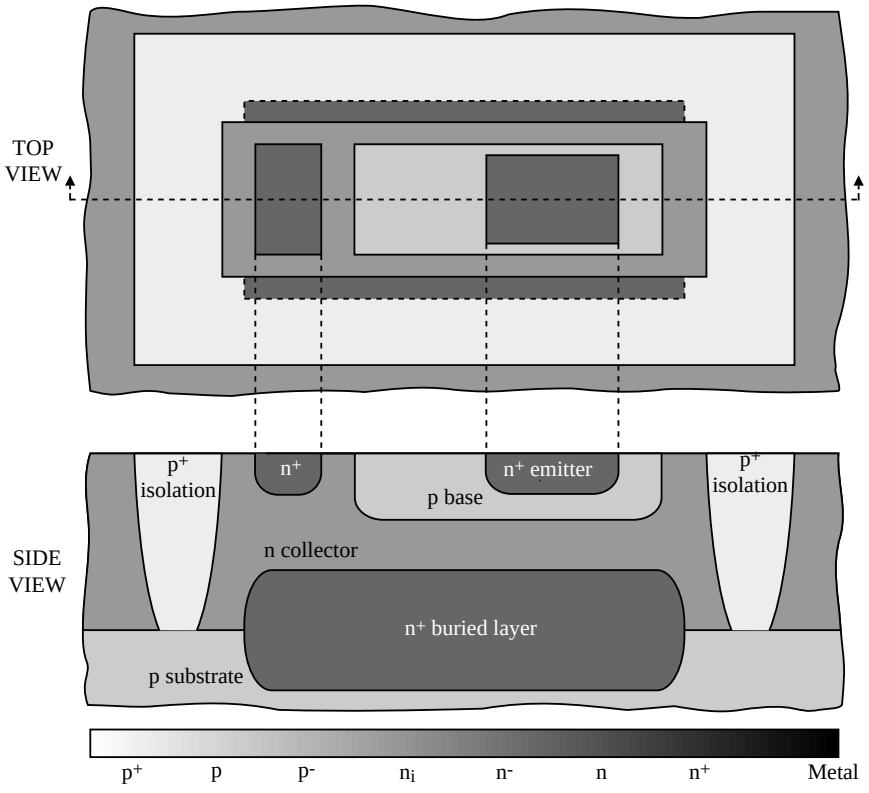


Fig.2.7-5

p^+ ohmic contact (Mask Step 5)

This step permits ohmic contact to the base region if it is not doped sufficiently high.

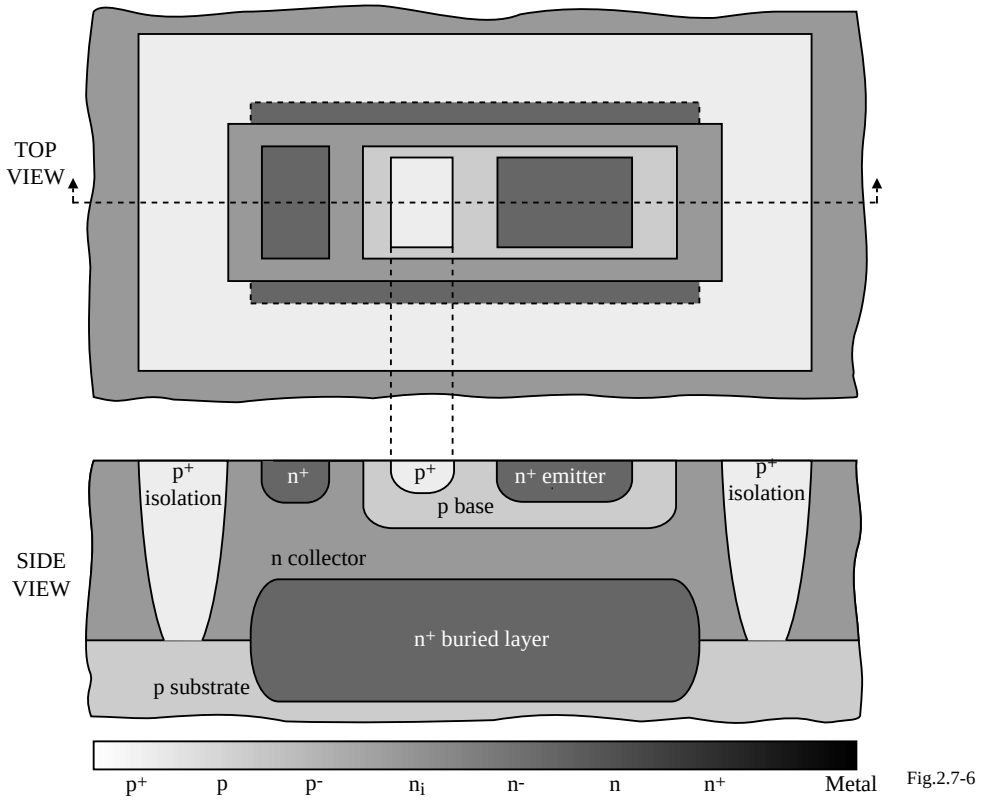


Fig.2.7-6

Contact etching (Mask Step 6)

This step opens up the areas in the dielectric area which metal will contact.

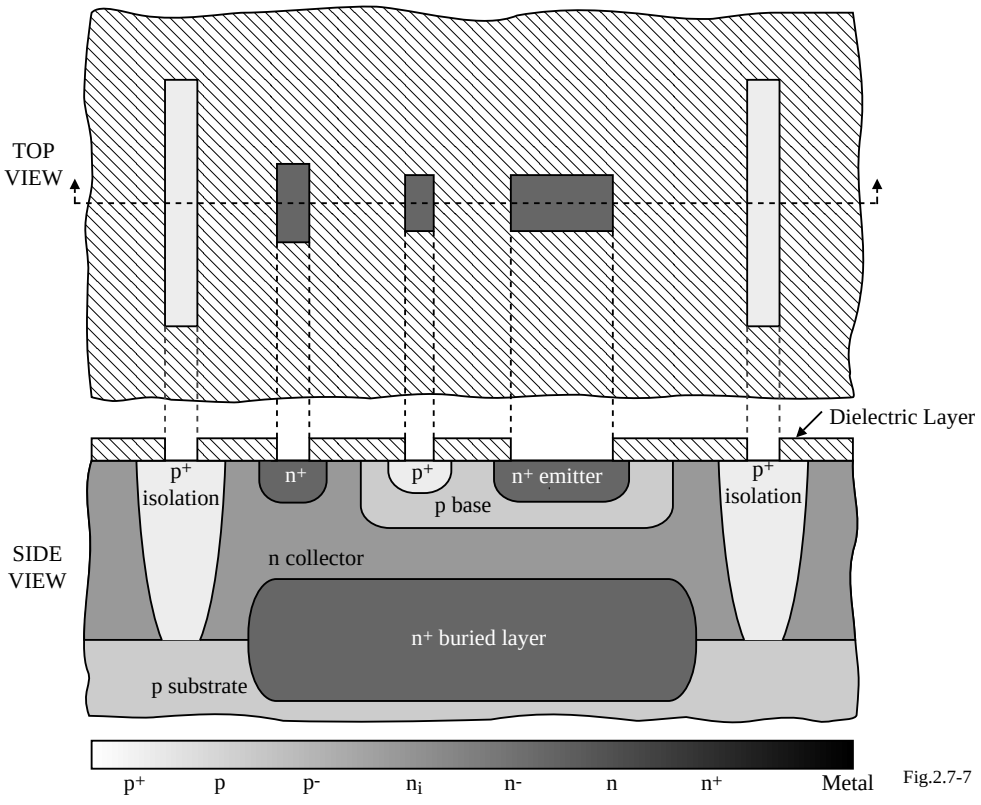


Fig.2.7-7

Metal deposition and etching (Mask Step 7)

In this step, metal is deposited over the entire wafer and removed where it is not wanted.

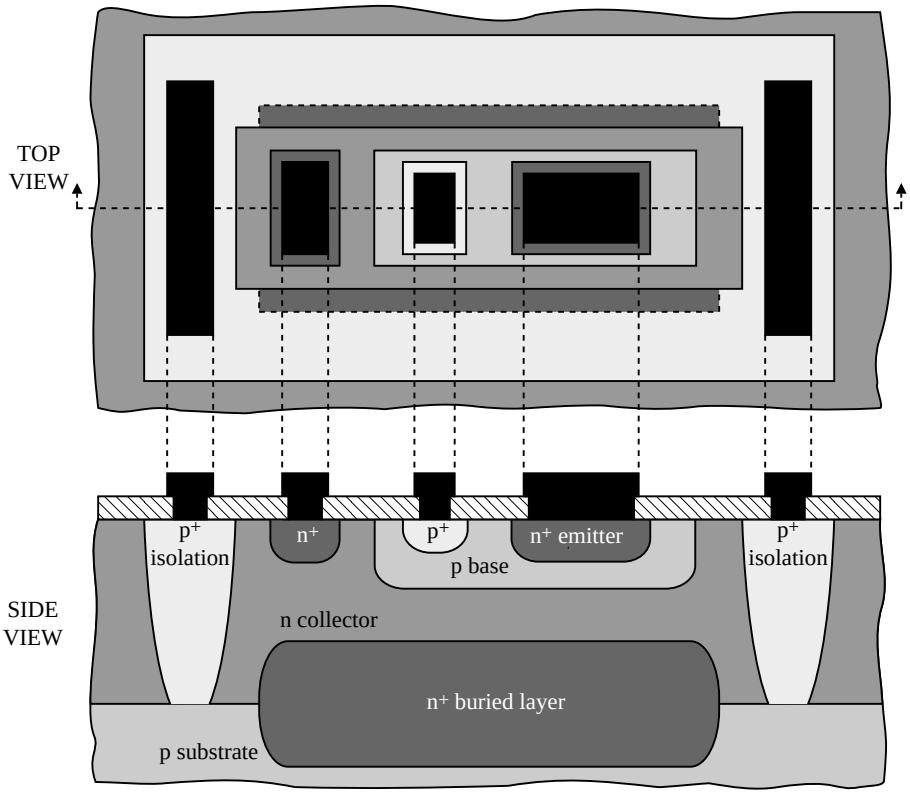


Fig.2.7-8

Passivation (Mask Step 8)

Cover the entire wafer with glass and open the area over bond pads (requires another mask).

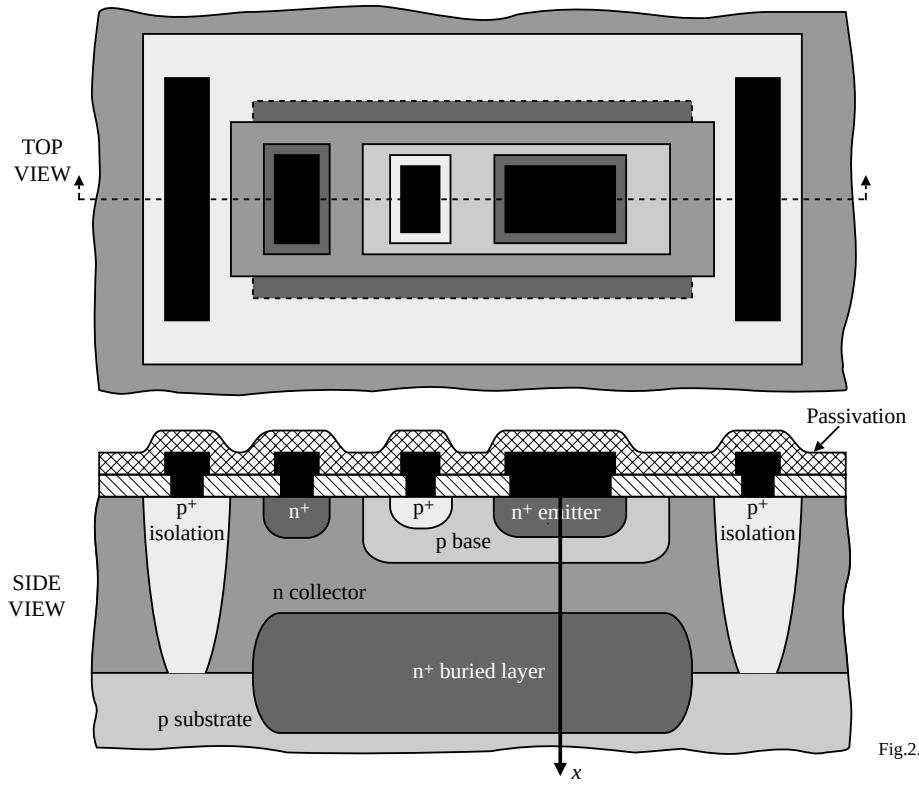


Fig.2.7-9

Typical Impurity Concentration Profile for the *npn* BJT

Taken along the line from the surface indicated in the last slide.

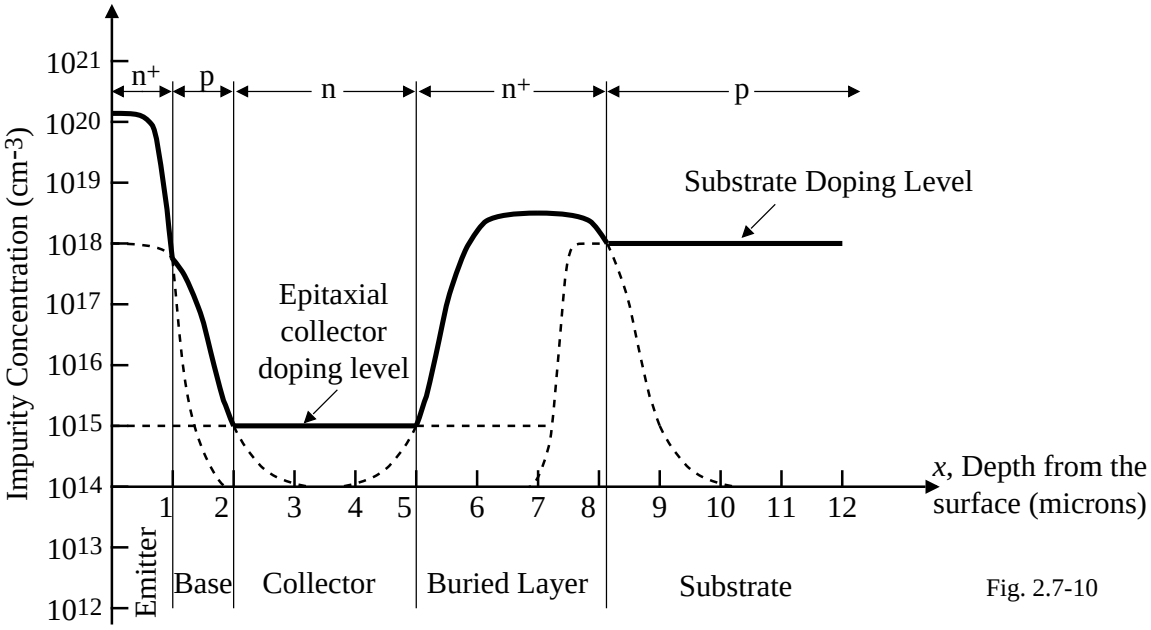


Fig. 2.7-10

Substrate *pnp* BJT

Collector is always connected to the substrate potential which is the most negative DC potential.

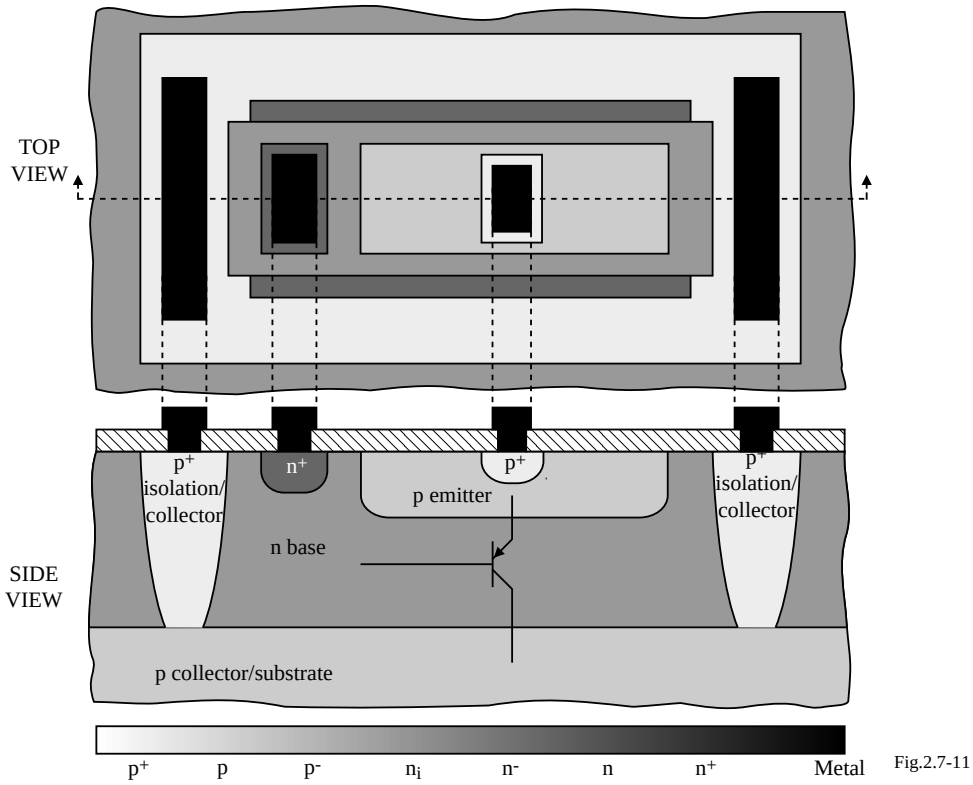


Fig.2.7-11

Lateral *pnp* BJT

Collector is not constrained to a fixed dc potential.

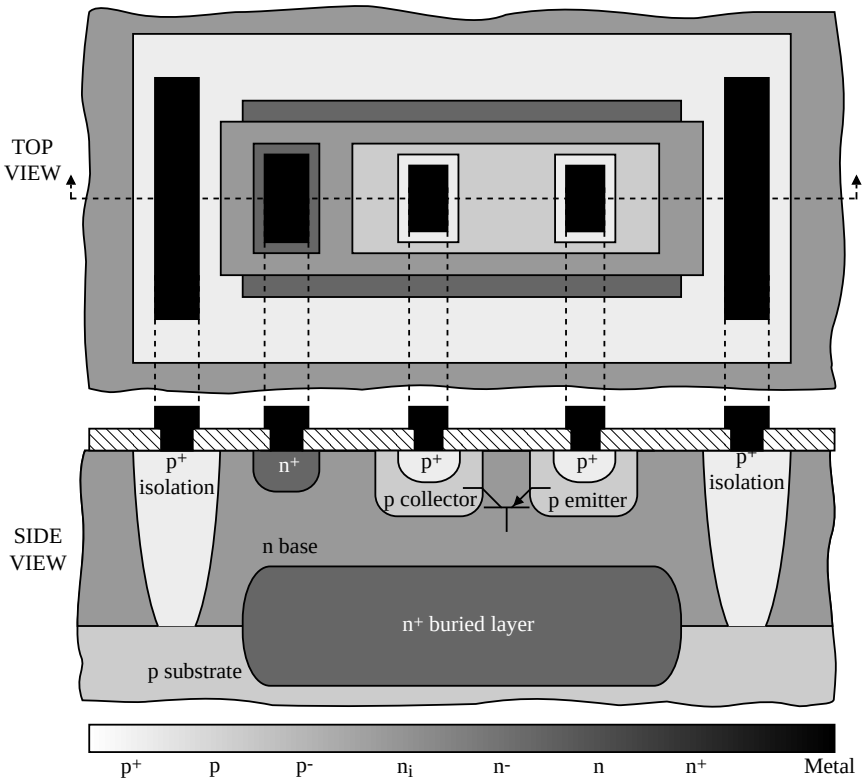


Fig.2.7-12

Types of Modifications to the Standard *npn* Technology

1.) Dielectric isolation - Isolation of the transistor from the substrate using an oxide layer.

2.) Double diffusion - A second, deeper n^+ emitter diffusion is used to create JFETs.

3.) Ion implanted JFETs - Use of an ion implantation to create the upper gate of a p-channel JFET

4.) Superbeta transistors - Use of a very thin base width to achieve higher values of β_F.

5.) Double diffused *pnp* BJT - Double diffusion is used to build a vertical *pnp* transistor whose performance more closely approaches that of the *npn* BJT.

SECTION 2.8 - BiCMOS TECHNOLOGY (OPTIONAL)

Typical 0.5µm BiCMOS Technology

Masking Sequence:

1. Buried n^+ layer
2. Buried p^+ layer
3. Collector tub
4. Active area
5. Collector sinker
6. n-well
7. p-well
8. Emitter window
9. Base oxide/implant
10. Emitter implant
11. Poly 1
12. NMOS lightly doped drain
13. PMOS lightly doped drain
14. n^+ source/drain
15. p^+ source/drain
16. Silicide protection
17. Contacts
18. Metal 1
19. Via 1
20. Metal 2
21. Via 2
22. Metal 3
23. Nitride passivation

Notation:

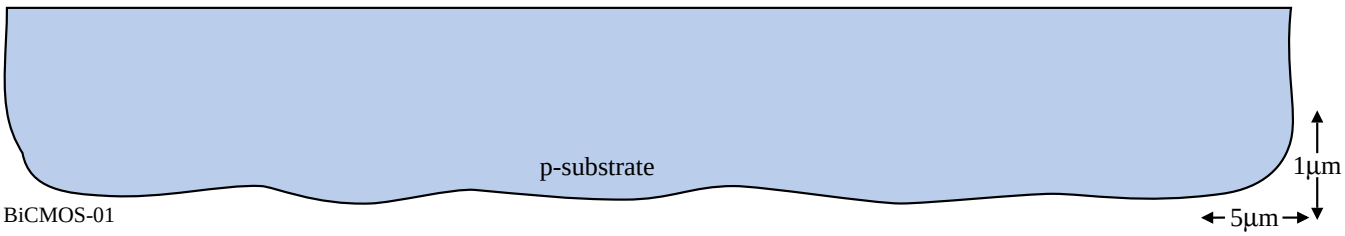
BSPG = Boron and Phosphorus doped Silicate Glass (oxide)

Kooi Nitride = A thin layer of silicon nitride on the silicon surface as a result of the reaction of silicon with the HN3 generated, during the field oxidation.

TEOS = Tetro-Ethyl-Ortho-Silicate. A chemical compound used to deposit conformal oxide films.

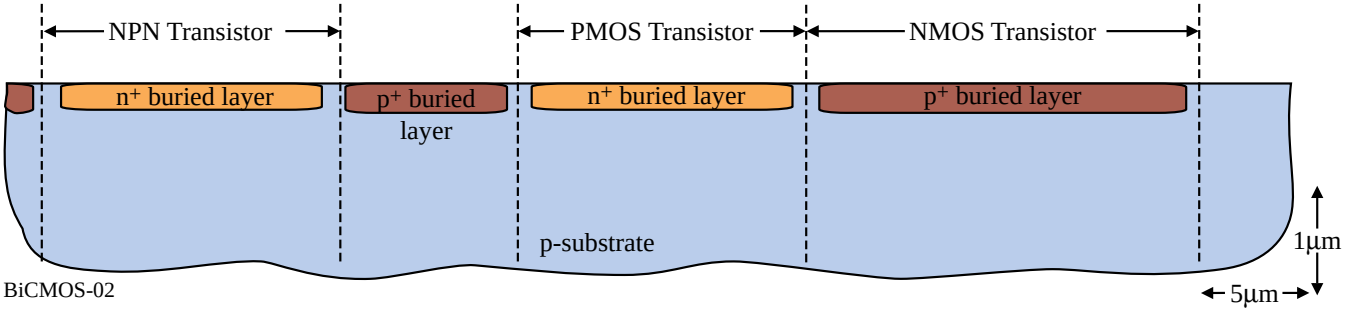
n^+ and p^+ Buried Layers

Starting Substrate:



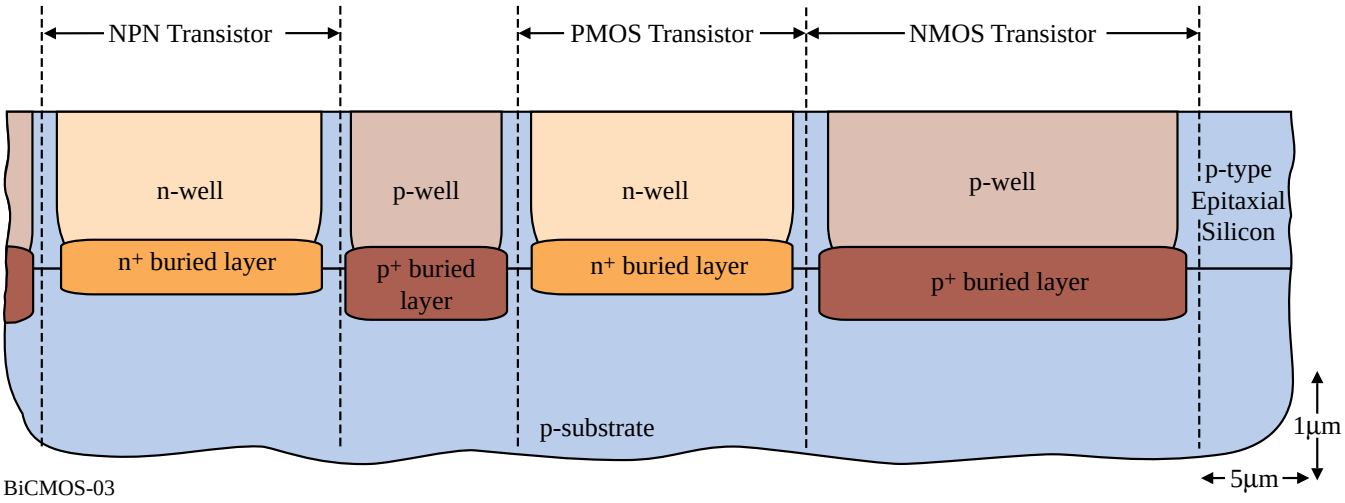
BiCMOS-01

n^+ and p^+ Buried Layers:



BiCMOS-02

Epitaxial Growth

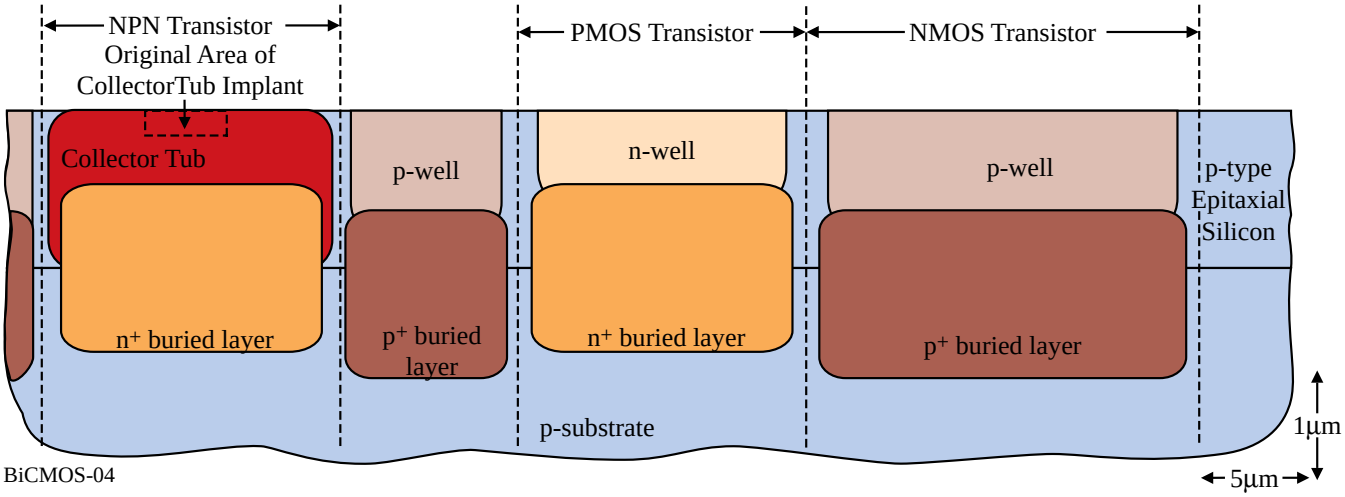


BiCMOS-03

Comment:

- As the epi layer grows vertically, it assumes the doping level of the substrate beneath it.
- In addition, the high temperature of the epitaxial process causes the buried layers to diffuse upward and downward.

Collector Tub

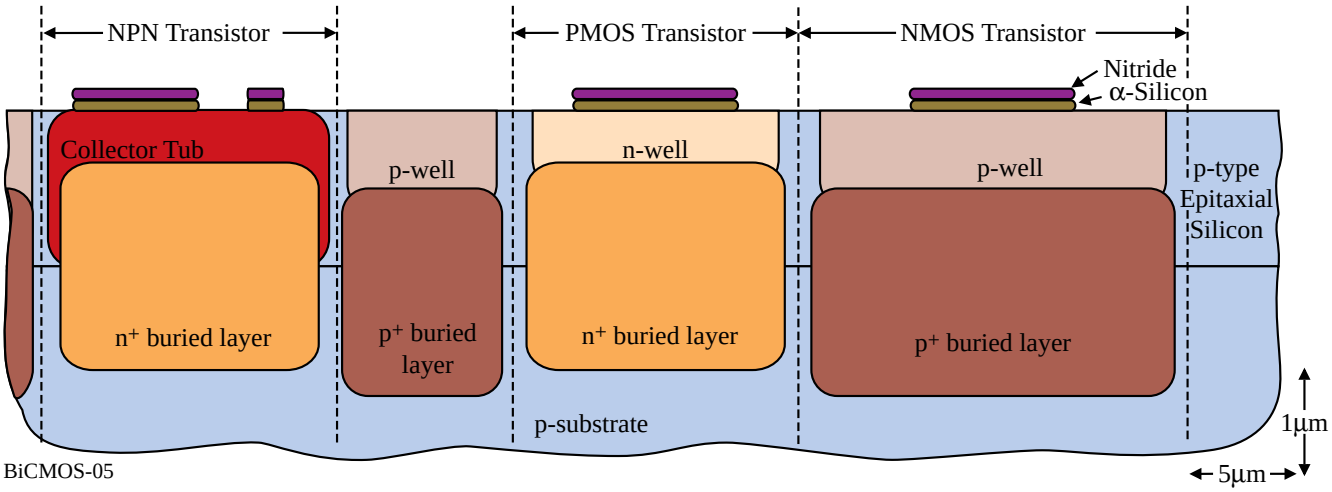


BiCMOS-04

Comment:

- The collector area is developed by an initial implant followed by a drive-in diffusion to form the collector tub.

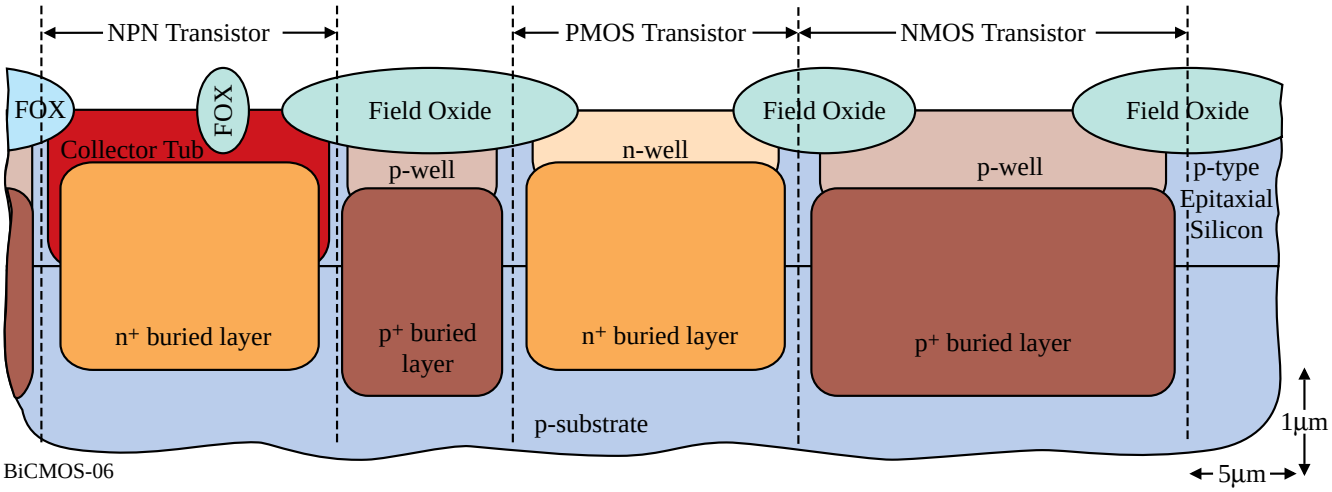
Active Area Definition



Comment:

- The silicon nitride is use to impede the growth of the thick oxide which allows contact to the substrate
- α-silicon is used for stress relief and to minimize the bird's beak encroachment

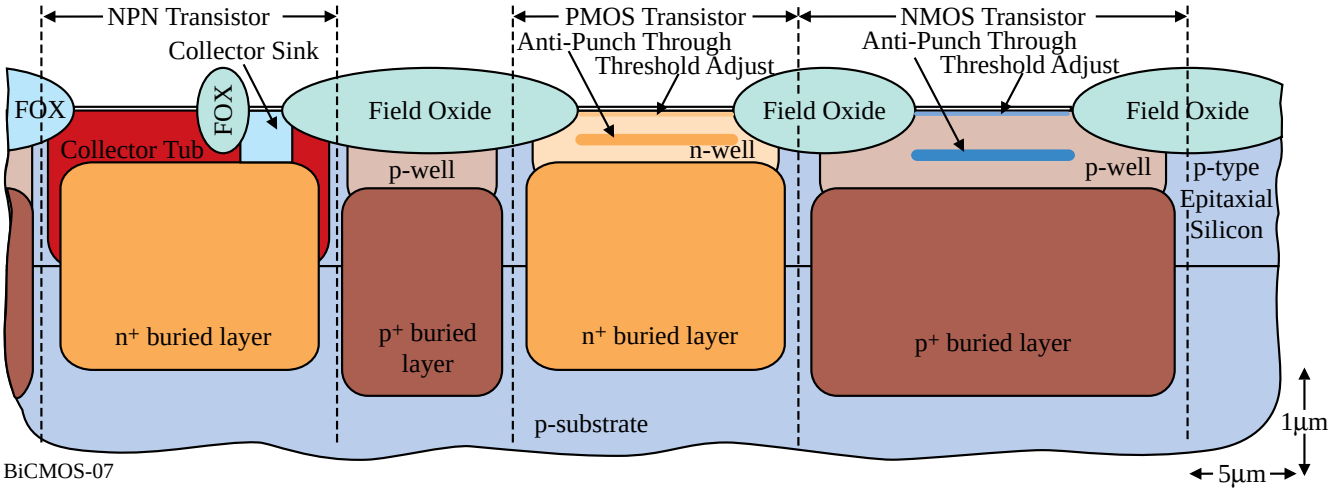
Field Oxide



Comments:

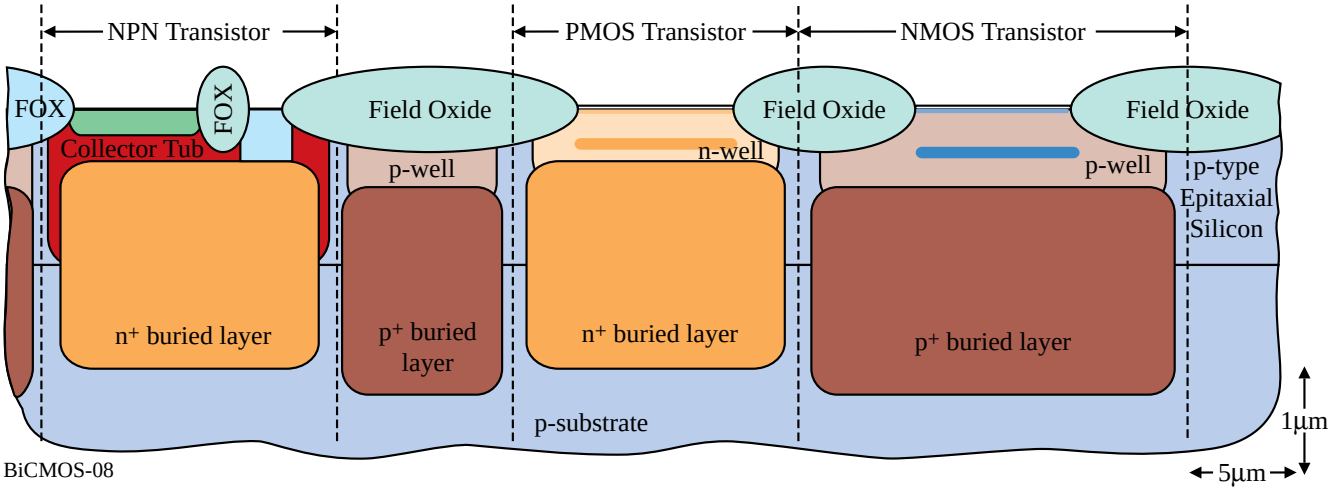
- The field oxide is used to isolate surface structures (i.e. metal) from the substrate

Collector Sink and n-Well and p-Well Definitions



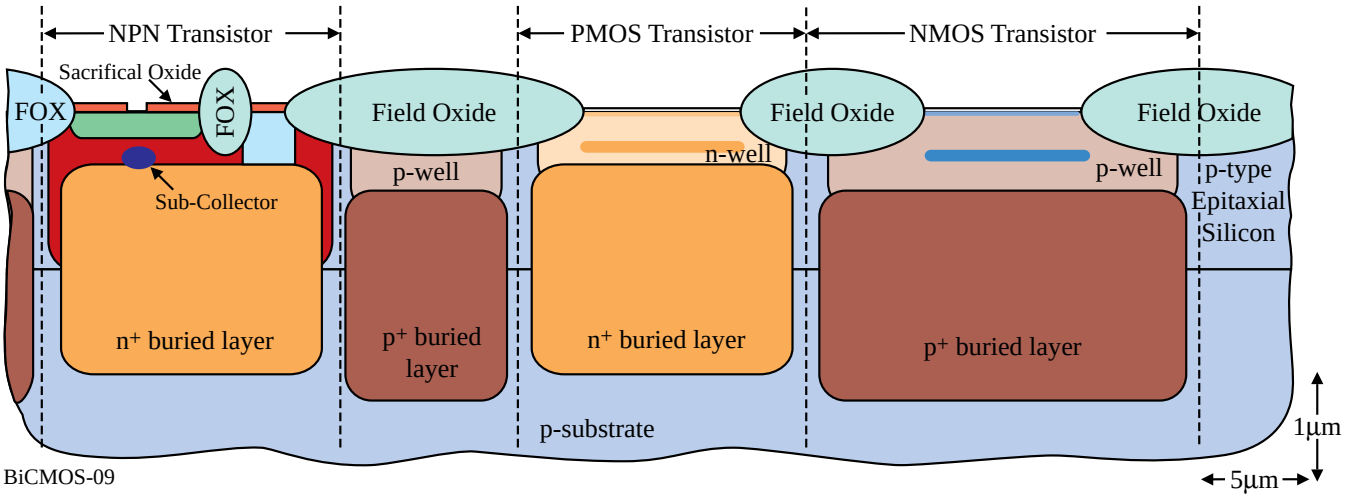
BiCMOS-07

Base Definition

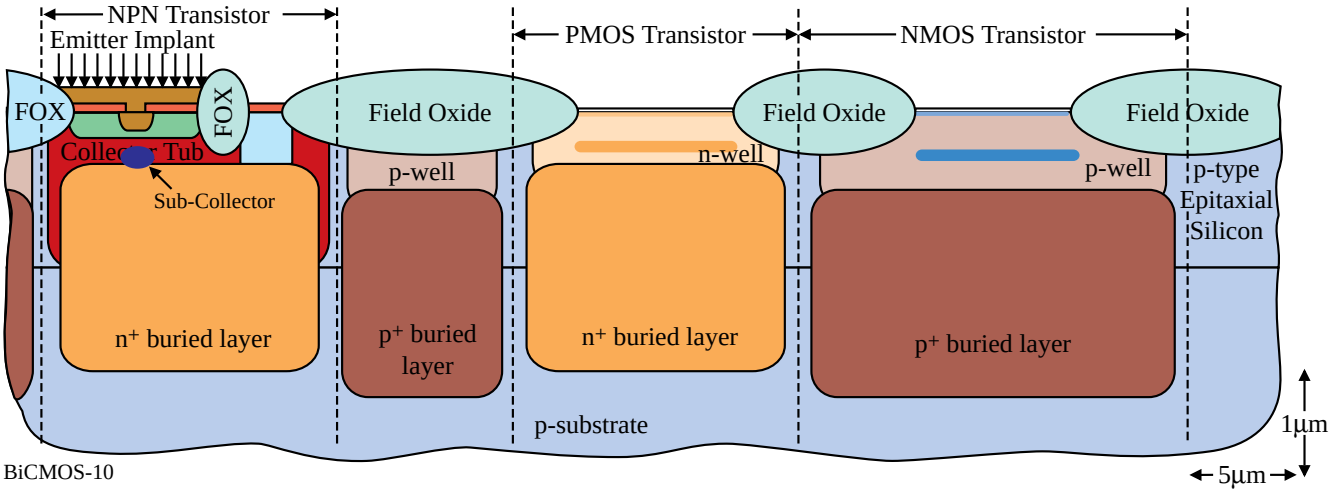


BiCMOS-08

Definition of the Emitter Window and Sub-Collector Implant



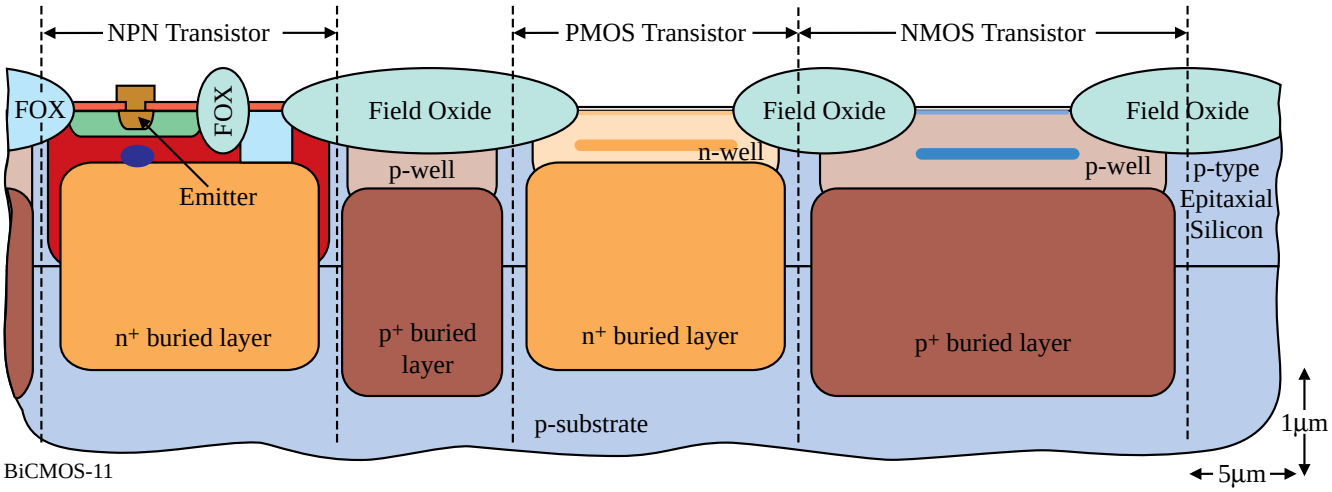
Emitter Implant



Comments:

- The polysilicon above the base is implanted with n-type carriers

Emitter Diffusion

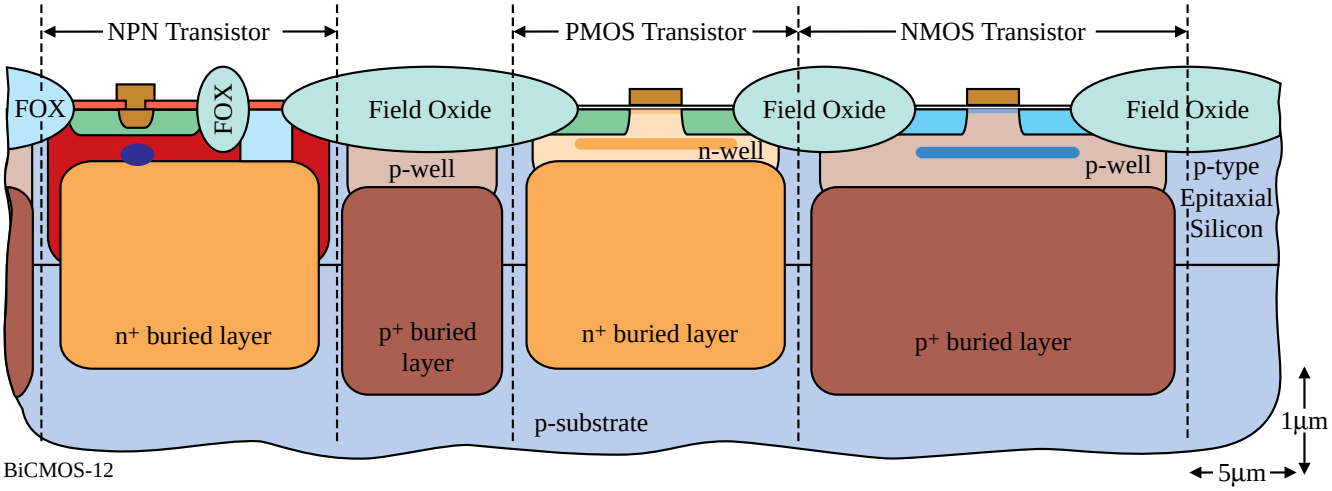


BiCMOS-11

Comments:

- The polysilicon not over the emitter window is removed and the n-type carriers diffuse into the base forming the emitter

Formation of the MOS Gates and LD Drains/Sources

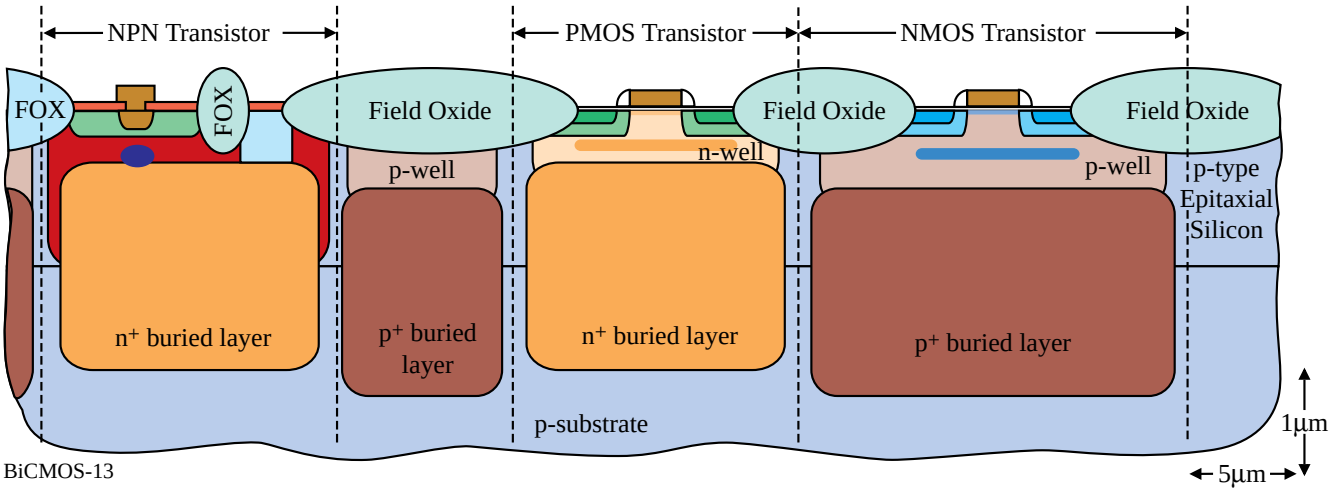


BiCMOS-12

Comments:

- The surface of the region where the MOSFETs are to be built is cleared and a thin gate oxide is deposited with a polysilicon layer on top of the thin oxide
- The polysilicon is removed over the source and drain areas
- A light source/drain diffusion is done for the NMOS and PMOS (separately)

Heavily Doped Source/Drain

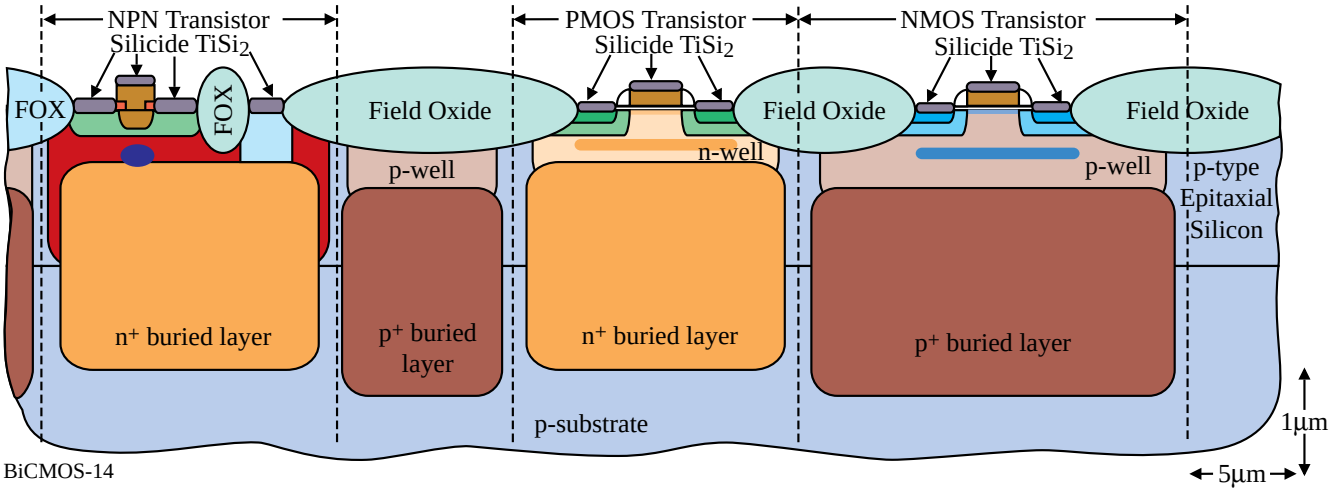


BiCMOS-13

Comments:

- The sidewall spacers prevent the heavy source/drain doping from being near the channel of the MOSFET

Siliciding

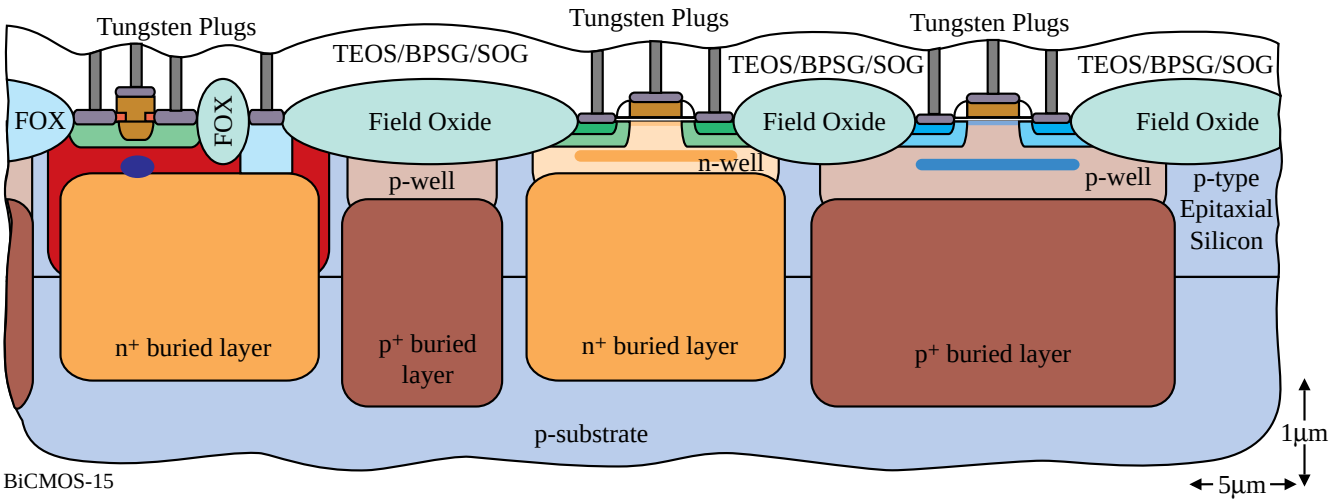


BiCMOS-14

Comments:

- Siliciding is used to reduce the resistance of the polysilicon and to provide ohmic contacts to the base, emitter, collector, sources and drains

Contacts

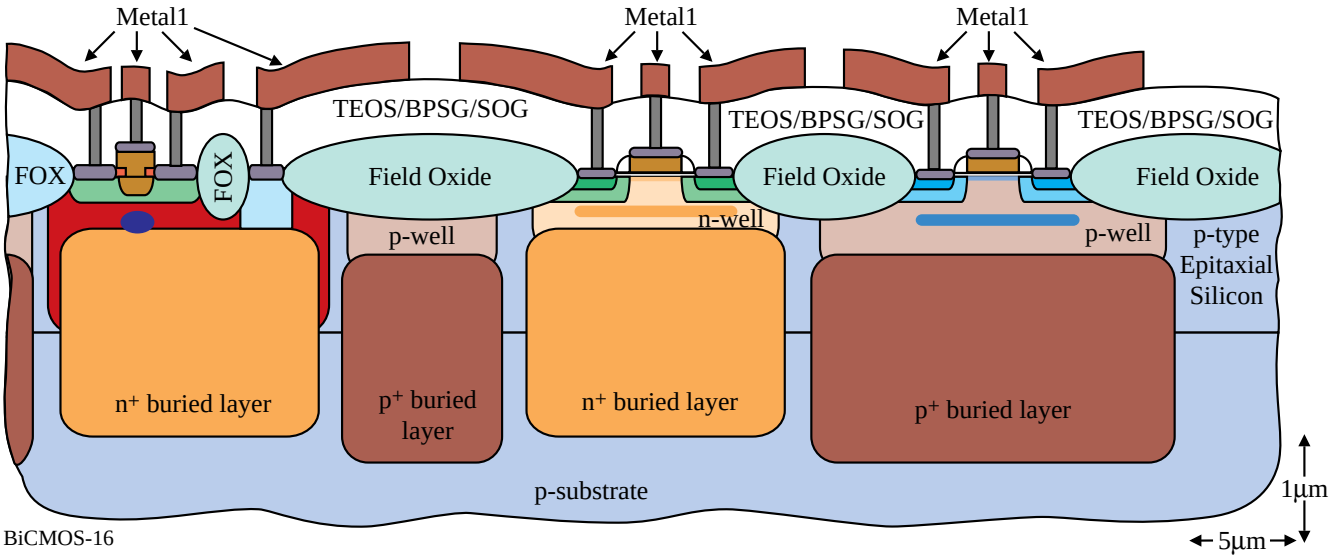


BiCMOS-15

Comments:

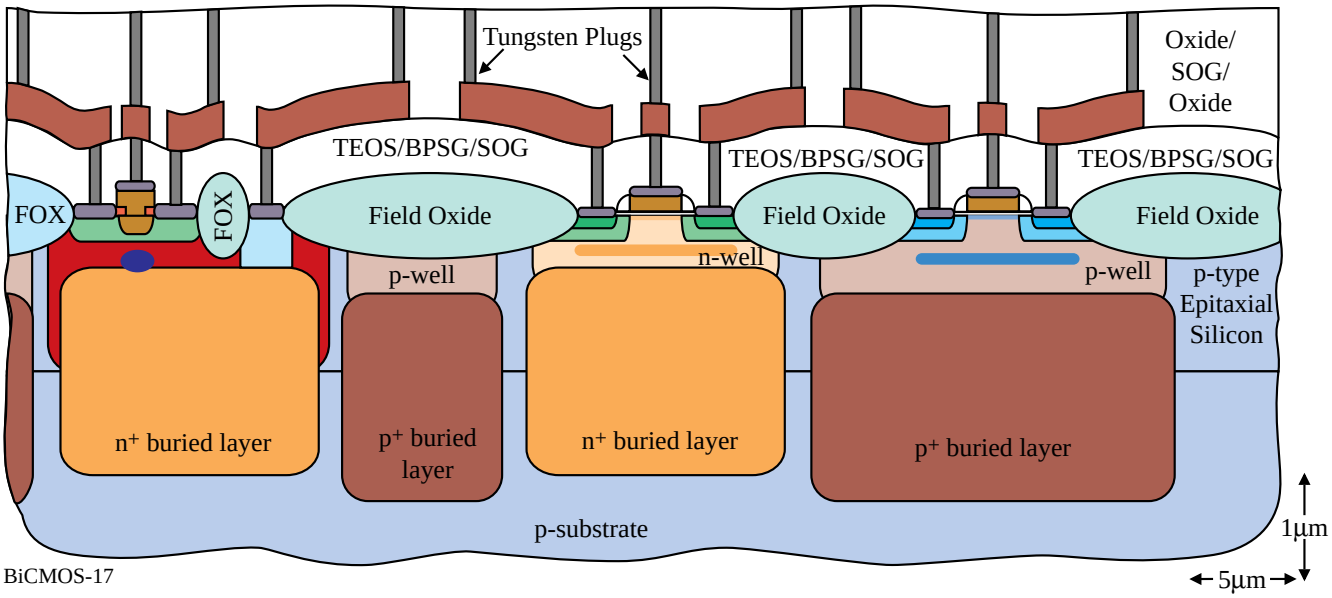
- A dielectric is deposited over the entire wafer
- One of the purposes of the dielectric is to smooth out the surface
- Tungsten plugs are used to make electrical contact between the transistors and metal1

Metal1



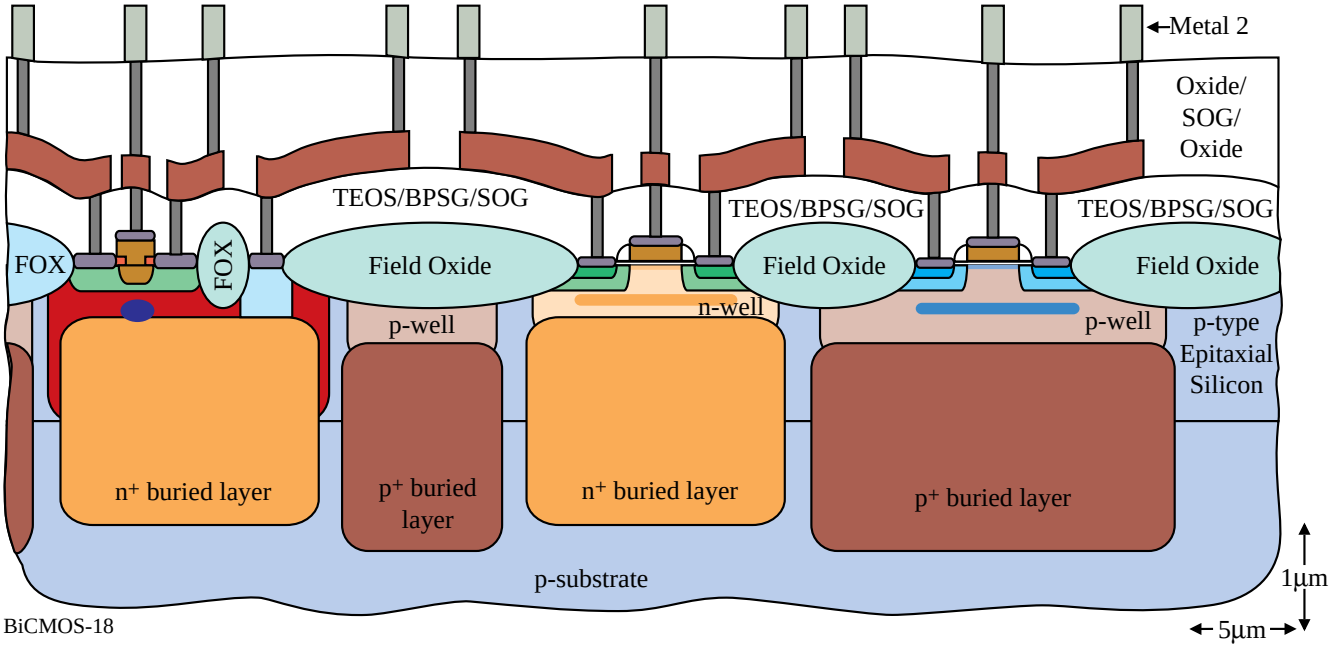
BiCMOS-16

Metal1-Metal2 Vias



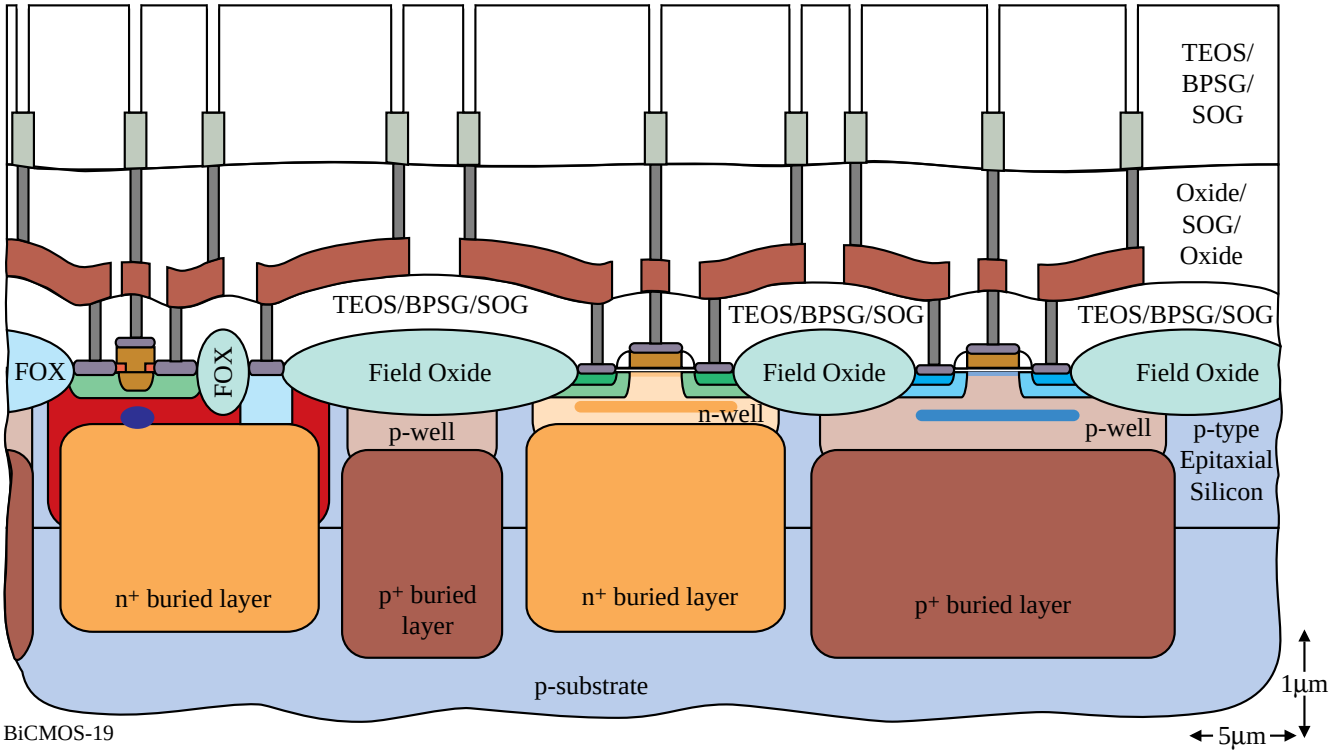
BiCMOS-17

Metal2



BiCMOS-18

Metal2-Metal3 Vias

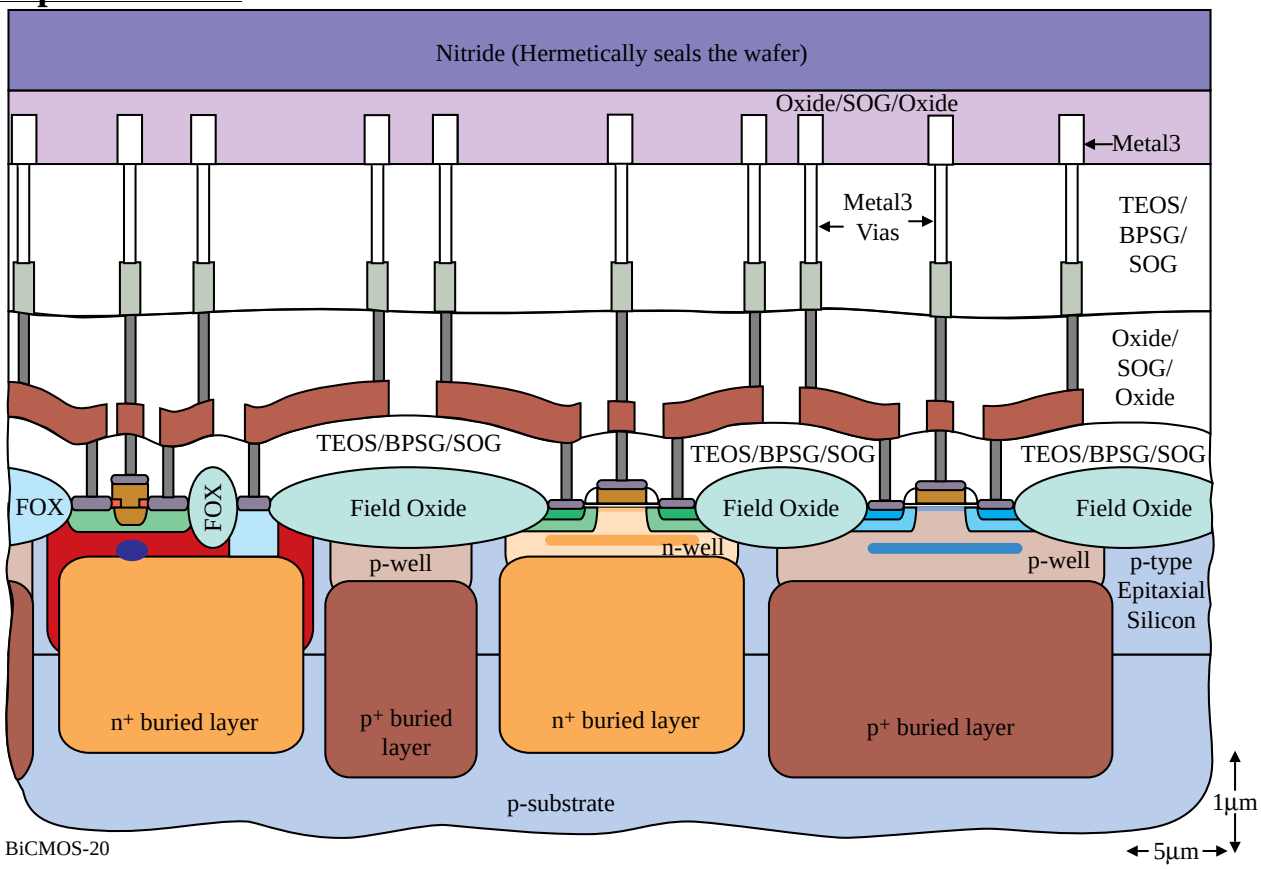


BiCMOS-19

Comments:

- The metal2-metal3 vias will be filled with metal3 as opposed to tungsten plugs

Completed Wafer



BiCMOS-20

SUMMARY

- This section has illustrated the major process steps for a 0.5micron BiCMOS technology.
- The performance of the active devices are:

  npn bipolar junction transistor:

  f_T = 12GHz, β_F = 100-140 BV_{CEO} = 7V

  n-channel FET:

  K' = 127μA/V^2 V_T = 0.64V $\lambda_N \approx 0.060$

  p-channel FET:

  K' = 34μA/V^2 V_T = -0.63V $\lambda_P \approx 0.072$
- Although today's state of the art is 0.25μm or 0.18μm BiCMOS, the processing steps illustrated above approximate that which is done in a smaller geometry.

SECTION 2.9 - SUMMARY

- Basic process steps include:

  1.) Oxide growth 2.) Thermal diffusion 3.) Ion implantation

  4.) Deposition 5.) Etching 6.) Epitaxy
- PN junctions are used to electrically isolate regions in CMOS
- A simple CMOS technology requires about 8 masks
- Bipolar technology provides a good vertical NPN and lateral and substrate PNPs
- BiCMOS combines the best of both BJT and CMOS technologies
- Passive component compatible with CMOS technology include:

  Capacitors - MOS, poly-poly, metal-metal, etc.
  Resistors - Diffused, implanted, well, etc.
  Inductors - Planar good only at very high frequencies
- CMOS technology has a reasonably good lateral BJT
- Other considerations in CMOS technology include:

  Latch-up
  ESD protection
  Temperature influence
  Noise influence
- Design rules are used to preserve the integrity of the technology