CHAPTER 8 - CMOS COMPARATORS

Chapter Outline
8.1 Characterization of Comparators
8.2 Two-Stage, Open-Loop Comparators
8.3 Other Open-Loop Comparators
8.4 Improving the Performance of Open-Loop Comparators
8.5 Discrete-Time Comparators
8.6 High-Speed Comparators
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SECTION 8.1 - CHARACTERIZATION OF COMPARATORS

Circuit Symbol for a Comparator

Static Characteristics
- Gain
- Output high and low states
- Input resolution
- Offset
- Noise

Dynamic Characteristics
- Propagation delay
- Slew rate
Noninverting and Inverting Comparators
The comparator output is binary with the two-level outputs defined as,
\( V_{OH} \) = the high output of the comparator
\( V_{OL} \) = the low level output of the comparator

Voltage transfer function of an Noninverting and Inverting Comparator:

Noninverting Comparator

\[
vo = \begin{cases} 
V_{OH} & \text{for } (v_P - v_N) > 0 \\
V_{OL} & \text{for } (v_P - v_N) < 0 
\end{cases}
\]

Inverting Comparator

\[
vo = \begin{cases} 
V_{OH} & \text{for } (v_P - v_N) > 0 \\
V_{OL} & \text{for } (v_P - v_N) < 0 
\end{cases}
\]

Gain = \( A_v = \lim_{\Delta V \to 0} \frac{V_{OH} - V_{OL}}{\Delta V} \) where \( \Delta V \) is the input voltage change
Static Characteristics - First-Order Model for a Comparator

Voltage transfer curve:

\[ V_{OH} \]
\[ V_{OL} \]
\[ V_{IL} \]
\[ V_{IH} \]
\[ V_{P-V_N} \]

where

\[ V_{IH} = \text{smallest input voltage at which the output voltage is } V_{OH} \text{ (noninverting comparator)} \]
\[ V_{IL} = \text{largest input voltage at which the output voltage is } V_{OL} \text{ (noninverting comparator)} \]

Model:

\[ f_1(v_{P-V_N}) = \begin{cases} 
V_{OH} & \text{for } (v_P - v_N) > 0 \\
V_{OL} & \text{for } (v_P - v_N) < 0 
\end{cases} \]

The voltage gain is \( A_v = \frac{V_{OH} - V_{OL}}{V_{IH} - V_{IL}} \)

Static Characteristics - First-Order Model including Input Offset Voltage

Voltage transfer curve:

\[ V_{OS} \]
\[ V_{P-V_N} \]
\[ V_{P-V_N}' \]

\[ V_{OS} = \text{the input voltage necessary to make the output equal } \frac{V_{OH}+V_{OL}}{2} \text{ when } v_P = v_N. \]

Model:

\[ f_1(v_{P-V_N}') = \begin{cases} 
\pm V_{OS} & \text{when } v_P = v_N 
\end{cases} \]

Other aspects of the model:

\[ ICMR = \text{input common mode voltage range (all transistors remain in saturation)} \]
\[ R_{in} = \text{input differential resistance} \]
\[ R_{icm} = \text{common mode input resistance} \]
**Static Characteristics - Comparator Noise**

Noise of a comparator is modeled as if the comparator were biased in the transition region.

![Diagram](image)

Noise leads to an uncertainty in the transition region which causes jitter or phase noise.

**Dynamic Characteristics - Propagation Time Delay**

Rising propagation delay time:

![Diagram](image)

Total propagation delay time = \( \frac{\text{Rising propagation delay time} + \text{Falling propagation delay time}}{2} \)
**Dynamic Characteristics - Single-Pole Response**

Model:

\[
A_v(s) = \frac{A_v(0)}{s \omega_c + 1} = \frac{A_v(0)}{s \tau_c + 1}
\]

where

- \(A_v(0)\) = dc voltage gain of the comparator
- \(\omega_c = \frac{1}{\tau_c}\) = -3dB frequency of the comparator or the magnitude of the pole

Step Response:

\[
v_o(t) = A_v(0) [1 - e^{-t/\tau_c}] V_{in}
\]

where

- \(V_{in}\) = the magnitude of the step input.

**Dynamic Characteristics - Propagation Time Delay**

The rising propagation time delay for a single-pole comparator is:

\[
\frac{V_{OH} - V_{OL}}{2} = A_v(0) [1 - e^{-t_p/\tau_c}] V_{in} \quad \rightarrow \quad t_p = \tau_c \ln \left[ \frac{1}{2} \frac{V_{OH} - V_{OL}}{A_v(0) V_{in}} \right]
\]

Define the minimum input voltage to the comparator as,

\[
V_{in}(min) = \frac{V_{OH} - V_{OL}}{A_v(0)} \quad \rightarrow \quad t_p = \tau_c \ln \left[ \frac{1}{2} \frac{V_{in}(min)}{V_{in}} \right]
\]

Define \(k\) as the ratio of the input step voltage, \(V_{in}\), to the minimum input voltage, \(V_{in}(min)\),

\[
k = \frac{V_{in}}{V_{in}(min)} \quad \rightarrow \quad t_p = \tau_c \ln \left[ \frac{2k}{2k-1} \right]
\]

Thus, if \(k = 1\), \(t_p = 0.693 \tau_c\).

Illustration:

![Figure 8.1-10](image)

Obviously, the more overdrive applied to the input, the smaller the propagation delay time.
Dynamic Characteristics - Slew Rate of a Comparator

If the rate of rise or fall of a comparator becomes large, the dynamics may be limited by the slew rate. Slew rate comes from the relationship,

\[ i = C \frac{dv}{dt} \]

where \( i \) is the current through a capacitor and \( v \) is the voltage across it.

If the current becomes limited, then the voltage rate becomes limited. Therefore for a comparator that is slew rate limited we have,

\[ t_p = \Delta T = \frac{\Delta V}{SR} = \frac{V_{OH} - V_{OL}}{2SR} \]

where

\( SR = \) slew rate of the comparator.

Example 8.1-1 - Propagation Delay Time of a Comparator

Find the propagation delay time of an open loop comparator that has a dominant pole at \( 10^3 \) radians/sec, a dc gain of \( 10^4 \), a slew rate of \( 1V/\mu s \), and a binary output voltage swing of \( 1V \). Assume the applied input voltage is \( 10mV \).

Solution

The input resolution for this comparator is \( 1V/10^4 \) or \( 0.1mV \). Therefore, the \( 10mV \) input is 100 times larger than \( v_{in}(min) \) giving a \( k \) of 100. Therefore, we get

\[ t_p = \frac{1}{10^7} \ln \left( \frac{2 \cdot 100}{2 \cdot 100 - 1} \right) = 10^{-3} \ln \left( \frac{200}{199} \right) = 5.01\mu s \]

For slew rate considerations, we get

\[ t_p = \frac{1}{2 \cdot 1 \times 10^6} = 0.5\mu s \]

Therefore, the propagation delay time for this case is the larger or \( 5.01\mu s \).
SECTION 8.2 - TWO-STAGE, OPEN-LOOP COMPARATORS

Two-Stage Comparator

An important category of comparators are those which use a high-gain stage to drive their outputs between $V_{OH}$ and $V_{OL}$ for very small input voltage changes.

The two-stage op amp without compensation is an excellent implementation of a high-gain, open-loop comparator.

![Figure 8.2-1](image)

Performance of the Two-Stage, Open-Loop Comparator

We know that the performance should be similar to the uncompensated two-stage op amp of Chapter 6.

Emphasis on comparator performance:

- Maximum output voltage
  \[ V_{OH} = V_{DD} - (V_{DD} - V_{G6}(\text{min}) - |V_{TP}|) \left( 1 - \sqrt{1 - \frac{8I_7}{\beta_6(V_{DD} - V_{G6}(\text{min}) - |V_{TP}|)^2}} \right) \]

- Minimum output voltage
  \[ V_{OL} = V_{SS} \]

- Small-signal voltage gain
  \[ A_v(0) = \frac{g_{m1}}{g_{ds2} + g_{ds4}} \left( \frac{g_{m6}}{g_{ds6} + g_{ds7}} \right) \]

- Poles
  Input:
  \[ p_1 = \frac{-1}{C \left( \frac{g_{ds2} + g_{ds4}}{g_{ds6} + g_{ds7}} \right)} \]
  Output:
  \[ p_2 = \frac{-1}{C \left( \frac{g_{ds6} + g_{ds7}}{g_{ds6} + g_{ds7}} \right)} \]

- Frequency response
  \[ A_v(s) = \frac{A_v(0)}{\left( \frac{s}{p_1} + 1 \right) \left( \frac{s}{p_2} + 1 \right)} \]
Example 8.2-1 - Performance of a Two-Stage Comparator

Evaluate $V_{OH}$, $V_{OL}$, $A_v(0)$, $V_{in}(min)$, $p_1$, $p_2$, for the two-stage comparator shown in Fig. 8.2-1. Assume that this comparator is the circuit of Ex. 6.3-1 with no compensation capacitor, $C_c$, and the minimum value of $V_G6 = 0V$. Also, assume that $C_I = 0.2pF$ and $C_H = 5pF$.

**Solution**

Using the above relations, we find that

$$V_{OH} = 2.5 - (2.5-0-0.7) \sqrt{1 - \frac{8.234 \times 10^{-6}}{50 \times 10^{-6} \cdot 38 \cdot (2.5-0-0.7)^2}} = 2.2V$$

The value of $V_{OL}$ is -2.5V. The gain was evaluated in Ex. 6.3-1 as $A_v(0) = 7696$. Therefore, the input resolution is

$$V_{in}(min) = V_{OH} - V_{OL} = \frac{V_{OH}}{A_v(0)} = \frac{2.2}{7696} = 0.611mV$$

Next, we find the poles of the comparator, $p_1$ and $p_2$. From Ex. 6.3-1 we find that

$$p_1 = \frac{g_{ds2} + g_{ds4}}{C_I} = \frac{15 \times 10^{-6} (0.04+0.05)}{0.2 \times 10^{-12}} = 6.75 \times 10^6 (1.074MHz)$$

and

$$p_2 = \frac{g_{ds6} + g_{ds7}}{C_H} = \frac{95 \times 10^{-6} (0.04+0.05)}{5 \times 10^{-12}} = 1.71 \times 10^6 (0.272MHz)$$

### Linear Step Response of the Two-Stage Comparator

The step response of a circuit with two real poles ($p_1 \neq p_2$) is,

$$v_{out}(t) = A_v(0) V_{in} \left[ 1 + \frac{p_2 e^{-p_1 t}}{p_1 - p_2} - \frac{p_1 e^{-p_2 t}}{p_1 - p_2} \right]$$

Normalizing gives,

$$v_{out}'(t_n) = \frac{v_{out}(t)}{A_v(0) V_{in}} = 1 - \frac{m}{m-1} e^{-t_n} + \frac{1}{m-1} e^{-m t_n}$$

where $m = \frac{p_2}{p_1} \neq 1$ and $t_n = t p_1 = \frac{t}{\tau_1}$

If $p_1 = p_2$ ($m = 1$), then

$$v_{out}'(t_n) = 1 - p_1 e^{-t_n} - \frac{t_n}{p_1} e^{-t_n} = 1 - e^{t_n} - t_n e^{t_n}$$

where $p_1 = 1$. 

![Normalized Output Voltage](Fig. 8.2-2)
Linear Step Response of the Two-Stage Comparator - Continued

The above results are valid as long as the slope of the linear response does not exceed the slew rate.

- Slope at $t = 0$ is zero
- Maximum slope occurs at ($m \neq 1$)
  
  $$t_n(\text{max}) = \frac{\ln(m)}{m-1}$$

  and is
  
  $$\frac{dv_{\text{out}}'(t_n(\text{max}))}{dt_n} = \frac{m}{m-1}[\exp\left(\frac{-\ln(m)}{m-1}\right) - \exp\left(\frac{-\ln(m)}{m-1}\right)]$$

- For the two-stage comparator using NMOS input transistors, the slew rate is
  
  $$SR^- = \frac{I_7}{C_L}$$
  
  $$SR^+ = \frac{I_6 I_7}{C_L} = \frac{\beta_6 (V_{DD} - V_G^6(\text{min}) - |V_{TP}|)^2 - I_7}{C_L}$$

Example 8.2-2 - Step Response of Ex. 8.2-1

Find the maximum slope of Ex. 8.2-1 and the time at which it occurs if the magnitude of the input step is $v_{in}(\text{min})$. If the dc bias current in M7 is 100µA, at what value of load capacitance, $C_L$ would the transient response become slew limited? If the magnitude of the input step is 100$v_{in}(\text{min})$, what would be the new value of $C_L$ at which slewing would occur?

Solution

The poles of the comparator were given in Ex. 8.2-1 as $p_1 = -6.75 \times 10^6$ rads/sec and $p_2 = -1.71 \times 10^6$ rads/sec. This gives a value of $m = 0.253$. From the previous expressions, the maximum slope occurs at $t_n(\text{max}) = 1.84$ secs. Dividing by $|p_1|$ gives $t(\text{max}) = 0.272$ µs. The slope of the transient response at this time is found as

$$\frac{dv_{\text{out}}'(t_n(\text{max}))}{dt_n} = -0.338[\exp(-1.84) - \exp(-0.253 \cdot 1.84)] = 0.159 \text{ V/sec}$$

Multiplying the above by $|p_1|$ gives

$$\frac{dv_{\text{out}}'(t(\text{max}))}{dt} = 1.072 \text{ V/µs}$$

Therefore, if the slew rate of the comparator is less than 1.072 V/µs, the transient response will experience slewing. Also, if the load capacitance, $C_L$, becomes larger than 100µA/1.072 V/µs or 93.3 pF, the comparator will experience slewing.

If the comparator is overdriven by a factor of 100$v_{in}(\text{min})$, then we must unnormalize the output slope as follows.

$$\frac{dv_{\text{out}}'(t(\text{max}))}{dt} = \frac{v_{io}}{v_{in}(\text{min})} \cdot \frac{dv_{\text{out}}'(t(\text{max}))}{dt} = 100 \cdot 1.072 \text{ V/µs} = 107.2 \text{ V/µs}$$

Therefore, the comparator will now slew with a load capacitance of 0.933 pF. For large overdrives, the comparator will generally experience slewing.
**Propagation Delay Time (Non-Slew)**

To find \( t_p \), we want to set 0.5(\( V_{OH} - V_{OL} \)) equal to \( v_{out}(t_n) \). However, \( v_{out}(t_n) \) is given as

\[
v_{out}(t_n) = A_v(0)V_{in} \left[ 1 - \frac{m}{m-1}e^{-m t_n} + \frac{1}{m-1}e^{-mt_n} - \frac{1}{m-1} \right]
\]

which can’t be easily solved so approximating the step response as a power series gives

\[
v_{out}(t_n) \approx A_v(0)V_{in} \left[ 1 - \frac{m}{m-1}t_n + \frac{1}{m-1}t_n^2 + \cdots \right] = \frac{mt_n^2 A_v(0)V_{in}}{2}
\]

Therefore, set \( v_{out}(t_n) = 0.5(V_{OH} - V_{OL}) \)

\[
\frac{V_{OH} + V_{OL}}{2} = \frac{mt_n^2 A_v(0)V_{in}}{2}
\]

or

\[
t_p = \sqrt{\frac{V_{OH} + V_{OL}}{mA_v(0)V_{in}}} = \sqrt{\frac{V_{in}(\text{min})}{mV_{in}}} = \frac{1}{\sqrt{mk}}
\]

This approximation is particularly good for large values of \( k \).

---

**Example 8.2-3 - Propagation Delay Time of a Two-Pole Comparator (Non-Slew)**

Find the propagation time delay of the comparator of Ex. 8.2-1 if \( V_{in} = 10\text{mV}, 100\text{mV} \) and 1V.

**Solution**

From Ex. 8.2-1 we know that \( V_{in}(\text{min}) = 0.611\text{mV} \) and \( m = 0.253 \). For \( V_{in} = 10\text{mV}, k = 16.366 \) which gives \( t_p = 0.491 \). The propagation time delay is equal to 0.491/6.75x10^6 or 72.9nS. This corresponds well with Fig. 8.2-2 where the normalized propagation time delay is the time at which the amplitude is 1/2k or 0.031 which corresponds to \( t_p \) of approximately 0.5. Similarly, for \( V_{in} = 100\text{mV} \) and 1V we get a propagation time delay of 23ns and 7.3ns, respectively.

![Fig. 8.2-2A](image-url)
Initial Operating States for the Two-Stage, Open-Loop Comparator

What are the initial operating states for the following comparator?

1.) Assume $v_{G2} = V_{REF}$ and $v_{G1} > V_{REF}$ with $i_1 < I_{SS}$ and $i_2 > 0$.

Initially, $i_4 > i_2$ and $v_{o1}$ increases. M4 becomes active and $i_4$ decreases until $i_3 = i_4$. $v_{o1}$ is in the range of,

$$V_{DD} - V_{SD4(sat)} < v_{o1} < V_{DD}$$

and the value of $v_{out}$ is

$$v_{out} = V_{SS}$$

2.) Assume $v_{G2} = V_{REF}$ and $v_{G1} >> V_{REF}$, therefore $i_1 = I_{SS}$ and $i_2 = 0$ which gives

$$v_{o1} = V_{DD}$$

and

$$v_{out} = V_{SS}$$

3.) Assume $v_{G2} = V_{REF}$ and $v_{G1} < V_{REF}$ with $i_1 > 0$ and $i_2 < I_{SS}$

Initially, $i_4 < i_2$ and $v_{o1}$ decreases. When $v_{o1} \leq V_{REF} - V_{TN}$, M2 becomes active and $i_2$ decreases. When $i_1 = i_2 = I_{SS}/2$ the circuit stabilizes and $v_{o1}$ is in the range of,

$$V_{REF} - V_{GS2} < v_{o1} < V_{REF} - V_{GS2} + V_{DS2(sat)}$$

or

$$V_{S2} < v_{o1} < V_{SS} + V_{DS2(sat)}$$

For the above conditions,

$$v_{out} = V_{DD} - (V_{DD} - V_{SS} - |V_{TP}|) \left[ 1 - \frac{\beta_7 I_{SS \beta_5 \beta_6}}{\beta_5 \beta_3 \beta_{0(V_{DD} - V_{SS} - |V_{TP}|)^2}} \right]$$

4.) Assume $v_{G2} = V_{REF}$ and $v_{G1} << V_{REF}$, therefore $i_2 = I_{SS}$ and $i_1 = 0$.

Same as in 3.) but now as $v_{o1}$ approaches $V_{SS}$ with $I_{SS}/2$ flowing, the value of $v_{GS2}$ becomes larger and M5 becomes active and $I_{SS}$ decreases. In the limit, $I_{SS} \rightarrow 0, V_{DS2} = 0$ and $V_{DS5} = 0$ resulting in

$$v_{o1} = V_{SS}$$

and

$$v_{out} = V_{DD} - (V_{DD} - V_{SS} - |V_{TP}|) \left[ 1 - \frac{\beta_7 I_{SS \beta_5 \beta_6}}{\beta_5 \beta_3 \beta_{0(V_{DD} - V_{SS} - |V_{TP}|)^2}} \right]$$
**Initial Operating States - Continued**

5.) Assume \( v_{G1} = V_{REF} \) and \( v_{G2} > V_{REF} \) with \( i_2 < I_{SS} \) and \( i_1 > 0 \).

Initially, \( i_4 < i_2 \) and \( v_{o1} \) falls, \( M2 \) becomes active and \( i_2 \) decreases until \( i_1 = i_2 = I_{SS}/2 \). Therefore,

\[
V_{REF} - V_{GS2}(I_{SS}/2) < v_{o1} < V_{REF} - V_{GS2}(I_{SS}/2) + V_{DS2}(sat)
\]

or

\[
V_{S2}(I_{SS}/2) < v_{o1} < V_{S2}(I_{SS}/2) + V_{DS2}(sat), \quad v_{G2} > V_{REF}, i_1 > 0 \text{ and } i_2 < I_{SS}
\]

and the value of \( v_{out} \) is

\[
v_{out} = V_{DD} - (V_{DD} - v_{o1})|V_{TP}|\left[1 - \sqrt{1 - \frac{\beta I_{SS}}{\beta_5 V_{DD} + V_{o1}}}ight]
\]

6.) Assume that \( v_{G1} = V_{REF} \) and \( v_{G2} > V_{REF} \). When the source voltage of \( M1 \) or \( M2 \) causes \( M5 \) to be active, then \( I_{SS} \) decreases and

\[
v_{o1} = V_{SS}
\]

and

\[
v_{out} = V_{DD} - (V_{DD} - V_{SS})|V_{TP}|\left[1 - \sqrt{1 - \frac{\beta I_{SS}}{\beta_5 V_{DD} + V_{SS}}}ight]
\]

7.) Assume \( v_{G1} = V_{REF} \) and \( v_{G2} < V_{REF} \) and \( i_1 < I_{SS} \) and \( i_2 > 0 \). Consequently, \( i_4 > i_2 \) which causes \( v_{o1} \) to increase. When \( M4 \) becomes active \( i_4 \) decreases until \( i_2 = i_4 \) at which \( v_{o1} \) stabilizes at

\[
V_{DD} - V_{SD4}(sat) < v_{o1} < V_{DD}, \quad v_{G2} < V_{REF}, i_1 < I_{SS} \text{ and } i_2 > 0
\]

\( M6 \) will be off under these conditions and \( v_{out} = V_{SS} \).

Summary of the Initial Operating States of the Two-Stage, Open-Loop Comparator using a N-channel, Source-coupled Input Pair:

<table>
<thead>
<tr>
<th>Conditions</th>
<th>Initial State of ( v_{o1} )</th>
<th>Initial State of ( v_{out} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( v_{G1} &gt; V_{G2}, i_1 &lt; I_{SS} \text{ and } i_2 &gt; 0 )</td>
<td>( V_{DD} - V_{SD4}(sat) &lt; v_{o1} &lt; V_{DD} )</td>
<td>( V_{SS} )</td>
</tr>
<tr>
<td>( v_{G1} &gt; V_{G2}, i_1 = I_{SS} \text{ and } i_2 = 0 )</td>
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<td>( V_{SS} )</td>
</tr>
<tr>
<td>( v_{G1} &lt; V_{G2}, i_1 &gt; 0 \text{ and } i_2 &lt; I_{SS} )</td>
<td>( v_{o1} = V_{G2} - V_{GS2}(I_{SS}/2), = V_{SS} \text{ if } M5 \text{ act.} )</td>
<td>Eq. (19), Sec. 5.1 for PMOS</td>
</tr>
<tr>
<td>( v_{G1} &lt; V_{G2}, i_1 &gt; 0 \text{ and } i_2 = I_{SS} )</td>
<td>( V_{SS} )</td>
<td>Eq. (19), Sec. 5.1 for PMOS</td>
</tr>
<tr>
<td>( v_{G2} = V_{G1}, i_1 &gt; 0 \text{ and } i_2 &lt; I_{SS} )</td>
<td>( V_{S2}(I_{SS}/2) &lt; v_{o1} &lt; V_{S2}(I_{SS}/2) + V_{DS2}(sat) )</td>
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<td>( V_{DD} )</td>
<td>( V_{SS} )</td>
</tr>
</tbody>
</table>
**Trip Point of an Inverter**

In order to determine the propagation delay time, it is necessary to know when the second stage of the two-stage comparator begins to “turn on”.

Second stage:

\[
\begin{array}{c}
\text{Vin} \\
M6 \\
\text{In} \\
M7 \\
\text{Vout} \\
V_{\text{DD}} \\
V_{\text{SS}} \\
\end{array}
\]

Trip point:

Assume that M6 and M7 are saturated. (We know that the steepest slope occurs for this condition.)

Equate \( i_6 \) to \( i_7 \) and solve for \( v_{\text{in}} \) which becomes the trip point.

\[
\therefore v_{\text{in}} = V_{\text{TRP}} = V_{\text{DD}} - |V_{\text{TP}}| - K_N(W_7/L_7) - K_P(W_6/L_6) (V_{\text{Bias}} - V_{\text{SS}} - V_{\text{TN}})
\]

Example:

If \( W_7/L_7 = W_6/L_6 \), \( V_{\text{DD}} = 2.5 \text{V}, V_{\text{SS}} = -2.5 \text{V}, \) and \( V_{\text{Bias}} = 0 \text{V} \) the trip point for the circuit above is

\[
V_{\text{TRP}} = 2.5 - 0.7 - \sqrt{110/50} (0 + 2.5 - 0.7) = -0.870 \text{V}
\]

**Propagation Delay Time of a Slewing, Two-Stage, Open-Loop Comparator**

Previously we calculated the propagation delay time for a nonslewing comparator.

If the comparator slews, then the propagation delay time is found from

\[
i_i = \frac{dv_i}{dt} = C_i \frac{\Delta v_i}{\Delta t_i}
\]

where

\( C_i \) is the capacitance to ground at the output of the \( i \)-th stage

The propagation delay time of the \( i \)-th stage is,

\[
t_i = \Delta t_i = C_i \frac{\Delta V_i}{I_i}
\]

The propagation delay time is found by summing the delays of each stage.

\[
t_p = t_1 + t_2 + t_3 + \cdots
\]
Example 8.2-5 - Calculation of the Propagation Time Delay of a Two-Stage, Open-Loop Comparator

For the two-stage comparator shown assume that $C_I = 0.2\, \text{pF}$ and $C_{II} = 5\, \text{pF}$. Also, assume that $v_{G1} = 0\, \text{V}$ and that $v_{G2}$ has the waveform shown. If the input voltage is large enough to cause slew to dominate, find the propagation time delay of the rising and falling output of the comparator and give the propagation time delay of the comparator.

**Solution**

The total delay will be given as the sum of the first and second stage delays, $t_1$ and $t_2$, respectively.

First, consider the change of $v_{G2}$ from $-2.5\, \text{V}$ to $2.5\, \text{V}$ at $0.2\, \mu\text{s}$. From Table 8.2-1, the last row, the initial states of $v_{o1}$ and $v_{out}$ are $+2.5\, \text{V}$ and $-2.5\, \text{V}$, respectively. To find the falling propagation time delay of the first stage $t_{f1}$ requires $C_I$, $\Delta V_{o1}$, and $I_5$. $C_I$ is given as $0.2\, \text{pF}$, $I_5 = 30\, \mu\text{A}$ and $\Delta V_{o1}$ can be calculated by finding the trip point of the output stage by setting the current of $M6$ when saturated equal to $234\, \mu\text{A}$.

$$\frac{\beta_6}{2} (V_{SG6}-|V_{TP}|)^2 = 234\, \mu\text{A} \rightarrow V_{SG6} = 0.7 + \frac{\sqrt{234\times2}}{110\times38} = 1.035\, \text{V}$$

Therefore, the trip point of the second stage is $V_{TRP2} = 2.5 - 1.035 = 1.465\, \text{V}$

Therefore, the falling propagation time delay of the first stage is

$$t_{fo1} = 0.2\, \text{pF} \left(\frac{1.035\, \text{V}}{30\, \mu\text{A}}\right) = 6.9\, \text{ns}$$

The rising propagation time delay of the second stage requires the knowledge of $C_{II}$, $\Delta V_{out}$, and $I_6$. $C_{II}$ is given as $5\, \text{pF}$, $\Delta V_{out} = 2.5\, \text{V}$ (assuming the trip point of the circuit connected to the output of the comparator is $0\, \text{V}$), and $I_6$ can be found as follows. When the gate of $M6$ is at $1.465\, \text{V}$, the current is $234\, \mu\text{A}$.

However, the output of the first stage will continue to fall so what value should be used for the gate in order to calculate $I_6$? The lowest value of $V_{G6}$ is given as

$$V_{G6} = V_{G1} - V_{GS1}(I_{SS}/2) + V_{DS1} = 0.7 - \frac{2\times15}{110\times3} = -1.00\, \text{V}$$

Let us take the approximate value of $V_{G6}$ as midway between $1.465\, \text{V}$ and $-1.00\, \text{V}$ which is $0.232\, \text{V}$. Therefore $V_{SG6} = 2.27\, \text{V}$ and the value of $I_6$ is

$$I_6 = \frac{\beta_6}{2} (V_{SG6}-|V_{TP}|)^2 = \frac{38.50}{2} (2.27 - 0.7)^2 = 2.342\, \mu\text{A}$$

which is a reminder that the active transistor can generally sink or source more current than the fixed transistor in the class-A inverting stage. The rising propagation time delay for the output can expressed as

$$t_{rout} = 5\, \text{pF} \left(\frac{2.5\, \text{V}}{2.342\, \mu\text{A} - 234\, \mu\text{A}}\right) = 5.93\, \text{ns}$$

Thus the total propagation time delay of the rising output of the comparator is approximately $12.8\, \text{ns}$ and most of this delay is attributable to the first stage.
Example 8.2-5 - Continued

Next consider the change of \(v_{G2}\) from 2.5V to -2.5V which occurs at 0.4\(\mu\)s. We shall assume that \(v_{G2}\) has been at 2.5V long enough for the conditions of Table 8.2-1 to be valid. Therefore, \(v_{o1} = 0V - V_{GS1}(30\mu A) = -1.13V\) and \(v_{out} = V_{DD}\). Rather than use Eq. (19) of Sec. 5.1 we have assumed that \(v_{out}\) is approximately \(V_{DD}\). The propagation time delays for the first and second stages are calculated as

\[
\begin{align*}
\tau_{rot} &= 0.2pF \frac{1.465V - (-1.13V)}{30\mu A} = 17.3ns \\
\tau_{fout} &= 5pF \frac{2.5V}{234\mu A} = 53.42ns
\end{align*}
\]

The total propagation time delay of the falling output is 70.72ns. Taking the average of the rising and falling propagation time delays gives a propagation time delay for this two-stage, open-loop comparator of about 41.76ns. These values compare favorably with the simulation of the comparator.

Design of a Two-Stage, Open-Loop Comparator

Table 8.2-2  Design of the Two-Stage, Open-Loop Comparator of Fig. 8.2-3 for a Linear Response.

<table>
<thead>
<tr>
<th>Step</th>
<th>Design Relationships</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>(</td>
<td>\mu</td>
</tr>
<tr>
<td>2</td>
<td>(\frac{W_6}{L_6} = \frac{2I_6}{K_P(V_{SD}(sat))^2}) and (\frac{W_7}{L_7} = \frac{2I_7}{K_N(V_{DS}(sat))^2})</td>
<td>(V_{SD}(sat) = V_{DD} - V_{OH})</td>
</tr>
<tr>
<td>3</td>
<td>Guess (C_I) as 0.1pF to 0.5pF (\therefore I_5 = I_7 \frac{C_I}{C_H})</td>
<td>A result of choosing (m = 1) Will check (C_I) later</td>
</tr>
<tr>
<td>4</td>
<td>(\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{I_5}{K_P(V_{SG3}(sat))^2})</td>
<td>(V_{SG3} = V_{DD} - V_{icm} + V_{TN})</td>
</tr>
<tr>
<td>5</td>
<td>(s_{m1} = \frac{A_v(0)(g_{ds2} + g_{ds4})(g_{ds6} + g_{ds7})}{s_{m6}})</td>
<td>If (C_I) is greater than the guess in step 3, then increase (C_I) and repeat steps 4 through 6</td>
</tr>
<tr>
<td>6</td>
<td>Find (C_I) and check assumption (C_I = C_{g2d} + C_{g4d} + C_{g6d} + C_{bd2} + C_{bd4})</td>
<td>If (V_{DS}(sat)) is less than 100mV, increase (W_1/L_1).</td>
</tr>
<tr>
<td>7</td>
<td>(V_{DS}(sat) = V_{icm} - V_{GS1} - V_{SS})</td>
<td></td>
</tr>
</tbody>
</table>

\(s_{m6} = \sqrt{\frac{2K_P W_6 L_6}{g_{m1}} - \frac{A_v(0)}{V_{in}(mm)}}\)
Example 8.2-6 - Design of the Two-Stage, Open-Loop Comparator of Fig. 8.2-3 for a Linear Response.

Assume the specifications of the comparator shown are given below.

\( t_p = 50 \text{ns} \)  \( V_{OH} = 2 \text{V} \)  \( V_{OL} = -2 \text{V} \)

\( V_{DD} = 2.5 \text{V} \)  \( V_{SS} = -2.5 \text{V} \)  \( C_{II} = 5 \text{pF} \)

\( V_{in(\text{min})} = 1 \text{mV} \)  \( V_{icm^+} = 2 \text{V} \)  \( V_{icm^-} = -1.25 \text{V} \)

Also assume that the overdrive will be a factor of 10. Use this architecture to achieve the above specifications and assume that all channel lengths are to be 1µm.

Solution

Following the procedure outlined in Table 8.2-2, we choose \( m = 1 \) to get

\[ \frac{|p_I|}{|p_{II}|} = \frac{10^9}{50 \text{V}} = 6.32 \times 10^6 \text{ rads/sec} \]

This gives

\[ I_6 = I_7 = \frac{6.32 \times 10^6 \times 5 \times 10^{-12}}{0.04 + 0.05} = 351 \mu\text{A} \]

\( \rightarrow I_6 = I_7 = 400 \mu\text{A} \)

Therefore,

\[ \frac{W_6}{L_6} = \frac{2 \times 400}{(0.5)^2 \times 50} = 64 \]

and

\[ \frac{W_7}{L_7} = \frac{2 \times 400}{(0.5)^2 \times 110} = 29 \]

Next, we guess \( C_I = 0.2 \text{pF} \). This gives \( I_5 = 32 \mu\text{A} \) and we will increase it to 40 µA for a margin of safety. Step 4 gives \( V_{SS3} \) as 1.2V which results in

\[ \frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{40}{50(1.2 - 0.7)^2} = 3.2 \]

\[ \rightarrow \frac{W_3}{L_3} = \frac{W_4}{L_4} = 4 \]

The desired gain is found to be 4000 which gives an input transconductance of

\[ g_{m1} = \frac{4000 \times 0.09 \times 20}{44.44} = 162 \mu\text{S} \]

This gives the \( W/L \) ratios of M1 and M2 as

\[ \frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{(162)^2}{110 \times 40} = 5.96 \]

\[ \rightarrow \frac{W_1}{L_1} = \frac{W_2}{L_2} = 6 \]

To check the guess for \( C_I \) we need to calculate it which is done as

\[ C_I = C_{gd2} + C_{gd4} + C_{gsb} + C_{bd2} + C_{bd4} = 0.9 \text{fF} + 1.3 \text{fF} + 119.5 \text{fF} + 20.4 \text{fF} + 36.8 \text{fF} = 178.9 \text{fF} \]

which is less than what was guessed so we will make no changes.
Example 8.2-6 - Continued
Finally, the \( W/L \) value of \( M5 \) is found by finding \( V_{GS1} \) as 0.946V which gives \( V_{DSS}(sat) = 0.304V \). This gives

\[
W_5 = \frac{2.40}{(0.304)^2 \cdot 110} = 7.87 = 8
\]

Obviously, \( M5 \) and \( M7 \) cannot be connected gate-gate and source-source. The value of \( I_5 \) and \( I_7 \) must be derived separately as illustrated below. The \( W \) values are summarized below assuming that all channel lengths are 1µm.

\[
W_1 = W_2 = 6µm \quad W_3 = W_4 = 4µm \quad W_5 = 8µm
\]

\[
W_6 = 64µm \quad W_7 = 29µm
\]

![Fig. 8.2-7](image-url)

### Design of a Two-Stage Comparator for a Slewing Response

Table 8.2-3  Design of the Two-Stage, Open-Loop Comparator of Fig. 8.2-3 for a Slewing Response.

<table>
<thead>
<tr>
<th>Step</th>
<th>Design Relationships</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>( I_1 = I_6 = \frac{dv_{in}}{dt} = \frac{C_f(V_{OH}-V_{OL})}{t_p} )</td>
<td>Assume the trip point of the output is ( (V_{OH}+V_{OL})/2 ).</td>
</tr>
<tr>
<td>2</td>
<td>( W_6 = \frac{2I_6}{K_p(V_{SD6}(sat))^2} ) and ( W_7 = \frac{2I_7}{K_N(V_{DS7}(sat))^2} )</td>
<td>( V_{SD6}(sat) = V_{DD-V_{OH}} ) and ( V_{DSS}(sat) = V_{OL-V_{SS}} ) Typically ( 0.1\mu F &lt; C_f &lt; 0.5\mu F )</td>
</tr>
<tr>
<td>3</td>
<td>Guess ( C_f ) as 0.1pF to 0.5pF ( \therefore I_5 = \frac{2C_f}{L_7C_{II}} )</td>
<td>Assume that ( v_{in} ) swings between ( V_{OH} ) and ( V_{OL} ).</td>
</tr>
<tr>
<td>4</td>
<td>( I_5 = \frac{dv_{in}}{dt} = \frac{C_4(V_{OH}+V_{OL})}{t_p} )</td>
<td>( V_{SG3} = V_{DD-V_{icm}+V_{TN}} )</td>
</tr>
<tr>
<td>5</td>
<td>( W_4 = \frac{W_1}{L_4} = \frac{K_p(V_{SG3}+V_{TP})^2}{2I_5} )</td>
<td>If ( C_f ) is greater than the guess in step 3, increase the value of ( C_f ) and repeat steps 4 through 6</td>
</tr>
<tr>
<td>6</td>
<td>( g_{m1} = \frac{A_f(0)g_{ds2}g_{ds4}(g_{ds6}+g_{ds7})}{g_{m6}} )</td>
<td>If ( V_{DSS}(sat) ) is less than 100mV, increase ( W_1/L_1 ).</td>
</tr>
<tr>
<td>7</td>
<td>Find ( C_f ) and check assumption ( C_f = C_gd2+C_gd4+C_gd6+C_{gd2}C_{gd4} )</td>
<td>( g_{m6} = \sqrt{\frac{2K_pW_5}{L_6}A_f(0)} = V_{oh}+V_{OL}(\min) )</td>
</tr>
<tr>
<td>8</td>
<td>( V_{DSS}(sat) = V_{icm} - V_{GS1} - V_{SS} ) ( \frac{W_5}{L_5} = \frac{2I_5}{K_N(V_{DSS}(sat))^2} )</td>
<td></td>
</tr>
</tbody>
</table>

Chapter 8 - CMOS Comparators (5/1/01) © P.E. Allen, 2001
Example 8.2-7 - Design of the Two-Stage, Open-Loop Comparator for a Slewing Response

Assume the specifications of Fig. 8.2-3 are given below.

\[
\begin{align*}
&I_p = 50\text{ns} & V_{OH} = 2\text{V} \quad V_{OL} = -2\text{V} \\
&V_{DD} = 2.5\text{V} & V_{SS} = -2.5\text{V} \\
&C_{II} = 5\text{pF} & V_{icm^+} = 2\text{V} \quad V_{icm^-} = -1.25\text{V} \\
&V_{in}(\text{min}) = 1\text{mV} & \\
\end{align*}
\]

Design a two-stage, open-loop comparator using the circuit of Fig. 8.2-3 to the above specifications and assume all channel lengths are to be 1µm.

Solution

Following the procedure outlined in Table 8.2-3, we calculate \( I_6 \) and \( I_7 \) as

\[
I_6 = I_7 = \frac{5 \times 10^{-12} \cdot 4}{50 \times 10^{-9}} = 400\mu\text{A}
\]

Therefore,

\[
\begin{align*}
W_6/L_6 &= \frac{2.400}{(0.5)^2 \cdot 50} = 64 & W_7 &= \frac{2.400}{(0.5)^2 \cdot 110} = 29 \\
\end{align*}
\]

Next, we guess \( C_I = 0.2\text{pF} \). This gives

\[
I_5 = \frac{0.2\text{pF}(4\text{V})}{50\text{ns}} = 16\mu\text{A} \quad \rightarrow \quad I_5 = 20\mu\text{A}
\]

Step 5 gives \( V_{SG3} \) as 1.2V which results in

\[
\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{20}{50(1.2-0.7)^2} = 1.6 \quad \rightarrow \quad \frac{W_3}{L_3} = \frac{W_4}{L_4} = 2
\]

To check the guess for \( C_I \) we need to calculate it which done as

\[
C_I = C_{gd2} + C_{gd4} + C_{gs6} + C_{bd2} + C_{bd4} = 0.9\text{fF} + 0.4\text{fF} + 119.5\text{fF} + 20.4\text{fF} + 15.3\text{fF} = 156.5\text{fF}
\]

which is less than what was guessed.

Finally, the \( W/L \) value of M5 is found by finding \( V_{GS1} \) as 1.00V which gives \( V_{DS5\text{(sat)}} = 0.25\text{V} \). This gives

\[
\frac{W_5}{L_5} = \frac{2.20}{(0.25)^2 \cdot 110} = 5.8 = 6
\]

As in the previous example, M5 and M7 cannot be connected gate-gate and source-source and a scheme like that of Example 8.2-6 must be used. The \( W \) values are summarized below assuming that all channel lengths are 1µm.

\[
\begin{align*}
W_1 &= W_2 = 2\mu\text{m} & W_3 = W_4 = 4\mu\text{m} & W_5 = 6\mu\text{m} & W_6 = 64\mu\text{m} & W_7 = 29\mu\text{m} \\
\end{align*}
\]
SECTION 8.3 - OTHER OPEN-LOOP COMPARATORS

Push-Pull Comparators

Clamped:

![Push-Pull Comparator Diagram](image1)

Comments:
- Gain reduced \(\rightarrow\) Larger input resolution
- Push-pull output \(\rightarrow\) Higher slew rates

Push-Pull Comparators - Improved

Cascode output stage:

![Improved Push-Pull Comparator Diagram](image2)

Comments:
- Can also use the folded cascode architecture
- Cascode output stage result in a slow linear response (dominant pole is small)
- Poorer noise performance
Comparators that Can Drive Large Capacitive Loads

![Comparator Circuit Diagram](image)

Comments:
- Slew rate = 3V/μs into 50pF
- Linear rise/fall time = 100ns into 50pF
- Propagation delay time ≈ 1μs
- Loop gain ≈ 32,000 V/V

Self-Biased Differential Amplifier

![Differential Amplifier Diagram](image)

Advantage:
Large sink or source current with out a large quiescent current.

Disadvantage:
Poor common mode range ($v_{in^+}$ slower than $v_{in^-}$)

---

SECTION 8.4 IMPROVING THE PERFORMANCE OF THE OPEN-LOOP COMPARATORS

Autozeroing Techniques

Use the comparator as an op amp to sample the dc input offset voltage and cancel the offset during operation.

![Model of Comparator, Autozero Cycle, Comparison Cycle]  

Comments:
- The comparator must be stable in the unity-gain mode (self-compensating comparators are good, the two-stage op comparator would require compensation to be switched in during the autozero cycle.)
- Complete offset cancellation is limited by charge injection

---

Differential Implementation of Autozeroed Comparators

![Differential Autozeroed Comparator, Comparator during φ1 phase, Comparator during φ2 phase]  

Fig. 8.4-2
**Single-Ended Autozeroed Comparators**

Noninverting:

![Noninverting Autozeroed Comparator Diagram](#)

Inverting:

![Inverting Autozeroed Comparator Diagram](#)

Comment on autozeroing:

Need to be careful about noise that gets sampled onto the autozeroing capacitor and is present on the comparison phase of the process.

**Influence of Input Noise on the Comparator**

Comparator without hysteresis:

![Comparator Without Hysteresis Diagram](#)

Comparator with hysteresis:

![Comparator With Hysteresis Diagram](#)
Use of Hysteresis for Comparators in a Noisy Environment

Transfer curve of a comparator with hysteresis:

Hysteresis is achieved by the use of positive feedback
- Externally
- Internally

Noninverting Comparator using External Positive Feedback

Circuit:

Upper Trip Point:
Assume that $v_{OUT} = V_{OL}$, the upper trip point occurs when,

$$0 = \left( \frac{R_1}{R_1+R_2} \right) V_{OL} + \left( \frac{R_2}{R_1+R_2} \right) V_{TRP}^+ \quad \Rightarrow \quad V_{TRP}^+ = -\frac{R_1}{R_2} V_{OL}$$

Lower Trip Point:
Assume that $v_{OUT} = V_{OH}$, the lower trip point occurs when,

$$0 = \left( \frac{R_1}{R_1+R_2} \right) V_{OH} + \left( \frac{R_2}{R_1+R_2} \right) V_{TRP}^- \quad \Rightarrow \quad V_{TRP}^- = -\frac{R_1}{R_2} V_{OH}$$

Width of the bistable characteristic:

$$\Delta V_{in} = V_{TRP}^+-V_{TRP}^- = \left( \frac{R_1}{R_2} \right) (V_{OH}-V_{OL})$$
Inverting Comparator using External Positive Feedback

Circuit:

Upper Trip Point:
\[ v_{IN} = V_{TRP^+} = \frac{R_1}{R_1 + R_2} V_{OH} \]

Lower Trip Point:
\[ v_{IN} = V_{TRP^-} = \frac{R_1}{R_1 + R_2} V_{OL} \]

Width of the bistable characteristic:
\[ \Delta V_{in} = V_{TRP^+} - V_{TRP^-} = \frac{R_1}{R_1 + R_2} (V_{OH} - V_{OL}) \]

Horizontal Shifting of the CCW Bistable Characteristic

Circuit:

Upper Trip Point:
\[ V_{REF} = \frac{R_1}{R_1 + R_2} V_{OH} + \frac{R_2}{R_1 + R_2} V_{TRP^+} \rightarrow V_{TRP^+} = \frac{R_1 + R_2}{R_1} V_{REF} \frac{R_1}{R_2} V_{OL} \]

Lower Trip Point:
\[ V_{REF} = \frac{R_1}{R_1 + R_2} V_{OH} + \frac{R_2}{R_1 + R_2} V_{TRP^-} \rightarrow V_{TRP^-} = \frac{R_1 + R_2}{R_1} V_{REF} \frac{R_1}{R_2} V_{OH} \]

Shifting Factor:
\[ \left( \frac{R_1 + R_2}{R_1} \right) V_{REF} \]
**Horizontal Shifting of the CW Bistable Characteristic**

Circuit:

![Circuit Diagram](image)

Upper Trip Point:

\[ v_{IN} = V_{TRP^+} = \left( \frac{R_1}{R_1 + R_2} \right) V_{OH} + \left( \frac{R_1}{R_1 + R_2} \right) V_{REF} \]

Lower Trip Point:

\[ v_{IN} = V_{TRP^-} = \left( \frac{R_1}{R_1 + R_2} \right) V_{OL} + \left( \frac{R_1}{R_1 + R_2} \right) V_{REF} \]

Shifting Factor:

\[ \left( \frac{R_1}{R_1 + R_2} \right) V_{REF} \]

---

**Example 8.4-1 Design of an Inverting Comparator with Hysteresis**

Use the inverting bistable to design a high-gain, open-loop comparator having an upper trip point of 1V and a lower trip point of 0V if \( V_{OH} = 2V \) and \( V_{OL} = -2V \).

**Solution**

Putting the values of this example into the above relationships gives

\[ 1 = \left( \frac{R_1}{R_1 + R_2} \right)^2 + \left( \frac{R_1}{R_1 + R_2} \right) V_{REF} \]

and

\[ 0 = \left( \frac{R_1}{R_1 + R_2} \right)(-2) + \left( \frac{R_1}{R_1 + R_2} \right) V_{REF} \]

Solving these two equations gives \( 3R_1 = R_2 \) and \( V_{REF} = 2V \).
**Hysteresis using Internal Positive Feedback**

Simple comparator with internal positive feedback:

```
VSS
  IBias
    |        |
    |        |
    M3     M6
  vo1    vo2
```

```
v1
  i1
```

```
vi1
  vi2
```

```
M1   M2
```

```
M3   M4
```

```
M6   M7
```

```
M5   M8
```

```
VDD
```

```
Fig. 8.4-11
```

**Internal Positive Feedback - Upper Trip Point**

Assume that the gate of M1 is on ground and the input to M2 is much smaller than zero. The resulting circuit is:

M1 on, M2 off → M3 and M6 on and M4 and M7 off.

∴ \( v_{o2} \) is high.

M6 would like to source the current \( i_6 = \frac{W_6}{L_6} i_1 \)

As \( v_{in} \) begins to increase towards the trip point, the current flow through M2 increases. When \( i_2 = i_6 \), the upper trip point will occur.

\[
\therefore \quad i_5 = i_1 + i_2 = i_3 + i_6 = i_3 + \left( \frac{W_6}{L_6} \right) i_3 = i_3 \left[ 1 + \frac{W_6}{W_3} \right]
\]

which gives

\[
\begin{align*}
i_1 &= i_3 = 1 + \frac{i_5}{\left( \frac{W_6}{L_6} \right) \left( \frac{W_3}{L_3} \right)} \\
i_2 &= i_3 - i_1 = i_5 - i_3
\end{align*}
\]

Also, \( i_2 = i_5 - i_1 = i_5 - i_3 \)

Knowing \( i_1 \) and \( i_2 \) allows the calculation of \( v_{GS1} \) and \( v_{GS2} \) which gives

\[
V_{TRP}^+ = v_{GS2} \cdot v_{GS1} = \sqrt{\frac{2i_2}{B_2}} + V_{T2} \cdot \sqrt{\frac{2i_1}{B_1}} - V_{T1}
\]
**Internal Positive Feedback - Lower Trip Point**

Assume that the gate of M1 is on ground and the input to M2 is much greater than zero. The resulting circuit is:

- M2 on, M1 off
- \( M4 \) and \( M7 \) on and \( M3 \) and \( M6 \) off.

\[ \therefore v_{o1} \text{ is high.} \]

M7 would like to source the current
\[ i_7 = \frac{W_7}{L_7} \cdot i_2 \]

As \( v_{in} \) begins to decrease towards the trip point, the current flow through M1 increases. When
\[ i_1 = i_7, \]

the lower trip point will occur.

\[ \therefore i_5 = i_1 + i_2 = i_7 + i_4 = \left( \frac{W_7}{L_7} \right) i_4 + i_4 = i_4 \left[ 1 + \frac{W_7/L_7}{W_4/L_4} \right] \]

which gives

\[ i_5 = i_4 = 1 + \left[ \frac{(W_7/L_7)}{(W_4/L_4)} \right] \]

Also, \( i_1 = i_5 - i_2 = i_5 - i_4 \)

Knowing \( i_1 \) and \( i_2 \) allows the calculation of \( v_{GS1} \) and \( v_{GS2} \) which gives

\[ V_{TRP} = v_{GS2} - v_{GS1} = \sqrt{2} i_2 \beta_2 + V_{T2} - \sqrt{2} i_1 \beta_1 - V_{T1} \]

---

**Example 8.4-2 - Calculation of Trip Voltages for a Comparator with Hysteresis**

Consider the circuit shown. Using the transistor device parameters given in Table 3.1-2 calculate the positive and negative threshold points if the device lengths are all 1 \( \mu \)m and the widths are given as: \( W_1 = W_2 = W_6 = 10 \mu m \) and \( W_3 = W_4 = 2 \mu m \). The gate of M1 is tied to ground and the input is the gate of M2. The current, \( i_5 = 20 \mu A \). Simulate the results using PSPICE.

**Solution**

To calculate the positive trip point, assume that the input has been negative and is heading positive.

\[ i_6 = \frac{(W/L)_6}{(W/L)_3} i_3 = (5/1) i_3 \]

\[ i_3 = \frac{i_5}{1 + [W/L)_6/(W/L)_3]} = i_1 = \frac{20 \mu A}{1 + 5} = 3.33 \mu A \]

\[ i_2 = 20 - 3.33 = 16.67 \mu A \]

\[ v_{GS1} = \left( \frac{2i_1}{\beta_1} \right)^{1/2} + V_{T1} = \left( \frac{2.333}{510} \right)^{1/2} + 0.7 = 0.81 V \]

\[ v_{GS2} = \left( \frac{2i_2}{\beta_2} \right)^{1/2} + V_{T2} = \left( \frac{2.1667}{510} \right)^{1/2} + 0.7 = 0.946 V \]

\[ V_{TRP+} = v_{GS2} - v_{GS1} = 0.946 - 0.810 = 0.136 V \]
Example 8.4-2 - Continued

Determining the negative trip point, similar analysis yields

\[ i_4 = 3.33 \, \mu A \]
\[ i_1 = 16.67 \, \mu A \]
\[ v_{GS2} = 0.81V \]
\[ v_{GS1} = 0.946V \]
\[ V_{TRP^-} \equiv v_{GS2} - v_{GS1} = 0.81 - 0.946 = -0.136V \]

PSPICE simulation results of this circuit are shown below.

![PSPICE simulation](image-url)

Complete Comparator with Internal Hysteresis

![Complete Comparator](image-url)
**Schmitt Trigger**

The Schmitt trigger is a circuit that has better defined switching points.

Consider the following circuit:

![Circuit Diagram](image)

How does this circuit work?

Assume the input voltage, \( v_{in} \), is low and the output voltage, \( v_{out} \), is high.

\[ \therefore M3, M4 and M5 \text{ are on and } M1, M2 and M6 \text{ are off.} \]

When \( v_{in} \) is increased from zero, M2 starts to turn on causing M3 to start turning off. Positive feedback causes M2 to turn on further and eventually both M1 and M2 are on and the output is at zero.

The upper switching point, \( V_{TRP^+} \) is found as follows:

When \( v_{in} \) is low, the voltage at the source of M2 (M3) is

\[ v_{S2} = VDD - VTN3 \]

\( V_{TRP^+} \) is defined as the point when M2 turns on given as

\[ V_{TRP^+} = VTN2 + v_{S2} \]

\( V_{TRP^+} \) occurs at the point where the input voltage causes the current in M3 to equal the current in M1.

Thus, \( iD1 = \beta1(V_{TRP^+} - V_{TN1})^2 = \beta3(V_{DD} - v_{S2} - VTN3)^2 = iD3 \)

which can be written as, assuming that \( VTN2 = VTN3 \).

\[ \beta1(V_{TRP^+} - V_{TN1})^2 = \beta3(V_{DD} - V_{TRP^+})^2 \Rightarrow V_{TRP^+} = \frac{V_{TN1} + \sqrt{\frac{\beta3}{\beta1}V_{DD}}}{1 + \sqrt{\frac{\beta3}{\beta1}}} \]

**Schmitt Trigger – Continued**

The switching point, \( V_{TRP^-} \) is found in a similar manner and is:

\[ \beta5(V_{DD} - V_{TRP^-} - VTP5)^2 = \beta6( V_{TRP^-} )^2 \Rightarrow V_{TRP^-} = \frac{\sqrt{\frac{\beta5}{\beta6}(V_{DD} - VTP5)}}{1 + \sqrt{\frac{\beta5}{\beta6}}} \]

The bistable characteristic is,
SECTION 8.5 - DISCRETE-TIME COMPARATORS

Switched Capacitor Comparator

\[ V_{1} \quad \phi_{1} \]
\[ V_{2} \quad \phi_{2} \]
\[ + \quad + \quad C \quad \phi_{1} \]
\[ V_{out} \]
\[ + \quad - \quad C_{p} \quad V_{OS} \]
\[ V_{1} \]
\[ V_{2} \]

A switched capacitor comparator

\[ V_{1} \quad \phi_{2} \]
\[ V_{2} \quad V_{OS} \]
\[ + \quad - \quad C_{p} \quad V_{OS} \]
\[ V_{out} \]

Fig. 8.5-1

\[ V_{out} = -A \left[ \frac{V_{2}}{C_{p}} + \frac{V_{1}}{C_{p}} \right] + AV_{OS} \]

\[ = -A \left[ \frac{V_{2}}{C_{p}} + \frac{V_{1}}{C_{p}} \right] + AV_{OS} = -A(V_{1} - V_{2}) \]

\[ C_{p} \]

\[ \phi_{1} \]

Phase:

The \( V_{1} \) input is sampled and the dc input offset voltage is autozeroed.

\[ V_{C}(\phi_{1}) = V_{1} - V_{OS} \quad \text{and} \quad V_{Cp}(\phi_{1}) = V_{OS} \]

\[ \phi_{2} \]

Phase:

\[ V_{out}(\phi_{2}) = -A \left[ \frac{V_{2}C}{C+C_{p}} + \frac{V_{1}C_{p}}{C+C_{p}} \right] + AV_{OS} \]

\[ = -A \left[ \frac{V_{2}}{C+C_{p}} + \frac{V_{1}}{C+C_{p}} \right] + AV_{OS} = -A(V_{1} - V_{2}) \]

if \( C_{p} \) is smaller than \( C \).

---

Differential-In, Differential-Out Switched Capacitor Comparator

\[ V_{in} \quad \phi_{2} \]
\[ \hat{V}_{in} \quad \phi_{1} \]
\[ V_{out} \]

Fig. 8.5-2

Comments:

- Reduces the influence of charge injection
- Eliminates even harmonics
Regenerative Comparators

Regenerative comparators use positive feedback to accomplish the comparison of two signals. Latches have a faster switching speed than the previous bistable comparators.

NMOS and PMOS latch:

![NMOS latch](image1)

![PMOS latch](image2)

Fig. 8.5-3

How is the input applied to a latch?

The inputs are initially applied to the outputs of the latch.

\[ V_{o1}' = \text{initial input applied to } v_{o1} \]

\[ V_{o2}' = \text{initial input applied to } v_{o2} \]

Step Response of a Latch

![Step Response of a Latch](image3)

Fig. 8.5-4

where \( R_i \) and \( C_i \) are the resistance and capacitance seen to ground from the \( i \)-th transistor.

Nodal equations:

\[ g_m v_{o2} + G_1 v_{o1} + s C_1 V_{o1}' \frac{V_{o1}'}{s} = g_m v_{o2} + G_1 v_{o1} + s C_1 V_{o1}' \frac{V_{o1}'}{s} = 0 \]

\[ g_m v_{o1} + G_2 v_{o2} + s C_2 V_{o2}' \frac{V_{o2}'}{s} = g_m v_{o1} + G_2 v_{o2} + s C_2 V_{o2}' \frac{V_{o2}'}{s} = 0 \]

Solving for \( V_{o1} \) and \( V_{o2} \) gives,

\[ V_{o1} = \frac{R_1 C_1}{s R_1 C_1 + 1} V_{o1}' - \frac{g_m R_1}{s R_1 C_1 + 1} V_{o2} = \frac{\tau_1}{s \tau_1 + 1} V_{o1}' - \frac{g_m R_1}{s \tau_1 + 1} V_{o2} \]

\[ V_{o2} = \frac{R_2 C_2}{s R_2 C_2 + 1} V_{o2}' - \frac{g_m R_2}{s R_2 C_2 + 1} V_{o1} = \frac{\tau_2}{s \tau_2 + 1} V_{o2}' - \frac{g_m R_2}{s \tau_2 + 1} V_{o1} \]

Defining the output, \( \Delta V_o \), and input, \( \Delta V_i \), as

\[ \Delta V_o = V_{o2} - V_{o1} \quad \text{and} \quad \Delta V_i = V_{o2}' - V_{o1}' \]
Step Response of the Latch - Continued
Solving for $\Delta V_o$ gives,

$$\Delta V_o = V_{o2} - V_{o1} = \frac{\tau}{\tau+1} \Delta V_i + \frac{g_m R}{\tau+1} \Delta V_o$$

or

$$\Delta V_o = \frac{\tau \Delta V_i}{\tau(1-g_m R)} = \frac{\tau \Delta V_i}{1-g_m R + 1} = \frac{\tau'}{\tau' + 1} \Delta V_i$$

where

$$\tau' = \frac{\tau}{1-g_m R}$$

Taking the inverse Laplace transform gives

$$\Delta v_o(t) = \Delta V_i e^{\tau' \tau} = \Delta V_i e^{\eta(1-g_m R)/\tau} = e^{g_m R \tau' \eta} \Delta V_i$$

if $g_m R >> 1$.

Define the latch time constant as

$$\tau_L = \frac{\tau}{g_m R} = \frac{C}{g_m} = \frac{0.67 W L C_{ox}}{\sqrt{2 K'(W/L)}} = 0.67 C_{ox} \sqrt{\frac{W L^3}{2 K' I}}$$

if $C = C_{gs}$.

.$\Delta V_{out}(t) = e^{\tau_L} \Delta V_i$

Step Response of a Latch - Continued
Normalize the output voltage by $(V_{OH} - V_{OL})$ to get

$$\frac{\Delta V_{out}(t)}{V_{OH} - V_{OL}} = e^{\tau_L} \frac{\Delta V_i}{V_{OH} - V_{OL}}$$

which is plotted as,

![Graph showing normalized output voltage vs time]

The propagation delay time is $t_p = \tau_L ln \left( \frac{V_{OH} - V_{OL}}{2 \Delta V_i} \right)$.
Example 8.5-1 - Time domain characteristics of a latch.

Find the time it takes from the time the latch is enabled until the output voltage, \( \Delta V_{\text{out}} \), equals \( V_{OH} - V_{OL} \) if the \( W/L \) of the latch NMOS transistors is 10µm/1µm and the latch dc current is 10µA when \( \Delta V_i = 0.1(V_{OH} - V_{OL}) \) and \( \Delta V_i = 0.01(V_{OH} - V_{OL}) \). Find the propagation time delay for the latch for each of these conditions.

Solution

The transconductance of the latch transistors is 
\[
g_m = \sqrt{2 \cdot 110 \cdot 10 \cdot 10} = 148\mu S
\]
The output conductance is 0.4µS which gives \( g_m R \) of 59.2V/V. Since \( g_m R \) is greater than 1, we can use the above results. Therefore the latch time constant is found as 
\[
\tau_L = 0.67 C_{ox} W L \frac{1}{\sqrt{2 K T}} = 0.67 (24 \times 10^{-4}) \sqrt{2 \cdot 110 \times 10^{-6} \cdot 10^{-6}} = 108\text{ns}
\]

If we assume that the propagation time delay is the time when the output is 0.5\((V_{OH} - V_{OL})\), then using the above results or Fig. 8.5-5 we find for \( \Delta V_i = 0.01(V_{OH} - V_{OL}) \) that \( \tau_p = 2.3 \tau_L = 174\text{ns} \) and for \( \Delta V_i = 0.1(V_{OH} - V_{OL}) \) that \( \tau_p = 2.306 \tau_L = 249\text{ns} \).

Comparator using a Latch with a Built-In Threshold

How does it operate?
1.) Devices in shaded region operate in the triode region.
2.) When the latch/reset goes high, the upper cross-coupled inverter-latch regenerates. The drain currents of M5 and M6 are steered to obtain a final state determined by the mismatch between the \( R_1 \) and \( R_2 \) resistances.
3.) The input voltage which causes \( R_1 \) and \( R_2 \) to be equal is given by
\[
\frac{1}{R_1} = K_N \left[ \frac{W_1}{L} (v_{in}^+ - V_T) + \frac{W_2}{L} (V_{REF}^- - V_T) \right]
\]
and
\[
\frac{1}{R_2} = K_N \left[ \frac{W_1}{L} (v_{in}^- - V_T) + \frac{W_2}{L} (V_{REF}^+ - V_T) \right]
\]

3.) The input voltage which causes \( R_1 \) and \( R_2 \) to be equal is given by 
\[
v_{in}(\text{threshold}) = \left( \frac{W_2}{W_1} \right) V_{REF}
\]
\( W_2/W_1 = 1/4 \) generates a threshold of \( \pm 0.25V_{REF} \).

Performance → 20Ms/s & 200µW

Simple, Low Power Latched Comparator

Dissipated 50µW when clocked at 2MHz.

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* A. Coban, “1.5V, 1mW, 98-dB Delta-Sigma ADC”, Ph.D. dissertation, School of ECE, Georgia Tech, Atlanta, GA 30332-0250.

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Dynamic Latch

Input offset voltage distribution:

Power dissipation/sampling rate = 4.3µW/Ms/s
**SECTION 8.6 - HIGH-SPEED COMPARATORS**

Conceptual Illustration of a Cascaded Comparator

How does a cascaded, high-speed comparator work?

![Diagram of cascaded comparator](image)

Assuming a small overdrive,

1.) The initial stage builds the driving capability.
2.) The latter stages swing rail-to-rail and build the ability to quickly charge and discharge capacitance.

Minimizing the Propagation Delay Time in Comparators

Fact:
- The input signal is equal to \( V_{in}(\text{min}) \) for worst case
- Amplifiers have a step response with a negative argument in the exponential
- Latches have a step response with a positive argument in the exponential

Result:
Use a cascade of linear amplifiers to quickly build up the signal level and apply this amplified signal level to a latch for quick transition to the full binary output swing.

Illustration of a preamplifier and latch cascade:

![Illustration of preamplifier and latch cascade](image)

Minimization of \( t_p \):

Q. If the preamplifier consists of \( n \) stages of gain \( A \) having a single-pole response, what is the value of \( n \) and \( A \) that gives minimum propagation delay time?

A. \( n = 6 \) and \( A = 2.62 \) but this is a very broad minimum and \( n \) is usually 3 and \( A = 6-7 \) to save area.
**Fully Differential, Three-Stage Amplifier and Latch Comparator**

Circuit:

Comments:
- Autozero and reset phase followed by comparison phase
- More switches are needed to accomplish the reset and autozero of all preamplifiers simultaneously
- Can run as high as 100Msps

**Preamplifier and Latch Circuits**

Gain:

\[ A_v = -\frac{g_{m1}}{g_{m3}} = -\frac{g_{m2}}{g_{m4}} = -\sqrt{\frac{K_N(W_1/L_1)}{K_P(W_2/L_3)}} \]

Dominant Pole:

\[ |p_{dominant}| = \frac{g_{m3}}{C} = \frac{g_{m4}}{C} \]

where \( C \) is the capacitance seen from the output nodes to ground.

If \((W_1/L_1)/(W_2/L_3) = 100\) and the bias current is 100µA, then \( A = -3.85 \) and the bandwidth is 15.9MHz if \( C = 0.5pF \).

Comments:
- If a buffer is used to reduce the output capacitance, one must take into account the loss of the buffer.
- The use of a preamplifier before the latch reduces the latch offset by the gain of the preamplifier so that the offset is due to the preamplifier only.
An Improved Preamplifier

Circuit:

\[ V_{out} = V_{BiasP} \]

\[ M1 \quad M2 \]

\[ M3 \quad M4 \]

\[ M5 \quad M6 \]

\[ M7 \quad M8 \]

\[ M9 \quad M10 \quad M11 \quad M12 \]

\[ V_{BiasN} \]

\[ V_{BiasP} \]

\[ v_{in}^+ \quad v_{in}^- \]

\[ v_{out}^+ \quad v_{out}^- \]

\[ F_B \]

\[ M9 \]

\[ M10 \]

\[ M11 \]

\[ M12 \]

Fig. 8.6-5

Gain:

\[ A_v = -\frac{g_{m1}}{g_{m3}} = -\sqrt{\frac{K_N'(W_1/L_1)I_1}{K_P'(W_3/L_3)I_3}} = -\sqrt{\frac{K_N'(W_1/L_1)}{K_P'(W_3/L_3)}} \sqrt{1+\frac{I_5}{I_3}} \]

If \( I_5 = 24I_3 \), the gain is increased by a factor of 5

Charge Transfer Preamplifier

The preamplifier can be replaced by the charge transfer circuit shown.

\[ v_{in} = V_{REF} \quad v_{out} = V_{PR} \]

\[ C_T \quad S_1 \quad C_O \]

Charge transfer amplifier. Precharge phase. Amplification phase. Fig. 8.6-6

Comments:

- Only positive values of voltage will be amplified.
- Large offset voltages result as a function of the subthreshold current.
A CMOS Charge Transfer Preamplifier

Circuit:

**Fig. 8.6-7**

Comments:
- NMOS and PMOS allow both polarities of input
- CMOS switches along with dummy switches reduce the charge injection
- Switch S3 prevents the subthreshold current influence
- Used as a preamplifier in a comparator with 8-bit resolution at 20Msps and a power dissipation of less than 5µW

A High-Speed Comparator

Circuit:

**Fig. 8.6-8**

Comments:
- Designed to have a $t_p = 10$ns with a 5pF load and a 10mV overdrive
- Not synchronous
- Comparator gain is greater than 2000V/V and the quiescent current was 100µA
SECTION 8.7 - SUMMARY

**Types of Comparators Presented**
- High-gain, open-loop
- Improved high-gain, open-loop, comparators
  - Hysteresis
  - Autozeroing
- Regenerative comparators
- Discrete-time comparators

**Performance Characterization**
- Propagation delay time
- Binary output swing
- Input resolution and/or gain
- Input offset voltage
- Power dissipation

**Important Principles**
- The speed of the comparator depends on the linear and slewing responses
- The dc input offset voltage depends on the matching and can be reduced by autozeroing.
  - Charge injection is the limit of autozeroing
- The gain of the comparator should be large enough for a binary output when $v_{in} = V_{in\text{min}}$
- In cascaded comparators, the early stages should have wide bandwidth and the latter stages high slew rate