CHAPTER 7 - HIGH-PERFORMANCE CMOS OPERATIONAL AMPLIFIERS

Chapter Outline

Goal

To illustrate the degrees of freedom and choices of different circuit architectures that can enhance the performance of a given op amp.

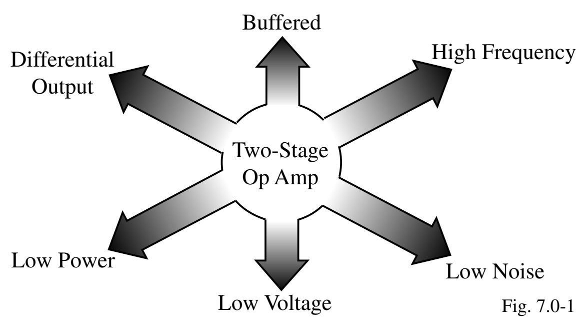


Fig. 7.0-1

SECTION 7.1 - BUFFERED OP AMPS

What is a Buffered Op Amp?

A buffered op amp is an op amp with a low value of output resistance, R_o.

Typically, $10\Omega \leq R_o \leq 1000\Omega$

Requirements

Generally the same as for the output amplifier:

- Low output resistance
- Large output signal swing
- Low distortion
- High efficiency

Types of Buffered Op Amps

- Buffered op amps using MOSFETs
  With and without negative feedback
- Buffered op amps using BJTs

Source-Follower, Push-Pull Output Op Amp

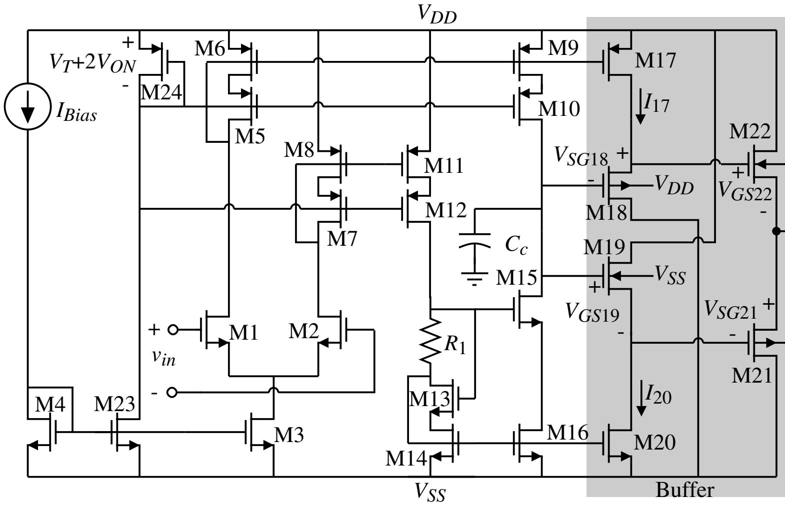


Fig. 7.1-1

$$R_{out} = \frac{1}{g_{m21}+g_{m22}} \le 1000\Omega, \quad A_v(0) = 65\text{dB for } I_{Bias} = 50\mu\text{A, and } GB = 60\text{MHz for } C_L = 1\text{pF}$$

Output bias current?

M18-M19-M21-M22 loop $\Rightarrow V_{SG18}+V_{GS19} = V_{SG21}+V_{GS22}$

which gives $$\sqrt{\frac{2I_{18}}{K_PS_{18}}}+\sqrt{\frac{2I_{19}}{K_NS_{19}}}=\sqrt{\frac{2I_{21}}{K_PS_{21}}}+\sqrt{\frac{2I_{22}}{K_NS_{22}}}$$

Crossover-Inverter, Buffer Stage Op Amp

Principle: If the buffer has high output resistance and voltage gain (common source), this is okay if when loaded by a small R_L the gain of this stage is approximately unity.

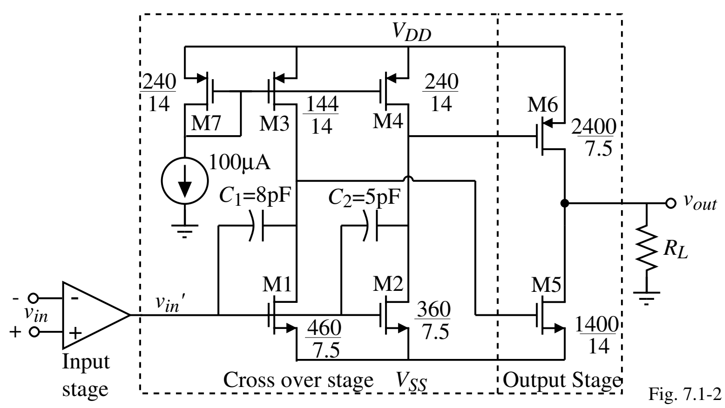


Fig. 7.1-2

This op amp is capable of delivering 160mW to a 100Ω load while only dissipating 7mW of quiescent power!

Crossover-Inverter, Buffer Stage Op Amp - Continued

How does the output buffer work?

The two inverters, M1-M3 and M2-M4 are designed to work over different regions of the buffer input voltage, v_{in}'.

Consider the idealized voltage transfer characteristic of the crossover inverters:

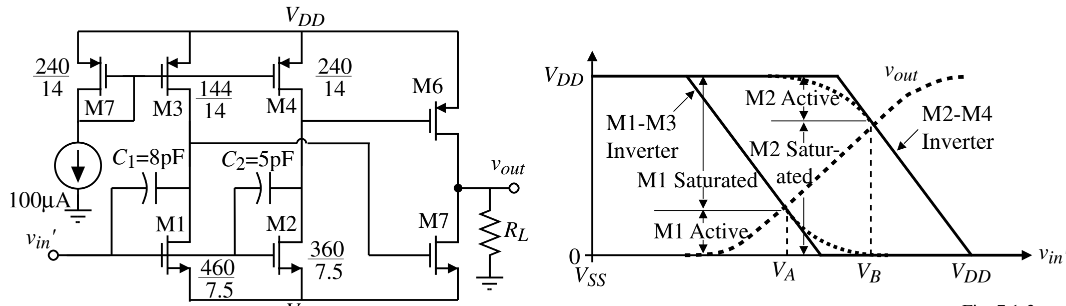


Fig. 7.1-3

Crossover voltage $\equiv V_C = V_B - V_A \geq 0$

V_C is designed to be small and positive for worst case variations in processing

(Maximum value of $V_C \approx$ 110mV)

Crossover-Inverter, Buffer Stage Op Amp - Continued

Performance Results for the Crossover-Inverter, Buffer Stage CMOS Op Amp

Specification	Performance
Supply Voltage	± 6 V
Quiescent Power	7 mW
Output Swing (100Ω Load)	8.1 Vpp
Open-Loop Gain (100Ω Load)	78.1 dB
Unity Gainbandwidth	260kHz
Voltage Spectral Noise Density at 1kHz	1.7 $\mu V/\sqrt{Hz}$
PSRR at 1kHz	55 dB
CMRR at 1kHz	42 dB
Input Offset Voltage (Typical)	10 mV

Compensation of Op Amps with Output Amplifiers

Compensation of a three-stage amplifier:

This op amp introduces a third pole, p'_3 (what about zeros?)

With no compensation,

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{-A_{vo}}{\left(\frac{s}{p'_1} - 1\right)\left(\frac{s}{p'_2} - 1\right)\left(\frac{s}{p'_3} - 1\right)}$$

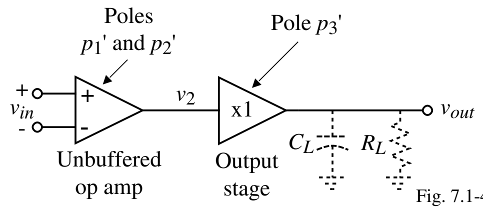
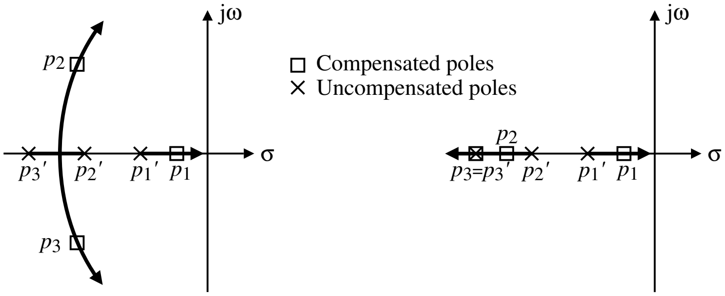


Fig. 7.1-4

Illustration of compensation choices:



Miller compensation applied around both the second and the third stage.

Miller compensation applied around the second stage only.

Fig. 7.1-5

Low Output Resistance Op Amp

To get low output resistance using MOSFETs, negative feedback must be used.

Ideal implementation:

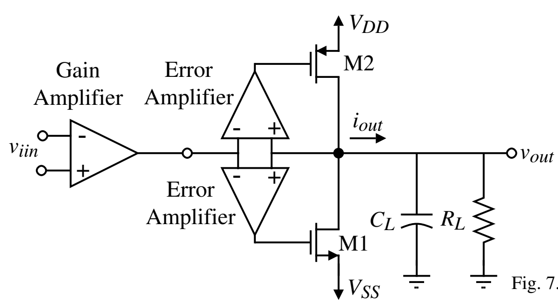


Fig. 7.1-5A

Comments:

- The output resistance will be equal to $r_{ds1}||r_{ds2}$ divided by the loop gain
- If the error amplifiers are not perfectly matched, the bias current in M1 and M2 is not defined

Low Output Resistance Op Amp - Continued

Offset correction circuitry:

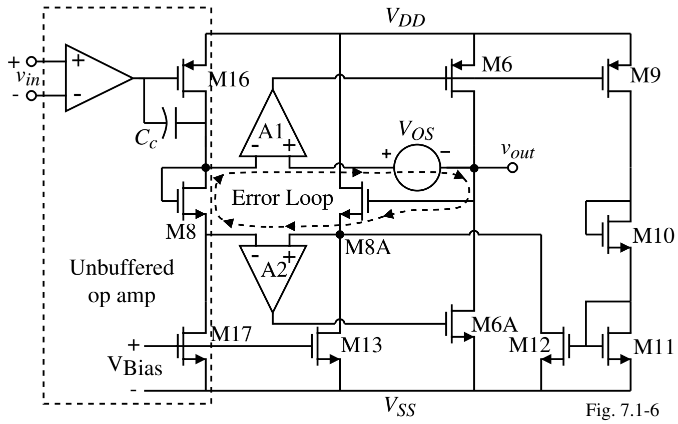


Fig. 7.1-6

The feedback circuitry of the two error amplifiers tries to insure that the voltages in the loop sum to zero. Without the M9-M12 feedback circuit, there is no way to adjust the output for any error in the loop. The circuit works as follows:

When V_{OS} is positive, M6 tries to turn off and so does M6A. I_{M9} reduces thus reducing I_{M12}. A reduction in I_{M12} reduces I_{M8A} thus decreasing V_{GS8A}. V_{GS8A} ideally decreases by an amount equal to V_{OS}. A similar result holds for negative offsets and offsets in EA2.

Low Output Resistance Op Amp - Continued

Error amplifiers:

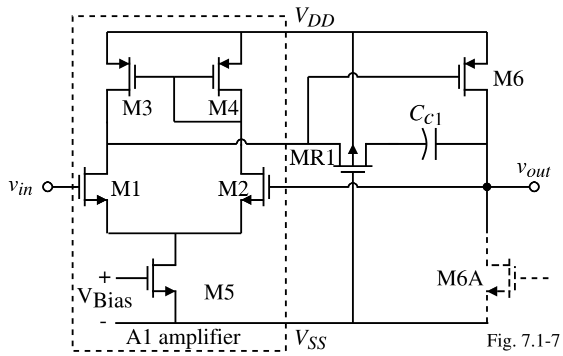


Fig. 7.1-7

Low Output Resistance Op Amp - Complete Schematic

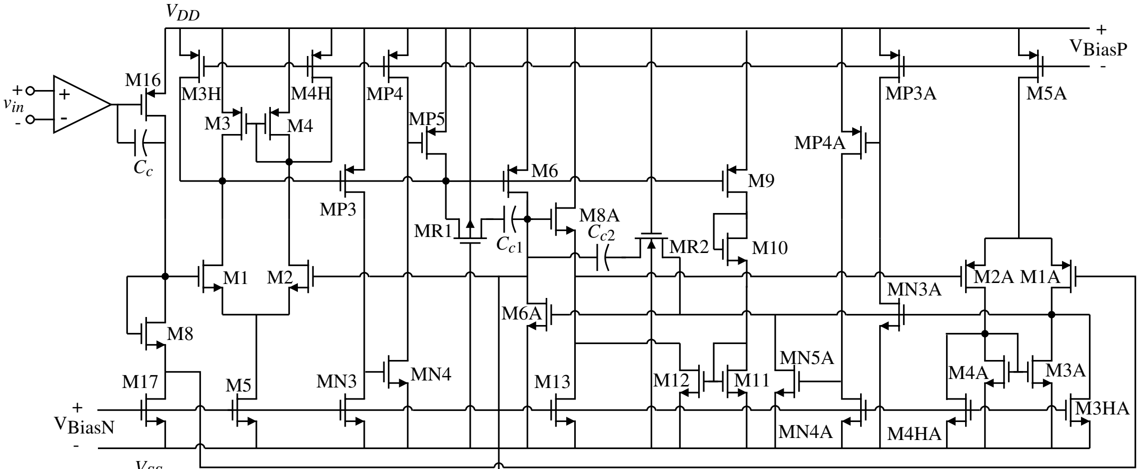


Fig. 7.1-8

Compensation:

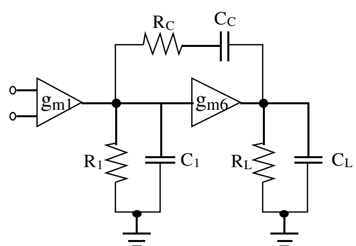
Uses nulling Miller compensation.

Short circuit protection:

MP3-MN3-MN4-MP4-MP5

MN3A-MP3A-MP4A-MN4A-MN5A

(max. output ±60mA)



Low Output Resistance Op Amp - Continued

Table 7.1-2 Performance Characteristics of the Low Output Resistance Op Amp:

Specification	Simulated Results	Measured Results
Power Dissipation	7.0 mW	5.0 mW
Open Loop Voltage Gain	82 dB	83 dB
Unity Gainbandwidth	500kHz	420 kHz
Input Offset Voltage	0.4 mV	1 mV
PSRR+(0)/PSRR-(0)	85 dB/104 dB	86 dB/106 dB
PSRR+(1kHz)/PSRR-(1kHz)	81 dB/98 dB	80 dB/98 dB
THD (V_{in} = 3.3V_{pp})		
R_L = 300Ω	0.03%	0.13%(1 kHz)
C_L = 1000pF	0.08%	0.32%(4 kHz)
THD (V_{in} = 4.0V_{pp})		
R_L = 15KΩ	0.05%	0.13%(1 kHz)
C_L = 200pF	0.16%	0.20%(4 kHz)
Settling Time (0.1%)	3 μs	<5 μs
Slew Rate	0.8 V/μs	0.6 V/μs
1/f Noise at 1kHz	-	130 nV/$\sqrt{\text{Hz}}$
Broadband Noise	-	49 nV/$\sqrt{\text{Hz}}$

$$R_{out} \approx \frac{r_{ds6}||r_{ds6A}}{\text{Loop Gain}} \approx \frac{50\text{k}\Omega}{5000} = 10\Omega$$

Low-Output Resistance Op Amp - Continued

Component sizes for the low-resistance op amp:

Transistor/Capacitor	μm/μm or pF	Transistor/Capacitor	μm/μm or pF
M16	184/9	M8A	481/6
M17	66/12	M13	66/12
M8	184/6	M9	27/6
M1, M2	36/10	M10	6/22
M3, M4	194/6	M11	14/6
M3H, M4H	16/12	M12	140/6
M5	145/12	MP3	8/6
M6	2647/6	MN3	244/6
MRC	48/10	MP4	43/12
C_C	11.0	MN4	12/6
M1A, M2A	88/12	MP5	6/6
M3A, M4A	196/6	MN3A	6/6
M3HA, M4HA	10/12	MP3A	337/6
M5A	229/12	MN4A	24/12
M6A	2420/6	MP4A	20/12
C_F	10.0	MN5A	6/6

Simpler Implementation of Negative Feedback to Achieve Low Output Resistance

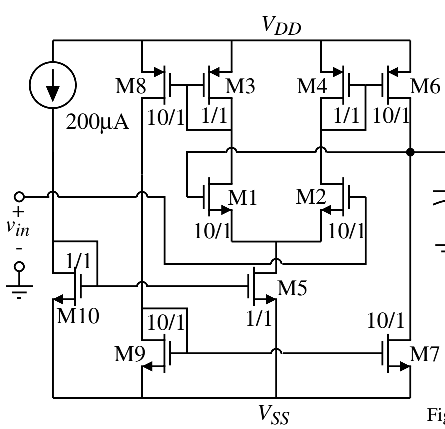


Fig. 7.1-9

Output Resistance:

$$R_{out} = \frac{R_o}{1+LG}$$

where

$$R_o = \frac{1}{g_{ds6}+g_{ds7}}$$

and

$$|LG| = \frac{g_{m2}}{2g_{m4}}(g_{m6}+g_{m7})R_o$$

Therefore, the output resistance is

$$R_{out} = \frac{1}{(g_{ds6}+g_{ds7})\left[1 + \left(\frac{g_{m2}}{2g_{m4}}\right)(g_{m6}+g_{m8})R_o\right]} .$$

Example 7.1-1 - Low Output Resistance Using the Simple Shunt Negative Feedback Buffer

Find the output resistance of above op amp using the model parameters of Table 3.1-2.

Solution

The current flowing in the output transistors, M6 and M7, is 1mA which gives R_o of

$$R_o = \frac{1}{(\lambda_N+\lambda_P)1\text{mA}} = \frac{1000}{0.09} = 11.11\text{k}\Omega$$

To calculate the loop gain, we find that

$$g_{m2} = \sqrt{2K_N'\cdot 10\cdot 100\mu\text{A}} = 469\mu\text{S}$$

$$g_{m4} = \sqrt{2K_P'\cdot 1\cdot 100\mu\text{A}} = 100\mu\text{S}$$

and

$$g_{m6} = \sqrt{2K_P'\cdot 10\cdot 1000\mu\text{A}} = 1\text{mS}$$

Therefore, the loop gain is

$$|LG| = \frac{469}{100}\ 2\cdot 11.11 = 104.2$$

Solving for the output resistance, R_{out}, gives

$$R_{out} = \frac{11.11\text{k}\Omega}{1 + 104.2} = 106\Omega \text{ (Assumes that } R_L \text{ is large)}$$

BJTs Available in CMOS Technology

Illustration of an NPN substrate BJT available in a p-well CMOS technology:

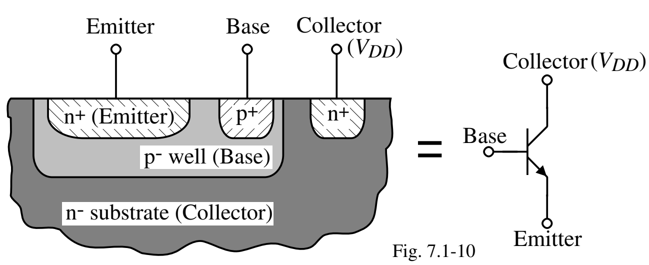


Fig. 7.1-10

Comments:

- g_m of the BJT is larger than the FET so that the output resistance w/o feedback is lower
- Can use the lateral or substrate BJT but since the collector is on ac ground, the substrate BJT is preferred
- Current is required to drive the BJT

Two-Stage Op Amp with a Class-A BJT Output Buffer Stage

Purpose of the M8-M9 source follower:

1.) Reduce the output resistance (includes whatever is seen from the base to ground divided by $1+\beta_F$)

2.) Reduces the output load at the drains of M6 and M7

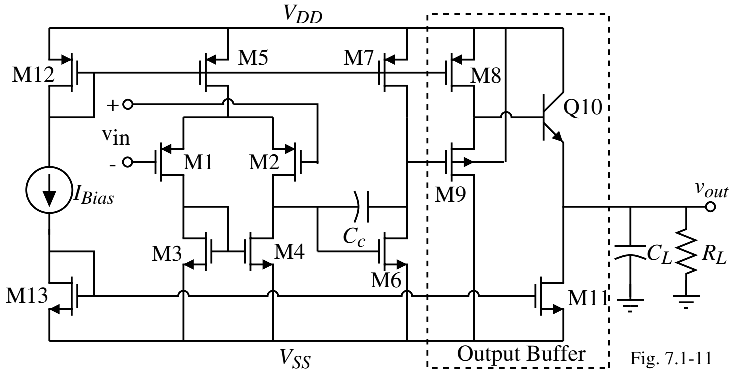


Fig. 7.1-11

Small-signal output resistance :

$$R_{out} \approx \frac{r_{\pi 10} + (1/g_{m9})}{1+\beta_F} = \frac{1}{g_{m10}} + \frac{1}{g_{m9}(1+\beta_F)}$$

$= 51.6\Omega + 6.7\Omega = 58.3\Omega$ where $I_{10} = 500\mu A$, $I_8 = 100\mu A$, $W_9/L_9 = 100$ and β_F is 100

Maximum output voltage:

$$v_{OUT}(\max) = V_{DD} - V_{SD8}(\text{sat}) - v_{BE10} = V_{DD} - \sqrt{\frac{2K_P'}{I_8(W_8/L_8)}} - V_t \ln\left(\frac{I_{c10}}{I_{s10}}\right)$$

Voltage gain:

$$\frac{v_{out}}{v_{in}} = \left(\frac{g_{m1}}{g_{ds2}+g_{ds4}}\right)\left(\frac{g_{m6}}{g_{ds6}+g_{ds7}}\right)\left(\frac{g_{m9}}{g_{m9}+g_{mbs9}+g_{ds8}+g_{\pi 10}}\right)\left(\frac{g_{m10}R_L}{1+g_{m10}R_L}\right)$$

Compensation will be more complex because of the additional stages.

Example 7.1-2 - Designing the Class-A, Buffered Op Amp

Use the parameters of Table 3.1-2 along with the BJT parameters of $I_s = 10^{-14}$A and $\beta_F = 100$ to design the class-A, buffered op amp to give the following specifications. Assume the channel length is to be 1µm.

$V_{DD} = 2.5$V	$V_{SS} = -2.5$V	$A_{vd}(0) \geq 5000$V/V
Slew rate ≥ 10V/µs	GB = 5MHz	$ICMR = -1$V to 2V
$R_{out} \leq 100\Omega$	$C_L = 100$pF	$R_L = 500\Omega$

Solution

Because the specifications above are similar to the two-stage design of Ex. 6.3-1, we can use these results for the first two stages of our design. However, we must convert the results of Ex. 6.3-1 to a PMOS input stage. The results of doing this give $W_1/L_1 = W_2/L_2 = 6\mu m/1\mu m$, $W_3/L_3 = W_4/L_4 = 7\mu m/1\mu m$, $W_5/L_5 = 11\mu m/1\mu m$, $W_6/L_6 = 43\mu m/1\mu m$, and $W_7/L_7 = 34\mu m/1\mu m$

The design of the two followers is next.

BJT follower:

$SR = 10$V/µs and 100pF capacitor give $I_{11} = 1$mA.

∴ If $W_{13} = 44\mu m$, then $W_{11} = 44\mu m(1000\mu A/30\mu A) = 1467\mu m$.

$I_{11} = 1$mA ⇒ $1/g_{m10} = 0.0258V/1mA = 25.8\Omega$

MOS follower:

To source 1mA, the BJT must provide 2mA which requires 20µA from the MOS follower stage.

Therefore, select a bias current of 100µA for M8.

If $W_{12} = 44\mu m$, then $W_8 = 44\mu m(100\mu A/30\mu A) = 146\mu m$.

Example 7.1-2 - Continued

If $1/g_{m10}$ is 25.8Ω, then design g_{m9} as

$$g_{m9} = \frac{1}{\left(R_{out} - \frac{1}{g_{m10}}\right)(1+\beta_F)} = \frac{1}{(100\text{-}25.8)(101)} = 133.4\mu S \qquad g_{m9} \text{ and } I_9 \Rightarrow W/L = 0.809.$$

Let us select W/L = 10 for M9 in order to make sure that the contribution of M9 to the output resistance is sufficiently small and to increase the gain closer to unity. This gives a transconductance of M9 of 469μS.

To calculate the voltage gain of the MOS follower we need to find g_{mbs9}. This value is given as

$$g_{mbs9} = \frac{g_{m9}\gamma_N}{2\sqrt{2\phi_F + V_{BS9}}} = \frac{469\cdot 0.4}{2\sqrt{0.7+2}} = 57.1\mu S$$

where we have assumed that the value of V_{SB9} is approximately 2V.

$$\therefore \qquad A_{MOS} = \frac{469\mu S}{469\mu S+57.1\mu S+4\mu S+5\mu S} = 0.8765 \text{ V/V}.$$

The voltage gain of the BJT follower is

$$A_{BJT} = \frac{500}{25.8+500} = 0.951 \text{ V/V}$$

Thus, the gain of the op amp is

$$A_{vd}(0) = (7777)(0.8765)(0.951) = 6483 \text{ V/V}$$

which meets the specification. The power dissipation of this amplifier is given as

$$P_{diss.} = 5V(30\mu A+30\mu A+95\mu A+100\mu A+1000\mu A) = 6.27mW$$

Two-Stage Op Amp with a Class-AB BJT Output Buffer Stage

This amplifier can reduce the quiescent power dissipation.

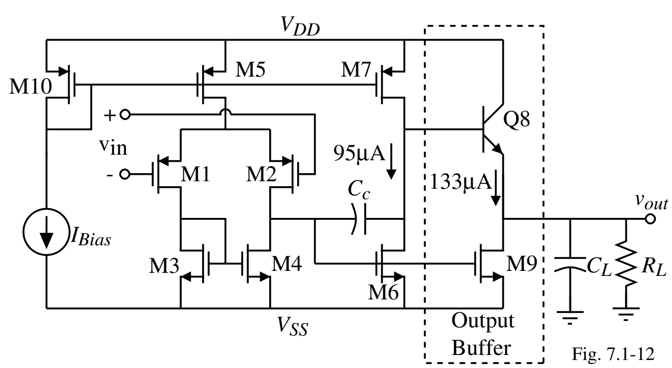


Fig. 7.1-12

Slew Rate:

$$SR^+ = \frac{I_{OUT}^+}{C_L} = \frac{(1+\beta_F)I_7}{C_L} \qquad \text{and} \qquad SR^- = \frac{\beta_9(V_{DD} - 1V + |V_{SS}| - V_{T0})^2}{2C_L}$$

If β_F = 100, C_L = 1000pF and I_7 = 95μA then SR^+ = 8.59V/μs.

Assuming a W_9/L_9 = 60 (I_9 = 133μA), ±2.5V power supplies and C_L = 1000pF gives SR^- = 35.9V/μs.

(The current is not limited by I_7 as it is for the positive slew rate.)

Two-Stage Op Amp with a Class-AB BJT Output Buffer Stage

Small-signal characteristics:

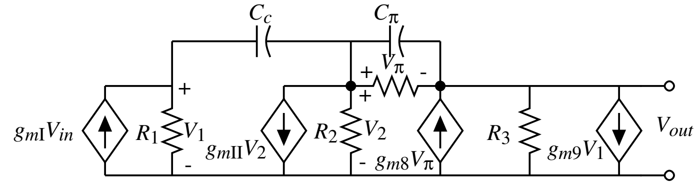


Fig. 7.1-13

Nodal equations:

$$g_{mI}V_{\rm in} = (G_I + sC_c)V_1 - sC_cV_2 + 0V_{out}$$

$$0 = (g_{mII} - sC_c)V_1 + (G_{II} + g_\pi + sC_c + sC_\pi)V_2 - (g_\pi + sC_\pi)V_{out}$$

$$0 \cong g_{m9}V_1 - (g_{m13} + sC_\pi)V_2 + (g_{m13} + sC_\pi)V_{out} \qquad \text{where } g_\pi > G_3$$

The approximate voltage transfer function is:

$$\frac{V_9(s)}{V_{\rm in}(s)} \approx A_{v0}\frac{\left(\frac{s}{z_1}-1\right)\left(\frac{s}{z_2}-1\right)}{\left(\frac{s}{p_1}-1\right)\left(\frac{s}{p_2}-1\right)}$$

where

$$A_{v0} = \frac{-g_{mI}g_{mII}}{G_IG_{II}} \qquad z_1 = \frac{1}{\frac{C_c}{g_{mII}} - \frac{C_\pi}{g_{m13}}\left[1+\frac{g_{m9}}{g_{mII}}\right]} \qquad z_2 = -\frac{g_{m13}}{C_\pi} + \frac{g_{mII}}{C_c}\left[1+\frac{g_{m9}}{g_{mII}}\right]$$

$$p_1 = \frac{-G_IG_{II}}{g_{mII}C_c}\left[\frac{1}{1+\frac{g_{m9}}{\beta_F g_{mII}} + \frac{C_\pi}{C_c}\left(\frac{G_IG_{II}}{g_{m13}g_{mII}}\right)}\right] \qquad p_2 \cong \frac{-g_{m13}g_{mII}}{(g_{mII}+g_{m9})C_\pi}$$

Two-Stage Op Amp with a Class-AB BJT Output Buffer Stage - Continued

Output stage current, I_{C8}:

$$I_{C8} = I_{D9} = \frac{S_9}{S_6}I_{D6} = \frac{60}{43}95\mu A = 133\mu A$$

Small-signal output resistance:

$$r_{\rm out} = \frac{r_\pi + R_{II}}{1+\beta_F} = \frac{19.668{\rm k}\Omega + 116.96{\rm k}\Omega}{101} = 1353\Omega$$

if $I_6 = I_7 = 95\mu A$, and $\beta_F = 100$.

Loading effect of R_L on the voltage transfer curve (increasing W_9/L_9 will improve the negative part at the cost of power dissipation):

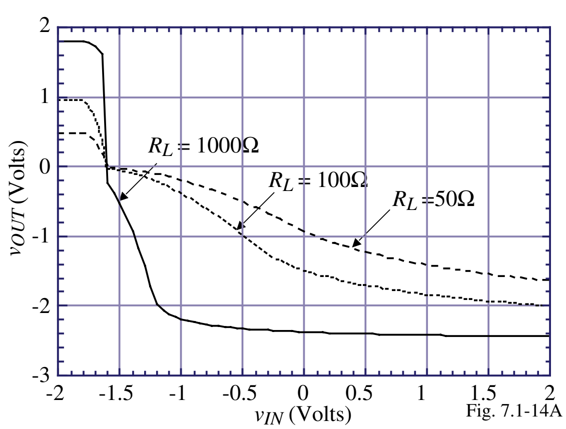


Fig. 7.1-14A

Example 7.1-3 - Performance of the Two-Stage, Class AB Output Buffer

Using the transistor currents given above for the output stages (output stage of the two-stage op amp and the buffer stage), find the small-signal output resistance and the maximum output voltage when R_L = 50Ω. Use the W/L values of Example 7.1-2 and assume that the NPN BJT has the parameters of β_F = 100 and I_S = 10fA.

Solution

It was shown on the previous slide that the small-signal output resistance is

$$r_{out} = \frac{r_\pi + r_{ds6}||r_{ds7}}{1+\beta_F} = \frac{19.668\text{k}\Omega + 116.96\text{k}\Omega}{101} = 1353\Omega$$

Obviously, the MOS buffer of Fig. 7.1-11 would decrease this value.

The maximum output voltage given previously is only valid if the load current is small. If this is not the case, then a better approach is to assume that all of the current in M7 becomes base current for Q8. This base current is multiplied by $1+\beta_F$ to give the sourcing current. If M9 is off, then all this current flows through the load resistor to give an output voltage of

$$v_{OUT}(\max) \approx (1+\beta_F)I_7R_L$$

If the value of v_{OUT}(max) is close to V_{DD}, then the source-drain voltage across M7 may be too small to be in saturation causing I_7 to decrease. Using the above equation, we calculate v_{OUT}(max) as (101)·95µA·50Ω or 0.48V which is close to the simulation results shown using the parameters of Table 3.1-2.

SECTION 7.2 - HIGH-SPEED/FREQUENCY OP AMPS

Objective

Explore op amps having high frequency response and/or high slew rate

Approaches

1.) Extending the GB of conventional op amps
2.) Switched op amps
3.) Current feedback op amps
4.) Parallel path op amps

What is the Influence of *GB* on the Frequency Response?

The op amp is primarily designed to be used with negative feedback. When the product of the op amp gain and feedback gain (loss) is not greater than unity, negative feedback does not work satisfactorily.

Example of a gain of -10 voltage amplifier:

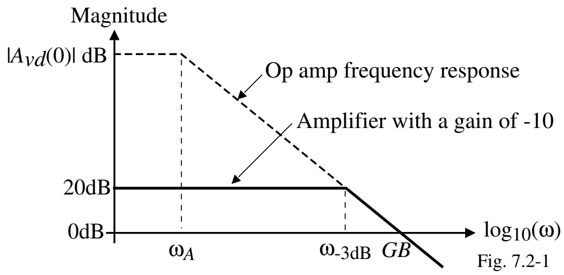


Fig. 7.2-1

What causes the *GB*?

We know that

$$GB = \frac{g_m}{C}$$

where g_m is the transconductance that converts the input voltage to current and C is the capacitor that causes the dominant pole.

This relationship assumes that all higher-order poles are greater than *GB*.

What is the Limit of *GB*?

The following illustrates what happens when the next higher pole is not greater than *GB*:

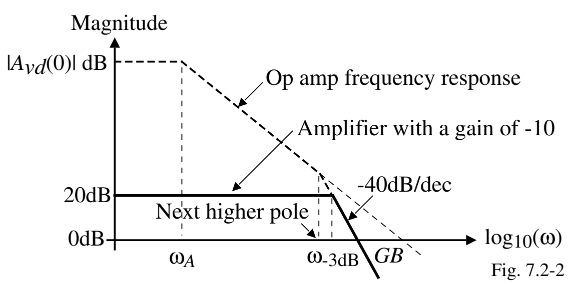


Fig. 7.2-2

For a two-stage op amp, the poles and zeros are:

1.) Dominant pole $\quad p_1 = \dfrac{-g_{m1}}{A_v(0)C_c}$

2.) Output pole $\quad p_2 = \dfrac{-g_{m6}}{C_L}$

3.) Mirror pole $\quad p_3 = \dfrac{-g_{m3}}{C_{gs3}+C_{gs4}}$

4.) Nulling pole $\quad p_4 = \dfrac{-1}{R_z C_I}$

5.) Nulling zero $\quad z_1 = \dfrac{-1}{R_z C_c-(C_c/g_{m6})}$

A Procedure to Increase the *GB* of a Two-Stage Op Amp

1.) Use the nulling zero to cancel the closest pole beyond the dominant pole.

2.) The maximum *GB* would be equal to the magnitude of the second closest pole beyond the dominant pole.

3.) Adjust the dominant pole so that $GB \approx 2.2$x(second closest pole beyond the dominant pole)

Illustration which assumes that p_2 is the next closest pole beyond the dominant pole:

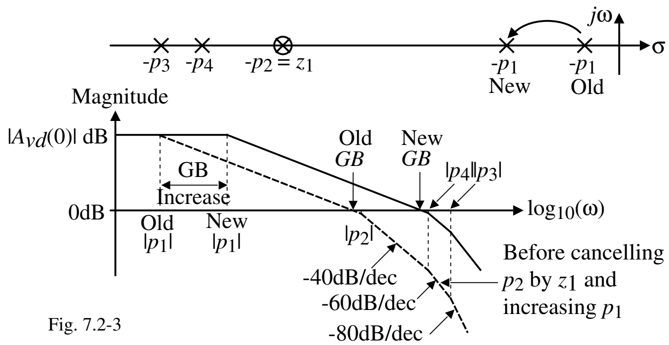


Fig. 7.2-3

Example 7.2-1 - Increasing the *GB* of the Two-Stage Op Amp Designed in Ex. 6.3-1

Use the two-stage op amp designed in Example 6.3-1 and apply the above approach to increase the gainbandwidth as much as possible.

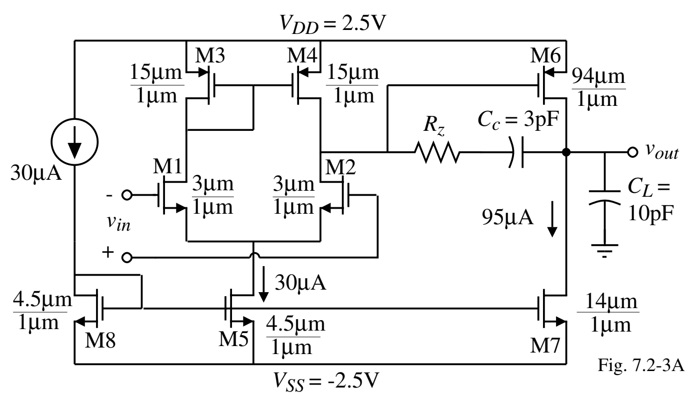


Fig. 7.2-3A

Solution

1.) We must first find the values of p_2, p_3, and p_4.

(a.) From Ex. 6.3-2, we see that $p_2 = -94.25\text{x}10^6$ rads/sec.

(b.) p_3 was found in Ex. 6.3-1 as $-2.81\text{x}10^9$ rads/sec.

(c.) To find p_4, we must find C_I which is the output capacitance of the first stage of the op amp. C_I consists of the following capacitors,

$$C_I = C_{bd2} + C_{bd4} + C_{gs6} + C_{gd2} + C_{gd4}$$

For C_{bd2} the width is 3µm $\Rightarrow$ L1+L2+L3 = 3µm $\Rightarrow$ AS/AD=9µm^2 and PS/PD = 12µm.

For C_{bd4} the width is 15µm $\Rightarrow$ L1+L2+L3 = 3µm $\Rightarrow$ AS/AD=45µm^2 and PS/PD = 36µm.

From Table 3.2-1:

$$C_{bd2} = (9\mu\text{m}^2)(770\text{x}10^{-6}\text{F/m}^2) + (12\mu\text{m})(380\text{x}10^{-12}\text{F/m}) = 6.93\text{fF}+4.56\text{fF} = 11.5\text{fF}$$

and

$$C_{bd4} = (45\mu\text{m}^2)(560\text{x}10^{-6}\text{F/m}^2) + (36\mu\text{m})(350\text{x}10^{-12}\text{F/m}) = 25.2\text{fF}+12.6\text{F} \approx 37.8\text{fF}$$

Example 7.2-1 - Continued

C_{gs6} is given by Eq. (10b) of Sec. 3.2 and is

$$C_{gs6} = CGDO\text{x}W_6 + 0.67(C_{ox}\cdot W_6\cdot L_6) = (220\text{x}10^{-12})(94\text{x}10^{-6}) + (0.67)(24.7\text{x}10^{-4})(94\text{x}10^{-12})$$

$$= 20.7\text{fF} + 154.8\text{fF} = 175.5\text{fF}$$

$$C_{gd2} = 220\text{x}10^{-12}\text{x}3\mu\text{m} = 0.66\text{fF} \quad \text{and} \quad C_{gd4} = 220\text{x}10^{-12}\text{x}15\mu\text{m} = 3.3\text{fF}$$

Therefore, C_I = 11.5fF + 37.8fF + 175.5fF + 0.66fF + 3.3fF = 228.8fF. Although C_{bd2} and C_{bd4} will be reduced with a reverse bias, let us use these values to provide a margin. In fact, we probably ought to double the whole capacitance to make sure that other layout parasitics are included. Thus let C_I be 300fF.

In Ex. 6.3-2, R_z was 4.591kΩ which gives p_4 = - 0.726x10^9 rads/sec.

2.) Using the nulling zero, z_1, to cancel p_2, gives p_4 as the next smallest pole.

For 60° phase margin $GB = |p_4|/2.2$ if the next smallest pole is more than 10GB (which is approximately true).

$$\therefore \quad GB = 0.726\text{x}10^9/2.2 = 0.330\text{x}10^9 \text{ rads/sec. or } 52.5\text{MHz.}$$

The compensating capacitor or g_{m1} (g_{m2}) is designed from the relationship that $GB = g_{m1}/C_c$ to give this value of GB. Assuming g_{m1} is constant, then $C_c = g_{m1}/GB = (94.25\text{x}10^{-6})/(0.330\text{x}10^9)$ = 286fF. It might be useful to increase g_{m1} in order to increase C_c above the surrounding parasitic capacitors. However, let us assume that this value of C_c is suitable (C_{gd6} = 20.7fF). Therefore the new GB is 52.5MHz. We have increased the GB from Example 6.3-1 by a factor of 10.5 times. The success of this method assumes that there are no other roots with a magnitude smaller than 10GB.

Example 7.2-2 - Increasing the *GB* of the Folded Cascode Op Amp of Ex. 6.5-3

Use the folded-cascode op amp designed in Example 6.5-3 and apply the above approach to increase the gainbandwidth as much as possible. Assume that the drain/source areas are equal to 2μm times the width of the transistor and that all voltage dependent capacitors are at zero voltage.

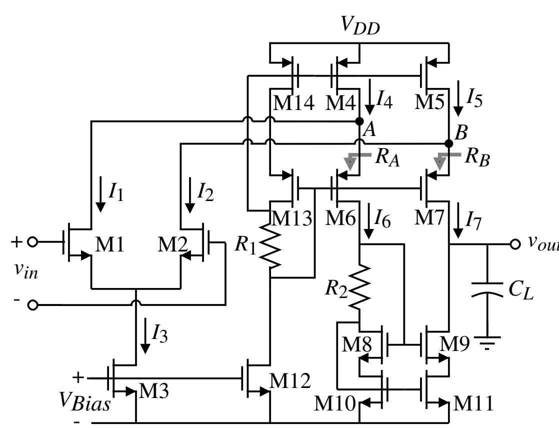


Fig. 6.5-7

Solution

The poles of the folded cascode op amp are:

$p_A \approx \dfrac{-1}{R_A C_A}$ (the pole at the source of M6)

$p_B \approx \dfrac{-1}{R_B C_B}$ (the pole at the source of M7)

$p_6 \approx \dfrac{-1}{(R_2+1/g_{m10})C_6}$ (the pole at the drain of M6)

$p_8 \approx \dfrac{-1}{C_8(r_{ds2}||r_{ds4}||r_{ds10})}$ (the pole at the source of M8)

$p_9 \approx \dfrac{-g_{m9}}{C_9}$ (the pole at the source of M9)

and

$p_{10} \approx \dfrac{-g_{m10}}{C_{10}}$ (the pole at the gates of M10 and M11)

Let us evaluate each of these poles.

1,) For p_A, the resistance R_A is approximately equal to g_{m6} and C_A is given as

$$C_A = C_{gs6} + C_{bd1} + C_{gd1} + C_{bd4} + C_{bs6} + C_{gd4}$$

Example 7.2-2 - Continued

From Ex. 6.5-3, g_{m6} = 744.6µS and capacitors giving C_A are found using the parameters of Table 3.2-1 as,

$$C_{gs6} = (220\text{x}10^{-12}\cdot 80\text{x}10^{-6}) + (0.67)(80\text{x}10^{-6}\cdot 10^{-6}\cdot 24.7\text{x}10^{-4}) = 149\text{fF}$$

$$C_{bd1} = (770\text{x}10^{-6})(35.9\text{x}10^{-6}\cdot 2\text{x}10^{-6}) + (380\text{x}10^{-12})(2\cdot 37.9\text{x}10^{-6}) = 84\text{fF}$$

$$C_{gd1} = (220\text{x}10^{-12}\cdot 35.9\text{x}10^{-6}) = 8\text{fF}$$

$$C_{bd4} = C_{bs6} = (560\text{x}10^{-6})(80\text{x}10^{-6}\cdot 2\text{x}10^{-6}) + (350\text{x}10^{-12})(2\cdot 82\text{x}10^{-6}) = 147\text{fF}$$

and

$$C_{gd4} = (220\text{x}10^{-12})(80\text{x}10^{-6}) = 17.6\text{fF}$$

Therefore,

$$C_A = 149\text{fF} + 84\text{fF} + 8\text{fF} + 147\text{fF} + 17.6\text{fF} + 147\text{fF} = 0.553\text{pF}$$

Thus,

$$p_A = \frac{-744.6\text{x}10^{-6}}{0.553\text{x}10^{-12}} = -1.346\text{x}10^{9}\ \text{rads/sec.}$$

2.) For the pole, p_B, the capacitance connected to this node is

$$C_B = C_{gd2} + C_{bd2} + C_{gs7} + C_{gd5} + C_{bd5}$$

The various capacitors above are found as

$$C_{gd2} = (220\text{x}10^{-12}\cdot 35.9\text{x}10^{-6}) = 8\text{fF}$$

$$C_{bd2} = (770\text{x}10^{-6})(35.9\text{x}10^{-6}\cdot 2\text{x}10^{-6}) + (380\text{x}10^{-12})(2\cdot 37.9\text{x}10^{-6}) = 84\text{fF}$$

$$C_{gs7} = (220\text{x}10^{-12}\cdot 80\text{x}10^{-6}) + (0.67)(80\text{x}10^{-6}\cdot 10^{-6}\cdot 24.7\text{x}10^{-4}) = 149\text{fF}$$

$$C_{gd5} = (220\text{x}10^{-12})(80\text{x}10^{-6}) = 17.6\text{fF}$$

and

$$C_{bd5} = (560\text{x}10^{-6})(80\text{x}10^{-6}\cdot 2\text{x}10^{-6}) + (350\text{x}10^{-12})(2\cdot 82\text{x}10^{-6}) = 147\text{fF}$$

Example 7.2-2 - Continued

The value of C_B is the same as C_A and g_{m6} is assumed to be the same as g_{m7} giving $p_B = p_A = -1.346\text{x}10^9$ rads/sec.

3.) For the pole, p_6, the capacitance connected to this node is

$$C_6 = C_{bd6} + C_{gd6} + C_{gs8} + C_{gs9}$$

The various capacitors above are found as

$$C_{bd6} = (560\text{x}10^{-6})(80\text{x}10^{-6}\cdot 2\text{x}10^{-6}) + (350\text{x}10^{-12})(2\cdot 82\text{x}10^{-6}) = 147\text{fF}$$

$$C_{gs8} = (220\text{x}10^{-12}\cdot 36.4\text{x}10^{-6}) + (0.67)(36.4\text{x}10^{-6}\cdot 10^{-6}\cdot 24.7\text{x}10^{-4}) = 67.9\text{fF}$$

and

$$C_{gs9} = C_{gs8} = 67.9\text{fF} \qquad C_{gd6} = C_{gd5} = 17.6\text{fF}$$

Therefore,

$$C_6 = 147\text{fF} + 17.6\text{fF} + 67.9\text{fF} + 67.9\text{fF} = 0.300\text{pF}$$

From Ex. 6.5-3, R_2 = 2kΩ and $g_{m6} = 744.6\text{x}10^{-6}$. Therefore, p_6, can be expressed as

$$-p_6 = \frac{1}{\left(2\text{x}10^3 + \frac{10^6}{744.6}\right)0.300\text{x}10^{-12}} = 0.966\text{x}10^{9}\ \text{rads/sec.}$$

4.) Next, we consider the pole, p_8. The capacitance connected to this node is

$$C_8 = C_{bd10} + C_{gd10} + C_{gs8} + C_{bs8}$$

These capacitors are given as,

$$C_{bs8} = C_{bd10} = (770\text{x}10^{-6})(36.4\text{x}10^{-6}\cdot 2\text{x}10^{-6}) + (380\text{x}10^{-12})(2\cdot 38.4\text{x}10^{-6}) = 85.2\text{fF}$$

$$C_{gs8} = (220\text{x}10^{-12}\cdot 36.4\text{x}10^{-6}) + (0.67)(36.4\text{x}10^{-6}\cdot 10^{-6}\cdot 24.7\text{x}10^{-4}) = 67.9\text{fF}$$

and

$$C_{gd10} = (220\text{x}10^{-12})(36.4\text{x}10^{-6}) = 8\text{fF}$$

Example 7.2-2 - Continued

The capacitance C_8 is equal to

$$C_8 = 67.9\text{fF} + 8\text{fF} + 85.2\text{fF} + 85.2\text{fF} = 0.246\text{pF}$$

Using the value of $gm8$ found in Ex. 6.5-3 of 774.6µS, the pole p_8 is found as, $-p_8 = 3.149\times10^9$ rads/sec.

5.) The capacitance for the pole at p_9 is identical with C_8. Therefore, since g_{m9} is also 774.6µS, the pole p_9 is equal to p_8 and found to be $-p_9 = 3.149\times10^9$ rads/sec.

6.) Finally, the capacitance associated with p_{10} is given as

$$C_{10} = C_{gs10} + C_{gs11} + C_{bd8}$$

These capacitors are given as

$$C_{gs10} = C_{gs11} = (220\times10^{-12}\cdot36.4\times10^{-6}) + (0.67)(36.4\times10^{-6}\cdot10^{-6}\cdot24.7\times10^{-4}) = 67.9\text{fF}$$

and

$$C_{bd8} = (770\times10^{-6})(36.4\times10^{-6}\cdot2\times10^{-6}) + (380\times10^{-12})(2\cdot38.4\times10^{-6}) = 85.2\text{fF}$$

Therefore,

$$C_{10} = 67.9\text{fF} + 67.9\text{fF} + 85.2\text{fF} = 0.221\text{pF}$$

which gives the pole p_{10} as $-744.6\times10^{-6}/0.246\times10^{-12} = -3.505\times10^9$ rads/sec.

The poles are summarized below:

$p_A = -1.346\times10^9$ rads/sec	$p_B = -1.346\times10^9$ rads/sec	$p_6 = -0.966\times10^9$ rads/sec
$p_8 = -3.149\times10^9$ rads/sec	$p_9 = -3.149\times10^9$ rads/sec	$p_{10} = -3.505\times10^9$ rads/sec

Example 7.2-2 - Continued

The smallest of these poles is p_6. Since p_A and p_B are not much larger than p_6, we will find the new GB by dividing p_6 by 5 (rather than 2.2) to get 200×10^6 rads/sec. Thus the new GB will be 200/2π or 32MHz. The magnitude of the dominant pole is given as

$$p_{dominant} = \frac{GB}{A_{vd}(0)} = \frac{200\times10^6}{7{,}464} = 26{,}795 \text{ rads/sec.}$$

The value of load capacitor that will give this pole is

$$C_L = \frac{1}{p_{dominant}\cdot R_{out}} = \frac{1}{26.795\times10^3\cdot19.4\text{M}\Omega} \approx 1.9\text{pF}$$

Thus, the load capacitor of the folded cascode op amp of Ex. 6.5-3 can be reduced to 1.9pF without sacrificing the phase margin. This corresponds to a new unity-gainbandwidth of 32 MHz compared with the old unity-gainbandwidth of 10 MHz..

Conclusion for Increasing the *GB* of Op Amps

Maximum GB depends on the input transconductance and the capacitance that causes the dominant pole.

Quantity	MOSFET Op Amp	BJT Op Amp
g_m dependence	$\sqrt{2K'\left(\frac{W}{L}\right)I_D}$	$\frac{I_C}{kT/q} = \frac{I_C}{V_t}$
Maximum g_m	≈ 1 mA/V	≈ 20 mA/V
GB for 10pF	15 MHz	300 MHz
GB for 1pF	150 MHz	3 GHz

Note that the power dissipation will be large for large GB because current is needed for large g_m.

Assumption:

All higher-order roots are above GB.

The larger GB, the more difficult this becomes.

Conclusion:

- The best CMOS op amps have a GB of 10-50MHz
- The best BJT op amps have a GB of 100-200MHz

Switched Amplifiers

Switched amplifiers are time varying circuits that yield circuits with smaller parasitic capacitors and therefore higher frequency response. Such circuits are called *dynamically biased*.

- Switched amplifiers require a nonoverlapping clock
- Switched amplifiers only work during a portion of a clock period
- Bias conditions are setup on one clock phase and then maintained by capacitance on the active phase
- Switched amplifiers use switches and capacitors resulting in feedthrough problems
- Simplified circuits on the active phase minimize the parasitics

Typical clock:

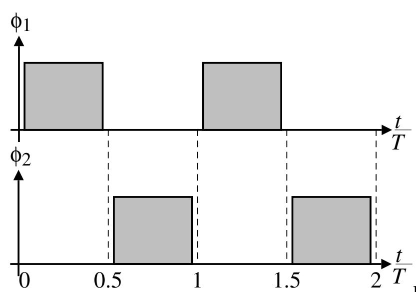


Fig. 7.2-3B

Dynamically Biased Inverting Amplifier

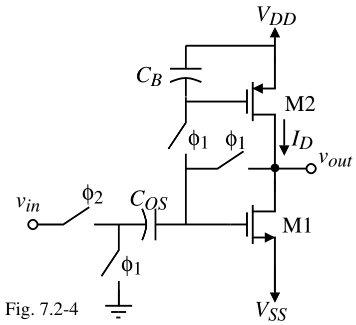


Fig. 7.2-4

During phase 1 the offset and bias of the inverter is sampled and applied to C_{OS} and C_B.

During phase 2 C_{OS} is connected in series with the input and provides offset canceling plus bias for M1. C_B provides the bias for M2.

(This circuit illustrates the concept of switched amplifiers but is too simple to illustrate the reduction of bias parasitics.)

Dynamically Biased, Push-Pull, Cascode Op Amp

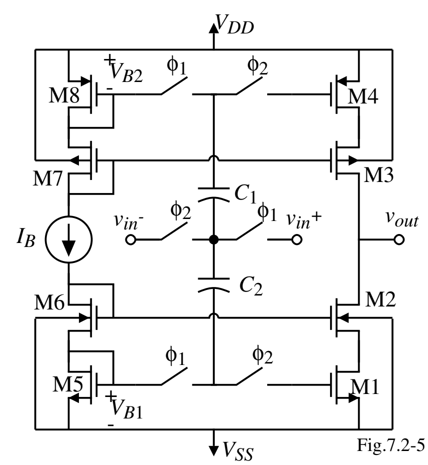


Fig.7.2-5

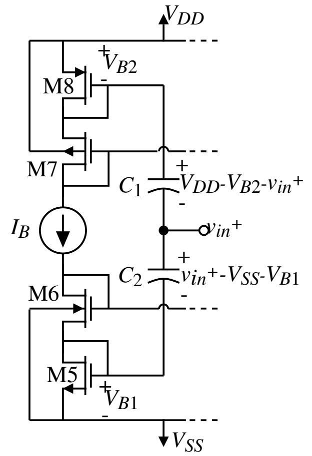
Push-pull, cascode amplifier: M1-M2 and M3-M4

Bias circuitry: M5-M6-C_2 and M7-M8-C_1

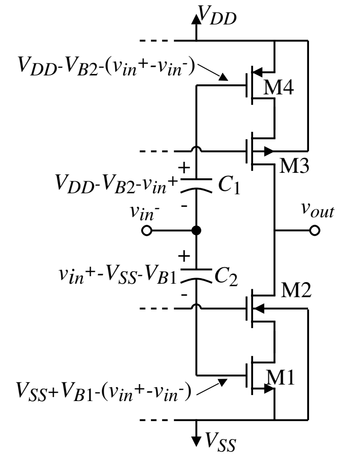
Parasitics can be further reduced by using a double-poly process to eliminate bulk-drain and bulk-source capacitances at the drain of M1-source of M2 and drain of M4-source of M3 (see Fig. 6.5-5).

Dynamically Biased, Push-Pull, Cascode Op Amp - Continued

Operation:



Equivalent circuit during the ϕ_1 clock period



Equivalent circuit during the ϕ_2 clock period.

Fig. 7.2-6

Dynamically Biased, Push-Pull, Cascode Op Amp - Continued

This circuit will operate on both clock phases[†] .

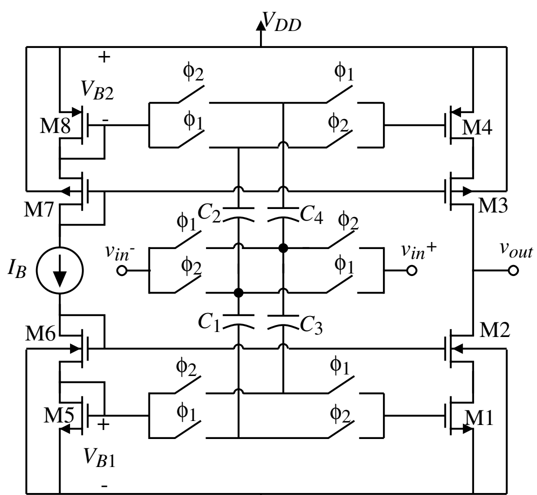


Fig. 7.2-7

Performance (1.5µm CMOS):

- 1.6mW dissipation
- $GB \approx$ 130MHz (C_L = 2.2pF)
- Settling time of 10ns (C_L = 10pF)

This amplifier was used with a 28.6MHz clock to realize a 5th-order switched capacitor filter having a cutoff frequency of 3.5MHz.

† S. Masuda, et. al., "CMOS Sampled Differential Push-Pull Cascode Op Amp," *Proc. of 1984 International Symposium on Circuits and Systems*, Montreal, Canada, May 1984, pp. 1211-12-14.

Current Feedback Op Amps

Why current feedback:

- Higher GB
- Less voltage swing $\Rightarrow$ more dynamic range

What is a current amplifier?

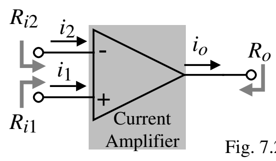


Fig. 7.2-8A

Requirements:

$i_o = A_i(i_1\text{-}i_2)$

$R_{i1} = R_{i2} = 0\Omega$

$R_o = \infty$

Ideal source and load requirements:

$R_{source} = \infty$

$R_{Load} = 0\Omega$

Bandwidth Advantage of a Current Feedback Amplifier

Consider the inverting voltage amplifier shown using a current amplifier with negative current feedback:

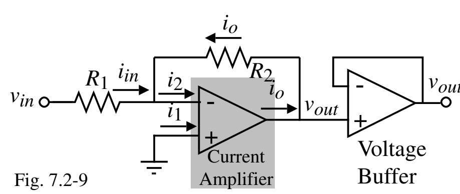


Fig. 7.2-9

The output current, i_o, of the current amplifier can be written as

$$i_o = A_i(s)(i_1\text{-}i_2) = \text{-}A_i(s)(i_{in} + i_o)$$

The closed-loop current gain, i_o/i_{in}, can be found as

$$\frac{i_o}{i_{in}} = \frac{-A_i(s)}{1+A_i(s)}$$

However, $v_{out} = i_oR_2$ and $v_{in} = i_{in}R_1$. Solving for the voltage gain, v_{out}/v_{in} gives

$$\frac{v_{out}}{v_{in}} = \frac{i_oR_2}{i_{in}R_1} = \left(\frac{-R_2}{R_1}\right)\left(\frac{A_i(s)}{1+A_i(s)}\right)$$

If $A_i(s) = \dfrac{A_o}{\dfrac{s}{\omega_A}+1}$, then

$$\frac{v_{out}}{v_{in}} = \left(\frac{-R_2}{R_1}\right)\left(\frac{A_o}{1+A_o}\right)\left(\frac{\omega_A(1+A_o)}{s+\omega_A(1+A_o)}\right) \quad\Rightarrow\quad A_v(0) = \frac{-R_2A_o}{R_1(1+A_o)} \quad \text{and} \quad \boxed{\omega_{\text{-3dB}} = \omega_A(1+A_o)}$$

Bandwidth Advantage of a Current Feedback Amplifier - Continued

The unity-gainbandwidth is,

$$GB = |A_v(0)|\ \omega_{\text{-3dB}} = \frac{R_2A_o}{R_1(1+A_o)} \cdot \omega_A(1+A_o) = \frac{R_2}{R_1}A_o{\cdot}\omega_A = \frac{R_2}{R_1}GB_i$$

where GB_i is the unity-gainbandwidth of the current amplifier.

Note that if GB_i is constant, then increasing R_2/R_1 (the voltage gain) increases GB.

Illustration:

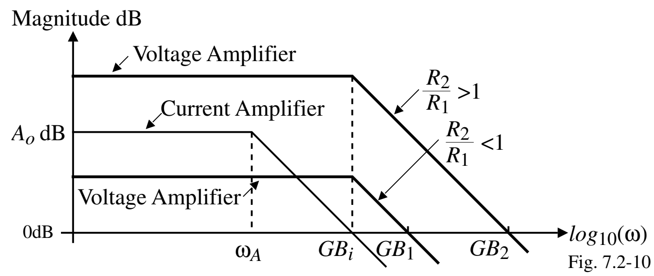


Fig. 7.2-10

Note that $GB_2 > GB_1 > GB_i$

The above illustration assumes that the GB of the voltage amplifier realizing the voltage buffer is greater than the GB achieved from the above method.

A Simple Current Mirror Implementation of a High Frequency Amplifier

Since the gain of the current amplifier does not need to be large, consider a unity-gain current mirror implementation:

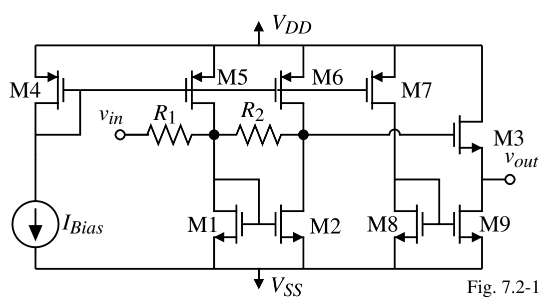


Fig. 7.2-11

An inverting amplifier with a gain of 10 is achieved if $R_2 = 20R_1$ assuming the gain of the current mirror is unity.

What is the GB of this amplifier?

$$GB = |A_v(0)|\omega_{\text{-3dB}} = \frac{R_2A_o}{R_1(1+A_o)} \cdot \frac{1}{R_2C_o} = \frac{A_o}{(1+A_o)R_1C_o} = \frac{1}{2R_1C_o}$$

where C_o is the capacitance seen at the output of the current mirror.

If $R_1 = 10\text{k}\Omega$ and $C_o = 250\text{fF}$, then $GB = 31.83\text{MHz}$.

Limitations:

$$R_1 > R_{in} = 1/g_{m1} \quad \text{and} \quad R_2 < r_{ds2}||r_{ds6} \quad \Rightarrow \quad \frac{R_2}{R_1} << g_{m1}(r_{ds2}||r_{ds6})$$

A Wide-Swing, Cascode Current Mirror Implementation of a High Frequency Amplifier

The current mirror shown below increases the value of R_2 by increasing the output resistance of the current mirror.

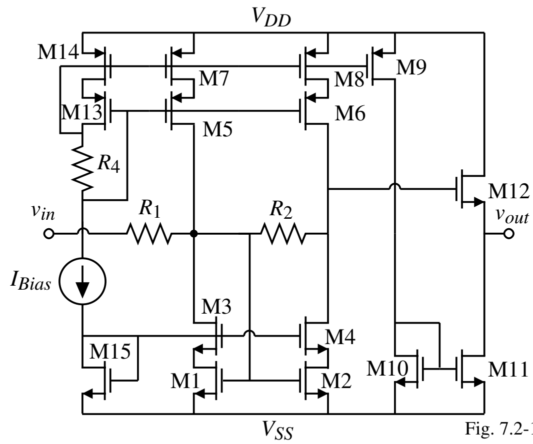


Fig. 7.2-12

New limitations:

$$R_1 > \frac{1}{g_{m1}} \quad \text{and} \quad R_2 < g_{m4}r_{ds4}r_{ds2} || g_{m6}r_{ds6}r_{ds8} \Rightarrow \quad \frac{R_2}{R_1} << g_{m1}(g_{m4}r_{ds4}r_{ds2} || g_{m6}r_{ds6}r_{ds8})$$

Example 7.2-3 - Design of a High *GB* Voltage Amplifier using Current Feedback

Design the wide-swing, cascode voltage amplifier to achieve a gain of -10V/V and a *GB* of 500MHz which corresponds to a -3dB frequency of 50MHz.

Solution

Since we know what the gain is to be, let us begin by assuming that C_o will be 100fF. Thus to get a *GB* of 500MHz, R_1 must be 3.2kΩ and R_2 = 32kΩ. Therefore, R_3 must be at least 300Ω. R_3 is designed by V_{ON}/I where V_{ON} is the saturation voltage of M1-M4. Therefore we can write

$$R_3 = \frac{V_{ON}}{I} = \sqrt{\frac{2}{IK'(W/L)}} = 300\Omega \quad \rightarrow \quad 22.2\text{x}10^{-6} = K'\cdot I\cdot\frac{W}{L} \quad \rightarrow \quad 0.202 = I\cdot\frac{W}{L}$$

At this point we have a problem because if *W/L* is small to minimize C_o, the current will be too high. If we select *W/L* = 200µm/1µm we will get a current of 1mA. However, using this *W/L* for M4 and M6 will give a value of C_o that is greater than 100fF.

Select *W/L* = 200 for M1, M3, M5 and M7 and *W/L* = 20µm/1µm for M2, M4, M6, and M8. which gives a current in these transistors of 100µA.

Since R_2/R_1 is multiplied by 1/11 let R_2 be 110 times R_1 or 352kΩ.

Now select a *W/L* for M12 of 20µm/1µm which will now permit us to calculate C_o. We will assume zero-bias on all voltage dependent capacitors. Furthermore, we will assume the diffusion area as 2µm times the *W*. C_o can be written as

$$C_o = C_{gd4} + C_{bd4} + C_{gd6} + C_{bd6} + C_{gs12}$$

Example 7.2-3 - Design of a High *GB* Voltage Amplifier using Current Feedback - Cont'd

The information required to calculate these capacitors is found from Table 3.2-1. The various capacitors are,

$C_{gd4} = C_{gd6} = CGDO$x10µm = (220x10^{-12})(20x10^{-6}) = 4.4fF

$C_{bd4} = CJ$xAD$_4$+$CJSW$xPD$_4$ = (770x10^{-6})(20x10^{-12})+(380x10^{-12})(44x10^{-6}) = 15.4fF+16.7fF = 32.1fF

C_{bd6} = (560x10^{-6})(20x10^{-12})+(350x10^{-12})(44x10^{-6}) = 26.6fF

C_{gs12} = (220x10^{-12})(20x10^{-6}) + (0.67)(20x10^{-6}·10^{-6}·24.7x10^{-4}) = 37.3fF

Therefore,

C_o = 4.4fF+32.1fF+4.4fF+26.6fF+37.3fF = 105fF

Note that if we had not reduced the *W/L* of M2, M4, M6, and M8 that C_o would have easily exceeded 100fF. Since 105fF is close to our original guess of 100fF, let us keep the values of R_1 and R_2. If this value was significantly different, then we would adjust the values of R_1 and R_2 so that the *GB* is 500MHz. One must also check to make sure that the input pole is greater than 500MHz.

The design is completed by assuming that I_{Bias} = 100µA and that the current in M9 through M12 be 100µA. Thus $W_{13}/L_{13} = W_{14}/L_{14}$ = 20µm,/1µm and W_9/L_9 through W_{12}/L_{12} are 20µm/1µm.

Example 7.2-3 - Design of a High *GB* Voltage Amplifier using Current Feedback - Cont'd

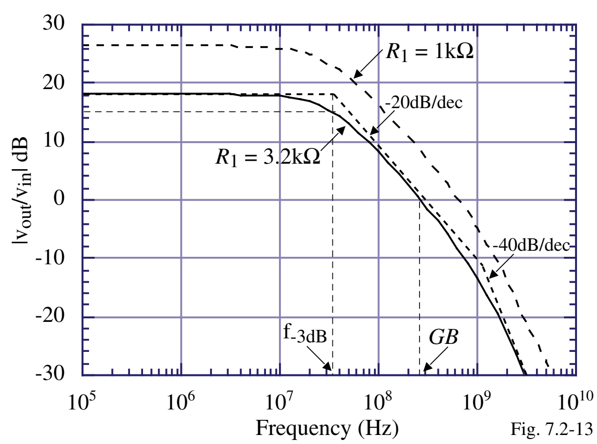


Fig. 7.2-13

Simulation Results:

f_{-3dB} ≈ 38MHz   *GB* ≈ 300MHz   Closed-loop gain = 18dB (Loss of -2dB is attributed to source follower and R_1)

Note second pole at about 1GHz. To get these results, it was necessary to bias the input at -1.7VDC using ±3V power supplies.

If R_1 is decreased to 1kΩ results in:

Gain of 26.4dB, f_{-3dB} = 32MHz, and *GB* = 630MHz

Parallel Path Op Amps

This type of op amp combines a high-gain, low-frequency path with a low-gain, high-frequency path.

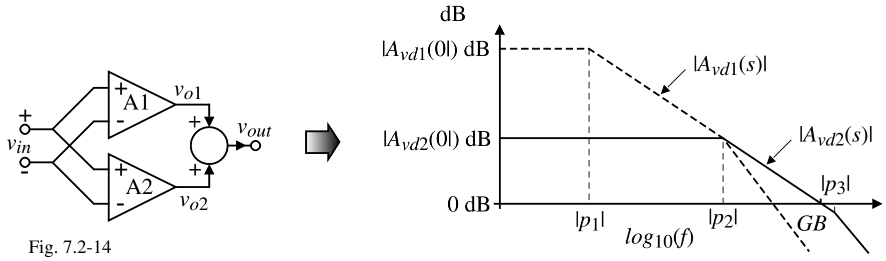


Fig. 7.2-14

Comments:

- Op amp will be conditionally stable
- Compensation will be challenging

Multipath Nested Miller Compensation†

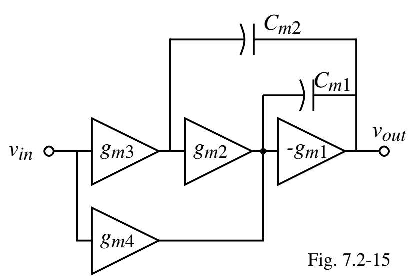


Fig. 7.2-15

Comments:

- All Miller capacitances must be around inverting stages
- Ensure that the RHP zeros generated by the Miller compensation are canceled
- Avoid pole-zero doublets which can introduce a slow time constant

† R.G.H. Eschauzier and J.H.Huijsing, *Frequency Compensation Techniques for Low-Power Operational Amplifiers,* Kluwer Academic publishers, 1995, Chapter 6.

Illustration of Hybrid Nested Miller Compensation†

(Note that this example is not multipath.)

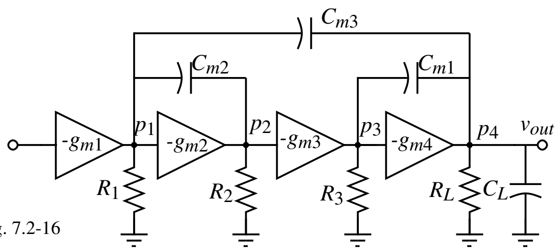


Fig. 7.2-16

Compensating Results:

1) C_{m1} pushes p_4 to higher frequencies and p_3 down to lower frequencies
2) C_{m2} pushes p_2 to higher frequencies and p_1 down to lower frequencies
3) C_{m3} pushes p_3 to higher frequencies (feedback path) & pulls p_1 further to lower frequencies

Equations:

$GB \approx g_{m1}/C_{m3}$ $\quad p_2 \approx g_{m2}/C_{m3}$ $\quad p_3 \approx g_{m3}C_{m3} / (C_{m1}C_{m2})$ $\quad p_4 \approx g_{m4}/C_L$

Design:

$GB < p_2, p_3, p_4$

† R.G. H. Eschauzier *et. al.*, "A Programmable 1.5V CMOS Class-AB Operational Amplifier with Hybrid Nested Miller Compensation for 120dB Gain and 6MHz UGT," *IEEE J. of Solid State Circuits*, vol. 29, No. 12, pp. 1497-1504, Dec. 1994.

Illustration of the Hybrid Nested Miller Compensation Technique

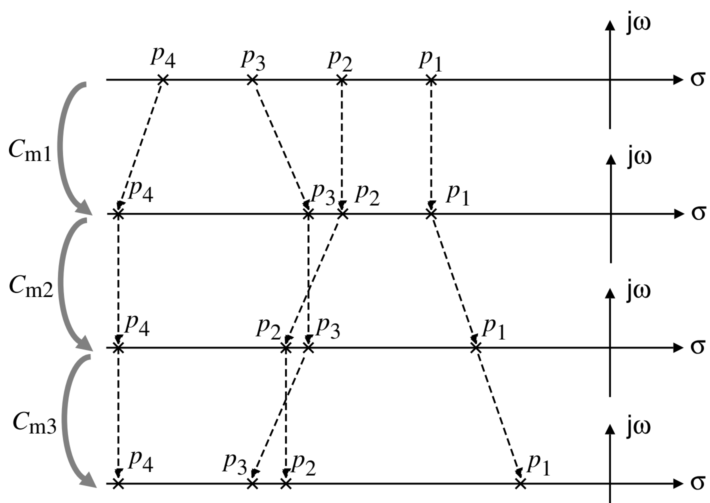


Fig. 7.2-17

Summary

- Normal op amps limited by g_m/C
- Typical limit for CMOS op amp is $GB \approx$ 50MHz
- Other approaches to high frequency CMOS op amps:
  - Current amplifiers (Transimpedance amplifiers)
  - Switched amplifier (simplifies the circuit $\Rightarrow$ reduce capacitances)
  - Parallel path op amps (compensation becomes more complex)
- What does the future hold?
  - Reduction of channel lengths mean:
    - * Reduced capacitances $\Rightarrow$ Higher GB's
    - * Higher transconductances (larger values of K') $\Rightarrow$ Higher GB's
    - * Increased channel conductance $\Rightarrow$ Lower gains (more stages required)
    - * Reduction of power supply $\Rightarrow$ Increased capacitances

  In otherwords, there should be some improvement in op amp GB's but it won't be inversely proportional to the decrease in channel length. I.e. maybe GB's $\approx$ 100MHz for 0.2μm CMOS.

SECTION 7.3 -DIFFERENTIAL OUTPUT OP AMPS

Why Differential Output Op Amps?

- Cancellation of common mode signals including clock feedthrough
- Increased signal swing

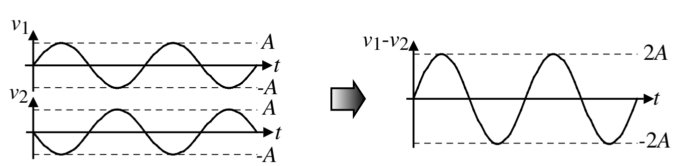


Fig. 7.3-1

- Cancellation of even-order harmonics

Symbol:

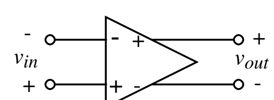


Fig. 7.3-1A

Common Mode Output Voltage Stabilization

If the common mode gain not small, it may cause the common mode output voltage to be poorly defined.

Illustration:

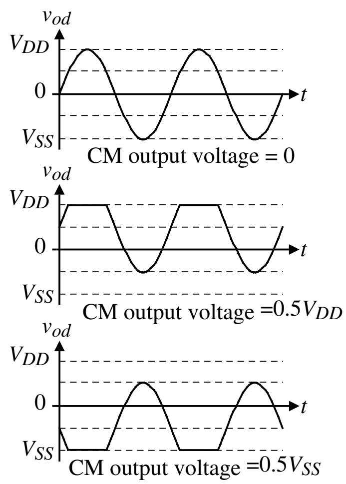


Fig. 7.3-2

Two-Stage, Miller, Differential-In, Differential-Out Op Amp

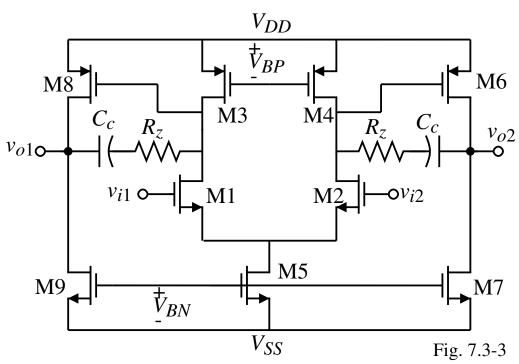


Fig. 7.3-3

Output common mode range ($OCMR$) = V_{DD}+ $|V_{SS}|$ - V_{SDP}(sat) - V_{DSN}(sat)

The maximum peak-to-peak output voltage ≤ 2·$OCMR$

Conversion between differential outputs and single-ended outputs:

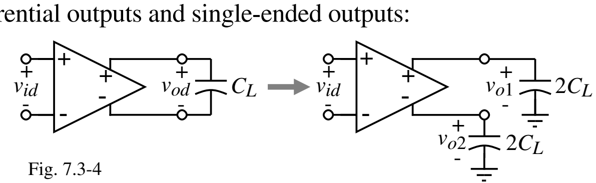


Fig. 7.3-4

Differential-Output, Folded-Cascode, Class-A Op Amp

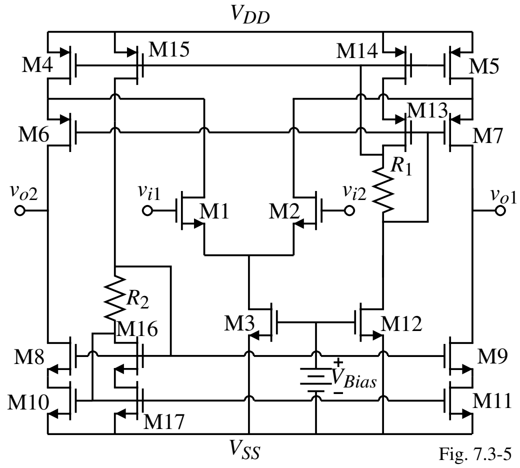


Fig. 7.3-5

$OCMR = V_{DD} + |V_{SS}| - 2V_{SDP}(\text{sat}) - 2V_{DSN}(\text{sat})$

Two-Stage, Miller, Differential-In, Differential-Out Op Amp with Push-Pull Output

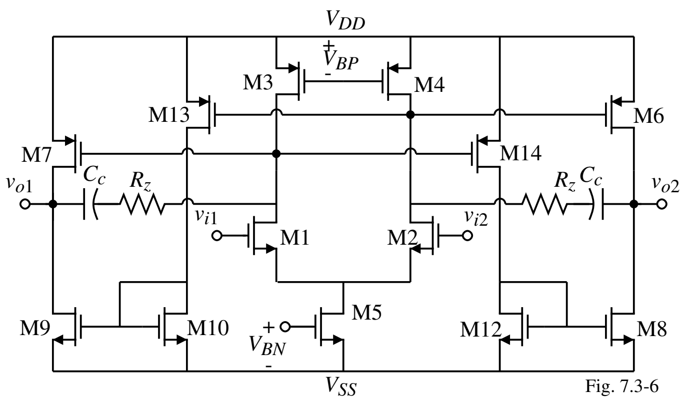


Fig. 7.3-6

Comments:

- Able to actively source and sink output current
- Output quiescent current poorly defined

Two-Stage, Differential Output, Folded-Cascode Op Amp

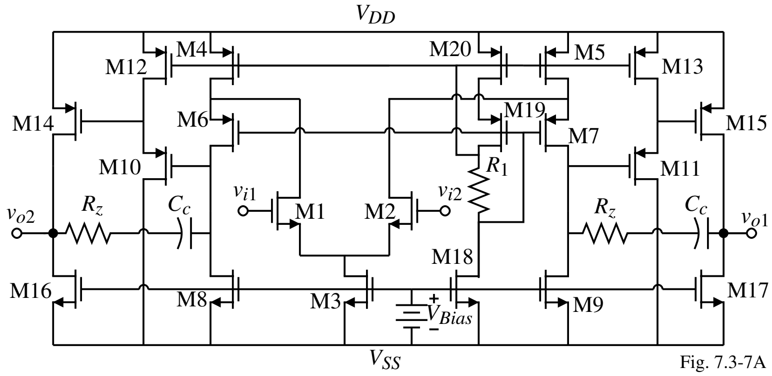


Fig. 7.3-7A

Note that the followers M11-M13 and M10-M12 are necessary for level translation to the output stage.

Unfolded Cascode Op Amp with Differential-Outputs

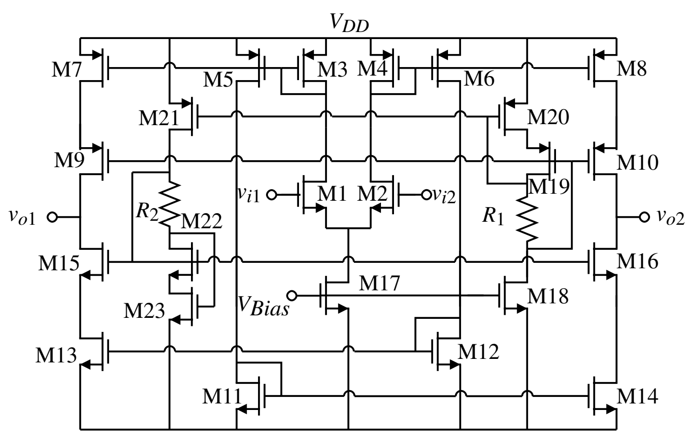


Fig. 7.3-8

Cross-Coupled Differential Amplifier Stage

One of the problems with some of the previous stages, is that the quiescent output current was not well defined.

The following input stage solves this problem.

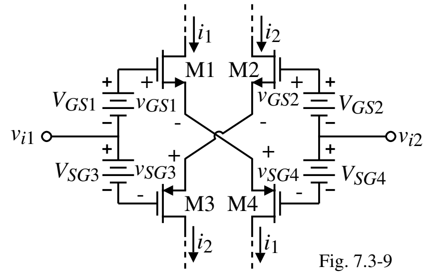


Fig. 7.3-9

Operation:

Voltage loop $v_{i1} - v_{i2} = -V_{GS1} + v_{GS1} + v_{SG4} - V_{SG4} = V_{SG3} - v_{SG3} - v_{GS2} + V_{GS2}$

Using the notation for ac, dc, and total variables gives,

$$v_{i2} - v_{i1} = v_{id} = (v_{sg1} + v_{gs4}) = -(v_{sg3} + v_{gs2})$$

If M1=M2=M3=M4, then half of the differential input is applied across each transistor with the correct polarity.

$\therefore \quad i_1 = \dfrac{g_{m1}v_{id}}{2} = \dfrac{g_{m4}v_{id}}{2}$ and $i_2 = -\dfrac{g_{m2}v_{id}}{2} = -\dfrac{g_{m3}v_{id}}{2}$

Class AB, Differential Output Op Amp using a Cross-Coupled Differential Input Stage

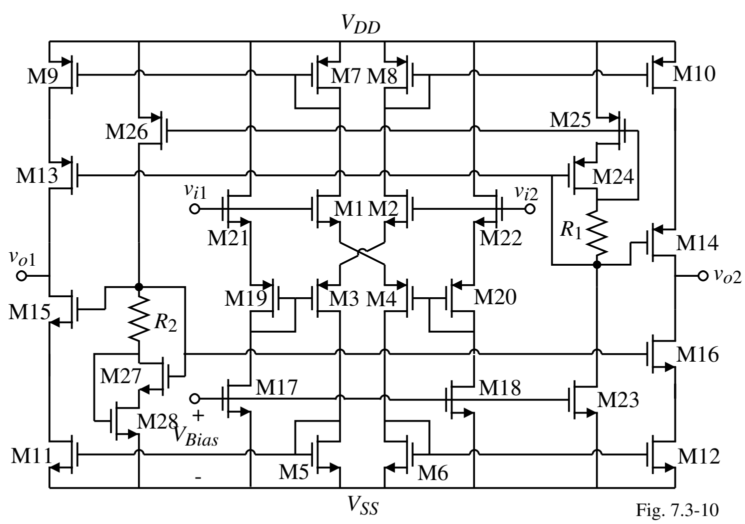


Fig. 7.3-10

Quiescent output currents are defined by the current in the input cross-coupled differential amplifier.

Common-Mode Output Voltage Stabilization

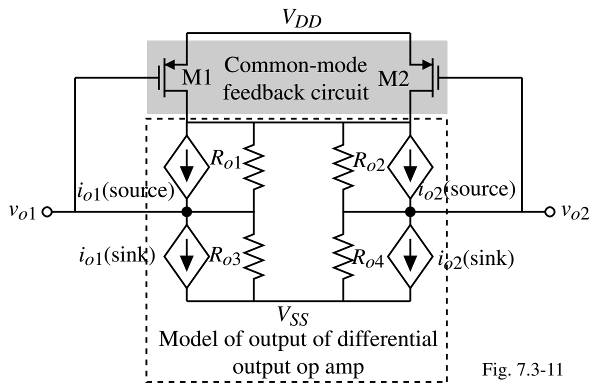


Fig. 7.3-11

Operation:

M1 and M2 sense the common-mode output voltage.

If this voltage rises, the currents in M1 and M2 decrease.

This decreased current flowing through R_{o3} and R_{o4} cause the common-mode output voltage to decrease with respect to V_{SS}.

Two-Stage, Miller, Differential-In, Differential-Out Op Amp with Common-Mode Stabilization

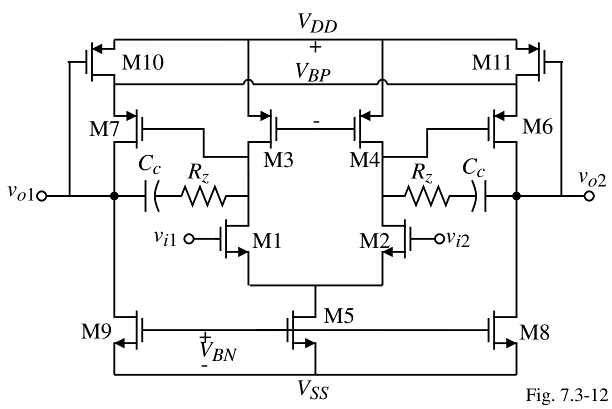


Fig. 7.3-12

Comments:

- Simple
- Unreferenced

A Referenced Common-Mode Output Voltage Stabilization Scheme

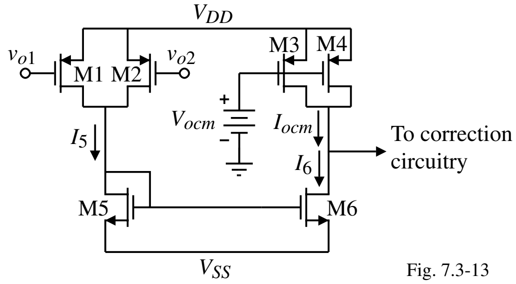


Fig. 7.3-13

Operation:

1.) The desired common-mode output voltage, V_{ocm}, creates I_{ocm}.

2.) The actual common-mode output voltage creates the current I_5 which is mirrored to I_6 .

3.) If M1 through M4 are matched and the current mirror is ideal, then when $I_{ocm} = I_6$ the actual common-mode output voltage should be equal to the desired common-mode output voltage.

4.) The above steps assume that a correction circuitry exists that changes the common-mode output voltage in the correct manner.

Common Model Feedback Circuits

Implementation of common mode feedback circuit:

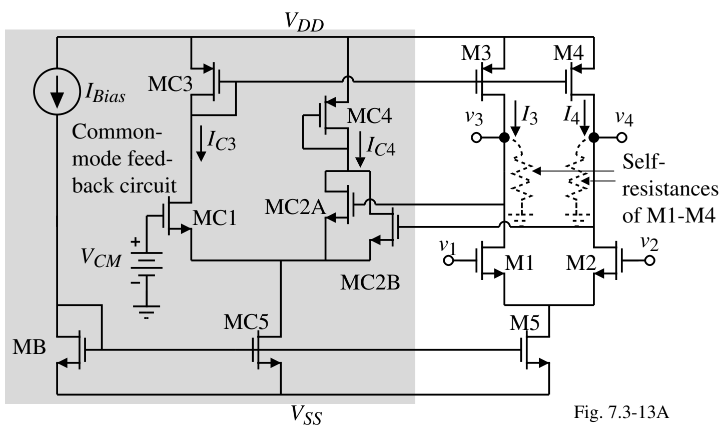


Fig. 7.3-13A

This scheme can be applied to any differential output amplifier.

Caution:

Be sure to check the stability of common-mode feedback loops, particularly those that are connected to op amps that have a cascode output. The gain of the common-mode feedback loop can easily reach that of a two-stage amplifier.

External Common-Mode Output Voltage Stabilization Scheme

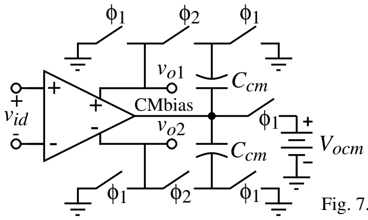


Fig. 7.3-14

Operation:

1.) During the ϕ_1 phase, both C_{cm} are charged to the desired value of V_{ocm} and CMbias = V_{ocm}.

2.) During the ϕ_2 phase, the C_{cm} capacitors are connected between the differential outputs and the CMbias node. The average value applied to the CMbias node will be V_{ocm}.

SECTION 7.4 - MICROPOWER OP AMPS

Objectives

- Minimize power dissipation
- Work at low values of power supply
- Tradeoff speed for less power

Subthreshold Operation

Most micropower op amps use transistors in the subthreshold region.

Subthreshold characteristics:

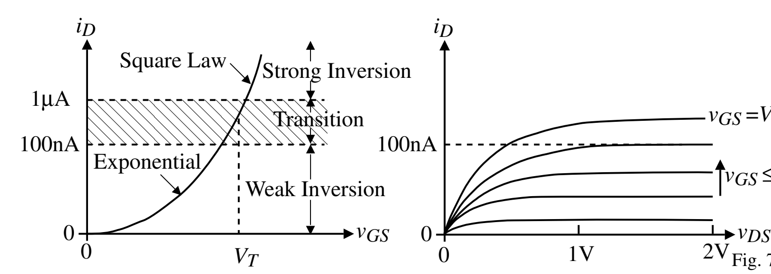


Fig. 7.4-0A

$$i_D = \frac{W}{L} I_{DO} \exp\left(\frac{q v_{GS}}{nkT}\right)(1+\lambda v_{DS}) \quad \Rightarrow \quad g_m = \frac{qI_D}{nkT} \quad \text{and} \quad g_{ds} \approx \lambda I_D$$

Two-Stage, Miller Op Amp Operating in Weak Inversion

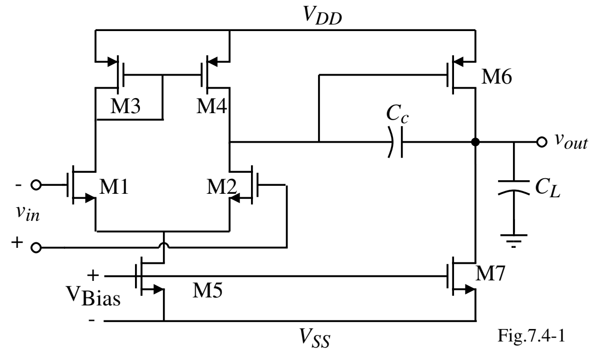


Fig.7.4-1

Low frequency response:

$$A_{vo} = g_{m2}g_{m6}\left(\frac{r_{o2}r_{o4}}{r_{o2}+r_{o4}}\right)\left(\frac{r_{o6}r_{o7}}{r_{o6}+r_{o7}}\right) = \frac{1}{n_2n_6(kT/q)^2(\lambda_2+\lambda_4)(\lambda_6+\lambda_7)} \quad \left(\text{No longer} \propto \frac{1}{\sqrt{I_D}}\right)$$

GB and *SR*:

$$GB = \frac{I_{D1}}{(n_1kT/q)C} \qquad \text{and} \qquad SR = \frac{I_{D5}}{C} = 2\,\frac{I_{D1}}{C} = 2GB\left(n_1\frac{kT}{q}\right) = 2GBn_1V_t$$

Example 7.4-1 Gain and GB Calculations for Subthreshold Op Amp.

Calculate the gain, *GB,* and *SR* of the op amp shown above. The currents are I_{D5} = 200 nA and I_{D7} = 500 nA. The device lengths are 1 μm. Values for n are 1.5 and 2.5 for p-channel and n-channel transistors respectively. The compensation capacitor is 5 pF. Use Table 3.1-2 as required. Assume that the temperature is 27 °C. If V_{DD} = 1.5V and V_{SS} = -1.5V, what is the power dissipation of this op amp?

Solution

The low-frequency small-signal gain is,

$$A_v = \frac{1}{(1.5)(2.5)(0.026)^2(0.04+0.05)(0.04+0.05)} = 43{,}701 \text{ V/V}$$

The gain bandwidth is

$$GB = \frac{100\times10^{-9}}{2.5(0.026)(5\times10^{-12})} = 307{,}690 \text{ rps} \cong 49.0 \text{ kHz}$$

The slew rate is

$$SR = (2)(153846)(2.5)(0.026) = 0.02 \text{ V}/\mu\text{s}$$

The power dissipation is,

$$P_{diss} = 3(0.7\mu\text{A}) = 2.1\mu\text{W}$$

Push-Pull Output Op Amp in Weak Inversion

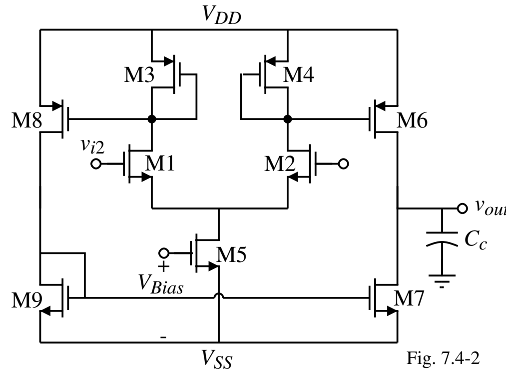


Fig. 7.4-2

First stage gain is,

$$A_{vo} = \frac{g_{m2}}{g_{m4}} = \frac{I_{D2}n_4V_t}{I_{D4}n_2V_t} = \frac{I_{D2}n_4}{I_{D4}n_2} \cong 1$$

Total gain is,

$$A_{vo} = \frac{g_{m1}(S_6/S_4)}{(g_{ds6} + g_{ds7})} = \frac{(S_6/S_4)}{(\lambda_6 + \lambda_7)n_1V_t}$$

At room temperature ($V_t = 0.0259$V) and for typical device lengths, gains of 60dB can be obtained.

The GB is,

$$GB = \frac{g_{m1}}{C}\left(\frac{S_6}{S_4}\right) = \frac{g_{m1}b}{C}$$

Increasing the Gain of the Previous Op Amp

1.) Can reduce the currents in M3 and M4 and introduce gain in the current mirrors.

2.) Use a cascode output stage (can't use self-biased cascode, currents are too low).

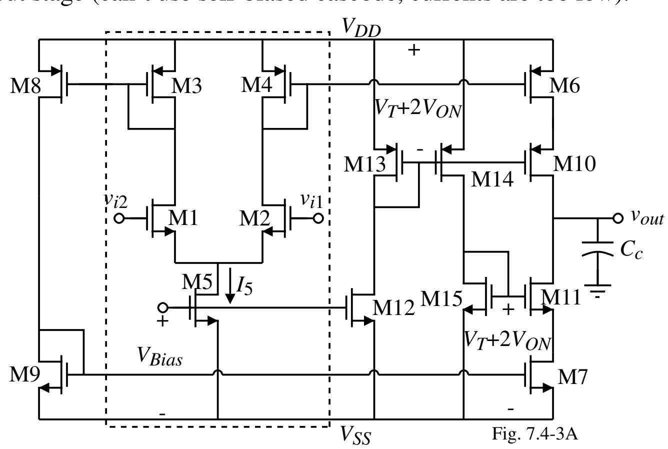


Fig. 7.4-3A

$$A_v = \left(\frac{g_{m1}+g_{m2}}{2}\right)R_{out} = \frac{g_{m1}}{\dfrac{g_{ds6}g_{ds10}}{g_{m10}} + \dfrac{g_{ds7}g_{ds11}}{g_{m11}}} = \frac{\dfrac{I_5}{2n_nV_t}}{\dfrac{I_7^2\cdot\lambda_n^2}{\dfrac{I_7}{n_nV_t}} + \dfrac{I_7^2\cdot\lambda_p^2}{\dfrac{I_7}{n_pV_t}}} = \left(\frac{I_5}{2I_7}\right)\left(\frac{1}{n_nV_t^2(n_n\lambda_n^2+n_p\lambda_p^2)}\right)$$

Can easily achieve gains greater than 80dB with power dissipation of less than 1μW.

Increasing the Output Current for Weak Inversion Operation

A significant disadvantage of the weak inversion is that very small currents are available to drive output capacitance so the slew rate becomes very small.

Dynamically biased differential amplifier input stage:

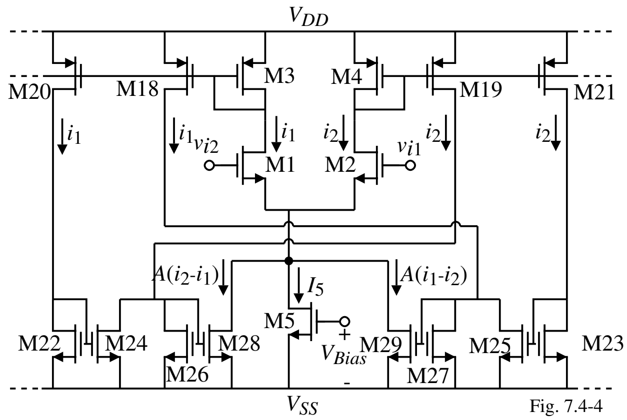


Fig. 7.4-4

Note that the sinking current for M1 and M2 is

$$I_{sink} = I_5 + A(i_2\text{-}i_1) + A(i_1\text{-}i_2) \qquad \text{where } (i_2\text{-}i_1) \text{ and } (i_1\text{-}i_2) \text{ are only positive or zero.}$$

If v_{i1}>v_{i2}, then i_2>i_1 and the sinking current is increased by $A(i_2\text{-}i_1)$.

If v_{i2}>v_{i1}, then i_1>i_2 and the sinking current is increased by $A(i_1\text{-}i_2)$.

Dynamically Biased Differential Amplifier - Continued

How much output current is available from this circuit if there is no current gain from the input to output stage?

Assume transistors M18 through M21 are equal to M3 and M4 and that transistors M22 through M27 are all equal.

Let $\dfrac{W_{28}}{L_{28}} = A\left(\dfrac{W_{26}}{L_{26}}\right)$ and $\dfrac{W_{29}}{L_{29}} = A\left(\dfrac{W_{27}}{L_{27}}\right)$

The output current available can be found by assuming that $v_{in} = v_{i1}\text{-}v_{i2} > 0$.

$\therefore\ i_1 + i_2 = I_5 + A(i_2\text{-}i_1)$

The ratio of i_2 to i_1 can be expressed as

$$\frac{i_2}{i_1} = \exp\left(\frac{v_{in}}{nV_t}\right)$$

Defining the output current as $i_{OUT} = b(i_2\text{-}i_1)$ and combining the above two equations gives,

$$i_{OUT} = \frac{bI_5\left[\exp\left(\frac{v_{in}}{nV_t}\right) - 1\right]}{(1+A) - (A\text{-}1)\exp\left(\frac{v_{in}}{nV_t}\right)} \quad \Rightarrow \quad i_{OUT} = \infty \text{ when } A = 2.16 \text{ and } \frac{v_{in}}{nV_t} = 1$$

where b corresponds to any current gain achieved through the current mirrors (M5-M4 and M8-M3).

Overdrive of the Dynamically Biased Differential Amplifier

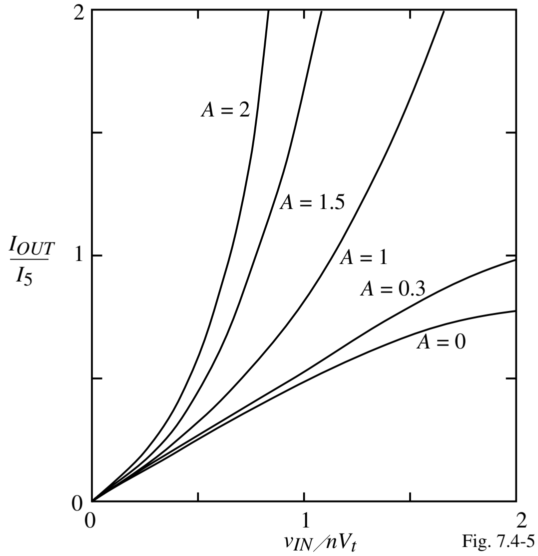


Fig. 7.4-5

The enhanced output current is accomplished by the use of positive feedback (M28-M2-M19-M28).

Loop gain is,

$$LG = \left(\frac{g_{m28}}{g_{m4}}\right)\left(\frac{g_{m19}}{g_{m26}}\right) = A\,\frac{g_{m19}}{g_{m4}} = A$$

Note that as the output current increases, the transistors leave the weak inversion region and the above analysis is no longer valid.

Increasing the Output Current for Strong Inversion Operation

An interesting technique is to bias the output transistor of a current mirror in the active region and then during large overdrive cause the output transistor to become saturated causing a significant current gain.

Illustration:

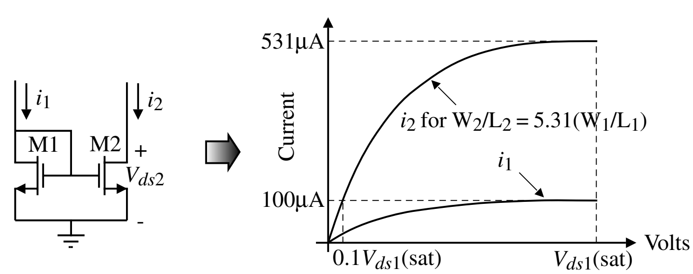


Fig. 7.4-6

Example 7.4-2 Current Mirror with M2 operating in the Active Region

Assume that M2 has a voltage across the drain-source of $0.1V_{ds}$(sat). Design the W_2/L_2 ratio so that $I_1 = I_2 = 100\mu A$ if $W_1/L_1 = 10$. Find the value of I_2 if M2 is saturated.

Solution

Using the parameters of Table 3.1-2, we find that the saturation voltage of M2 is

$$V_{ds1}(\text{sat}) = \sqrt{\frac{2I_1}{K_N'(W_2/L_2)}} = \sqrt{\frac{200}{110\cdot 10}} = 0.4264\text{V}$$

Now using the active equation of M2, we set $I_2 = 100\mu A$ and solve for W_2/L_2.

$$100\mu A = K_N'(W_2/L_2)[V_{ds1}(\text{sat})\cdot V_{ds2} - 0.5V_{ds2}^2]$$

$$= 110\mu A/V^2(W_2/L_2)[0.426\cdot 0.0426 - 0.5\cdot 0.0426^2]V^2 = 1.883\text{x}10^6(W_2/L_2)$$

Thus,

$$100 = 1.883(W_2/L_2) \rightarrow \quad \frac{W_2}{L_2} = 53.12$$

Now if M2 should become saturated, the value of the output current of the mirror with 100µA input would be 531µA or a boosting of 5.31 times I_1.

Implementation of the Current Mirror Boosting Concept

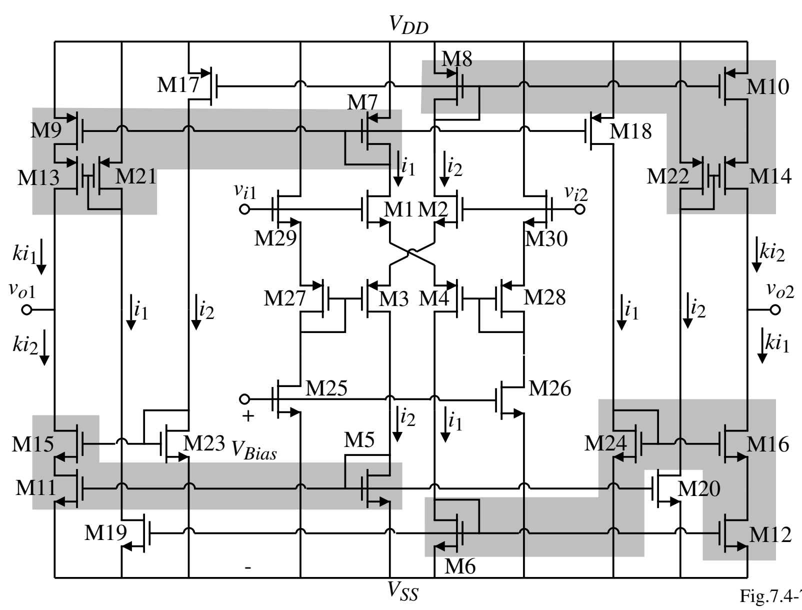


Fig.7.4-7

k = overdrive factor of the current mirror

A Better Way to Achieve the Current Mirror Boosting

It was found that when the current mirror boosting idea illustrated on the previous slide was used that when the current increased through the cascode device (M16) that V_{GS16} increased limiting the increase of V_{DS12}. This can be overcome by the following circuit.

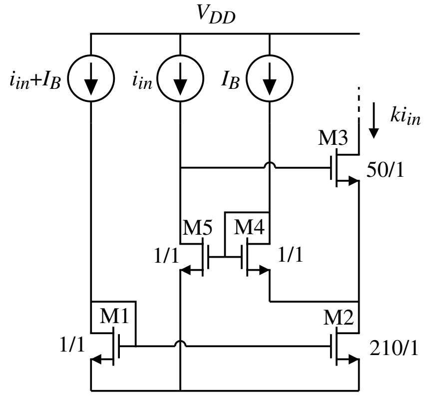


Fig. 7.4-7A

Summary of Low Power Op Amps

- Operation of transistors is generally in weak inversion
- Boosting techniques are needed to get output sourcing and sinking currents that are larger than that available during quiescent operation
- Be careful about using circuits at weak inversion, i.e. the self-biased cascode will cause the resistor to be too large

SECTION 7.5 - LOW-NOISE OP AMPS

Introduction

Why do we need low noise op amps?

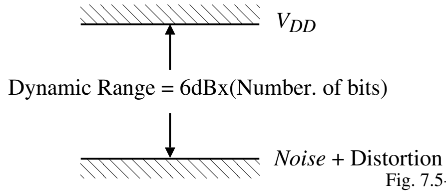


Fig. 7.5-0B

Dynamic range.

$$\text{Signal-to-noise ratio } (SNR) = \frac{\text{Maximum RMS Signal}}{\text{Noise}} \qquad (SNDR)$$

Consider a 14 bit digital-to-analog converter with a 1V reference with a bandwidth of 1MHz.

Maximum RMS signal is $\frac{0.5\text{V}}{\sqrt{2}} = 0.3535$ Vrms

A 14 bit D/A converter requires 14x6dB dynamic range or 84 dB or 16,400.

$\therefore$ The value of the least significant bit (LSB) $= \frac{0.3535}{16,400} = 21.6\mu$Vrms

If the equivalent input noise of the op amp is not less than this value, then the LSB cannot be resolved and the D/A converter will be in error. An op amp with an equivalent input-noise spectral density of 10nV/$\sqrt{\text{Hz}}$ will have an rms noise voltage of approximately 10nV/$\sqrt{\text{Hz}}\cdot 1000\sqrt{\text{Hz}}$ = 10μVrms.

Transistor Noise Sources (Low-Frequency)

Drain current model:

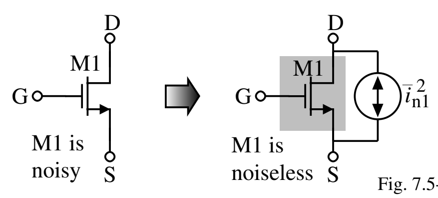


Fig. 7.5-0A

$$\overline{i_n^2} = \left[\frac{8kTg_m}{3} + \frac{(KF)I_D}{fC_{ox}L^2}\right] \quad \text{or} \quad \overline{i_n^2} = \left[\frac{8kTg_m(1+\eta)}{3} + \frac{(KF)I_D}{fC_{ox}L^2}\right] \text{ if } v_{BS} \neq 0$$

Recall that $\eta = \frac{g_m}{g_{mbs}}$

Gate voltage model assuming common source operation:

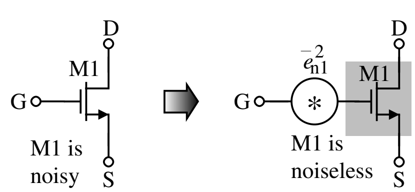


Fig. 7.5-0C

$$\overline{e_n^2} = \frac{\overline{i_N^2}}{g_m^2} = \left[\frac{8kT}{3g_m} + \frac{KF}{2fC_{ox}WLK'}\right] \quad \text{or} \quad \overline{e_n^2} = \left[\frac{8kT(1+\eta)}{3g_m} + \frac{KF}{2fC_{ox}WLK'}\right] \text{ if } v_{BS} \neq 0$$

Minimization of Noise in Op Amps

1.) Maximize the signal gain as close to the input as possible. (As a consequence, only the input stage will contribute to the noise of the op amp.)

2.) To minimize the 1/f noise:

  a.) Use PMOS input transistors with appropriately selected dc currents and W and L values.

  b.) Use lateral BJTs to eliminate the 1/*f* noise.

  c.) Use chopper stabilization to reduce the low-frequency noise.

Noise Analysis

1.) Insert a noise generator for each transistor that contributes to the noise. (Generally ignore the current source transistor of source-coupled pairs.)

2.) Find the output noise voltage across an open-circuit or output noise current into a short circuit.

3.) Reflect the total output noise back to the input resulting in the equivalent input noise voltage.

A Low-Noise, Two-Stage, Miller Op Amp

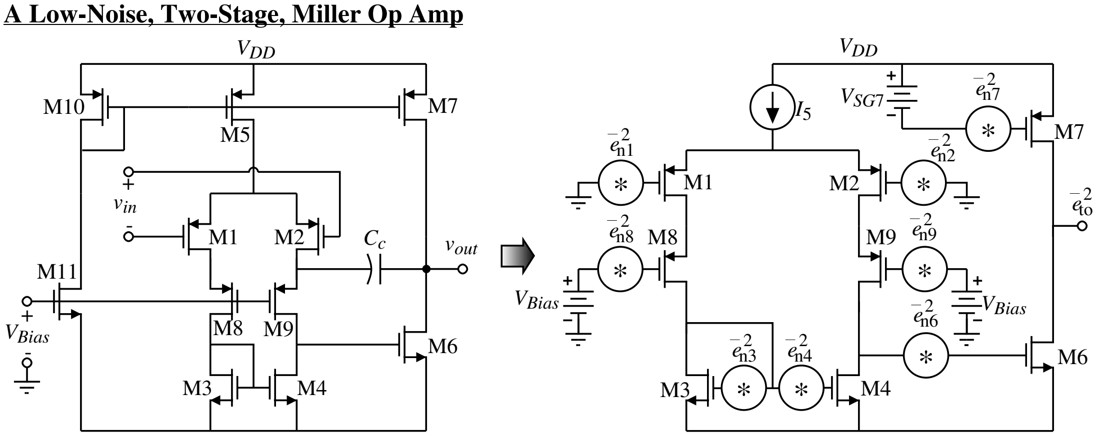


Fig. 7.5-1

The total output-noise voltage spectral density, $\overline{e_{to}^2}$, is found as follows where $g_{m8}(\text{eff}) \approx 1/r_{ds1}$,

$$\overline{e_{to}^2} = g_{m6}^2 R_{II}^2 \left[\overline{e_{n6}^2} + \overline{e_{n7}^2} + R_I^2 \left(g_{m1}^2 \overline{e_{n1}^2} + g_{m2}^2 \overline{e_{n2}^2} + g_{m3}^2 \overline{e_{n3}^2} + g_{m4}^2 \overline{e_{n4}^2} + \frac{\overline{e_{n8}^2}}{r_{ds1}^2} + \frac{\overline{e_{n9}^2}}{r_{ds2}^2} \right) \right]$$

Dividing by $(g_{m1}R_I g_{m6}R_{II})^2$ gives the equivalent input-noise voltage spectral density, $\overline{e_{eq}^2}$, as

$$\overline{e_{eq}^2} = \frac{\overline{e_{to}^2}}{(g_{m1}g_{m6}R_I R_{II})^2} = \frac{2\overline{e_{n6}^2}}{g_{m1}^2 R_I^2} + 2\overline{e_{n1}^2}\left[1 + \left(\frac{g_{m3}}{g_{m1}}\right)^2 \left(\frac{\overline{e_{n3}^2}}{\overline{e_{n1}^2}}\right) + \frac{\overline{e_{n8}^2}}{g_{m1}^2 r_{ds1}^2 \overline{e_{n1}^2}} \right] \approx 2\overline{e_{n1}^2}\left[1 + \left(\frac{g_{m3}}{g_{m1}}\right)^2 \left(\frac{\overline{e_{n3}^2}}{\overline{e_{n1}^2}}\right)^2 \right]$$

where $\overline{e_{n6}^2} = \overline{e_{n7}^2}$, $\overline{e_{n3}^2} = \overline{e_{n4}^2}$, $\overline{e_{n1}^2} = \overline{e_{n2}^2}$ and $\overline{e_{n8}^2} = \overline{e_{n9}^2}$ and $g_{m1}R_I$ is large.

1/*f* Noise of a Two-Stage, Miller Op Amp

Consider the 1/*f* noise:

Therefore the noise generators are replaced by,

$$\overline{e_{ni}^2} = \frac{B}{fW_iL_i} \quad (\mathrm{V^2/Hz}) \qquad \text{and} \qquad \overline{i_{ni}^2} = \frac{2BK'I_i}{fL_i^2} \quad (\mathrm{A^2/Hz})$$

Therefore, the approximate equivalent input-noise voltage spectral density is,

$$\overline{e_{eq}^2} = 2\overline{e_{n1}^2}\left[1 + \left(\frac{K_N'B_N}{K_P'B_P}\right)\left(\frac{L_1}{L_3}\right)^2\right] \ (\mathrm{V^2/Hz})$$

Comments;

- Because we have selected PMOS input transistors, $\overline{e_{n1}^2}$ has been minimized if we choose W_1L_1 (W_2L_2) large.
- Make $L_1 << L_3$ to remove the influence of the second term in the brackets.

Thermal Noise of a Two-Stage, Miller Op Amp

Let us focus next on the thermal noise:

The noise generators are replaced by,

$$\overline{e_{ni}^2} \approx \frac{8kT}{3g_m} \quad (\mathrm{V^2/Hz}) \qquad \text{and} \qquad \overline{i_{ni}^2} \approx \frac{8kTg_m}{3} \quad (\mathrm{A^2/Hz})$$

where the influence of the bulk has been ignored.

The approximate equivalent input-noise voltage spectral density is,

$$\overline{e_{eq}^2} = 2\overline{e_{n1}^2}\left[1 + \frac{g_{m3}}{g_{m1}} + \frac{g_{m8}}{g_{m1}}\right] = 2\overline{e_{n1}^2}\left[1 + \sqrt{\frac{K_NW_3L_1}{K_PW_1L_3}}\,\right] (\mathrm{V^2/Hz})$$

Comments:

- The choices that reduce the 1/*f* noise also reduce the thermal noise.

Noise Corner:

Equating the equivalent input-noise voltage spectral density for the 1/*f* noise and the thermal noise gives the noise corner, f_c, as

$$f_c = \frac{3g_mB}{8kTWL}$$

Example 7.5-1 Design of A Two-Stage, Miller Op Amp for Low 1/*f* Noise

Use the parameters of Table 3.1-2 along with the value of KF = 4x10^{-28} F·A for NMOS and 0.5x10^{-28} F·A for PMOS and design the previous op amp to minimize the 1/f noise. Calculate the corresponding thermal noise and solve for the noise corner frequency. From this information, estimate the rms noise in a frequency range of 1Hz to 100kHz. What is the dynamic range of this op amp if the maximum signal is a 1V peak-to-peak sinusoid?

Solution

1.) The 1/f noise constants, B_N and B_P are calculated as follows.

$$B_N = \frac{KF}{2C_{ox}K_N'} = \frac{4\text{x}10^{-28}\text{F·A}}{2·24.7\text{x}10^{-4}\text{F/m}^2·110\text{x}10^{-6}\text{A}^2\text{/V}} = 7.36\text{x}10^{-22}\ (\text{V·m})^2$$

and

$$B_P = \frac{KF}{2C_{ox}K_P'} = \frac{0.5\text{x}10^{-28}\text{F·A}}{2·24.7\text{x}10^{-4}\text{F/m}^2·50\text{x}10^{-6}\text{A}^2\text{/V}} = 2.02\text{x}10^{-22}\ (\text{V·m})^2$$

2.) Now select the geometry of the various transistors that influence the noise performance.

To keep $\overline{e_{n1}^2}$ small, let W_1 = 100µm and L_1 = 1µm. Select W_3 = 100µm and L_3 = 20µm and let W_8 and L_8 be the same as W_1 and L_1 since they little influence on the noise.

Of course, M1 is matched with M2, M3 with M4, and M8 with M9.

$$\therefore \quad \overline{e_{n1}^2} = \frac{B_P}{fW_1L_1} = \frac{2.02\text{x}10^{-22}}{f·100\mu\text{m}·1\mu\text{m}} = \frac{2.02\text{x}10^{-12}}{f}\ (\text{V}^2\text{/Hz})$$

$$\overline{e_{eq}^2} = 2\text{x}\frac{2.02\text{x}10^{-12}}{f}\left[1 + \left(\frac{110·7.36}{50·2.02}\right)^2\left(\frac{1}{100}\right)^2\right] = \frac{4.04\text{x}10^{-12}}{f}1.0064 \quad = \frac{4.066\text{x}10^{-12}}{f}(\text{V}^2\text{/Hz})$$

Note that at 100Hz, the voltage noise in a 1Hz band is approximately 4x10^{-14}V^2(rms) or 0.202µV(rms).

Example 7.5-1 - Continued

3.) The thermal noise at room temperature is

$$\overline{e_{n1}^2} = \frac{8kT}{3g_m} = \frac{8·1.38\text{x}10^{-23}·300}{3·707\text{x}10^{-6}} = 1.562\text{x}10^{-17}\ (\text{V}^2\text{/Hz})$$

which gives

$$\overline{e_{eq}^2} = 2·1.562\text{x}10^{-17}\left[1 + \sqrt{\frac{110·100·1}{50·100·20}}\right] = 3.124\text{x}10^{-17}·1.33 = 4.164\text{x}10^{-17}\ (\text{V}^2\text{/Hz})$$

4.) The noise corner frequency is found by equating the two expressions for $\overline{e_{eq}^2}$ to get

$$f_c = \frac{4.689\text{x}10^{-12}}{4.164\text{x}10^{-17}} = 112.6\text{kHz}$$

This noise corner is indicative of the fact that the thermal noise is much less than the 1/f noise.

5.) To estimate the rms noise in the bandwidth from 1Hz to 100,000Hz, we will ignore the thermal noise and consider only the 1/f noise. Performing the integration gives

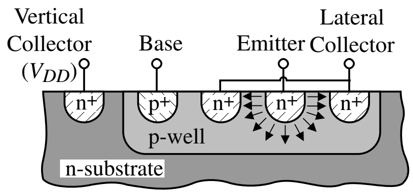
$$V_{eq}(\text{rms})^2 = \int_1^{10^5}\frac{4.689\text{x}10^{-12}}{f}df = 4.066\text{x}10^{-12}[ln(100{,}000) - ln(1)] = 0.540\text{x}10^{-10}\ \text{V}^2(\text{rms}) = 7.348\ \mu\text{V(rms)}$$

The maximum signal in rms is 0.353V. Dividing this by 7.348µV gives 48,044 or 93.63dB which is equivalent to about 15 bits of resolution.

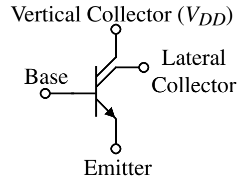
6.) Note that the design of the remainder of the op amp will have little influence on the noise and is not included in this example.

Lateral BJT

Since the $1/f$ noise is associated with current flowing at the surface of the channel, the lateral BJT offers a lower $1/f$ noise input device because the majority of current flows beneath the surface.



Cross-section of a NPN lateral BJT.



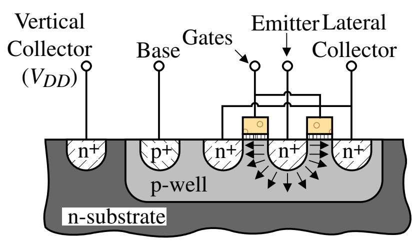
Symbol. Fig. 7.5-3

Comments:

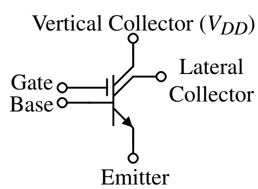
- Base of the BJT is the well
- Two collectors-one horizontal (desired) and one vertical (undesired)
- Collector efficiency is defined as $\frac{\text{Lateral collector current}}{\text{Total collector current}}$ and is 60-70%
- Reverse biased collector-base acts like a photodetector and is often used for light-sensing purposes

Field-Aided Lateral BJT

Polysilicon gates are used to ensure that the region beneath the gate does not invert forcing all current flow away from the surface and further eliminating the $1/f$ noise.



Cross-section of a field-aided NPN lateral BJT.



Symbol. Fig. 7.5-4

Physical Layout of a Lateral PNP Transistor

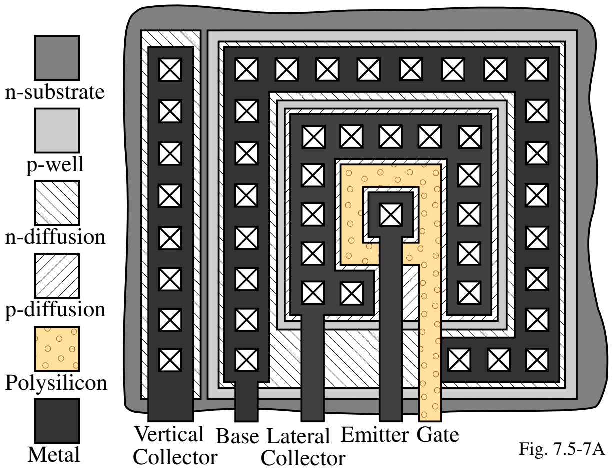


Fig. 7.5-7A

Generally, the above structure is made as small as possible and then paralleled with identical geometries to achieve the desired BJT.

Experimental Results for a x40 PNP lateral BJT:

Characteristic	Value
Transistor area	$0.006mm^2$
Lateral β	90
Lateral efficiency	70%
Base resistance	150Ω
$\overline{e}_n$ at 5 Hz	$2.46nV/\sqrt{Hz}$
$\overline{e}_n$ at midband	$1.92nV/\sqrt{Hz}$
$f_c(\overline{e}_n)$	3.2Hz
$\overline{i}_n$ at 5 Hz	$3.53pA/\sqrt{Hz}$
$\overline{i}_n$ at midband	$0.61pA/\sqrt{Hz}$
$f_c(\overline{i}_n)$	162 Hz
f_T	85 MHz
Early voltage	16V
1.2µm CMOS with n-well	

Low-Noise Op Amp using Lateral BJT's at the Input

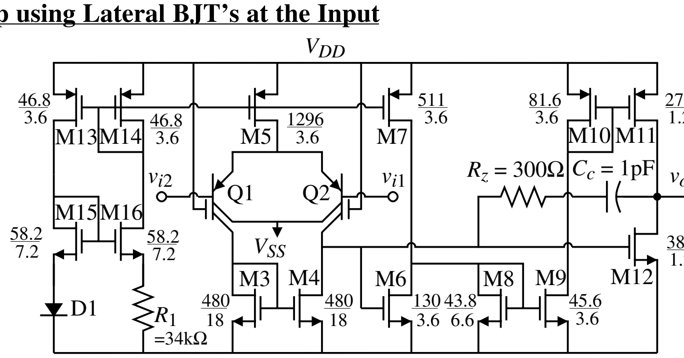


Fig. 7.5-6

Experimental noise performance:

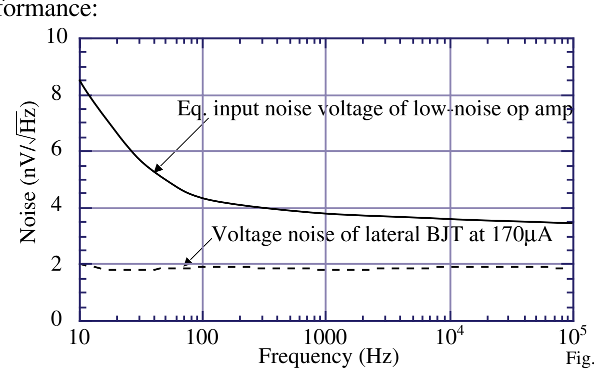


Fig. 7.5-7

Summary of Experimental Performance for the Low-Noise Op Amp

Experimental Performance	Value
Circuit area (1.2μm)	0.211 mm^2
Supply Voltages	±2.5 V
Quiescent Current	2.1 mA
-3dB frequency (at a gain of 20.8 dB)	11.1 MHz
$\overline{e}_n$ at 1Hz	23.8 nV/$\sqrt{\text{Hz}}$
$\overline{e}_n$ (midband)	3.2 nV/$\sqrt{\text{Hz}}$
$f_c(\overline{e}_n)$	55 Hz
$\overline{i}_n$ at 1Hz	5.2 pA/$\sqrt{\text{Hz}}$
$\overline{i}_n$ (midband)	0.73 pA/$\sqrt{\text{Hz}}$
$f_c(\overline{i}_n)$	50 Hz
Input bias current	1.68 μA
Input offset current	14.0 nA
Input offset voltage	1.0 mV
CMRR(DC)	99.6 dB
PSRR$^+$(DC)	67.6 dB
PSRR$^-$(DC)	73.9 dB
Positive slew rate (60 pF, 10 kΩ load)	39.0 V/μS
Negative slew rate (60 pF, 10 kΩ load)	42.5 V/μS

Chopper-Stabilized Op Amps - Doubly Correlated Sampling (DCS)

Illustration of the use of chopper stabilization to remove the undesired signal, v_u, form the desired signal, v_{in}.

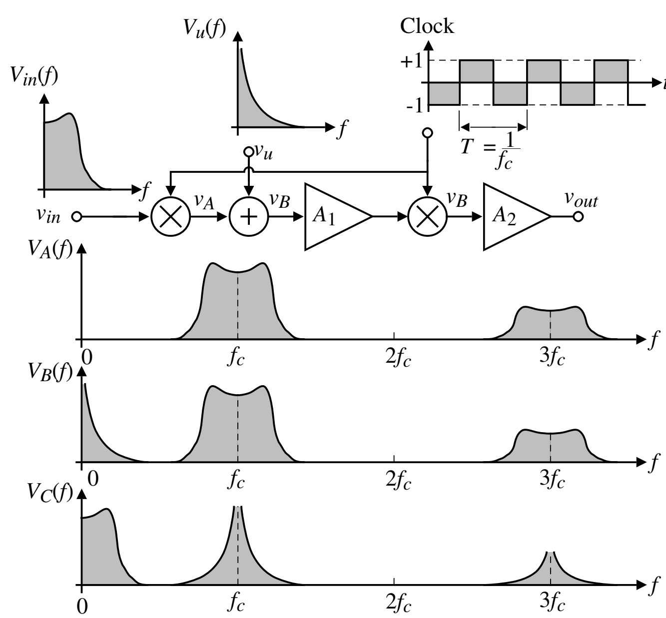


Fig. 7.5-8

Chopper-Stabilized Amplifier

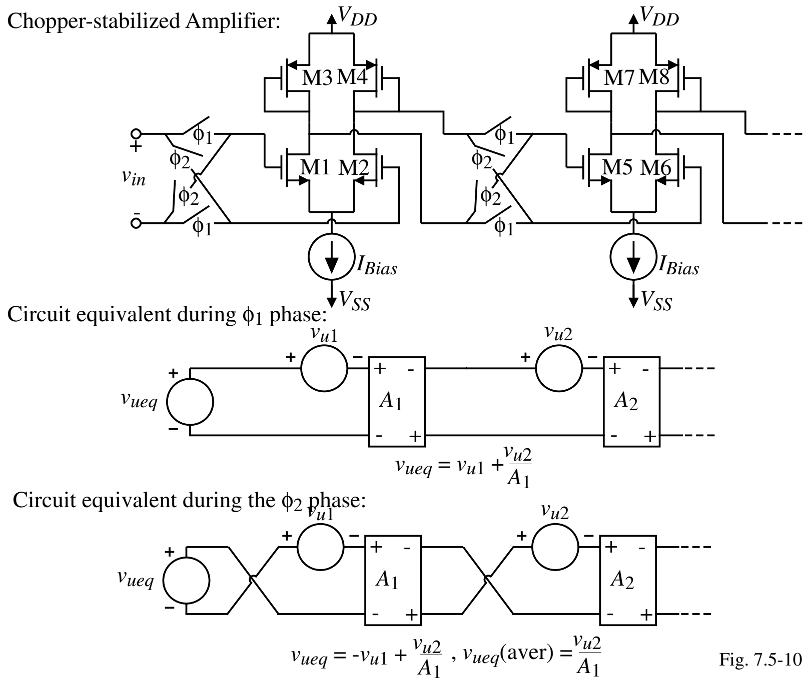


Fig. 7.5-10

Experimental Noise Response of the Chopper-Stabilized Amplifier

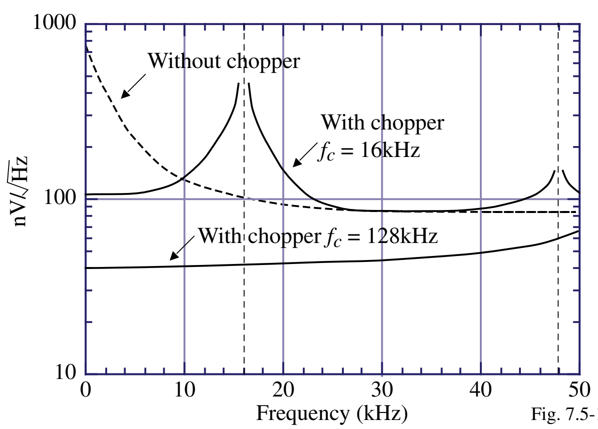


Fig. 7.5-11

Comments:

- The switches in the chopper-stabilized op amp introduce a thermal noise equal to kT/C where k is Boltzmann's constant, T is absolute temperature and C are capacitors charged by the switches(parasitics in the case of the chopper-stabilized amplifier)
- Requires two-phase, non-overlapping clocks
- Trade-off between the lowering of $1/f$ noise and the introduction of the kT/C noise.

SECTION 7.6 - LOW VOLTAGE OP AMPS

Introduction

While low voltage op amps can be easily designed in weak inversion, strong inversion leads to higher performance and is the focus of this section.

Semiconductor Industry Associates Roadmap for Power Supplies:

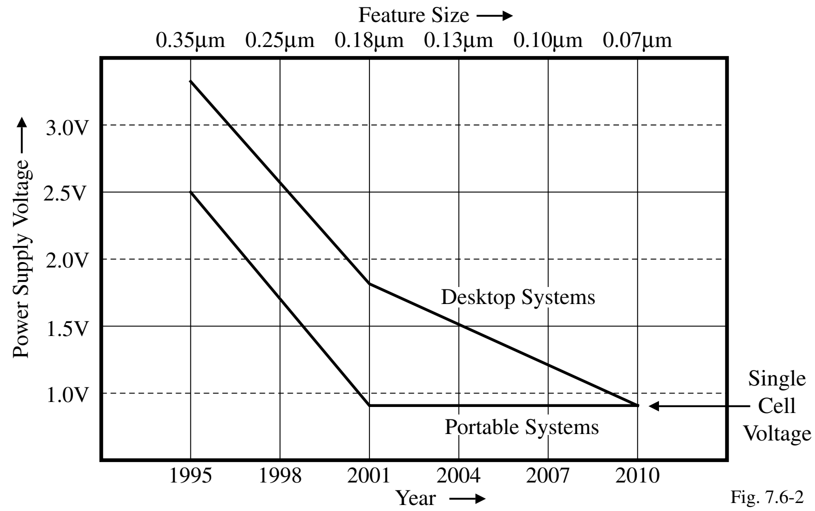


Fig. 7.6-2

Threshold voltages will remain about 0.5 to 0.7V in order to allow the MOSFET to be turned off.

Implications of Low-Voltage, Strong-Inversion Operation

- Reduced power supply means decreased dynamic range
- Nonlinearity will increase because the transistor is working close to V_{DS}(sat)
- Large values of λ because the transistor is working close to V_{DS}(sat)
- Increased drain-bulk and source-bulk capacitances because they are less reverse biased.
- Large values of currents and *W/L* ratios to get high transconductance
- Small values of currents and large values of *W/L* will give small V_{DS}(sat)
- Severely reduced input common mode range
- Switches will require charge pumps

Approach

- Low voltage input stages with reasonable *ICMR*
- Low voltage bias and load circuits
- Low voltage op amps

Differential Amplifier with Current Source Loads

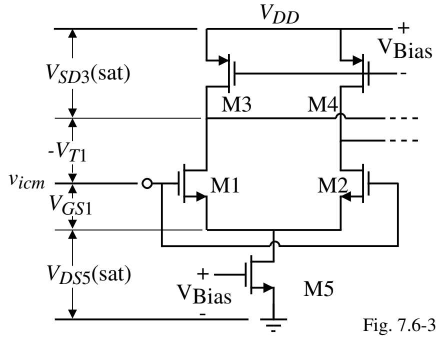


Fig. 7.6-3

Minimum power supply ($ICMR = 0$):

$$V_{DD}(\min) = V_{SD3}(\text{sat}) - V_{T1} + V_{GS1} + V_{DS5}(\text{sat}) = V_{SD3}(\text{sat}) + V_{DS1}(\text{sat}) + V_{DS5}(\text{sat})$$

Input common-mode range:

$$V_{icm}(\text{upper}) = V_{DD} - V_{SD3}(\text{sat}) + V_{T1}$$

$$V_{icm}(\text{lower}) = V_{DS5}(\text{sat}) + V_{GS1}$$

Example:

If the threshold magnitudes are 0.7V, $V_{DD} = 1.5$V and the saturation voltages are 0.3V, then

$V_{icm}(\text{upper}) = 1.5 - 0.3 + 0.7 = 1.9\text{V}$ and $V_{icm}(\text{lower}) = 0.3 + 1.0 = 1.3\text{V}$

giving an *ICMR* of 0.6V.

Increasing the *ICMR* using Parallel Input Stages

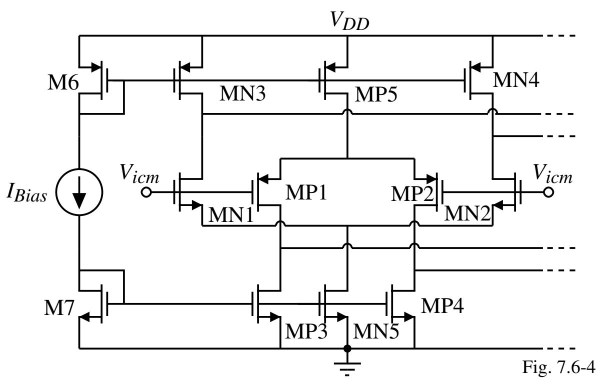


Fig. 7.6-4

Turn-on voltage for the n-channel input:

$$V_{onn} = V_{DSN5}(\text{sat}) + V_{GSN1}$$

Turn-on voltage for the p-channel input:

$$V_{onp} = V_{DD} - V_{SDP5}(\text{sat}) - V_{SG1}$$

The sum of V_{onn} and V_{onp} equals the minimum power supply.

Regions of operation:

$V_{DD} > V_{icm} > V_{onp}$: (n-channel on and p-channel off) $g_m(\text{eq}) = g_{mN}$

$V_{onp} \geq V_{icm} \geq V_{onn}$: (n-channel on and p-channel on) $g_m(\text{eq}) = g_{mN} + g_{mP}$

$V_{onn} > V_{icm} > 0$: (n-channel input off and p-channel input on) $g_m(\text{eq}) = g_{mP}$

where g_m(eq) is the equivalent input transconductance of the above input stage, g_{mN} is the input transconductance for the n-channel input and g_{mP} is the input transconductance for the p-channel input.

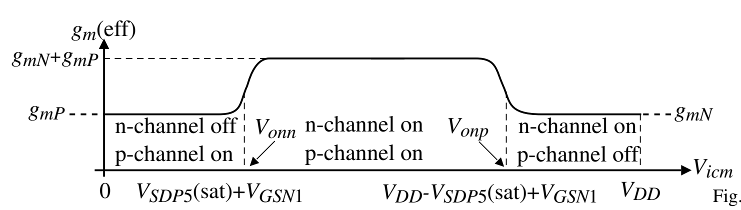


Fig. 7.6-5

Removing the Nonlinearity in Transconductances as a Function of *ICMR*

Increase the bias current in the differential amplifier that is on when the other differential amplifier is off.

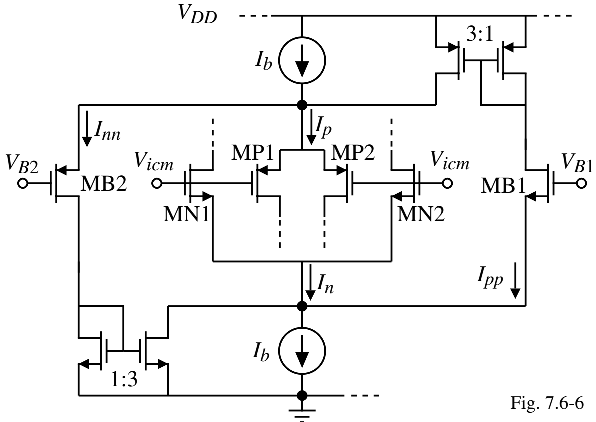


Fig. 7.6-6

Three regions of operation depending on the value of V_{icm}:

1.) $V_{icm} < V_{onn}$: n-channel diff. amp. off and p-channel on with $I_p = 4I_b \Rightarrow g_m(\text{eff}) = \sqrt{\frac{K_P' W_P}{L_P}}\, 2\sqrt{I_b}$

2.) $V_{onn} < V_{icm} < V_{onp}$: both on with $I_n = I_p = I_b \Rightarrow g_m(\text{eff}) = \sqrt{\frac{K_N' W_N}{L_N}}\sqrt{I_b} + \sqrt{\frac{K_P' W_P}{L_P}}\sqrt{I_b}$

3.) $V_{icm} > V_{onp}$: p-channel diff. amp. off and n-channel on with $I_n = 4I_b \Rightarrow g_m(\text{eff}) = \sqrt{\frac{K_N' W_N}{L_N}}\, 2\sqrt{I_b}$

How Does the Current Compensation Work?

Set $V_{B1} = V_{onn}$ and $V_{B2} = V_{onp}$.

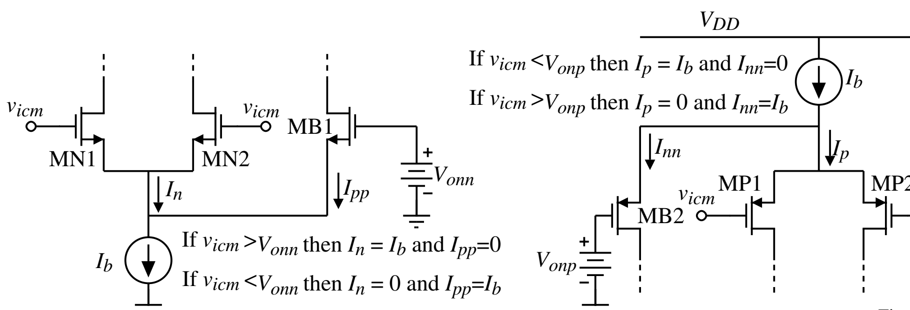


Fig. 7.6-6A

Result:

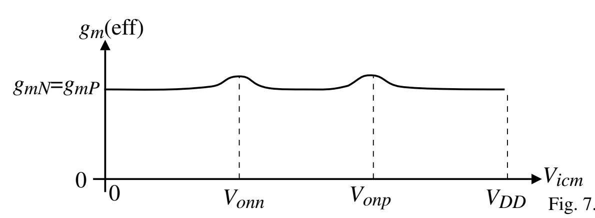


Fig. 7.6-7

The above techniques and many similar ones are good for power supply values down to about 1.5V. Below than, different techniques must be used or the technology must be modified (natural devices).

Bulk-Driven MOSFET

A depletion device would permit large *ICMR* even with very small power supply voltages because V_{GS} is zero or negative.

When a MOSFET is driven from the bulk with the gate held constant, it acts like a depletion transistor.

Cross-section of an n-channel bulk-driven MOSFET:

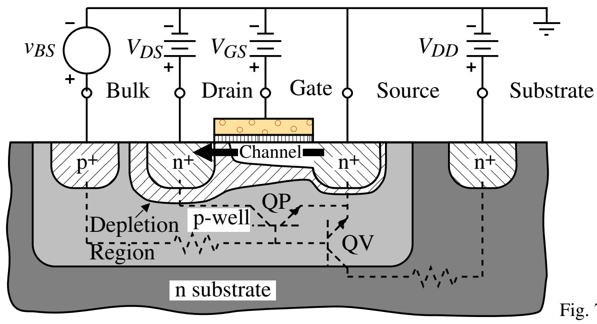


Fig. 7.6-8

Large signal equation:

$$i_D = \frac{K_N'W}{2L}\left[V_{GS} - V_{T0} - \gamma\sqrt{2|\phi_F| - v_{BS}} + \gamma\sqrt{2|\phi_F|}\right]^2$$

Small-signal transconductance:

$$g_{mbs} = \frac{\gamma\sqrt{(2K_N'W/L)I_D}}{2\sqrt{2|\phi_F| - V_{BS}}}$$

Bulk-Driven MOSFET - Continued

Transconductance characteristics:

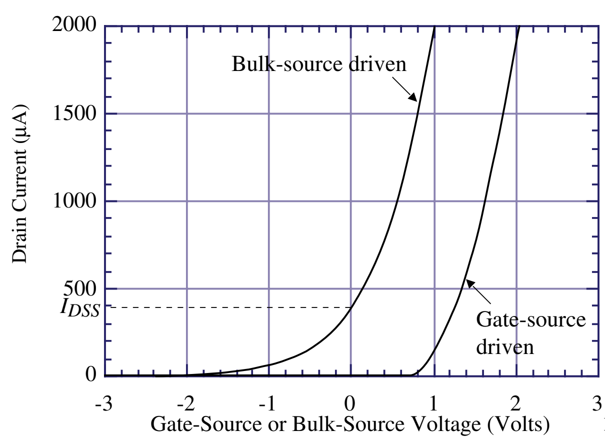


Fig. 7.6-9

Saturation: $V_{DS} > V_{BS} - V_P$ $\Rightarrow$ $V_{BS} = V_P + V_{ON}$ $i_D = I_{DSS}\left(1 - \frac{V_{BS}}{V_P}\right)^2$

Comments:

- g_m (bulk) > g_m(gate) if $V_{BS} > 0$ (forward biased)
- Noise of both configurations are the same (any differences comes from the gate versus bulk noise)
- Bulk-driven MOSFET tends to be more linear at lower currents than the gate-driven MOSFET
- Very useful for generation of I_{DSS} floating current sources.

Bulk-Driven, n-channel Differential Amplifier

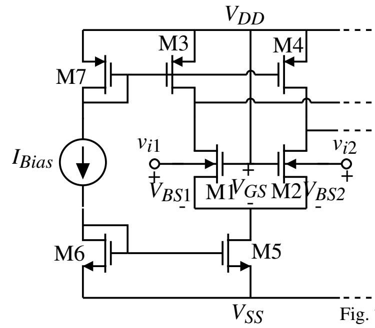


Fig. 7.6-10

What is the *ICMR*?

$V_{icm}(\min) = V_{SS} + V_{DS5}(\text{sat}) + V_{BS1} = V_{SS} + V_{DS5}(\text{sat}) - |V_{P1}| + V_{DS1}(\text{sat})$

Note that V_{icm} can be less than V_{SS} if $|V_{P1}| > V_{DS5}(\text{sat}) + V_{DS1}(\text{sat})$

$V_{icm}(\max) = ?$

As V_{icm} increases, the current through M1 and M2 is constant so the source increases. However, the gate voltage stays constant so that V_{GS1} decreases. Since the current must remain constant through M1 and M2 because of M5, the bulk-source voltage becomes less negative causing V_{TN1} to decrease and maintain the currents through M1 and M2 constant. If V_{icm} is increased sufficiently, the bulk-source voltage will become positive. However, current does not start to flow until V_{BS} is greater than 0.3 volts so the effective $V_{icm}(\max) \approx V_{DD} - V_{SD3}(\text{sat}) - V_{DS1}(\text{sat}) + V_{BS1}$.

Illustration of the *ICMR* of the Bulk-Driven, Differential Amplifier

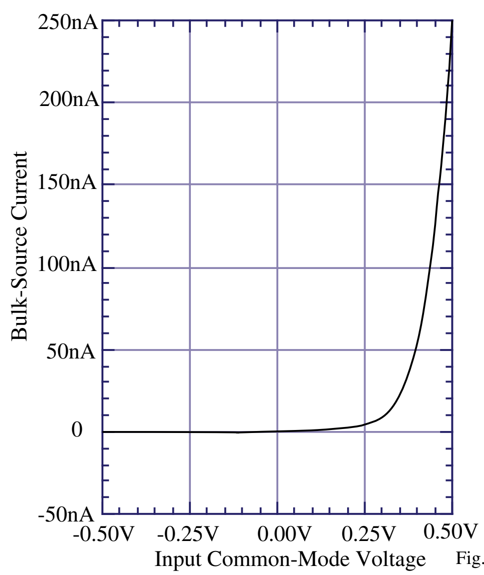


Fig. 7.6-10A

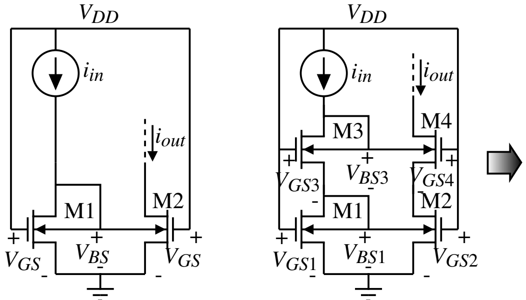
Comments:

- Effective *ICMR* is from V_{SS} to V_{DD} -0.3V
- The transconductance of the input stage can vary as much as 100% over the *ICMR* which makes it very difficult to compensate

Low-Voltage Current Mirrors using the Bulk-Driven MOSFET

The biggest problem with current mirrors is the large minimum input voltage required for previously examined current mirrors.

If the bulk-driven MOSFET is biased with a current that exceeds I_{DSS} then it is enhancement and can be used as a current mirror.



Simple bulk-driven current mirror

Cascodebulk-driven current mirror.

Fig.7.6-11

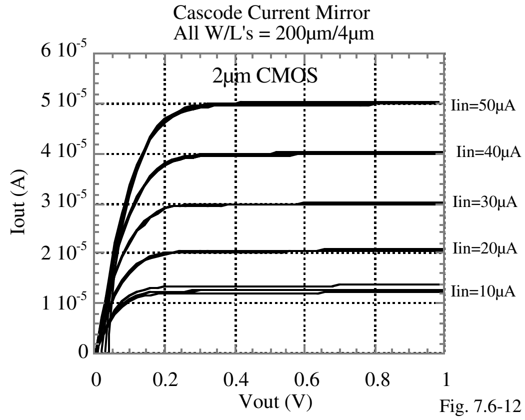


Fig. 7.6-12

The cascode current mirror gives a minimum input voltage of less than 0.5V for currents less than 100µA

Simple Current Mirror with Level Shifting

Since the drain can be V_T less than the gate, the drain could be biased to reduce the minimum input voltage as illustrated.

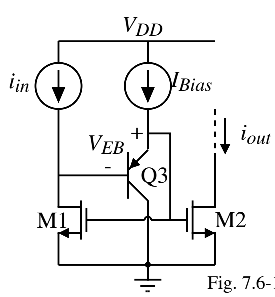


Fig. 7.6-13

A Low-Voltage Current Mirror with Wide Input and Output Swings

The current mirror below requires a power supply of V_T+3V_{ON} and has a V_{in}(min) = V_{ON} and a V_{out}(min) = 2V_{ON} (less for the regulated cascode output mirror).

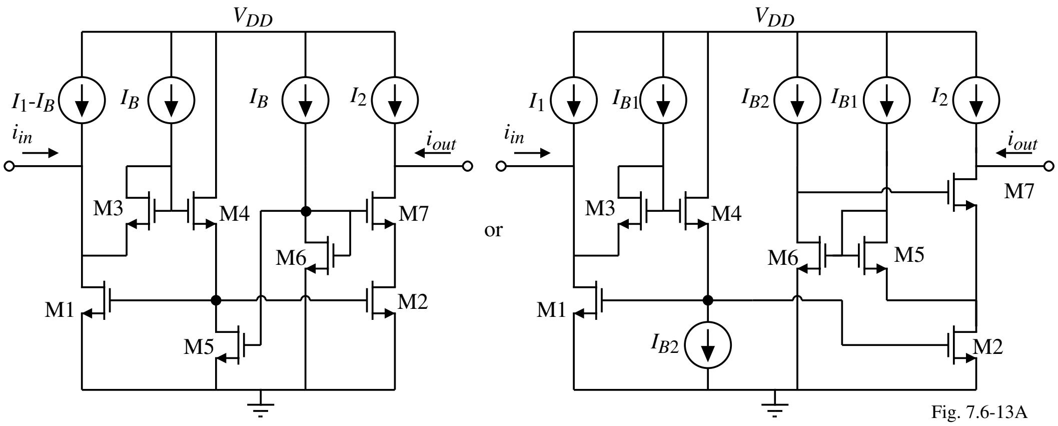
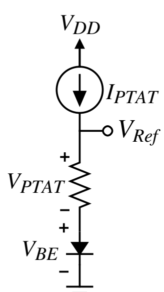
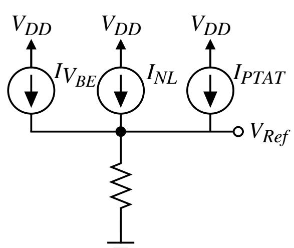


Fig. 7.6-13A

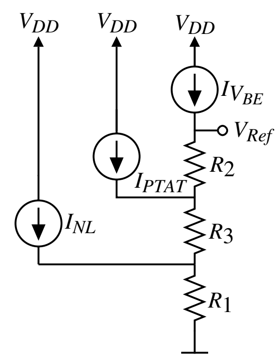
Bandgap Topologies Compatible with Low Voltage Power Supply



Voltage-mode bandgap topology.



Current-mode bandgap topology.



Voltage-current mode bandgap topology.

Fig. 7.6-14

Method of Generating Currents with *VBE* and PTAT Temperature Coefficients

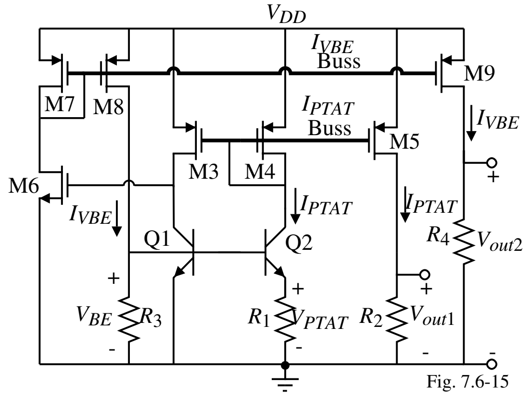
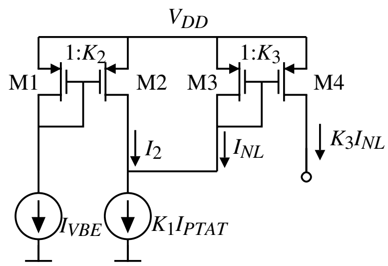


Fig. 7.6-15

$$V_{out1} = I_{PTAT}R_2 = \left(\frac{V_{PTAT}}{R_1}\right)R_2 = V_{PTAT}\frac{R_2}{R_1}$$

$$V_{out2} = I_{VBE}R_4 = \left(\frac{V_{BE}}{R_3}\right)R_4 = V_{BE}\frac{R_4}{R_3}$$

Technique for Canceling the Bandgap Curvature



Circuit to generate nonlinear correction term, I_{NL}.

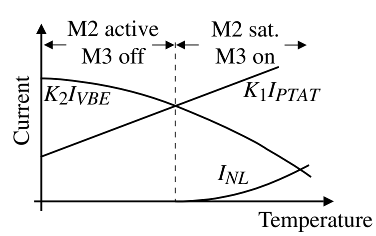


Illustration of the various currents.

Fig. 7.6-16

$$I_{NL} = \begin{cases} 0, & K_2I_{VBE} > K_1I_{PTAT} \\ K_1I_{PTAT} - K_2I_{VBE}, & K_2I_{VBE} < K_1I_{PTAT} \end{cases}$$

The combination of the above concept with the previous slide yielded a curvature-corrected bandgap reference of 0.596V with a TC of 20ppm/C° from -15C° to 90C° using a 1.1V power supply.† In addition, the line regulation was 408 ppm/V for $1.2 \le V_{DD} \le 10$V and 2000 ppm/V for $1.1 \le V_{DD} \le 10$V. The quiescent current was 14μA.

† G.A. Rincon-Mora and P.E. Allen, "A 1.1-V Current-Mode and Piecewise-Linear Curvature-Corrected Bandgap Reference," *J. of Solid-State Circuits*, vol. 33, no. 10, October 1998, pp. 1551-1554.

Low-Voltage Op Amp using Classical Techniques ($V_{DD} \geq 2V_T$)

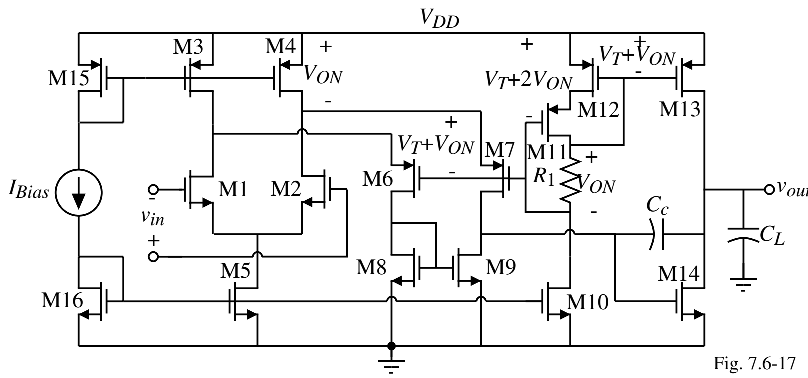


Fig. 7.6-17

Clever use of classical techniques.

Balanced inputs.

Example 7.6-1 - Design of a Low-Voltage Op Amp using the Previous Topology

Use the parameters of Table 3.1-2 to design the op amp above to meet the specifications given below.

V_{DD} = 2V V_{icm}(max) = 2.5V V_{icm}(min) = 1V

V_{out}(max) = 1.75V V_{out}(min) = 0.5V GB = 10MHz

Slew rate = ±10V/μs Phase margin = 60° for C_L = 10pF

Solution

Assuming the conditions for a two-stage op amp necessary to achieve 60° phase margin and that the RHP zero is at least 10*GB* gives

$$C_c = 0.2C_L = 2\text{pF}$$

The slew rate is directly related to the current in M5 and gives

$$I_5 = C_c \cdot SR = 2\text{x}10^{-12} \cdot 10^7 = 20\mu\text{A}$$

We also know the input transconductances from GB and C_c. They are given as

$$g_{m1} = g_{m2} = GB \cdot C_c = 20\pi\text{x}10^6 \cdot 2\text{x}10^{-12} = 125.67\mu\text{S}$$

Knowing the current flow in M1 and M2 gives the W/L ratios as

$$\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{g_{m1}{}^2}{2K_N'(I_1/2)} = \frac{(125.67\text{x}10^{-6})^2}{2 \cdot 110\text{x}10^{-6} \cdot 10\text{x}10^{-6}} = 7.18$$

Example 7.6-1 - Continued

Next, we find the W/L of M5 that will satisfy V_{icm}(min) specification.

$$V_{icm}(\text{min}) = V_{DS5}(\text{sat}) + V_{GS1}(10\mu\text{A}) = 1\text{V}$$

This gives

$$V_{DS5}(\text{sat}) = 1 - \sqrt{\frac{2\cdot 10}{110\cdot 7.18}} - 0.75 = 1\text{-}0.159\text{-}0.75 = 0.0909\text{V}$$

Therefore,

$$V_{DS5}(\text{sat}) = 0.909 = \sqrt{\frac{2\cdot I_5}{K_N'(W_5/L_5)}} \quad\rightarrow\quad \frac{W_5}{L_5} = \frac{2\cdot 20}{110\cdot(0.0909)^2} = 44$$

The design of M3 and M4 is accomplished from the upper input common mode voltage and is

$$V_{icm}(\text{max}) = V_{DD}\text{-}V_{SD3}(\text{sat})+V_{TN} = 2\text{-}V_{SD3}(\text{sat})+0.75 = 2.5\text{V}$$

Solving for V_{SD3}(sat) gives 0.25V. Let us assume that the currents in M6 and M7 are 20µA. This gives a current of 30µA in M3 and M4. Knowing the current in M3 (M4) gives

$$V_{SD3}(\text{sat}) \le \sqrt{\frac{2\cdot 30}{50\cdot(W_3/L_3)}} \quad\rightarrow\quad \frac{W_3}{L_3} = \frac{W_4}{L_4} \ge \frac{2\cdot 30}{(0.25)^2\cdot 50} = 19.2$$

Next, using the V_{SD}(sat) = V_{ON} of M3 and M4, design M10 through M12. Let us assume that I_{10} = I_5 = 20µA which gives W_{10}/L_{10} = 44. R_1 is designed as R_1 = 0.25V/20µA = 12.5kΩ. The W/L ratios of M11 and M12 can be expressed as

$$\frac{W_{11}}{L_{11}} = \frac{W_{12}}{L_{12}} = \frac{2\cdot I_{11}}{K_P'\cdot V_{SD11}(\text{sat})^2} = \frac{2\cdot 20}{50\cdot(0.25)^2} = 12.8$$

Example 7.6-1 - Continued

Since the source-gate voltages and currents of M6 and M7 are the same as M11 and M12 then the W/L values are equal. Thus

$$\frac{W_6}{L_6} = \frac{W_7}{L_7} = 12.8$$

M8 and M9 should be as small as possible to reduce the parasitic (mirror) pole. However, the voltage drop across M4, M6 and M8 must be less than the power supply. Using this to design the gate-source voltage of M8 gives

$$V_{GS8} = V_{DD} - 2V_{ON} = 2\text{V} - 2\cdot 0.25 = 1.5\text{V}$$

Thus,

$$\frac{W_8}{L_8} = \frac{W_9}{L_9} = \frac{2\cdot I_8}{K_N'\cdot V_{DS8}(\text{sat})^2} = \frac{2\cdot 30}{110\cdot(0.75)^2} = 0.97 \approx 1$$

Because M8 and M9 are small, the mirror pole will be insignificant. The next poles of interest would be those at the sources of M6 and M7. Assuming the channel length is 1µm, these poles are given as

$$p_6 \approx \frac{g_{m6}}{C_{GS6}} = \frac{\sqrt{2K_P'\cdot(W_6/L_6)\cdot I_6}}{(2/3)\cdot W_6\cdot L_6\cdot C_{ox}} = \frac{\sqrt{2\cdot 50\cdot 12.8\cdot 20}\text{ x}10^{-6}}{(2/3)\cdot 12.8\cdot 1\cdot 2.47\text{x}10^{-15}} = 7.59\text{x}10^9 \text{ rads/sec}$$

which is about 100 greater than GB.

Finally, the W/L ratios of the second stage must be designed. We can either use the relationship for 60° phase margin of $g_{m14} = 10g_{m1}$ = 1256.7µS or consider proper mirroring between M9 and M14. Combining the equations for saturation region, we get

$$\frac{W}{L} = \frac{g_m}{K_N'\, V_{DS}(\text{sat})}$$

Example 7.6-1 - Continued

Substituting 1256.7µS for g_{m14} and 0.5V for V_{DS14} gives W_{14}/L_{14} = 22.85 which gives I_{14} = 314µA. The W/L of M13 is designed by the necessary current ratio desired between the two transistors and is

$$\frac{W_{13}}{L_{13}} = \frac{I_{13}}{I_{12}} I_{12} = \frac{314}{20} \cdot 12.8 = 201$$

Now, we must check to make sure that the V_{out}(max) is satisfied. The saturation voltage of M13 is

$$V_{SD13}(\text{sat}) = \sqrt{\frac{2 \cdot I_{13}}{K_P' (W_{13}/L_{13})}} = \sqrt{\frac{2 \cdot 314}{50 \cdot 201}} = 0.25\text{V}$$

which exactly meets the specification. For proper mirroring, the W/L ratio of M14 should be

$$\frac{W_9}{L_9} = \frac{I_9}{I_{14}} \frac{W_{14}}{L_{14}} = 1.46$$

Since W_9/L_9 was selected as 1, this is close enough.

Let us check to see what gain is achieved at low frequencies. The parameters are g_{ds7} = 1µS, g_{ds8} = 0.8µS, g_{ds13} = 15.7µS and g_{ds14} = 12.56µS. Therefore small signal voltage gain is

$$\frac{v_{out}}{v_{in}} = \left(\frac{g_{m1}}{g_{ds7}+g_{ds9}}\right)\left(\frac{g_{m14}}{g_{ds13}+g_{ds14}}\right) = \left(\frac{125.6}{1.8}\right)\left(\frac{1256.7}{28.26}\right) = 69.78 \cdot 44.47 = 3103\text{V/V}$$

The power dissipation, including I_{bias} of 20µA, is 708µW. The minimum power supply possible without regard to the input common mode voltage range is $V_T + 3\Delta V$. With V_T = 0.7V and $\Delta V \approx$ 0.25V, this op amp should be capable of operating with a power supply of 1.5V.

A 1-Volt, Two-Stage Op Amp

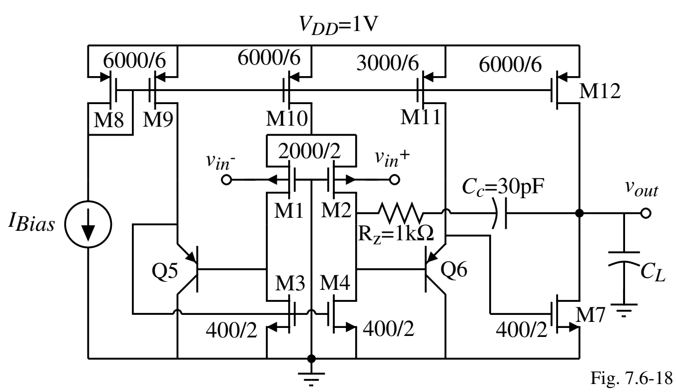


Fig. 7.6-18

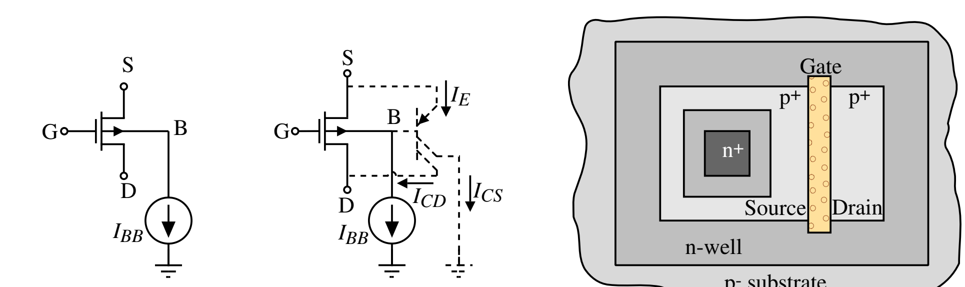
Performance of the 1-Volt, Two-Stage Op Amp

Specification (V_{DD}=0.5V, V_{SS}=-0.5V)	Measured Performance (C_L = 22pF)
DC open-loop gain	49dB (V_{icm} mid range)
Power supply current	300μA
Unity-gainbandwidth (GB)	1.3MHz (V_{icm} mid range)
Phase margin	57° (V_{icm} mid range)
Input offset voltage	±3mV
Input common mode voltage range	-0.475V to 0.450V
Output swing	-0.475V to 0.491V
Positive slew rate	+0.7V/μsec
Negative slew rate	-1.6V/μsec
THD, closed loop gain of -1V/V	-60dB (0.75Vp-p, 1kHz sinewave) -59dB (0.75Vp-p, 10kHz sinewave)
THD, closed loop gain of +1V/V	-59dB (0.75Vp-p, 1kHz sinewave) -57dB (0.75Vp-p, 10kHz sinewave)
Spectral noise voltage density	367nV/$\sqrt{\text{Hz}}$ @ 1kHz 181nV/$\sqrt{\text{Hz}}$ @ 10kHz, 81nV/$\sqrt{\text{Hz}}$ @ 100kHz 444nV/$\sqrt{\text{Hz}}$ @ 1MHz
Positive Power Supply Rejection	61dB at 10kHz, 55dB at 100kHz, 22dB at 1MHz
Negative Power Supply Rejection	45dB at 10kHz, 27dB at 100kHz, 5dB at 1MHz

Further Considerations of the using the Bulk - Current Driven Bulk[†]

The bulk can be used to reduce the threshold sufficiently to permit low voltage applications. The key is to keep the substrate current confined.

One possible technique is:



Reduced Threshold MOSFET Parasitic BJT Layout Fig. 7.6-19

Problem:

Want to limit the BJT current to some value called, I_{max}.

Therefore,

$$I_{BB} = \frac{I_{max}}{\beta_{CS} + \beta_{CD} + 1}$$

† T. Lehmann and M. Cassia, "1V Power Supply CMOS Cascode Amplifier," *IEEE J. of Solid-State Circuits*, Vol. 36, No. 7, 2001

Current-Driven Bulk Technique - Continued

Bias circuit for keeping the I_{max} defined independent of BJT betas.

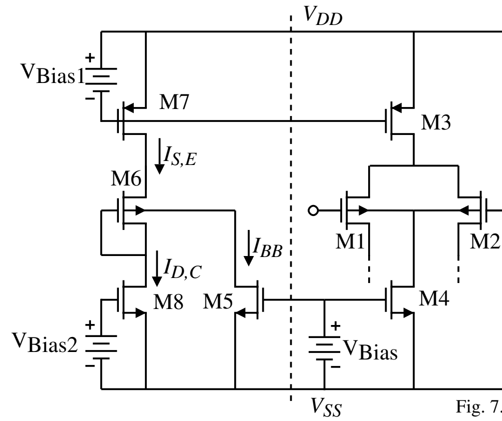


Fig. 7.6-20

Use V_{Bias1} and V_{Bias2} to set $I_{D,C} = 1.1I_D$ and $I_{E,S} = 1.2I_D$ which sets I_{BB} at $0.1I_D$.

A 1-Volt, Folded-Cascode OTA using the Current-Driven Bulk Technique

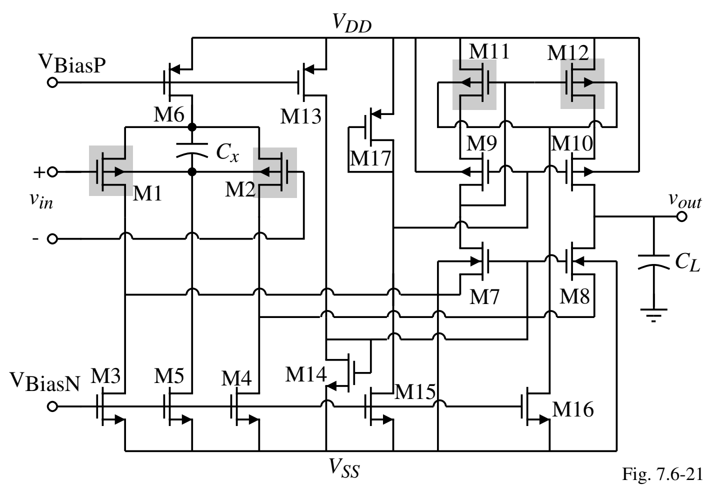


Fig. 7.6-21

Transistors with forward-biased bulks are in a shaded box.

For large common mode input changes, C_x , is necessary to avoid slewing in the input stage.

To get more voltage headroom at the output, the transistors of the cascode mirror have their bulks current driven.

A 1-Volt, Folded-Cascode OTA using the Current-Driven Bulk Technique - Continued

Experimental results:

0.5µm CMOS, 40µA total bias current (C_x = 10pF)

Supply Voltage	1.0V	0.8V	0.7V
Common-mode input range	0.0V-0.65V	0.0V-0.4V	0.0V-0.3V
High gain output range	0.35V-0.75V	0.25V-0.5V	0.2V-0.4V
Output saturation limits	0.1V-0.9V	0.15V-0.65V	0.1V-0.6V
DC gain	62dB-69dB	46dB-53dB	33dB-36dB
Gain-Bandwidth	2.0MHz	0.8MHz	1.3MHz
Slew-Rate (C_L=20pF)	0.5V/µs	0.4V/µs	0.1V/µs
Phase margin (C_L=20pF)	57°	54°	48°

The nominal value of bulk current is 10nA gives a 10% increase in differential pair quiescent current assuming a BJT β of 100.

CHAPTER 7 - SUMMARY

This chapter has considered improved op amp performance in the areas of:

- Op amps that can drive low output load resistances and large output capacitances
- Op amps with improved bandwidth
- Op amps with differential output
- Op amps having low power dissipation
- Op amps having low noise
- Op amps that can work at low voltages

The objective of this chapter has been to show how to improve the performance of an op amp.

- We found that improvements are always possible
- The key is to balance the tradeoffs against the particular performance improvement
- This chapter is an excellent example of the degrees of freedom and choices that different circuit architectures can offer.

We also illustrated further the approaches to designing op amps

The next chapter begins the transition from analog to digital with the introduction of the comparator.

