CHAPTER 5 - CMOS AMPLIFIERS

Chapter Outline

5.1 Inverters
5.2 Differential Amplifiers
5.3 Cascode Amplifiers
5.4 Current Amplifiers
5.5 Output Amplifiers
5.6 High-Gain Architectures

Goal

To develop an understanding of the amplifier building blocks used in CMOS analog circuit design.

Design Hierarchy

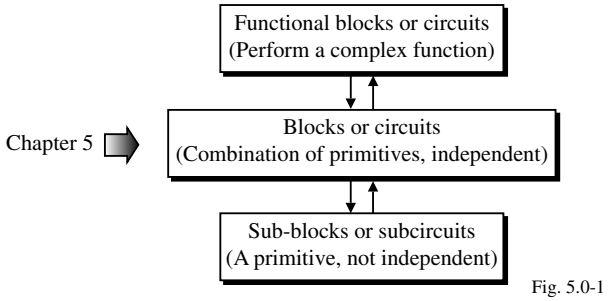


Fig. 5.0-1

Illustration of Hierarchy in Analog Circuits for an Op Amp

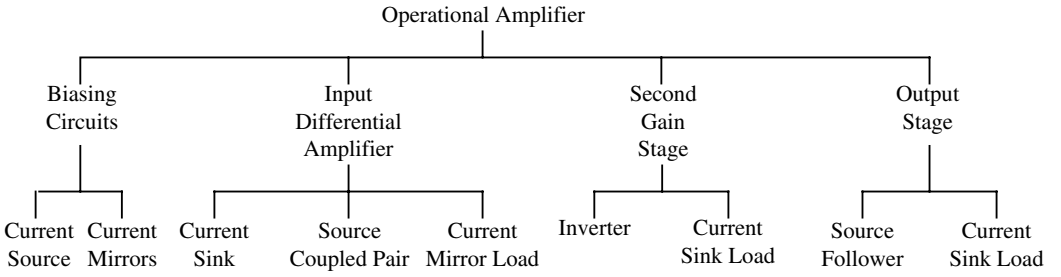


Fig. 5.0-2

SECTION 5.1 - CMOS INVERTING AMPLIFIERS

Characterization of Amplifiers

Amplifiers will be characterized by the following properties:

- Large-signal voltage transfer characteristics
- Large-signal voltage swing limitations
- Small-signal, frequency independent performance
  - Gain
  - Input resistance
  - Output resistance
- Small-signal, frequency response
- Other properties
  - Noise
  - Power dissipation
  - Etc.

Inverters

The inverting amplifier is an amplifier which amplifies and inverts the input signal. The inverting amplifier generally has the source on ac ground or the common-source configuration.

Various types of inverting CMOS amplifiers:

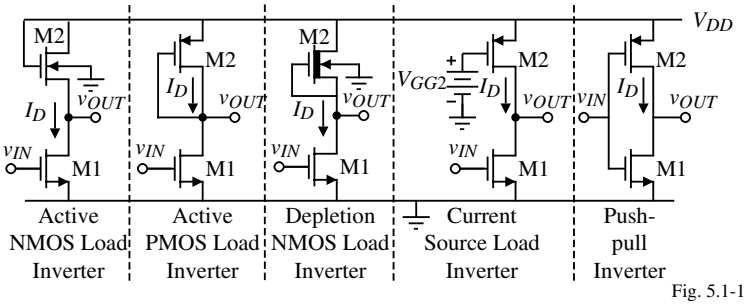


Fig. 5.1-1

We will consider:

- Active PMOS Load Inverter (active load inverter)
- Current Source Load Inverter
- Push-pull Inverter

Voltage Transfer Characteristic of the Active Load Inverter

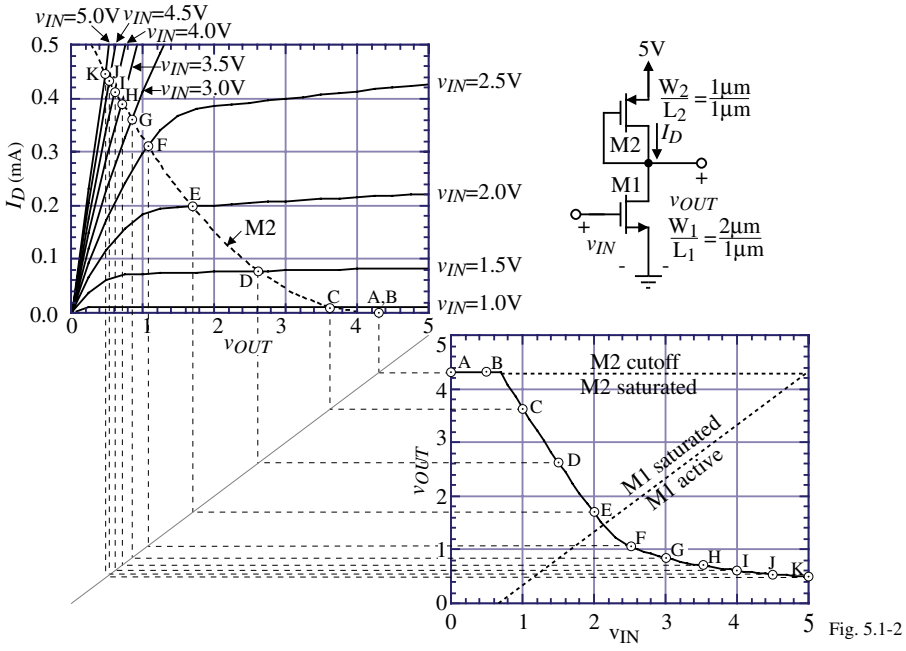


Fig. 5.1-2

The boundary between active and saturation operation for M1 is

$$v_{DS1} \geq v_{GS1} - V_{TN} \quad \rightarrow \quad v_{OUT} \geq v_{IN} - 0.7\text{V}$$

Large-Signal Voltage Swing Limits of the Active Load Inverter

Maximum output voltage, v_{OUT}(max):

$$\boxed{v_{OUT}(\text{max}) \cong V_{DD} - |V_{TP}|}$$

(ignores subthreshold current influence on the MOSFET)

Minimum output voltage, v_{OUT}(min):

Assume that M1 is nonsaturated and that $V_{T1} = |V_{T2}| = V_T$.

$$v_{DS1} \geq v_{GS1} - V_{TN} \quad \rightarrow \quad v_{OUT} \geq v_{IN} - 0.7\text{V}$$

The current through M1 is

$$i_D = \beta_1\left((v_{GS1} - V_T)v_{DS1} - \frac{v_{DS1}^2}{2}\right) = \beta_1\left((V_{DD} - V_T)(v_{OUT}) - \frac{(v_{OUT})^2}{2}\right)$$

and the current through M2 is

$$i_D = \frac{\beta_2}{2}(v_{SG2} - V_T)^2 = \frac{\beta_2}{2}(V_{DD} - v_{\text{OUT}} - V_T)^2 = \frac{\beta_2}{2}(v_{OUT} + V_T - V_{DD})^2$$

Equating these currents gives the minimum v_{OUT} as,

$$\boxed{v_{OUT}(\text{min}) = V_{DD} - V_T - \frac{V_{DD} - V_T}{\sqrt{1 + (\beta_2/\beta_1)}}}$$

Small-Signal Midband Performance of the Active Load Inverter

The development of the small-signal model for the active load inverter is shown below:

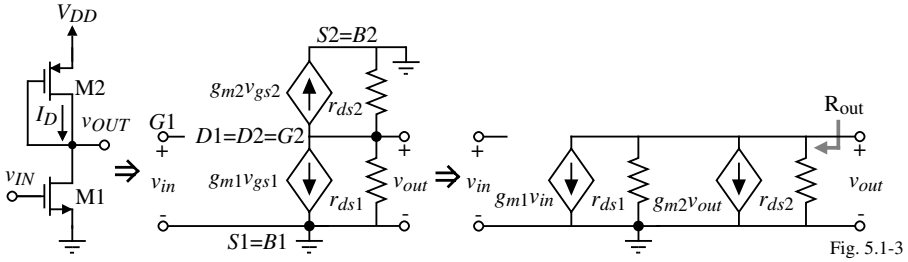


Fig. 5.1-3

Sum the currents at the output node to get,

$$g_{m1}v_{in} + g_{ds1}v_{out} + g_{m2}v_{out} + g_{ds2}v_{out} = 0$$

Solving for the voltage gain, v_{out}/v_{in}, gives

$$\frac{v_{\text{out}}}{v_{\text{in}}} = \frac{-g_{m1}}{g_{ds1} + g_{ds2} + g_{m2}} \cong -\frac{g_{m1}}{g_{m2}} = -\left(\frac{K'_N W_1 L_2}{K'_P L_1 W_2}\right)^{1/2}$$

The small-signal output resistance can also be found from the above by letting $v_{in} = 0$ to get,

$$R_{\text{out}} = \frac{1}{g_{ds1} + g_{ds2} + g_{m2}} \cong \frac{1}{g_{m2}}$$

Frequency Response of the Active Load Inverter

Incorporation of the parasitic capacitors into the small-signal model (x is connected to v_{out}):

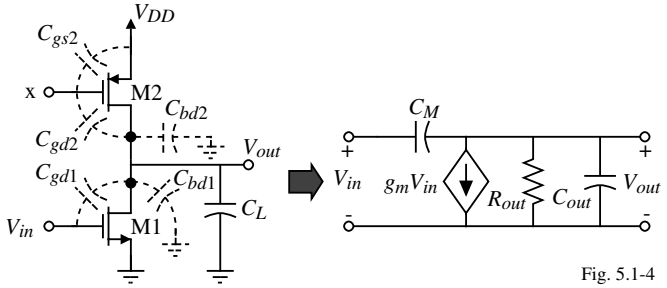


Fig. 5.1-4

If we assume the input voltage has a small source resistance, then we can write the following:

$$\frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = \frac{-g_m R_{out}\left(1 - \frac{s}{z_1}\right)}{1 - \frac{s}{p_1}}$$

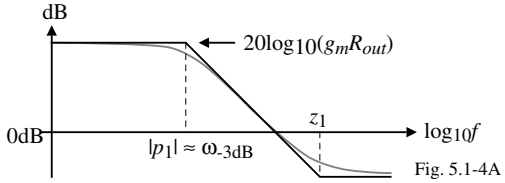


Fig. 5.1-4A

where

$$g_m = g_{m1}, \quad p_1 = \frac{-1}{R_{out}(C_{out}+C_M)}, \quad \text{and}$$

$$z_1 = \frac{g_m}{C_M}$$

and

$$R_{out} = [g_{ds1} + g_{ds2} + g_{m2}]^{-1} \cong 1/g_m, \quad C_M = C_{gd1}, \quad \text{and} \quad C_{out} = C_{bd1} + C_{bd2} + C_{gs2} + C_L$$

If $|p_1| < z_1$, then the -3dB frequency is approximately equal to $[R_{out}(C_{out}+C_M)]^{-1}$.

Example 5.1-1 - Performance of an Active Resistor-Load Inverter

Calculate the output-voltage swing limits for V_{DD} = 5 volts, the small-signal gain, the output resistance, and the -3 dB frequency of active load inverter if (W_1/L_1) is 2 µm/1 µm and W_2/L_2 = 1 µm/1 µm, C_{gd1} = 100fF, C_{bd1} = 200fF, C_{bd2} = 100fF, C_{gs2} = 200fF, C_L = 1 pF, and $I_{D1} = I_{D2}$ = 100µA, using the parameters in Table 3.1-2.

Solution

From the above results we find that:

v_{OUT}(max) = 4.3 volts

v_{OUT}(min) = 0.418 volts

Small-signal voltage gain = -1.92V/V

R_{out} = 9.17 kΩ including g_{ds1} and g_{ds2} and 10 kΩ ignoring g_{ds1} and g_{ds2}

z_1 = 2.10x10^9 rads/sec

p_1 = -64.1x10^6 rads/sec.

Thus, the -3 dB frequency is 10.2 MHz.

Voltage Transfer Characteristic of the Current Source Inverter

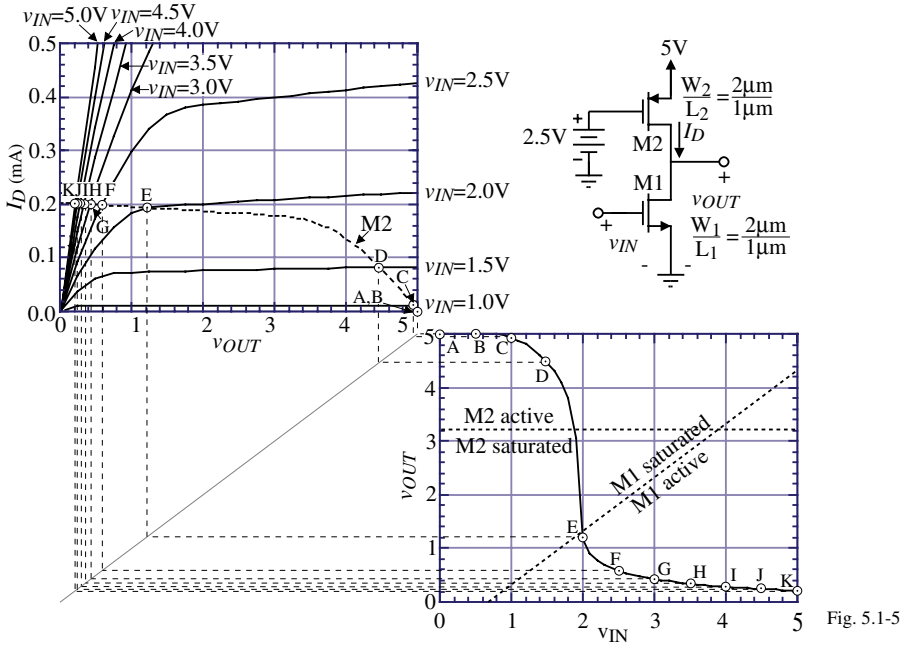


Fig. 5.1-5

Regions of operation for the transistors:

M1: $v_{DS1} \geq v_{GS1} - V_{Tn} \rightarrow v_{OUT} \geq v_{IN} - 0.7V$

M2: $v_{SD2} \geq v_{SG2} - |V_{Tp}| \rightarrow V_{DD} - v_{OUT} \geq V_{DD} - V_{GG2} - |V_{Tp}| \rightarrow v_{OUT} \leq 3.2V$

Large-Signal Voltage Swing Limits of the Current Source Load Inverter

Maximum output voltage, v_{OUT}(max):

$$\boxed{v_{OUT}(\max) \cong V_{DD}}$$

Minimum output voltage, v_{OUT}(min):

Assume that M1 is nonsaturated. The minimum output voltage is,

$$v_{OUT}(\min) = \boxed{v_{OUT}(\min) = (V_{DD} - V_{T1})\left[1 - \sqrt{1 - \left(\frac{\beta_2}{\beta_1}\right)\left(\frac{V_{DD} - V_{GG} - |V_{T2}|}{V_{DD} - V_{T1}}\right)^2}\right]}$$

This result assumes that v_{IN} is taken to V_{DD}.

Small-Signal Midband Performance of the Current Source Load Inverter

Small-Signal Model:

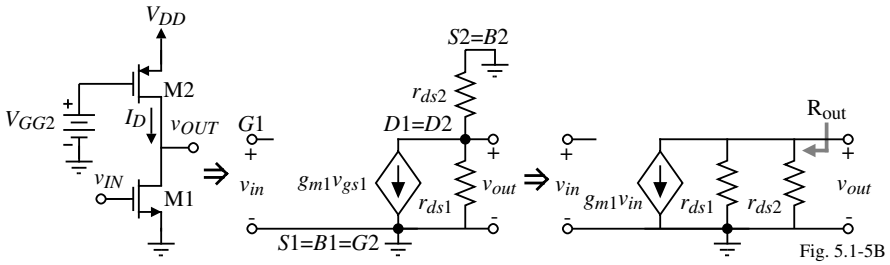


Fig. 5.1-5B

Midband Performance:

$$\frac{v_{\text{out}}}{v_{\text{in}}} = \frac{-g_{m1}}{g_{ds1} + g_{ds2}} = \left(\frac{2K'_N W_1}{L_1 I_D}\right)^{1/2}\left(\frac{-1}{\lambda_1 + \lambda_2}\right) \propto \frac{1}{\sqrt{I_D}} \quad \text{!!!} \quad \text{and} \quad R_{\text{out}} = \frac{1}{g_{ds1} + g_{ds2}} \cong \frac{1}{I_D(\lambda_1 + \lambda_2)}$$

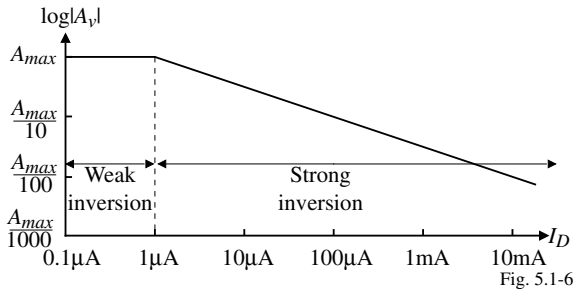


Fig. 5.1-6

Frequency Response of the Current Source Load Inverter

Incorporation of the parasitic capacitors into the small-signal model (x is connected to V_{GG2}):

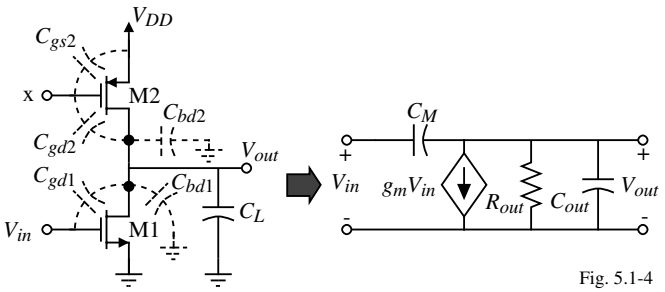


Fig. 5.1-4

If we assume the input voltage has a small source resistance, then we can write the following:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{-g_m R_{out}\left(1 - \frac{s}{z_1}\right)}{1 - \frac{s}{p_1}}$$

where $g_m = g_{m1}$, $p_1 = \frac{-1}{R_{out}(C_{out}+C_M)}$, and $z_1 = \frac{g_m}{C_M}$

and $R_{out} = \frac{1}{g_{ds1} + g_{ds2}}$ and $C_{out} = C_{gd2} + C_{bd1} + C_{bd2} + C_L$ $C_M = C_{gd1}$

Therefore, if $|p_1|<|z_1|$, then the −3 dB frequency response can be expressed as

$$\omega_{-3dB} \approx \omega_1 = \frac{g_{ds1} + g_{ds2}}{C_{gd1} + C_{gd2} + C_{bd1} + C_{bd2} + C_L}$$

Example 5.1-2 - Performance of a Current-Sink Inverter

The performance of a current-sink CMOS inverter is to be examined. The current-sink inverter is shown in Fig. 5.1-7. Assume that $W_1 = 2\ \mu$m, $L_1 = 1\ \mu$m, $W_2 = 1\ \mu$m, $L_2 = 1\mu$m, $V_{DD} = 5$ volts, $V_{GG1} = 3$ volts, and the parameters of Table 3.1-2 describe M1 and M2. Use the capacitor values of Example 5.1-1 ($C_{gd1} = C_{gd2}$). Calculate the output-swing limits and the small-signal performance.

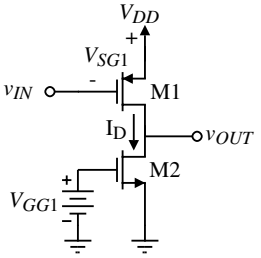


Figure 5.1-7 Current sink CMOS inverter.

Solution

To attain the output signal-swing limitations, we treat Fig. 5.1-7 as a current source CMOS inverter with PMOS parameters for the NMOS and NMOS parameters for the PMOS and use NMOS equations. Using a prime notation to designate the results of the current source CMOS inverter which exchanges the PMOS and NMOS model parameters, we get

$$v_{OUT}(\text{max})' = 5\text{V} \quad \text{and} \quad v_{OUT}(\text{min})' = (5\text{-}0.7)\left[1 - \sqrt{1 - \left(\frac{110\cdot 1}{50\cdot 2}\right)\left(\frac{3\text{-}0.7}{5\text{-}0\text{-}0.7}\right)^2}\right] = 0.74\text{V}$$

In terms of the current sink CMOS inverter, these limits are subtracted from 5V to get

$$v_{OUT}(\text{max}) = 4.26\text{V} \quad \text{and} \quad v_{OUT}(\text{min}) = 0\text{V}.$$

To find the small signal performance, we must first calculate the dc current. The dc current, I_D, is

$$I_D = \frac{K_N' W_1}{2L_1}(V_{GG1}\text{-}V_{TN})^2 = \frac{110\cdot 1}{2\cdot 1}(3\text{-}0.7)^2 = 291\mu\text{A}$$

$v_{out}/v_{in} = -9.2$V/V, $R_{out} = 38.1$ kΩ, and $f_{-3dB} = 2.78$ MHz.

Voltage Transfer Characteristic of the Push-Pull Inverter

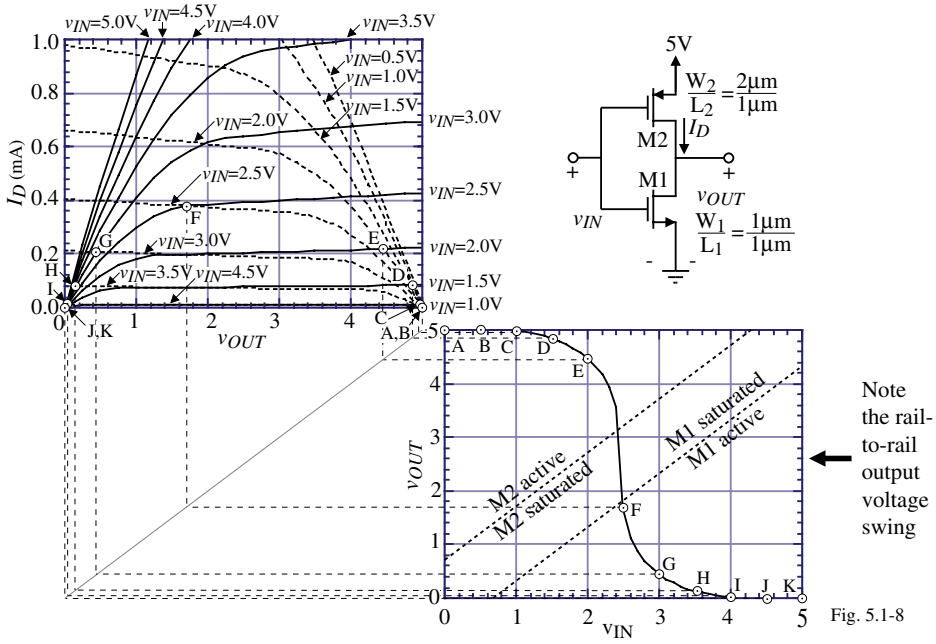


Fig. 5.1-8

Regions of operation for M1 and M2:

M1: $v_{DS1} \geq v_{GS1} - V_{T1} \rightarrow \quad v_{OUT} \geq v_{IN} - 0.7\text{V}$

M2: $v_{SD2} \geq v_{SG2} - |V_{T2}| \rightarrow V_{DD} - v_{OUT} \geq V_{DD} - v_{IN} - |V_{T2}| \rightarrow v_{OUT} \leq v_{IN} + 0.7\text{V}$

Small-Signal Performance of the Push-Pull Amplifier

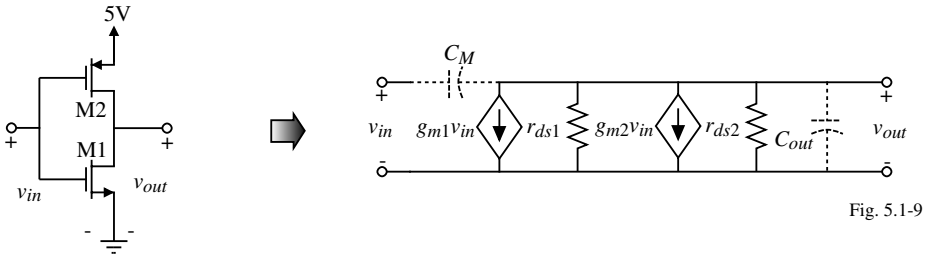


Fig. 5.1-9

Small-signal analysis gives the following results:

$$\frac{v_{out}}{v_{in}} = \frac{-(g_{m1}+g_{m2})}{g_{ds1}+g_{ds2}} = -\sqrt{(2/I_D)}\left[\frac{\sqrt{K'_N(W_1/L_1)}+\sqrt{K'_P(W_2/L_2)}}{\lambda_1+\lambda_2}\right]$$

$$R_{out} = \frac{1}{g_{ds1}+g_{ds2}}$$

$$z = \frac{g_{m1}+g_{m2}}{C_M} = \frac{g_{m1}+g_{m2}}{C_{gd1}+C_{gd2}}$$

and

$$p_1 = \frac{-(g_{ds1}+g_{ds2})}{C_{gd1}+C_{gd2}+C_{bd1}+C_{bd2}+C_L}$$

If $z_1 > |p_1|$, then

$$\omega_{-3\text{dB}} = \frac{g_{ds1}+g_{ds2}}{C_{gd1}+C_{gd2}+C_{bd1}+C_{bd2}+C_L}$$

Example 5.1-3 - Performance of a Push-Pull Inverter

The performance of a push-pull CMOS inverter is to be examined. Assume that $W_1 = 1\ \mu$m, $L_1 = 1\ \mu$m, $W_2 = 2\ \mu$m, $L_2 = 1\mu$m, $V_{DD} = 5$ volts, and use the parameters of Table 3.1-2 to model M1 and M2. Use the capacitor values of Example 5.1-1 ($C_{gd1} = C_{gd2}$). Calculate the output-swing limits and the small-signal performance assuming that $I_{D1} = I_{D2} = 300\mu$A.

Solution

The output swing is seen to be from 0V to 5V. In order to find the small signal performance, we will make the important assumption that both transistors are operating in the saturation region. Therefore:

$$\frac{v_{out}}{v_{in}} = \frac{-257\mu S - 245\mu S}{12\mu S + 15\mu S} = -18.6 V/V$$

$$R_{out} = 37\ k\Omega$$

$$f_{-3dB} = 2.86\ MHz$$

and

$$z_1 = 399\ MHz$$

Noise Analysis of Inverting Amplifiers

Noise model:

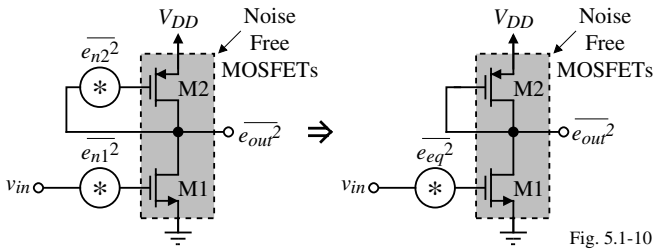


Fig. 5.1-10

Approach:

1.) Assume a mean-square input-voltage-noise spectral density $\overline{e_n^2}$ in series with the gate of each MOSFET. (This step assumes that the MOSFET is the common source configuration.)

2.) Calculate the output-voltage-noise spectral density, $\overline{e_{out}^2}$ (Assume all sources are additive).

3.) Refer the output-voltage-noise spectral density back to the input to get equivalent input noise $\overline{e_{eq}^2}$.

4.) Substitute the type of noise source, 1/f or thermal.

Noise Analysis of the Active Load Inverter

1.) See model to the right.

2.) $\overline{e_{out}}^2 = \overline{e_{n1}}^2 \left(\frac{g_{m1}}{g_{m2}}\right)^2 + \overline{e_{n2}}^2$

3.) $\overline{e_{eq}}^2 = \overline{e_{n1}}^2 \left[1 + \left(\frac{g_{m2}}{g_{m1}}\right)^2 \left(\frac{\overline{e_{n2}}}{\overline{e_{n1}}}\right)^2\right]$

Up to this point, the type of noise is not defined.

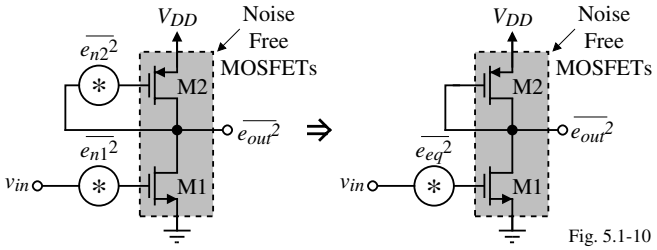


Fig. 5.1-10

1/f Noise

Substituting $\overline{e_n^2} = \frac{KF}{2fC_{ox}WLK'} = \frac{B}{fWL}$, into the above gives,

$$\overline{e_{eq\ (1/f)}} = \left(\frac{B_1}{fW_1L_1}\right)^{1/2}\left[1 + \left(\frac{K'_2B_2}{K'_1B_1}\right)\left(\frac{L_1}{L_2}\right)^2\right]^{1/2}$$

To minimize 1/f noise, 1.) Make $L_2 >> L_1$, 2.) increase the value of W_1 and 3.) choose M1 as a PMOS.

Thermal Noise

Substituting $\overline{e_n^2} = \frac{8kT}{3g_m}$ into the above gives,

$$\overline{e_{eq\ (th)}} = \left\{\left(\frac{8kT(1+\eta_1)}{3[2K'_1(W/L)_1I_1]^{1/2}}\right)\left[1 + \left(\frac{W_2L_1K'_2}{L_2W_1K'_1}\right)^{1/2}\right]\right\}^{1/2}$$

To minimize thermal noise, maximize the gain of the inverter.

Noise Analysis of the Active Load Inverter - Continued

When calculating the contribution of $\overline{e_{n2}^2}$ to $\overline{e_{out}^2}$, it was assumed that the gain was unity. To verify this assumption consider the following model:

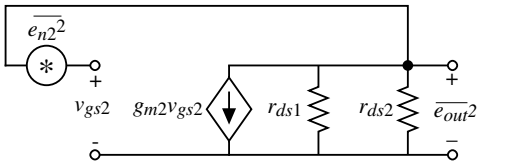


Fig. 5.1-11

We can show that,

$$\frac{\overline{e_{out}}^2}{\overline{e_{n2}}^2} = \left[\frac{g_{m2}(r_{ds1}\|r_{ds2})}{1 + g_{m2}(r_{ds1}\|r_{ds2})}\right]^2 \approx 1$$

Noise Analysis of the Current Source Load Inverting Amplifier

Model:

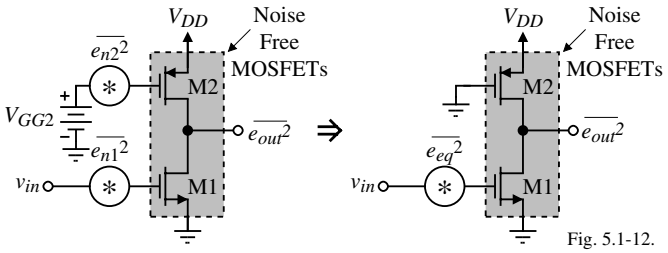


Fig. 5.1-12.

The output-voltage-noise spectral density of this inverter can be written as,

$$\overline{e_{out}}^2 = (g_{m1}r_{out})^2\,\overline{e_{n1}}^2 + (g_{m2}r_{out})^2\,\overline{e_{n2}}^2$$

or

$$\overline{e_{eq}}^2 = \overline{e_{n1}}^2 + \frac{(g_{m2}r_{out})^2}{(g_{m1}r_{out})^2}\overline{e_{n2}}^2 = \overline{e_{n1}}^2\left[1 + \left(\frac{g_{m2}}{g_{m1}}\right)^2 \frac{\overline{e_{n2}}^2}{\overline{e_{n1}}^2}\right]$$

This result is identical with the active load inverter.

Thus the noise performance of the two circuits are equivalent although the small-signal voltage gain is significantly different.

Noise Analysis of the Push-Pull Amplifier

Model:

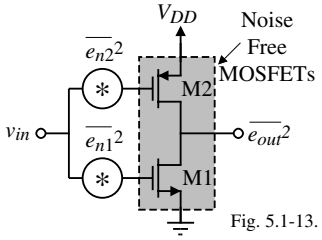


Fig. 5.1-13.

The equivalent input-voltage-noise spectral density of the push-pull inverter can be found as

$$\overline{e_{eq}} = \sqrt{\left(\frac{g_{m1}\,\overline{e_{n1}}}{g_{m1}+g_{m2}}\right)^2 + \left(\frac{g_{m2}\,\overline{e_{n2}}}{g_{m1}+g_{m2}}\right)^2}$$

If the two transconductances are balanced ($g_{m1} = g_{m2}$), then the noise contribution of each device is divided by two.

The total noise contribution can only be reduced by reducing the noise contribution of each device.

(Basically, both M1 and M2 act like the "load" transistor and "input" transistor, so there is no defined input transistor that can cause the noise of the load transistor to be insignificant.)

Summary of CMOS Inverting Amplifiers

Inverter	AC Voltage Gain	AC Output Resistance	Bandwidth (C_{GB}=0)	Equivalent, input-referred,mean-square noise voltage
p-channel active load inverter	$\frac{-g_{m1}}{g_{m2}}$	$\frac{1}{g_{m2}}$	$\frac{g_{m2}}{C_{BD1}+C_{GS1}+C_{GS2}+C_{BD2}}$	$\overline{e_{n1}}^2 + \overline{e_{n2}}^2\left(\frac{g_{m2}}{g_{m1}}\right)^2$
n-channel active load inverter	$\frac{-g_{m1}}{g_{m2}+g_{mb2}}$	$\frac{1}{g_{m2}+g_{mb2}}$	$\frac{g_{m2}+g_{mb2}}{C_{BD1}+C_{GD1}+C_{GS2}+C_{BS2}}$	$\overline{e_{n1}}^2 + \overline{e_{n2}}^2\left(\frac{g_{m2}}{g_{m1}}\right)^2$
Current source load inverter	$\frac{-g_{m1}}{g_{ds1}+g_{ds2}}$	$\frac{1}{g_{ds1}+g_{ds2}}$	$\frac{g_{ds1}+g_{ds2}}{C_{BD1}+C_{GD1}+C_{DG2}+C_{BD2}}$	$\overline{e_{n1}}^2 + \overline{e_{n2}}^2\left(\frac{g_{m2}}{g_{m1}}\right)^2$
n-channel depletion load inverter	$\sim\frac{-g_{m1}}{g_{mb2}}$	$\frac{1}{g_{mb2}+g_{ds1}+g_{ds2}}$	$\frac{g_{mb2}+g_{ds1}+g_{ds2}}{C_{BD1}+C_{GD1}+C_{GS2}+C_{BD2}}$	$\overline{e_{n1}}^2 + \overline{e_{n2}}^2\left(\frac{g_{m2}}{g_{m1}}\right)^2$
Push-Pull inverter	$\frac{-(g_{m1}+g_{m2})}{g_{ds1}+g_{ds2}}$	$\frac{1}{g_{ds1}+g_{ds2}}$	$\frac{g_{ds1}+g_{ds2}}{C_{BD1}+C_{GD1}+C_{GS2}+C_{BD2}}$	$\left(\frac{\overline{e_{n1}}g_{m1}}{g_{m1}+g_{m2}}\right)^2 + \left(\frac{\overline{e_{n2}}g_{m2}}{g_{m1}+g_{m2}}\right)^2$

Inverting configurations we did not examine.

SECTION 5.2 - DIFFERENTIAL AMPLIFIERS

What is a Differential Amplifier?

A differential amplifier is an amplifier that amplifies the difference between two voltages and rejects the average or common mode value of the two voltages.

Symbol for a differential amplifier:

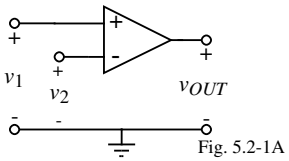


Fig. 5.2-1A

Differential and common mode voltages:

v_1 and v_2 are called *single-ended* voltages. They are voltages referenced to ac ground.

The *differential-mode* input voltage, v_{ID}, is the voltage difference between v_1 and v_2.

The *common-mode* input voltage, v_{IC}, is the average value of v_1 and v_2.

$$\therefore \quad v_{ID} = v_1 - v_2 \quad \text{and} \quad v_{IC} = \frac{v_1+v_2}{2} \quad \Rightarrow \quad v_1 = v_{IC} + 0.5v_{ID} \quad \text{and} \quad v_2 = v_{IC} - 0.5v_{ID}$$

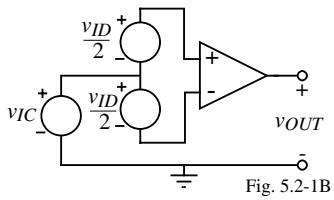


Fig. 5.2-1B

$$v_{OUT} = A_{VD}v_{ID} \pm A_{VC}v_{IC} = A_{VD}(v_1 - v_2) \pm A_{VC}\left(\frac{v_1 + v_2}{2}\right)$$

where

A_{VD} = differential-mode voltage gain

A_{VC} = common-mode voltage gain

Differential Amplifier Definitions

- Common mode rejection rato (*CMRR*)

$$CMRR = \left|\frac{A_{VD}}{A_{VC}}\right|$$

CMRR is a measure of how well the differential amplifier rejects the common-mode input voltage in favor of the differential-input voltage.

- Input common-mode range (*ICMR*)

The input common-mode range is the range of common-mode voltages over which the differential amplifier continues to sense and amplify the difference signal with the same gain.

Typically, the *ICMR* is defined by the common-mode voltage range over which all MOSFETs remain in the saturation region.

- Output offset voltage (V_{OS}(out))

The output offset voltage is the voltage which appears at the output of the differential amplifier when the input terminals are connected together.

- Input offset voltage (V_{OS}(in) = V_{OS})

The input offset voltage is equal to the output offset voltage divided by the differential voltage gain.

$$V_{OS} = \frac{V_{OS}(\text{out})}{A_{VD}}$$

Transconductance Characteristic of the Differential Amplifier

Consider the following n-channel differential amplifier (sometimes called a source-coupled pair):

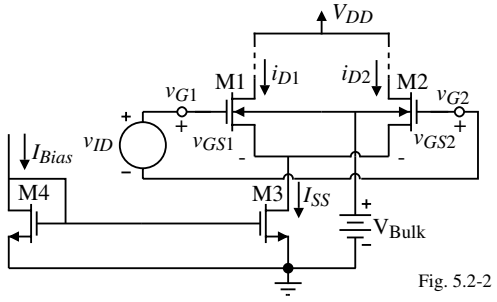


Fig. 5.2-2

Where should bulk be connected? Consider a p-well, CMOS technology,

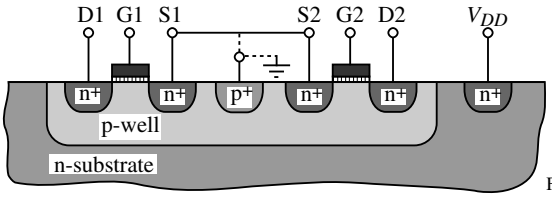


Fig. 5.2-3

1.) Bulks connected to the sources: No modulation of V_T but large common mode parasitic capacitance.

2.) Bulks connected to ground: Smaller common mode parasitic capacitors, but modulation of V_T.

If the technology is n-well CMOS, there is no choice. The bulks must be connected to ground.

Transconductance Characteristic of the Differential Amplifier - Continued

Defining equations:

$$v_{ID} = v_{GS1} - v_{GS2} = \left(\frac{2i_{D1}}{\beta}\right)^{1/2} - \left(\frac{2i_{D2}}{\beta}\right)^{1/2} \qquad \text{and} \qquad I_{SS} = i_{D1} + i_{D2}$$

Solution:

$$i_{D1} = \frac{I_{SS}}{2} + \frac{I_{SS}}{2}\left(\frac{\beta v_{ID}^2}{I_{SS}} - \frac{\beta^2 v_{ID}^4}{4I_{SS}^2}\right)^{1/2} \qquad \text{and} \qquad i_{D2} = \frac{I_{SS}}{2} - \frac{I_{SS}}{2}\left(\frac{\beta v_{ID}^2}{I_{SS}} - \frac{\beta^2 v_{ID}^4}{4I_{SS}^2}\right)^{1/2}$$

which are valid for $v_{ID} < (2I_{SS}/\beta)^{1/2}$.

Illustration of the result:

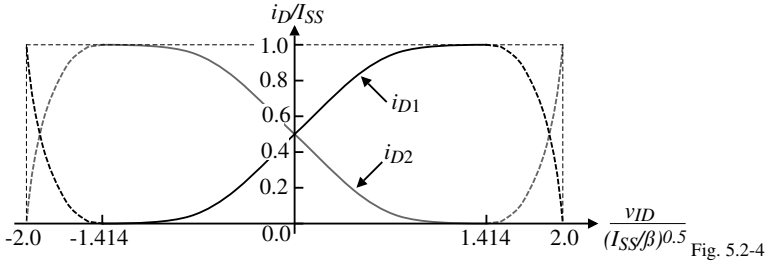


Fig. 5.2-4

Differentiating i_{D1} (or i_{D2}) with respect to v_{ID} and setting V_{ID} =0V gives

$$g_m = \frac{di_{D1}}{dv_{ID}}(V_{ID} = 0) = (\beta I_{SS}/4)^{1/2} = \left(\frac{K'_1 I_{SS} W_1}{4L_1}\right)^{1/2} \qquad \text{(half the } g_m \text{ of an inverting amplifier)}$$

Voltage Transfer Characteristic of the Differential Amplifier

In order to obtain the voltage transfer characteristic, a load for the differential amplifier must be defined. We will select a current mirror load as illustrated below.

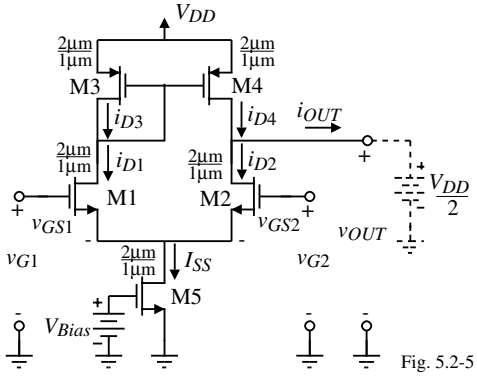


Fig. 5.2-5

Note that output signal to ground is equivalent to the differential output signal due to the current mirror.

The short-circuit, transconductance is given as

$$g_m = \frac{di_{OUT}}{dv_{ID}}(V_{ID} = 0) = (\beta I_{SS})^{1/2} = \left(\frac{K'_1 I_{SS} W_1}{L_1}\right)^{1/2}$$

Voltage Transfer Function of the Differential Amplifer with a Current Mirror Load

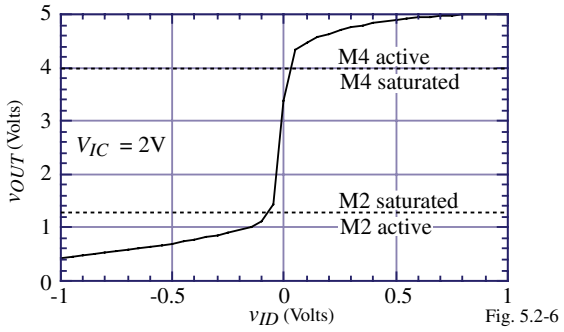


Fig. 5.2-6

Regions of operation of the transistors:

M2 is saturated when,

$$v_{DS2} \geq v_{GS2} - V_{TN} \rightarrow v_{OUT} - V_{S1} \geq V_{IC} - 0.5v_{ID} - V_{S1} - V_{TN} \rightarrow v_{OUT} \geq V_{IC} - V_{TN}$$

where we have assumed that the region of transition for M2 is close to $v_{ID} = 0$V.

M4 is saturated when,

$$v_{SD4} \geq v_{SG4} - |V_{TP}| \rightarrow V_{DD} - v_{OUT} \geq V_{SG4} - |V_{TP}| \rightarrow v_{OUT} \leq V_{DD} - V_{SG4} + |V_{TP}|$$

The regions of operations shown on the voltage transfer function assume $I_{SS} = 100\mu A$.

Note: $V_{SG4} = \sqrt{\frac{2 \cdot 50}{50 \cdot 2}} + |V_{TP}| = 1 + |V_{TP}| \quad \Rightarrow \quad v_{OUT} \leq 5 - 1 - 0.7 + 0.7 = 4\text{V}$

Differential Amplifier Using p-channel Input MOSFETs

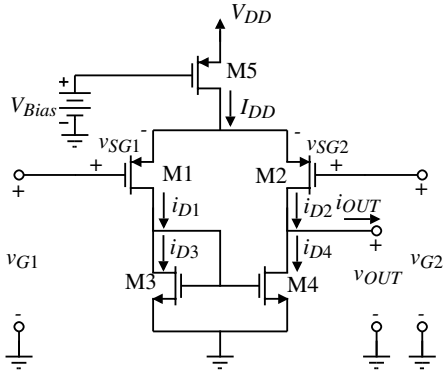


Fig. 5.2-7

Input Common Mode Range (ICMR)

ICMR is found by setting $v_{ID} = 0$ and varying v_{IC} until one of the transistors leaves the saturation region.

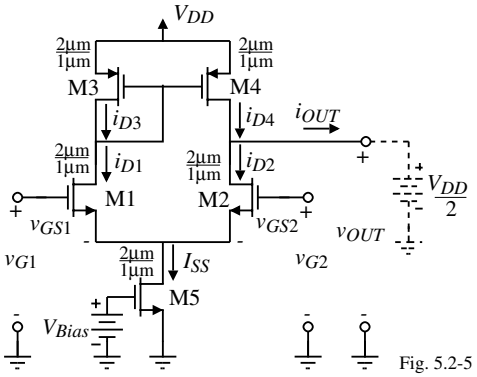


Fig. 5.2-5

Highest Common Mode Voltage

Path from G1 through M1 and M3 to V_{DD}:

$$V_{IC}(\max) = V_{G1}(\max) = V_{G2}(\max)$$
$$= V_{DD} - V_{SG3} - V_{DS1}(\text{sat}) + V_{GS1}$$

or

$$V_{IC}(\max) = V_{DD} - V_{SG3} + V_{TN1}$$

Path from G2 through M2 and M4 to V_{DD}:

$$V_{IC}(\max)' = V_{DD} - V_{SD4}(\text{sat}) - V_{DS2}(\text{sat}) + V_{GS2}$$
$$= V_{DD} - V_{SD4}(\text{sat}) + V_{TN2}$$

$$\therefore \boxed{V_{IC}(\max) = V_{DD} - V_{SG3} + V_{TN1}}$$

Lowest Common Mode Voltage

$$\boxed{V_{IC}(\min) = V_{DS5}(\text{sat}) + V_{GS1} = V_{DS5}(\text{sat}) + V_{GS2}}$$

where we have assumed that $V_{GS1} = V_{GS2}$ during changes in the input common mode voltage.

Example 5.2-1 - Calculation of the Worst-Case Input Common-Mode Range of the n-Channel Input, Differential Amplifier

Assume that V_{DD} varies from 4 to 6 volts and that $V_{SS} = 0$, and use the values of Table 3.1-2 under worst-case conditions to calculate the input common-mode range of n-channel input differential amplifier with a current mirror load. Assume that I_{SS} is 100 μA, $W_1/L_1 = W_2/L_2 = 5$, $W_3/L_3 = W_4/L_4 = 1$, and $V_{DS5}(\text{sat}) = 0.2$ V. Include worst-case variation in K' in calculations.

Solution

If V_{DD} varies 5 ± 1 volts, then the upper common-mode voltage is,

$$V_{IC}(\max) = 4 - \left(\sqrt{\frac{2 \cdot 50\mu A}{45\mu A/V^2 \cdot 1}} + 0.85\right) + 0.55 = 4 - 2.34 + 0.55 = 2.21 \text{ volts}$$

The lower common-mode voltage is,

$$V_{IC}(\min) = 0 + 0.2 + \left(\sqrt{\frac{2 \cdot 50\mu A}{99\mu A/V^2 \cdot 5}} + 0.85\right) = 0.2 + 1.30 = 1.50 \text{ volts}$$

which gives a worst-case input common-mode range of 0.71 volts with a nominal 5-volt power supply.

Reducing V_{DD} by several volts more will result in a worst-case common-mode range of zero. We have assumed in this example that all bulk-source voltages are zero.

Small-Signal Analysis of the Differential-Mode of the Differential Amplifier

A requirement for differential-mode operation is that the differential amplifier is perfectly balanced†.

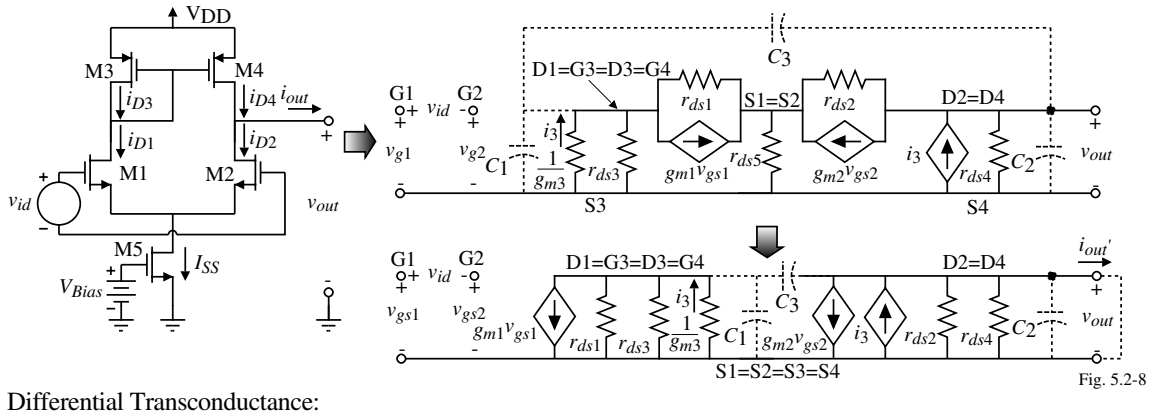


Fig. 5.2-8

Differential Transconductance:

Assume that the output of the differential amplifier is an ac short.

$$i_{\text{out}}' = \frac{g_{m1}g_{m3}r_{p1}}{1+g_{m3}r_{p1}}v_{gs1} - g_{m2}v_{gs2} \approx g_{m1}v_{gs1} - g_{m2}v_{gs2} = g_{md}v_{id}$$

where $g_{m1} = g_{m2} = g_{md}$, $r_{p1} = r_{ds1} \,||\, r_{ds3}$ and i'_{out} designates the output current into a short circuit.

† It can be shown that the current mirror causes this requirement to be invalid because the drain loads are not matched. However, we will continue to use the assumption regardless. See Problem 5.2-16.

Small-Signal Analysis of the Differential-Mode of the Differential Amplifier - Continued

$$r_{\text{out}} = \frac{1}{g_{ds2}+g_{ds4}} = r_{ds2}||r_{ds4}$$

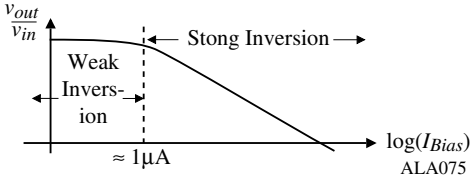
Differential Voltage Gain:

$$A_v = \frac{v_{\text{out}}}{v_{id}} = \frac{g_{md}}{g_{ds2}+g_{ds4}}$$

If we assume that all transistors are in saturation and replace the small signal parameters of g_m and r_{ds} in terms of their large-signal model equivalents, we achieve

$$A_v = \frac{v_{\text{out}}}{v_{id}} = \frac{(K'_1 I_{SS}W_1/L_1)^{1/2}}{(\lambda_2+\lambda_4)(I_{SS}/2)} = \frac{2}{\lambda_2+\lambda_4}\left(\frac{K'_1W_1}{I_{SS}L_1}\right)^{1/2} \propto \frac{1}{\sqrt{I_{SS}}}$$

Note that the small-signal gain is inversely proportional to the square root of the bias current!



Example:

If W_1/L_1 = 2μm/1μm and I_{SS} = 50μA (10μA), then

A_v(n-channel) = 46.6V/V (104.23V/V)

A_v(p-channel) = 31.4V/V (70.27V/V)

$$r_{\text{out}} = \frac{1}{g_{ds2}+g_{ds4}} = \frac{1}{25\mu\text{A}\cdot 0.09\text{V}^{-1}} = 0.444\text{M}\Omega \ (2.22\text{M}\Omega)$$

Common Mode Analysis for the Current Mirror Load Differential Amplifier

The current mirror load differential amplifier is not a good example for common mode analysis because the current mirror rejects the common mode signal.

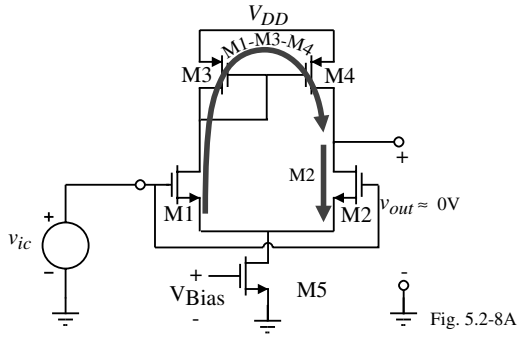


Fig. 5.2-8A

$$\begin{bmatrix}\text{Total common mode Output due to } v_{ic}\end{bmatrix} = \begin{bmatrix}\text{Common mode output due to M1-M3-M4 path}\end{bmatrix} - \begin{bmatrix}\text{Common mode output due to M2 path}\end{bmatrix}$$

Therefore

- The common mode output voltage should ideally be zero.
- Any voltage that exists at the output is due to mismatches in the gain between the two different paths.

Small-Signal Analysis of the Common-Mode of the Differential Amplifier

The common-mode gain of the differential amplifier with a current mirror load is ideally zero.

To illustrate the common-mode gain, we need a different type of load so we will consider the following:

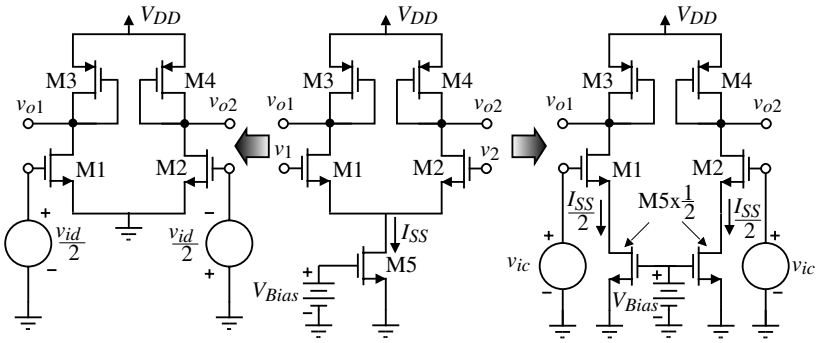


Fig. 5.2-9

Differential-Mode Analysis:

$$\frac{v_{o1}}{v_{id}} \approx -\frac{g_{m1}}{2g_{m3}}$$

and

$$\frac{v_{o2}}{v_{id}} \approx +\frac{g_{m2}}{2g_{m4}}$$

Note that these voltage gains are half of the active load inverter voltage gain.

Small-Signal Analysis of the Common-Mode of the Differential Amplifier - Continued

Common-Mode Analysis:

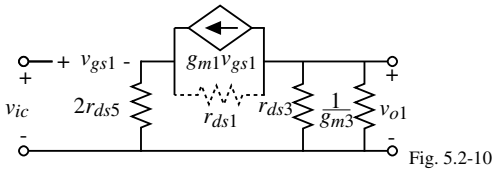


Fig. 5.2-10

Assume that r_{ds1} is large and can be ignored (greatly simplifies the analysis).

$\therefore \quad v_{gs1} = v_{g1} - v_{s1} = v_{ic} - 2g_{m1}r_{ds5}v_{gs1}$

Solving for v_{gs1} gives

$$v_{gs1} = \frac{v_{ic}}{1 + 2g_{m1}r_{ds5}}$$

The single-ended output voltage, v_{o1}, as a function of v_{ic} can be written as

$$\frac{v_{o1}}{v_{ic}} = -\frac{g_{m1}[r_{ds3}\|(1/g_{m3})]}{1 + 2g_{m1}r_{ds5}} \approx -\frac{(g_{m1}/g_{m3})}{1 + 2g_{m1}r_{ds5}} \approx -\frac{g_{ds5}}{2g_{m3}}$$

Common-Mode Rejection Ratio (*CMRR*):

$$CMRR = \frac{|v_{o1}/v_{id}|}{|v_{o1}/v_{ic}|} = \frac{g_{m1}/2g_{m3}}{g_{ds5}/2g_{m3}} = g_{m1}r_{ds5}$$

How could you easily increase the *CMRR* of this differential amplifier?

Frequency Response of the Differential Amplifer (Differential Mode)

Back to the current mirror load differential amplifier:

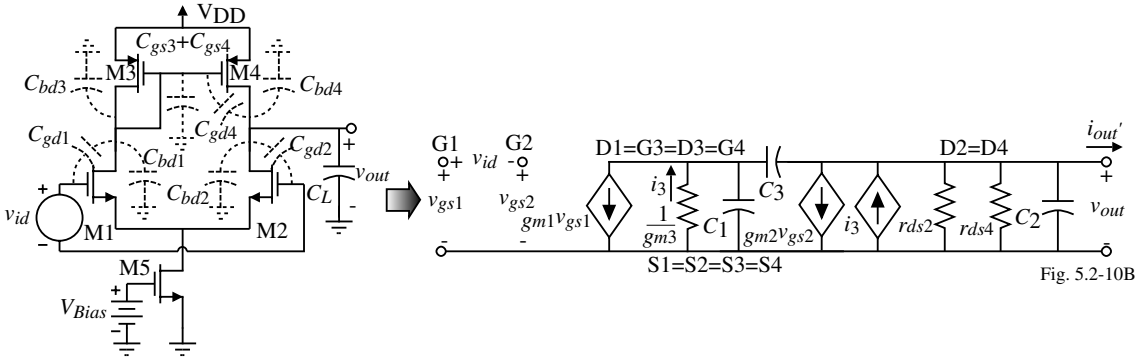


Fig. 5.2-10B

Ignore the zeros that occur due to C_{gd1}, C_{gd2} and C_{gd4}.

$C_1 = C_{gd1} + C_{bd1} + C_{bd3} + C_{gs3} + C_{gs4}$, $\quad C_2 = C_{bd2} + C_{bd4} + C_{gd2} + C_L \quad$ and $\quad C_3 = C_{gd4}$

If $C_3 \approx 0$, then we can write

$$V_{out}(s) \cong \frac{g_{m1}}{g_{ds2} + g_{ds4}}\left[\left(\frac{g_{m3}}{g_{m3} + sC_1}\right)V_{gs1}(s) - V_{gs2}(s)\right]\left(\frac{\omega_2}{s + \omega_2}\right) \qquad \text{where } \omega_2 = \frac{g_{ds2} + g_{ds4}}{C_2}$$

If we further assume that $\frac{g_{m3}}{C_1} >> \frac{g_{ds2} + g_{ds4}}{C_2}$

then the frequency response of the differential amplifier reduces to

$$\frac{V_{out}(s)}{V_{id}(s)} \cong \left(\frac{g_{m1}}{g_{ds2} + g_{ds4}}\right)\left(\frac{\omega_2}{s + \omega_2}\right)$$

(A more detailed analysis will be made later)

An Intuitive Method of Small Signal Analysis

Small signal analysis is used so often in analog circuit design that it becomes desirable to find faster ways of performing this important analysis.

Intuitive Analysis (or Schematic Analysis)

Technique:

1.) Identify the transistor(s) that convert the input voltage to current (these transistors are called *transconductance transistors*).

2.) Trace the currents to where they flow into an equivalent resistance to ground.

3.) Multiply this resistance by the current to get the voltage at this node to ground.

4.) Repeat this process until the output is reached.

Simple Example:

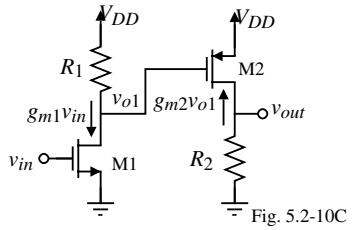


Fig. 5.2-10C

$v_{o1} = -(g_{m1}v_{in})\,R_1 \quad \rightarrow \quad v_{out} = -(g_{m2}v_{o1})R_2 \rightarrow \quad v_{out} = (g_{m1}R_1 g_{m2}R_2)v_{in}$

Intuitive Analysis of the Current-Mirror Load Differential Amplifier

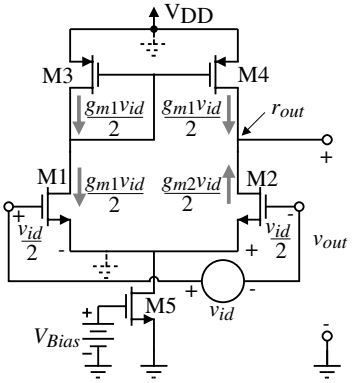


Fig. 5.2-11

1.) $i_1 = 0.5g_{m1}v_{id}$ and $i_2 = -0.5g_{m2}v_{id}$

2.) $i_3 = i_1 = 0.5g_{m1}v_{id}$

3.) $i_4 = i_3 = 0.5g_{m1}v_{id}$

4.) The resistance at the output node, r_{out}, is $r_{ds2} \| r_{ds4}$ or $\dfrac{1}{g_{ds2} + g_{ds4}}$

5.) $\therefore \quad v_{out} = (0.5g_{m1}v_{id} + 0.5g_{m2}v_{id})r_{out} = \dfrac{g_{m1}v_{in}}{g_{ds2}+g_{ds4}} = \dfrac{g_{m2}v_{in}}{g_{ds2}+g_{ds4}} \Rightarrow \quad \dfrac{v_{out}}{v_{in}} = \dfrac{g_{m1}}{g_{ds2}+g_{ds4}}$

Some Concepts to Help Extend the Intuitive Method of Small-Signal Analysis

1.) Approximate the output resistance of any cascode circuit as

$$R_{out} \approx (g_{m2}r_{ds2})r_{ds1}$$

where M1 is a transistor cascoded by M2.

2.) If there is a resistance, R, in series with the source of the transconductance transistor, let the effective transconductance be

$$g_{m(eff)} = \frac{g_m}{1+g_mR}$$

Proof:

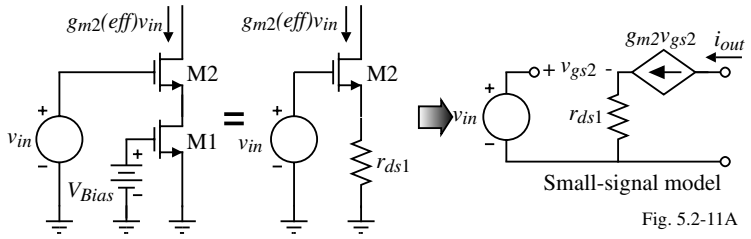


Fig. 5.2-11A

$$\therefore\ v_{gs2} = v_{g2} - v_{s2} = v_{in} - (g_{m2}r_{ds1})v_{gs2} \ \Rightarrow\ v_{gs2} = \frac{v_{in}}{1+g_{m2}r_{ds1}}$$

Thus, $i_{out} = \dfrac{g_{m2}v_{in}}{1+g_{m2}r_{ds1}} = g_{m2}(eff)\ v_{in}$

Slew Rate of the Differential Amplifier

Slew Rate (SR) = Maximum output-voltage rate (either positive or negative)

It is caused by the relationship, $i_{OUT} = C_L\dfrac{dv_{OUT}}{dt}$. When i_{OUT} is a constant, the rate becomes a constant.

Consider the following current-mirror load, differential amplifiers:

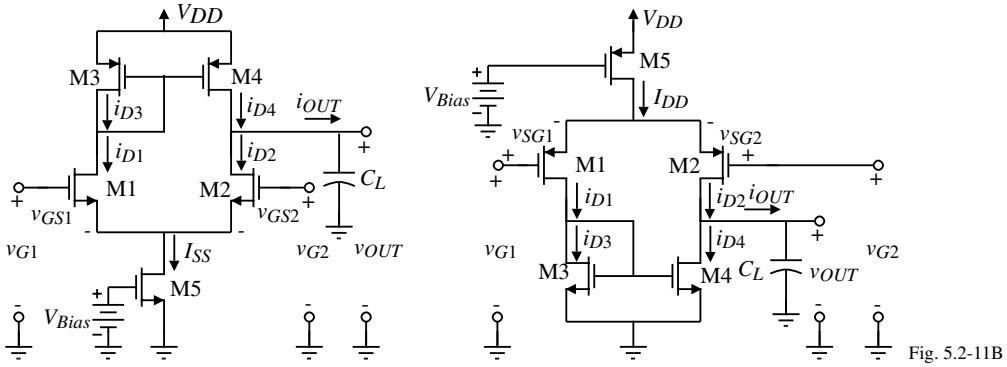


Fig. 5.2-11B

Note that slew rate can only occur when the differential input signal is large enough to cause I_{SS} (I_{DD}) to flow through only one of the differential input transistors.

$$SR = \frac{I_{SS}}{C_L} = \frac{I_{DD}}{C_L} \quad \Rightarrow \quad \text{If } C_L = 5\text{pF and } I_{SS} = 10\mu\text{A, the slew rate is } SR = 2\text{V}/\mu\text{s}.$$

(For the BJT differential amplifier slewing occurs at ±100mV whereas for the MOSFET differential amplifier it can be ±2V or more.)

Noise Analysis of the Differential Amplifier

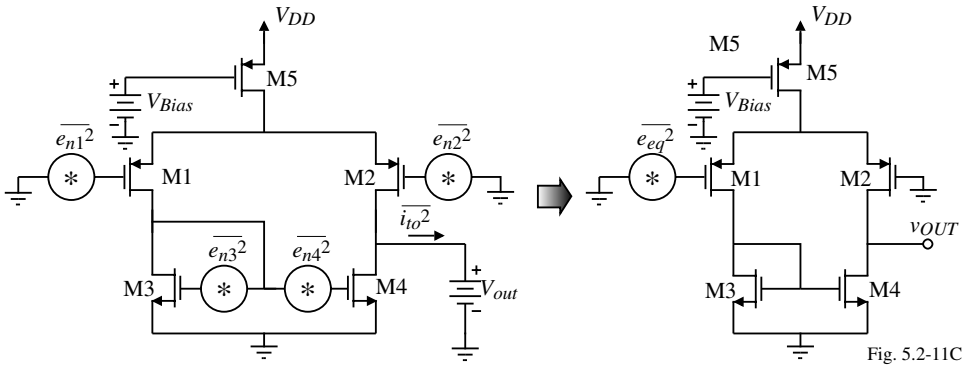


Fig. 5.2-11C

Solve for the total output-noise current to get,

$$\overline{i_{to}^2} = g_{m1}^2\overline{e_{n1}^2} + g_{m2}^2\overline{e_{n2}^2} + g_{m3}^2\overline{e_{n3}^2} + g_{m4}^2\overline{e_{n4}^2}$$

This output-noise current can be expressed in terms of an equivalent input noise voltage, $\overline{e_{eq}^2}$, given as

$$\overline{i_{to}^2} = g_{m1}^2\overline{e_{eq}^2}$$

Equating the above two expressions for the total output-noise current gives,

$$\overline{e_{eq}^2} = \overline{e_{n1}^2} + \overline{e_{n2}^2} + \left(\frac{g_{m3}}{g_{m1}}\right)^2\left[\overline{e_{n3}^2} + \overline{e_{n4}^2}\right]$$

1/f Noise ($\overline{e_{n1}} = \overline{e_{n2}}$ and $\overline{e_{n3}} = \overline{e_{n4}}$):

$$\overline{e_{eq(1/f)}} = \sqrt{\frac{2B_P}{fW_1L_1}}\sqrt{1 + \left(\frac{K'_N B_N}{K'_P B_P}\right)\left(\frac{L_1}{L_3}\right)^2}$$

Thermal Noise ($\overline{i_{n1}} = \overline{i_{n2}}$ and $\overline{i_{n3}} = \overline{i_{n4}}$):

$$\overline{e_{eq(th)}} = \sqrt{\left(\frac{16kT}{3[2K'_1(W/L)_1 I_1]^{1/2}}\right)\left[1 + \left(\frac{W_3L_1K'_3}{L_3W_1K'_1}\right)^{1/2}\right]}$$

Current-Source Load Differential Amplifier

Gives a truly balanced differential amplifier.

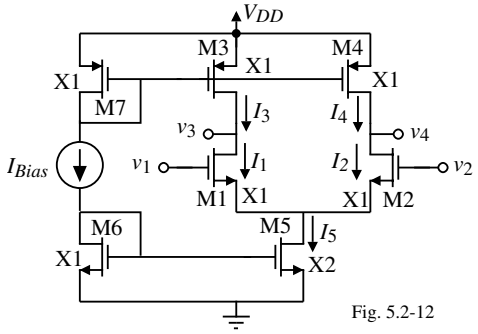


Fig. 5.2-12

Also, the upper input common-mode range is extended.

However, a problem occurs if $I_1 \neq I_3$ or if $I_2 \neq I_4$.

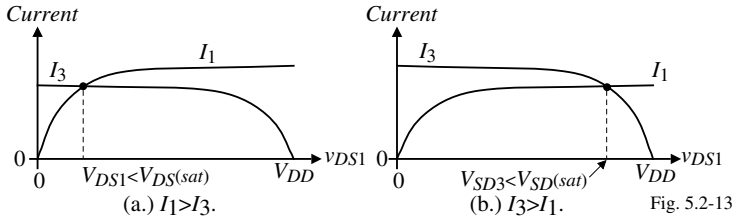


Fig. 5.2-13

A Differential-Output, Differential-Input Amplifier

Probably the best way to solve the current mismatch problem is through the use of common-mode feedback. Consider the following solution to the previous problem.

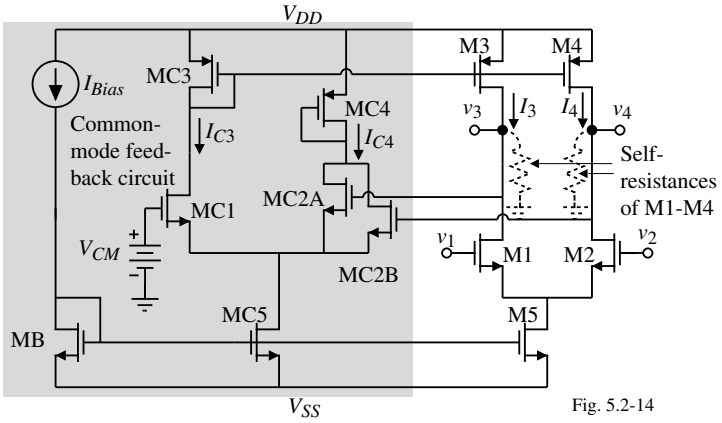


Fig. 5.2-14

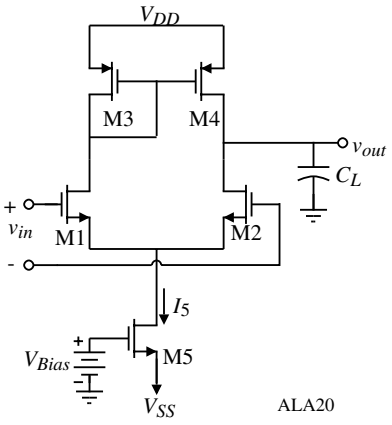
Operation:

- Common mode output voltages are sensed at the gates of MC2A and MC2B and compared to V_{CM}.
- The current in MC3 provides the negative feedback to drive the common mode output voltage to the desired level.

Design of a CMOS Differential Amplifier with a Current Mirror Load

Design Considerations:

Constraints	Specifications
Power supply	Small-signal gain
Technology	Frequency response (C_L)
Temperature	ICMR
	Slew rate (C_L)
	Power dissipation



ALA20

Relationships

$A_v = g_{m1}R_{out}$

$\omega_{-3dB} = 1/R_{out}C_L$

$V_{IC}(\text{max}) = V_{DD} - V_{SG3} + V_{TN1}$

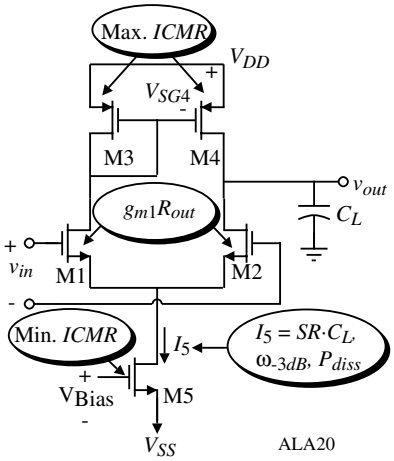
$V_{IC}(\text{min}) = V_{SS} + V_{DS5}(\text{sat}) + V_{GS1} = V_{SS} + V_{DS5}(\text{sat}) + V_{GS2}$

$SR = I_{SS}/C_L$

$P_{diss} = (V_{DD}+|V_{SS}|)$xAll dc currents flowing from V_{DD} or to V_{SS}

Design of a CMOS Differential Amplifier with a Current Mirror Load - Continued

Schematic-wise, the design procedure is illustrated as shown:



Procedure:

1.) Pick I_{SS} to satisfy the slew rate knowing C_L or the power dissipation

2.) Check to see if R_{out} will satisfy the frequency response, if not change I_{SS} or modify circuit

3.) Design W_3/L_3 (W_4/L_4) to satisfy the upper *ICMR*

4.) Design W_1/L_1 (W_2/L_2) to satisfy the gain

5.) Design W_5/L_5 to satisfy the lower *ICMR*

6.) Iterate where necessary

Example 5 - Design of a MOS Differential Amplifier with a Current Mirror Load

Design the currents and *W/L* values of the current mirror load MOS differential amplifier to satisfy the following specifications: $V_{DD} = -V_{SS} = 2.5\text{V}$, $SR \geq 10\text{V/}\mu\text{s}$ (C_L=5pF), $f_{-3\text{dB}} \geq 100\text{kHz}$ (C_L=5pF), a small signal gain of 100V/V, $-1.5\text{V} \leq ICMR \leq 2\text{V}$ and $P_{diss} \leq 1\text{mW}$. Use the parameters of $K_N' = 110\mu\text{A/V}^2$, $K_P' = 50\mu\text{A/V}^2$, $V_{TN} = 0.7\text{V}$, $V_{TP} = -0.7\text{V}$, $\lambda_N = 0.04\text{V}^{-1}$ and $\lambda_P = 0.05\text{V}^{-1}$.

Solution

1.) To meet the slew rate, $I_{SS} \geq 50\mu\text{A}$. For maximum P_{diss}, $I_{SS} \leq 200\mu\text{A}$.

2.) $f_{-3\text{dB}}$ of 100kHz implies that $R_{out} \leq 318\text{k}\Omega$. This gives $R_{out} = \dfrac{2}{(\lambda_N+\lambda_P)I_{SS}} \leq 318\text{k}\Omega$

$\therefore\ I_{SS} \geq 70\mu\text{A}$ Thus, pick $I_{SS} = 100\mu\text{A}$

3.) $V_{IC}(\text{max}) = V_{DD} - V_{SG3} + V_{TN1} \rightarrow\ 2\text{V} = 2.5 - V_{SG3} + 0.7 \rightarrow\ V_{SG3} = 1.2\text{V} = \sqrt{\dfrac{2 \cdot 50\mu\text{A}}{50\mu\text{A/V}^2(W_3/L_3)}} + 0.7$

$\therefore\ \dfrac{W_3}{L_3} = \dfrac{W_4}{L_4} = \dfrac{2}{(0.5)^2} = 8$

4.) $100\text{V/V} = g_{m1}R_{out} = \dfrac{g_{m1}}{g_{ds2}+g_{ds4}} = \dfrac{\sqrt{2 \cdot 110\mu\text{A/V}^2(W_1/L_1)}}{(0.04+0.05)\sqrt{50\mu\text{A}}} = 23.31\sqrt{W_1/L_1} \qquad \rightarrow \dfrac{W_1}{L_1} = \dfrac{W_2}{L_2} = 18.4$

5.) $V_{IC}(\text{min}) = V_{SS} + V_{DS5}(\text{sat}) + V_{GS1} \ \rightarrow\ -1.5 = -2.5 + V_{DS5}(\text{sat}) + \sqrt{\dfrac{2 \cdot 50\mu\text{A}}{110\mu\text{A/V}^2(18.4)}} + 0.7$

$V_{DS5}(\text{sat}) = 0.3 - 0.222 = 0.0777\text{!!} \ \Rightarrow\ \dfrac{W_5}{L_5} = \sqrt{\dfrac{2I_{SS}}{K_N' V_{DS5}(\text{sat})^2}} = 300$

We probably should increase W_1/L_1 to reduce V_{GS1} and allow a smaller W_5/L_5. If we choose $W_1/L_1 = 40$, then $W_5/L_5 = 9$. (Larger than specified gain should be okay.)

SECTION 5.3 - CASCODE AMPLIFIER

Why Use the Cascode Amplifier?

- Can provide higher output resistance and larger gain if the load is also high resistance.
- It reduces the Miller effect when the driving source has a large source resistance.

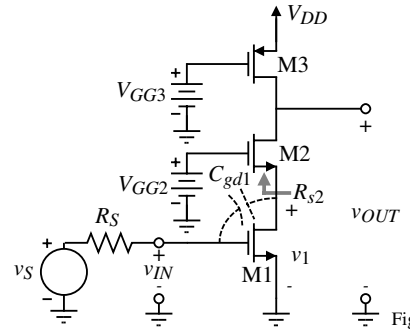


Fig. 5.3-1

The Miller effect causes C_{gd1} to be increased by the value of $1 + (v_1/v_{in})$ and appear in parallel with the gate-source of M1 causing a dominant pole to occur.

The cascode amplifier eliminates this dominant pole by keeping the value of v_1/v_{in} small by making the value of R_2 to be approximately $2/g_{m2}$.

Large-Signal Characteristics of the Cascode Amplifier

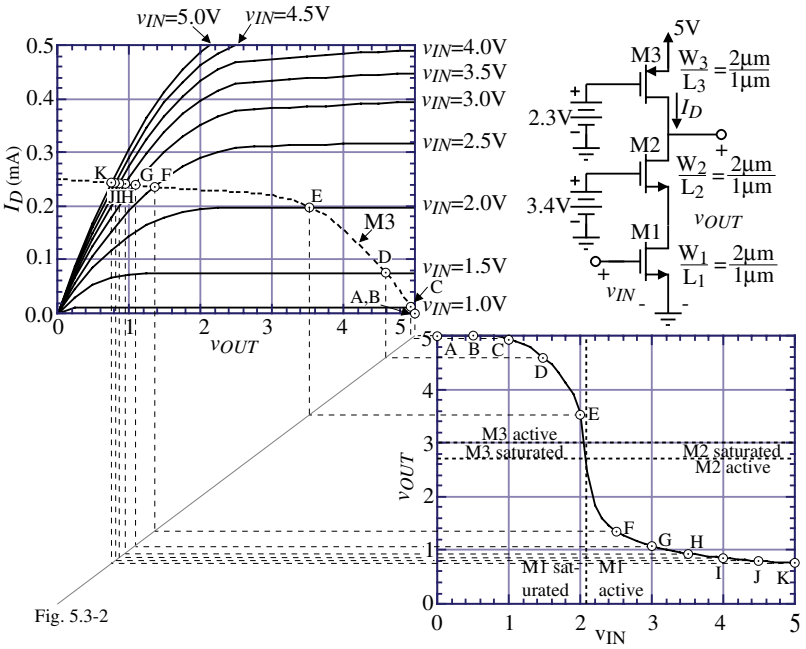


Fig. 5.3-2

M1 is saturated when $V_{GG2} - V_{GS2} \geq V_{GS1} - V_T \rightarrow v_{IN} \leq 0.5(V_{GG2} + V_{TN})$ where $V_{GS1} = V_{GS2}$

M2 is saturated when $V_{DS2} \geq V_{GS2} - V_{TN} \rightarrow v_{OUT} - V_{DS1} \geq V_{GG2} - V_{DS1} - V_{TN} \rightarrow v_{OUT} \geq V_{GG2} - V_{TN}$

M3 is saturated when $V_{DD} - v_{OUT} \geq V_{DD} - V_{GG3} - |V_{TP}| \rightarrow v_{OUT} \leq V_{GG3} + |V_{TP}|$

Large-Signal Voltage Swing Limits of the Cascode Amplifier

Maximum output voltage, v_{OUT}(max):

$$\boxed{v_{OUT}(\max) = V_{DD}}$$

Minimum output voltage, v_{OUT}(min):

Referencing all potentials to the negative power supply (ground in this case), we may express the current through each of the devices, M1 through M3, as

$$i_{D1} = \beta_1\left((V_{DD} - V_{T1})v_{DS1} - \frac{v_{DS1}^2}{2}\right) \cong \beta_1(V_{DD} - V_{T1})v_{DS1}$$

$$i_{D2} = \beta_2\left((V_{GG2} - v_{DS1} - V_{T2})(v_{OUT} - v_{DS1}) - \frac{(v_{OUT} - v_{DS1})^2}{2}\right)$$

$$\cong \beta_2(V_{GG2} - v_{DS1} - V_{T2})(v_{OUT} - v_{DS1})$$

and

$$i_{D3} = \frac{\beta_3}{2}(V_{DD} - V_{GG3} - |V_{T3}|)^2$$

where we have also assumed that both v_{DS1} and v_{OUT} are small, and $v_{IN} = V_{DD}$.
Solving for v_{OUT} by realizing that $i_{D1} = i_{D2} = i_{D3}$ and $\beta_1 = \beta_2$ we get,

$$\boxed{v_{OUT}(\min) = \frac{\beta_3}{2\beta_2}(V_{DD} - V_{GG3} - |V_{T3}|)^2\left(\frac{1}{V_{GG2} - V_{T2}} + \frac{1}{V_{DD} - V_{T1}}\right)}$$

Example 5.3-1 - Calculation of the Minimum Output Voltage for the Simple Cascode Amplifier

(a.) Assume the values and parameters used for the cascode configuration plotted in the previous slide on the voltage transfer function and calculate the value of v_{OUT}(min).

(b.) Find the value of v_{OUT}(max) and v_{OUT}(min) where all transistors remain in saturation.

Solution

(a.) Using the previous result gives,

v_{OUT}(min) = 0.50 volts.

We note that simulation gives a value of about 0.75 volts. If we include the influence of the channel modulation on M3 in the previous derivation, the calculated value is 0.62 volts which is closer. The difference is attributable to the assumption that both v_{DS1} and v_{OUT} are small.

(b.) The largest output voltage for which all transistors of the cascode amplifier are in saturation is given as

$v_{OUT}(\max) = V_{DD} - V_{SD3}(\text{sat})$

and the corresponding minimum output voltage is

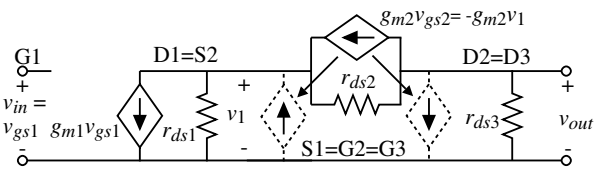
$v_{OUT}(\min) = V_{DS1}(\text{sat}) + V_{DS2}(\text{sat})$.

For the cascode amplifier of Fig. 5.3-2, these limits are 3.0V and 2.7V.

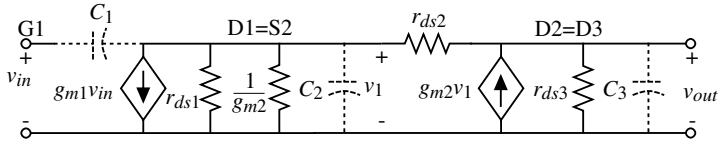
Consequently, the range over which all transistors are saturated is quite small for a 5V power supply.

Small-Signal Midband Performance of the Cascode Amplifier

Small-signal model:



Small-signal model of cascode amplifier neglecting the bulk effect on M2.



Simplified equivalent model of the above circuit. Fig. 5.3-3

Using nodal analysis, we can write,

$$[g_{ds1} + g_{ds2} + g_{m2}]v_1 - g_{ds2}v_{\text{out}} = -g_{m1}v_{\text{in}}$$

$$-[g_{ds2} + g_{m2}]v_1 + (g_{ds2} + g_{ds3})v_{\text{out}} = 0$$

Solving for $v_{\text{out}}/v_{\text{in}}$ yields

$$\frac{v_{\text{out}}}{v_{\text{in}}} = \frac{-g_{m1}(g_{ds2} + g_{m2})}{g_{ds1}g_{ds2} + g_{ds1}g_{ds3} + g_{ds2}g_{ds3} + g_{ds3}g_{m2}} \cong \frac{-g_{m1}}{g_{ds3}} = -\sqrt{\frac{2K'_1W_1}{L_1I_D\lambda^2_3}}$$

The small-signal output resistance is,

$$r_{out} = [r_{ds1} + r_{ds2} + g_{m2}r_{ds1}r_{ds2}]\|r_{ds3} \cong r_{ds3}$$

Small-Signal Analysis of the Cascode Amplifier - Continued

It is of interest to examine the voltage gain of v_1/v_{in}. From the previous nodal equations we can solve for this gain as,

$$\frac{v_1}{v_{\text{in}}} = \frac{-g_{m1}(g_{ds2} + g_{ds3})}{g_{ds1}g_{ds2} + g_{ds1}g_{ds3} + g_{ds2}g_{ds3} + g_{ds3}g_{m2}} \approx \left(\frac{g_{ds2} + g_{ds3}}{g_{ds3}}\right)\left(\frac{-g_{m1}}{g_{m2}}\right) \cong \frac{-2g_{m1}}{g_{m2}} = -2\sqrt{\frac{W_1L_2}{L_1W_2}}$$

If the *W/L* ratios of M1 and M2 are identical and $g_{ds2} = g_{ds3}$, then v_1/v_{in} is approximately –2.

Why is this gain -2 instead of -1?

Consider the small-signal model looking into the source of M2:

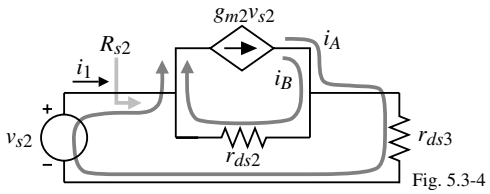


Fig. 5.3-4

The voltage loop is written as,

$$v_{s2} = (i_1 - g_{m2}v_{s2})r_{\text{ds2}} + i_1r_{ds3}$$

$$= i_1(r_{ds2} + r_{\text{ds3}}) - g_{m2}\,r_{ds2}v_{s2}$$

Solving this equation for the ratio of v_{s2} to i_1 gives

$$R_{s2} = \frac{v_{s2}}{i_1} = \frac{r_{ds2} + r_{ds3}}{1 + g_{m2}r_{ds2}}$$

We see that R_{s2} is indeed equal to $2/g_{m2}$ if $r_{ds2} \approx r_{ds3}$. Thus, if $g_{m1} \approx g_{m2}$, the voltage gain $v_1/v_{in} \approx -2$.

Note that:

$r_{ds3} = 0$ that $R_{s2} \approx 1/g_{m2}$ or $r_{ds3} = r_{ds2}$ that $R_{s2} \approx 2/g_{m2}$ or $r_{ds3} \approx r_{ds2}g_mr_{ds}$ that $R_{s2} \approx r_{ds}$!!!

Principle: *The small-signal resistance looking into the source of a MOSFET depends on the resistance connected from the drain of the MOSFET to ac ground.*

Frequency Response of the Cascode Amplifier

Small-signal model ($R_S = 0$):

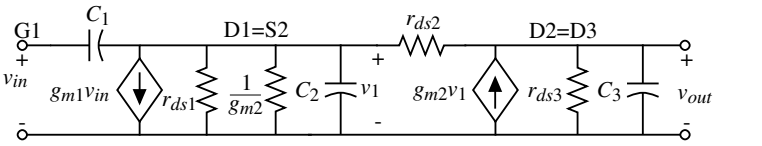


Fig. 5.3-4A

where

$$C_1 = C_{gd1},\quad C_2 = C_{bd1} + C_{bs2} + C_{gs2} \quad \text{and} \quad C_3 = C_{bd2} + C_{bd3} + C_{gd2} + C_{gd3} + C_L$$

The nodal equations now become:

$$(g_{m2} + g_{ds1} + g_{ds2} + sC_1 + sC_2)v_1 - g_{ds2}v_{\text{out}} = -(g_{m1} - sC_1)v_{\text{in}}$$

and

$$-(g_{ds2} + g_{m2})v_1 + (g_{ds2} + g_{ds3} + sC_3)v_{\text{out}} = 0$$

Solving for $V_{\text{out}}(s)/V_{\text{in}}(s)$ gives,

$$\frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = \left(\frac{1}{1 + as + bs^2}\right)\left(\frac{-(g_{m1} - sC_1)(g_{ds2} + g_{m2})}{g_{ds1}g_{ds2} + g_{ds3}(g_{m2} + g_{ds1} + g_{ds2})}\right)$$

where

$$a = \frac{C_3(g_{ds1} + g_{ds2} + g_{m2}) + C_2(g_{ds2} + g_{ds3}) + C_1(g_{ds2} + g_{ds3})}{g_{ds1}g_{ds2} + g_{ds3}(g_{m2} + g_{ds1} + g_{ds2})}$$

and

$$b = \frac{C_3(C_1 + C_2)}{g_{ds1}g_{ds2} + g_{ds3}(g_{m2} + g_{ds1} + g_{ds2})}$$

A Simplified Method of Finding an Algebraic Expression for the Two Poles

Assume that a general second-order polynomial can be written as:

$$P(s) = 1 + as + bs^2 = \left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right) \qquad = 1 - s\left(\frac{1}{p_1} + \frac{1}{p_2}\right) + \frac{s^2}{p_1p_2}$$

Now if $|p_2| >> |p_1|$, then $P(s)$ can be simplified as

$$P(s) \approx 1 - \frac{s}{p_1} + \frac{s^2}{p_1p_2}$$

Therefore we may write p_1 and p_2 in terms of a and b as

$$p_1 = \frac{-1}{a} \qquad \text{and} \qquad p_2 = \frac{-a}{b}$$

Applying this to the previous problem gives,

$$p_1 = \frac{-[g_{ds1}g_{ds2} + g_{ds3}(g_{m2} + g_{ds1} + g_{ds2})]}{C_3(g_{ds1} + g_{ds2} + g_{m2}) + C_2(g_{ds2} + g_{ds3}) + C_1(g_{ds2} + g_{ds3})} \approx \frac{-g_{ds3}}{C_3}$$

The nondominant root p_2 is given as

$$p_2 = \frac{-[C_3(g_{ds1} + g_{ds2} + g_{m2}) + C_2(g_{ds2} + g_{ds3}) + C_1(g_{ds2} + g_{ds3})]}{C_3(C_1 + C_2)} \approx \frac{-g_{m2}}{C_1 + C_2}$$

Assuming that C_1, C_2, and C_3 are the same order of magnitude, and that g_{m2} is greater than g_{ds3}, then $|p_1|$ is smaller than $|p_2|$ (closer to the origin). Therefore the approximation of $|p_2| >> |p_1|$ is valid.

Note that there is a right-half plane zero at $z_1 = \frac{g_{m1}}{C_1}$.

Driving Amplifiers from a High Resistance Source - The Miller Effect

Examine the frequency response of a current-source load inverter driven from a high resistance source:

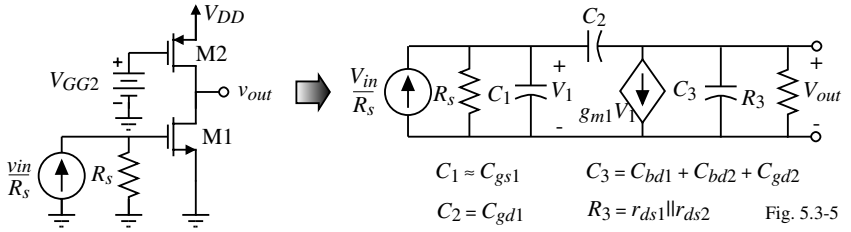


Fig. 5.3-5

Assuming the input is I_{in}, the nodal equations are,

$$[G_1 + s(C_1 + C_2)]V_1 - sC_2V_{out} = I_{in} \quad \text{and} \quad (g_{m1} - sC_2)V_1 + [G_3 + s(C_2 + C_3)]V_{out} = 0$$

where

$G_1 = G_s\ (=1/R_s)$, $G_3 = g_{ds1} + g_{ds2}$, $C_1 = C_{gs1}$, $C_2 = C_{gd1}$ and $C_3 = C_{bd1}+C_{bd2} + C_{gd2}$.

Solving for $V_{out}(s)/V_{in}(s)$ gives

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{(sC_2-g_{m1})G_1}{G_1G_3+s[G_3(C_1+C_2)+G_1(C_2+C_3)+g_{m1}C_2]+(C_1C_2+C_1C_3+C_2C_3)s^2}$$

or

$$\frac{V_{out}(s)}{V_{in}(s)} = \left(\frac{-g_{m1}}{G_3}\right)\frac{[1-s(C_2/g_{m1})]}{1+[R_1(C_1+C_2)+R_3(C_2+C_3)+g_{m1}R_1R_3C_2]s+(C_1C_2+C_1C_3+C_2C_3)R_1R_3s^2}$$

Assuming that the poles are split allows the use of the previous technique to get,

$$p_1 = \frac{-1}{R_1(C_1 + C_2) + R_3(C_2 + C_3) + g_{m1}R_1R_3C_2} \cong \frac{-1}{g_{m1}R_1R_3C_2} \text{ and } \quad p_2 \cong \frac{-g_{m1}C_2}{C_1C_2 + C_1C_3 + C_2C_3}$$

The Miller effect has caused the input pole, $1/R_1C_1$, to be decreased by a value of $g_{m1}R_3$.

How does the Cascode Amplifier Solve the Miller Effect?

The dominant pole of the inverting amplifier with a large source resistance was found to be

$$p_1(\text{inverter}) = \frac{-1}{R_1(C_1+C_2)+R_3(C_2+C_3)+g_{m1}R_1R_3C_2}$$

Now if a cascode amplifier is used, R_3, can be approximated as $2/g_m$ of the cascoding transistor (assuming the drain sees an r_{ds} to ac ground).

$$\therefore \quad p_1(\text{cascode}) = \frac{-1}{R_1(C_1+C_2)+\left(\frac{2}{g_m}\right)(C_2+C_3)+g_{m1}R_1\left(\frac{2}{g_m}\right)C_2} = \frac{-1}{R_1(C_1+C_2)+\left(\frac{2}{g_m}\right)(C_2+C_3)+2R_1C_2}$$

$$\approx \frac{-1}{R_1(C_1+3C_2)}$$

Thus we see that $p_1(\text{cascode}) >> p_1(\text{inverter})$.

High Gain and High Output Resistance Cascode Amplifier

If the load of the cascode amplifier is a cascode current source, then both high output resistance and high voltage gain is achieved.

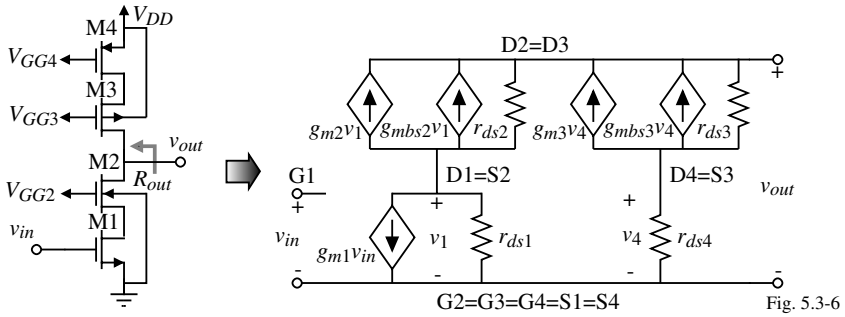


Fig. 5.3-6

The output resistance is,

$$r_{out} = [r_{ds1}+r_{ds2}+g_{m2}r_{ds1}r_{ds2}(1+\eta_2)] \,||\, [r_{ds3}+r_{ds4}+g_{m3}r_{ds3}r_{ds4}(1+\eta_3)] \cong [g_{m2}r_{ds1}r_{ds2}] \,||\, [g_{m3}r_{ds3}r_{ds4}]$$

$$r_{out} \cong \frac{I_D^{-1.5}}{\dfrac{\lambda_1\lambda_2}{\sqrt{2K'_2(W/L)_2}} + \dfrac{\lambda_3\lambda_4}{\sqrt{2K'_3(W/L)_3}}}$$

Knowing r_{out}, the gain is simply

$$A_v = -g_{m1}r_{out} \cong -g_{m1}\{[g_{m2}r_{ds1}r_{ds2}] \,||\, [g_{m3}r_{ds3}r_{ds4}]\} \cong \frac{\sqrt{2K'_1(W/L)_1}I_D^{-1}}{\dfrac{\lambda_1\lambda_2}{\sqrt{2K'_2(W/L)_2}} + \dfrac{\lambda_3\lambda_4}{\sqrt{2K'_3(W/L)_3}}}$$

Example 5.3-2 - Comparison of the Cascode Amplifier Performance

Calculate the small-signal voltage gain, output resistance, the dominant pole, and the nondominant pole for the low-gain, cascode amplifier and the high-gain, cascode amplifier. Assume that $I_D = 200$ microamperes, that all W/L ratios are 2μm/1μm, and that the parameters of Table 3.1-2 are valid. The capacitors are assumed to be: $C_{gd} = 3.5$ fF, $C_{gs} = 30$ fF, $C_{bsn} = C_{bdn} = 24$ fF, $C_{bsp} = C_{bdp} = 12$ fF, and $C_L = 1$ pF.

Solution

The low-gain, cascode amplifier has the following small-signal performance:

$A_v = -37.1$V/V

$R_{out} = 125$kΩ

$p_1 \approx -g_{ds3}/C_3 = 1.22$ MHz

$p_2 \approx g_{m2}/(C_1+C_2) = 605$ MHz.

The high-gain, cascode amplifier has the following small-signal performance:

$A_v = -414$V/V

$R_{out} = 1.40$ MΩ

$p_1 \approx 1/R_{out}C_3 = 108$ kHz

$p_2 \approx g_{m2}/(C_1+C_2) = 579$ MHz

(Note that at this frequency, the drain of M2 is shorted to ground by the load capacitance, C_L)

Designing Cascode Amplifiers

Pertinent design equations for the simple cascode amplifier.

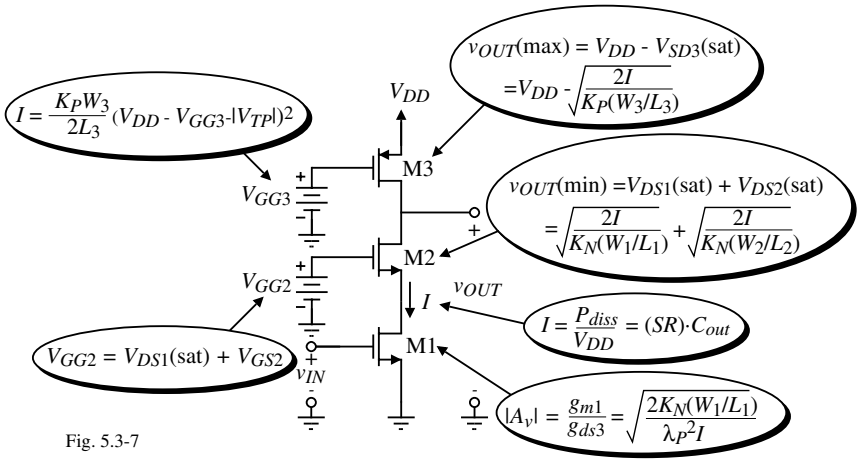


Fig. 5.3-7

Example 5.3-3 - Design of a Cascode Amplifier

The specifications for a cascode amplifier are $V_{DD} = 5\text{V}$, $P_{diss} = 1\text{mW}$, $A_v = -50\text{V/V}$, $v_{OUT}(\max) = 4\text{V}$, and $v_{OUT}(\min) = 1.5\text{V}$. The slew rate with a 10pF load should be 10V/μs or greater.

Solution

The slew rate requires a current greater than 100μA while the power dissipation requires a current less than 200μA. Let us compromise with a current of 150μA. We will first begin with M3.

$$\frac{W_3}{L_3} = \frac{2I}{K_P[V_{DD} - v_{OUT}(\max)]^2} = \frac{2\cdot 150}{50(1)^2} = 6$$

From this find V_{GG3}: $$V_{GG3} = V_{DD} - |V_{TP}| - \sqrt{\frac{2I}{K_P(W_3/L_3)}} = 5 - 1 - \sqrt{\frac{2\cdot 150}{50\cdot 6}} = 3\text{V}$$

Next, $$\frac{W_1}{L_1} = \frac{(A_v\lambda)^2 I}{2K_N} = \frac{(50\cdot 0.05)^2(150)}{2\cdot 110} = 2.73$$

To design W_2/L_2, we will first calculate $V_{DS1}(\text{sat})$ and use the $v_{OUT}(\min)$ specification to define $V_{DS2}(\text{sat})$.

$$V_{DS1}(\text{sat}) = \sqrt{\frac{2I}{K_N(W_1/L_1)}} = \sqrt{\frac{2\cdot 150}{110\cdot 4.26}} = 0.8\text{V}$$

Subtracting this value from 1.5V gives $V_{DS2}(\text{sat}) = 0.7\text{V}$.

$\therefore$ $$\frac{W_2}{L_2} = \frac{2I}{K_N V_{DS2}(\text{sat})^2} = \frac{2\cdot 150}{110\cdot 0.7^2} = 5.57$$

Finally, $$V_{GG2} = V_{DS1}(\text{sat}) + \sqrt{\frac{2I}{K_N(W_2/L_2)}} + V_{TN} = 0.8\text{V} + 0.7\text{V} + 0.7\text{V} = 2.2\text{V}$$

SECTION 5.4 - CURRENT AMPLIFIERS

What is a Current Amplifier?

- An amplifier that has a defined output-input current relationship
- Low input resistance
- High output resistance

Application of current amplifiers:

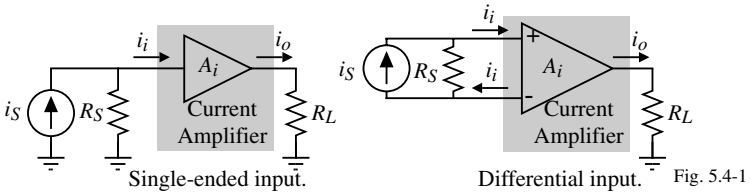


Fig. 5.4-1

$R_S >> R_{in}$ and $R_{out} >> R_L$

Advantages of current amplifiers:

- Currents are not restricted by the power supply voltages so that wider dynamic ranges are possible with lower power supply voltages.
- -3dB bandwidth of a current amplifier using negative feedback is independent of the closed loop gain.

Frequency Response of a Current Amplifier with Current Feedback

Consider the following current amplifier with resistive negative feedback applied.

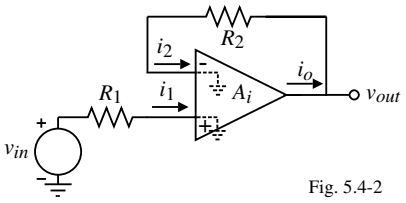


Fig. 5.4-2

Assuming that the small-signal resistance looking into the current amplifier is much less than R_1 or R_2,

$$i_o = A_i(i_1 - i_2) = A_i\left(\frac{v_{in}}{R_1} - i_o\right)$$

Solving for i_o gives

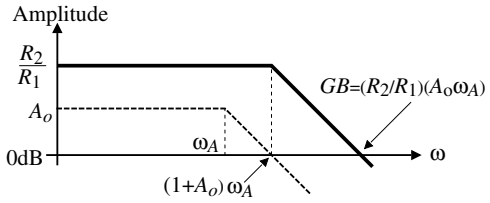
$$i_o = \left(\frac{A_i}{1+A_i}\right)\frac{v_{in}}{R_1} \quad \rightarrow \quad v_{out} = R_2 i_o = \frac{R_2}{R_1}\left(\frac{A_i}{1+A_i}\right)v_{in}$$

If $A_i(s) = \dfrac{A_o}{\frac{s}{\omega_A} + 1}$, then $\dfrac{v_{out}}{v_{in}} = \dfrac{R_2}{R_1}\left(\dfrac{1}{1+\frac{1}{A_i(s)}}\right) = \dfrac{R_2}{R_1}\left(\dfrac{A_o}{\frac{s}{\omega_A}+(1+A_o)}\right) = \dfrac{R_2}{R_1}\left(\dfrac{A_o}{1+A_o}\right)\left(\dfrac{1}{\frac{s}{\omega_A(1+A_o)}+1}\right)$

$\therefore \quad \omega_{-3dB} = \omega_A(1+A_o)$

The unity-gainbandwidth is

$$GB = \frac{R_2}{R_1}\left(\frac{A_o}{1+A_o}\right)\cdot \omega_A(1+A_o) = \frac{R_2}{R_1}(\omega_A A_o) = \frac{R_2}{R_1}GB_i$$



Current Amplifier using the Simple Current Mirror

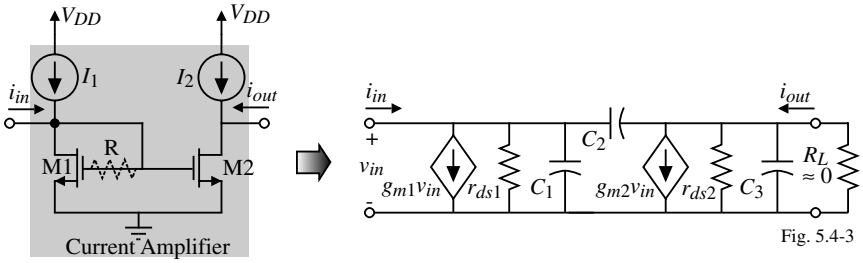


Fig. 5.4-3

$$R_{in} = \frac{1}{g_{m1}} \quad R_{out} = \frac{1}{\lambda_1 I_o} \quad \text{and} \quad A_i = \frac{W_2/L_2}{W_1/L_1} .$$

Frequency response:

$$p_1 = \frac{-(g_{m1}+g_{ds1})}{C_1+C_2} = \frac{-(g_{m1}+g_{ds1})}{C_{bd1}+C_{gs1}+C_{gs2}+C_{gd2}} \approx \frac{-g_{m1}}{C_{bd1}+C_{gs1}+C_{gs2}+C_{gd2}}$$

Note that the bandwidth can be almost doubled by including the resistor, R.
(R removes C_{gs1} from p_1)

Example 5.4-1- Performance of a Simple Current Mirror as a Current Amplifier

Find the small-signal current gain, A_i, the input resistance, R_{in}, the output resistance, R_{out}, and the -3dB frequency in Hertz for the current amplifier of Fig. 5.4-3(a) if $10I_1 = I_2 = 100\mu A$ and $W_2/L_2 = 10W_1/L_1 = 10\mu m/1\mu m$. Assume that $C_{bd1} = 10fF$, $C_{gs1} = C_{gs2} = 100fF$, and $C_{gs2} = 50fF$.

Solution

Ignoring channel modulation and mismatch effects, the small-signal current gain,

$$A_i = \frac{W_2/L_2}{W_1/L_1} \approx 10 A/A.$$

The small-signal input resistance, R_{in}, is approximately $1/g_{m1}$ and is

$$R_{in} \approx \frac{1}{\sqrt{2K_N(1/1)10\mu A}} = \frac{1}{46.9\mu S} = 21.3k\Omega$$

The small-signal output resistance is equal to

$$R_{out} = \frac{1}{\lambda_N I_2} = 250k\Omega.$$

The -3dB frequency is

$$\omega_{-3dB} = \frac{46.9\mu S}{260fF} = 180.4x10^6 \text{ radians/sec.} \quad \rightarrow \quad f_{-3dB} = 28.7 \text{ MHz}$$

Self-Biased Cascode Current Mirror Implementation of a Current Amplifier

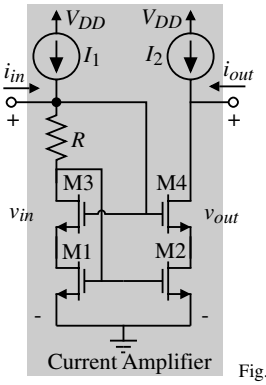


Fig. 5.4-4

$$R_{in} \approx R + \frac{1}{g_{m1}}, \qquad R_{out} \approx r_{ds2} g_{m4} r_{ds4}, \qquad \text{and} \qquad A_i = \frac{W_2/L_2}{W_1/L_1}$$

Example 5.4 -2 - Current Amplifier Implemented by the Self-Biased, Cascode Current Mirror

Assume that I_1 and I_2 of the self-biased cascode current mirror are 100μA. R has been designed to give a V_{ON} of 0.1V. Thus R = 1kΩ. Find the value of R_{in}, R_{out}, and A_i if the W/L ratios of all transistors are 182μm/1μm.

Solution

The input resistance requires g_{m1} which is $\sqrt{2 \cdot 110 \cdot 182 \cdot 100}$ = 2mS

$\therefore$ $R_{in} \approx 1000\Omega + 500\Omega = 1.5k\Omega$

From our knowledge of the cascode configuration, the small signal output resistance should be

$R_{out} \approx g_{m4} r_{ds4} r_{ds2}$ = (2001μS)(250kΩ)(250kΩ) = 125MΩ

Because $V_{DS1} = V_{DS2}$, the small-signal current gain is

$$A_i = \frac{W_2/L_2}{W_1/L_1} = 1$$

Simulation results using the level 1 model for this example give

R_{in}=1.497kΩ

R_{out} = 164.7MΩ

and

A_i = 1.000 A/A.

Low-Input Resistance Current Amplifier

To decrease R_{in} below $1/g_m$ requires the use of negative, shunt feedback. Consider the following example.

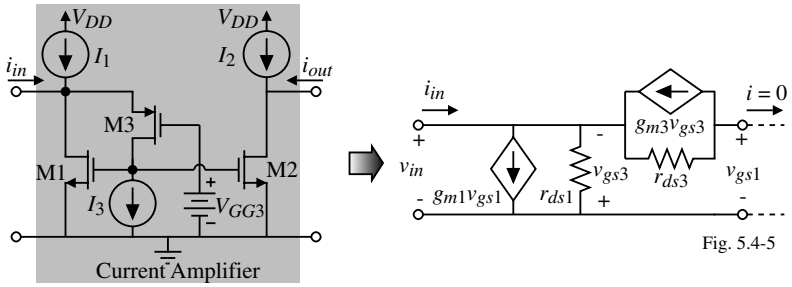


Fig. 5.4-5

Feedback concept:

Input resistance without feedback $\approx r_{ds1}$.

Loop gain $\approx \left(\frac{g_{m1}}{g_{ds1}}\right)\left(\frac{g_{m3}}{g_{ds3}}\right)$ assuming that the resistances of I_1 and I_3 are very large.

$$\therefore\ R_{in} = \frac{R_{in}(\text{no fb.})}{1 + \text{Loop gain}} \approx \frac{r_{ds1}}{g_{m1}r_{ds1}g_{m3}r_{ds3}} = \frac{1}{g_{m1}g_{m3}r_{ds3}}$$

Small signal analysis:

$$i_{in} = g_{m1}v_{gs1} - g_{ds1}v_{gs3}$$

and $\quad v_{gs3} = -v_{in} \quad v_{gs1} = v_{in} - (g_{m3}\, v_{gs3}r_{ds3}) = v_{in}(1+g_{m3}r_{ds3})$

$$\therefore \quad i_{in} = g_{m1}(1+g_{m3}r_{ds3})v_{in} + g_{ds1}v_{in} \approx g_{m1}g_{m3}r_{ds3}v_{in} \quad \Rightarrow \quad R_{in} \approx \frac{1}{g_{m1}g_{m3}r_{ds3}}$$

Differential-Input, Current Amplifiers

Definitions for the differential-mode, i_{ID}, and common-mode, i_{IC}, input currents of the differential-input current amplifier.

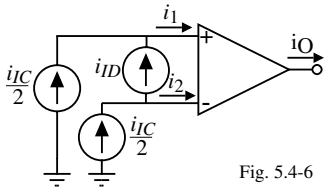
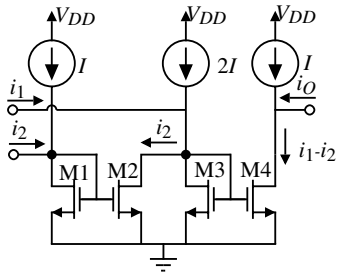


Fig. 5.4-6

$$i_O = A_{ID}i_{ID} \pm A_{IC}i_{IC} = A_{ID}(i_1 - i_2) \pm A_{IC}\left(\frac{i_1+i_2}{2}\right)$$

Implementations:



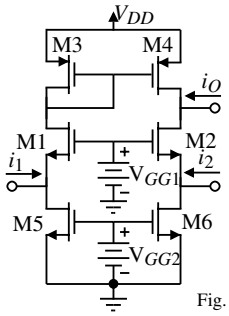


Fig. 5.4-7

Summary

- Current amplifiers have a low input resistance, high output resistance, and a defined output-input current relationship
- Input resistances less than $1/g_m$ require feedback

  However, all feedback loops have internal poles that cause the benefits of negative feedback to vanish at high frequencies.

  In addition, these feedback loops can have a slow time constant from a pole-zero pair.
- Voltage amplifiers using a current amplifier have high values of gain-bandwidth
- Current amplifiers are useful at low power supplies and for switched current applications

SECTION 5.5 - OUTPUT AMPLIFIERS

General Considerations of Output Amplifiers

Requirements:

1.) Provide sufficient output power in the form of voltage or current.
2.) Avoid signal distortion.
3.) Be efficient
4.) Provide protection from abnormal conditions (short circuit, over temperature, etc.)

Types of Output Amplifiers:

1.) Class A amplifiers
2.) Source followers
3.) Push-pull amplifiers
4.) Substrate BJT amplifiers
5.) Amplifiers using negative shunt feedback

Class A Amplifiers

Current source load inverter:

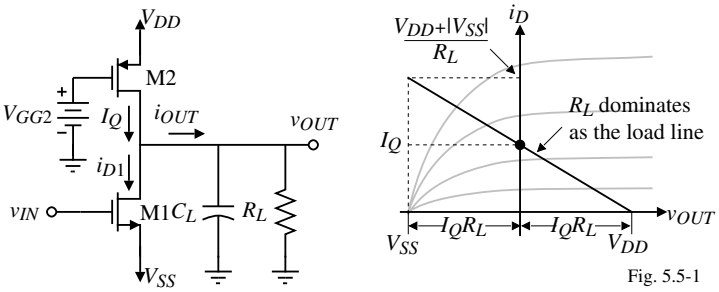


Fig. 5.5-1

A Class A circuit has current flow in the MOSFETs during the entire period of a sinusoidal signal.

Characteristics of Class A amplifiers:

- Unsymmetrical sinking and sourcing
- Linear
- Poor efficiency

$$\text{Efficiency} = \frac{P_{RL}}{P_{Supply}} = \frac{\frac{v_{OUT}(\text{peak})^2}{2R_L}}{(V_{DD}\text{-}V_{SS})I_Q} = \frac{\frac{v_{OUT}(\text{peak})^2}{2R_L}}{(V_{DD}\text{-}V_{SS})\left(\frac{(V_{DD}\text{-}V_{SS})}{2R_L}\right)} = \left(\frac{v_{OUT}(\text{peak})}{V_{DD}\text{-}V_{SS}}\right)^2$$

Maximum efficiency occurs when $v_{OUT}(\text{peak}) = V_{DD} = |V_{SS}|$ which gives 25%.

Specifying the Performance of a Class A Amplifier

Output resistance:

$$r_{out} = \frac{1}{g_{ds1} + g_{ds2}} = \frac{1}{(\lambda_1+\lambda_2)I_D}$$

Current:

- Maximum sinking current is,

$$I_{OUT}^{-} = \frac{K'_1W_1}{2L_1}(V_{DD} - V_{SS} - V_{T1})^2 - I_Q$$

- Maximum sourcing current is,

$$I_{OUT}^{+} = \frac{K'_2W_2}{2L_2}(V_{DD} - V_{GG2} - |V_{T2}|)^2 \le I_Q$$

Requirements:

- Want $r_{out} << R_L$
- $|I_{OUT}| > C_L \cdot SR$
- $|I_{OUT}| > \frac{v_{OUT}(\text{peak})}{R_L}$

The maximum current will be determined by **both** the current required to provide the necessary slew rate (C_L) and the current required to provide a voltage across the load resistor (R_L).

Small-Signal Performance of the Class A Amplifier

Although we have considered the small-signal performance of the Class A amplifier as the current source load inverter, let us include the influence of the load.

The modified small-signal model:

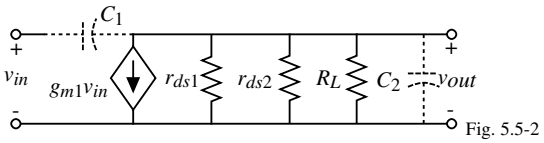


Fig. 5.5-2

The small-signal voltage gain is:

$$\frac{v_{out}}{v_{in}} = \frac{-g_{m1}}{g_{ds1}+g_{ds2}+G_L}$$

The small-signal frequency response includes:

A zero at

$$z = \frac{g_{m1}}{C_{gd1}}$$

and a pole at

$$p = \frac{-(g_{ds1}+g_{ds2}+G_L)}{C_{gd1}+C_{gd2}+C_{bd1}+C_{bd2}+C_L}$$

Example 5.5-1 - Design of a Simple Class-A Output Stage

Use the values of Table 3.1-2 and design the *W/L* ratios of M1 and M2 so that a voltage swing of ±2 volts and a slew rate of ≅1 volt/μs is achieved if R_L = 20 kΩ and C_L = 1000 pF. Assume that $V_{DD} = |V_{SS}| = 3$ volts and $V_{GG2} = 0$ volts. Let the channel lengths be 2 μm and assume that C_{gd1} = 100fF.

Solution

Let us first consider the effects of R_L and C_L.

$$i_{OUT}(\text{peak}) = \frac{\pm 2\text{V}}{20\text{k}\Omega} = \pm 100\mu\text{A} \quad \text{and} \quad C_L \cdot SR = 10^{-9}\cdot 10^{6} = 1000\mu\text{A}$$

Since the slew rate current is so much larger than the current needed to meet the voltage specification across R_L, we can safely assume that all of the current supplied by the inverter is available to charge C_L.

Using a value of ±1 mA,

$$\frac{W_1}{L_1} = \frac{2(I_{OUT}^{-}+I_Q)}{K_N'(V_{DD}+|V_{SS}| - V_{TN})^2} = \frac{4000}{110\cdot(5.3)^2} \approx \frac{3\mu\text{m}}{2\mu\text{m}}$$

and

$$\frac{W_2}{L_2} = \frac{2I_{OUT}^{+}}{K_P'(V_{DD}-V_{GG2}-|V_{TP}|)^2} = \frac{2000}{50\cdot(2.3)^2} \approx \frac{15\mu\text{m}}{2\mu\text{m}}$$

The small-signal performance of this amplifier is,

A_v = -8.21 V/V (includes R_L = 20kΩ) $\qquad$ r_{out} = 50kΩ

The roots are,

Zero = $g_{m1}/C_{gd1} \Rightarrow$ 1.59GHz and $\qquad$ Pole = $1/[(R_L \| r_{out})C_L)] \Rightarrow$ -11.14kHz

Broadband Harmonic Distortion

The linearity of an amplifier can be characterized by its influence on a pure sinusoidal input signal.

Assume the input is,

$$V_{in}(\omega) = V_p \sin(\omega t)$$

The output of an amplifier with distortion will be

$$V_{out}(\omega) = a_1 V_p \sin(\omega t) + a_2 V_p \sin(2\omega t) + \cdots + a_n V_p \sin(n\omega t)$$

Harmonic distortion (*HD*) for the *i*th harmonic can be defined as the ratio of the magnitude of the *i*th harmonic to the magnitude of the fundamental.

For example, second-harmonic distortion would be given as

$$HD_2 = \frac{a_2}{a_1}$$

Total harmonic distortion (*THD*) is defined as the square root of the ratio of the sum of all of the second and higher harmonics to the magnitude of the first or fundamental harmonic.

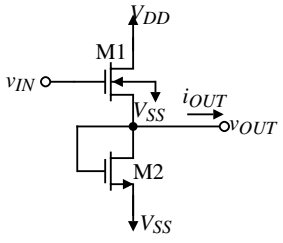
Thus, *THD* can be expressed as

$$THD = \frac{[a_2^2 + a_3^2 + \cdots + a_n^2]^{1/2}}{a_1}$$

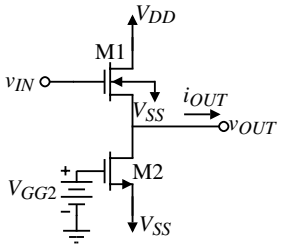
The distortion of the class A amplifier is good for small signals and becomes poor at maximum output swings because of the nonlinearity of the voltage transfer curve for large-signal swing

Source Follower

Two types of source followers:



Source follower with a MOS diode load.



Source Follower with a current-sink load.

Fig. 5.5-3

Large signal considerations:

$v_{OUT}(\min) \approx V_{SS}$ and $v_{OUT}(\max) = V_{DD} - V_{T1} - V_{ON1} \approx V_{DD} - V_{T1}$

But, we need to include the bulk effect on V_{T1}:

$$V_{T1} = V_{T0} + \gamma\sqrt{2|\phi_F| - v_{BS}} - \sqrt{2|\phi_F|} \approx V_{T0} + \gamma\sqrt{v_{SB}} = V_{T01} + \gamma_1\sqrt{v_{OUT}(\max) - V_{SS}}$$

$$\therefore\ v_{OUT}(\max) - V_{SS} \approx V_{DD} - V_{T01} - \gamma_1\sqrt{v_{OUT}(\max) - V_{SS}}$$

or putting this equation in quadratic form,

$$v_{OUT}(\max) - V_{SS} + \gamma_1\sqrt{v_{OUT}(\max) - V_{SS}} - (V_{DD} - V_{T01}) = 0$$

Solving the quadratic gives, $v_{OUT}(\max) \approx V_{DD} + \frac{\gamma_1^2}{4} - V_{T01} - \frac{\gamma_1}{2}\sqrt{\gamma_1^2 + 4(V_{DD} - V_{SS} - V_{T01})}$

Therefore if $V_{DD} = |V_{SS}| = 2.5\text{V}$, then $v_{OUT}(\max) = 1.46\text{V}$

Maximum Sourcing and Sinking Currents for the Source Follower

Maximum Sourcing Current:

We assume that the transistors are in saturation and $V_{DD} = -V_{SS} = 2.5\text{V}$, thus

$$I_{OUT}(\text{sourcing}) = \frac{K'_1 W_1}{2L_1}[V_{DD} - v_{OUT} - V_{T1}]^2 - I_{D2}$$

where v_{IN} is assumed to be equal to V_{DD}.

If $W_1/L_1 = 10$, $v_{OUT} = 0\text{V}$ and $I_{D2} = 0.5\text{mA}$, then $V_{T1} = 1.08\text{V} \Rightarrow I_{OUT}$ equal to 0.608 mA.

However, as v_{OUT} increases above 0V, the current rapidly decreases.

Maximum Sinking Current:

Depends on M2.

- For the MOS diode load, the sinking current is

$$I_{OUT}(\text{sinking}) = \frac{K_2 W_2}{2L_2}[v_{OUT} - V_{T1}]^2 \quad \text{(as } v_{OUT} \text{ approaches } V_{T1}\text{, the current goes to zero)}$$

- For the current sink load, the sinking current is whatever the sink is biased to provide.

$$I_{OUT}(\text{sinking}) = \frac{K_2 W_2}{2L_2}[V_{GG2} - V_{T1}]^2 = I_{D2}$$

Comments:

- The efficiency is the same as the class A amplifier
- The distortion should be better because of the inherent negative feedback of the source follower.

Small Signal Performance of the Source Follower

Small-signal model (Set $g_{m2} = 0$ for the current sink load follower) :

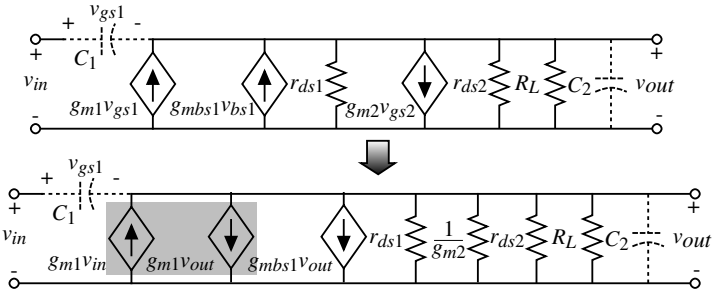


Fig. 5.5-4

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}}{g_{ds1} + g_{ds2} + g_{m1} + g_{mbs1} + g_{m2}} \cong \frac{g_{m1}}{g_{m1} + g_{mbs1} + g_{m2}}$$

If $V_{DD} = -V_{SS} = 2.5\text{ V}$, $V_{\text{out}} = 0\text{ V}$, $W_1/L_1 = 10\ \mu\text{m}/1\ \mu\text{m}$, $W_2/L_2 = 1\ \mu\text{m}/1\ \mu\text{m}$, and $I_D = 500\ \mu\text{A}$, then for the MOS diode load follower:

$\frac{V_{out}}{V_{in}} = 0.682$, if the bulk effect were not present, $g_{mbs1} = 0$, then $\frac{V_{out}}{V_{in}} = 0.738$.

For the current sink load follower ($g_{m2} = 0$):

$\frac{V_{out}}{V_{in}} = 0.869$, if the bulk effect were ignored, then $\frac{V_{out}}{V_{in}} = 0.963$

Small Signal Performance of the Source Follower - Continued

The output resistance ($g_{m2} = 0$ for the current sink load follower) is:

$$R_{out} = \frac{1}{g_{m1} + g_{mbs1} + g_{m2} + g_{ds1} + g_{ds2}}$$

For the MOS diode load follower:

$$R_{out} = 651\Omega$$

For the current sink load follower:

$$R_{out} = 830\Omega$$

The frequency response of the source follower ($g_{m2} = 0$ for the current sink load follower) :

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{(g_{m1} + sC_1)}{g_{ds1} + g_{ds2} + g_{m1} + g_{mbs1} + g_{m2} + G_L + s(C_1 + C_2)}$$

where

C_1 = capacitances connected between the input and output $\approx C_{GS1}$

$C_2 = C_{bs1} + C_{bd2} + C_{gd2}$(or C_{gs2}) + C_L

$$\therefore \quad z = -\frac{g_{m1}}{C_1} \qquad \text{and} \qquad p \approx -\frac{g_{m1}+G_L}{C_1+C_2}$$

The presence of a LHP zero leads to the possibility that in most cases the pole and zero will provide some degree of cancellation leading to a broadband response.

Push-Pull Source Follower

Can both sink and source current and provide a slightly lower output resistance.

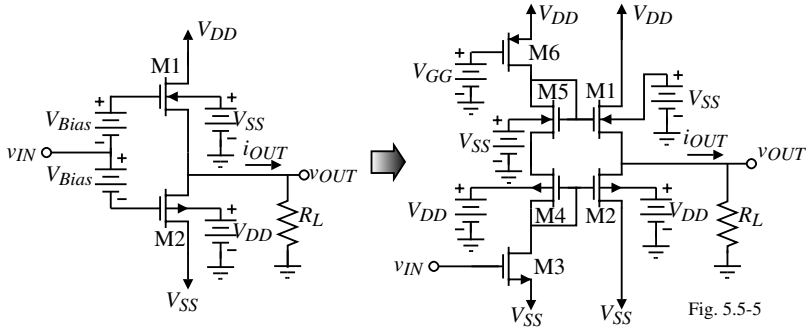


Fig. 5.5-5

Efficiency:

Depends on how the transistors are biased.

- Class B - one transistor has current flow for only 180° of the sinusoid (half period)

$$\therefore \text{ Efficiency} = \frac{P_{RL}}{P_{VDD}} = \frac{\dfrac{v_{OUT}(\text{peak})^2}{2R_L}}{(V_{DD}-V_{SS})\left(\dfrac{1}{2}\right)\left(\dfrac{2v_{OUT}(\text{peak})}{\pi R_L}\right)} = \frac{\pi}{2}\frac{v_{OUT}(\text{peak})}{V_{DD}-V_{SS}}$$

Maximum efficiency occurs when $v_{OUT}(\text{peak}) = V_{DD}$ and is 78.5%

- Class AB - each transistor has current flow for more than 180° of the sinusoid.

Maximum efficiency is between 25% and 78.5%

Illustration of Class B and Class AB Push-Pull, Source Follower

Output current and voltage characteristics of the push-pull, source follower (R_L = 1kΩ):

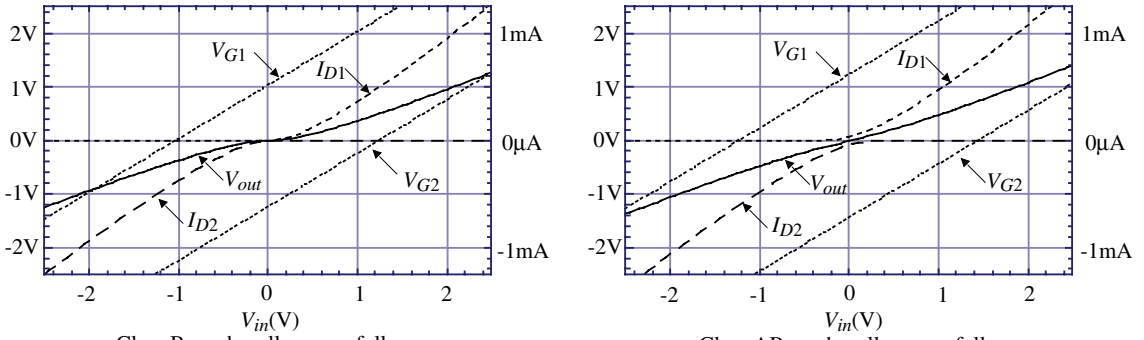


Fig. 5.5-6B

Comments:

- Note that v_{OUT} cannot reach the extreme values of V_{DD} and V_{SS}
- I_{OUT}^{+}(max) and I_{OUT}^{-}(max) is always less than V_{DD}/R_L or V_{SS}/R_L
- For v_{OUT} = 0V, there is quiescent current flowing in M1 and M2 for Class AB
- Note that there is significant distortion at v_{IN} =0V for the Class B push-pull follower

Small-Signal Performance of the Push-Pull Follower

Model:

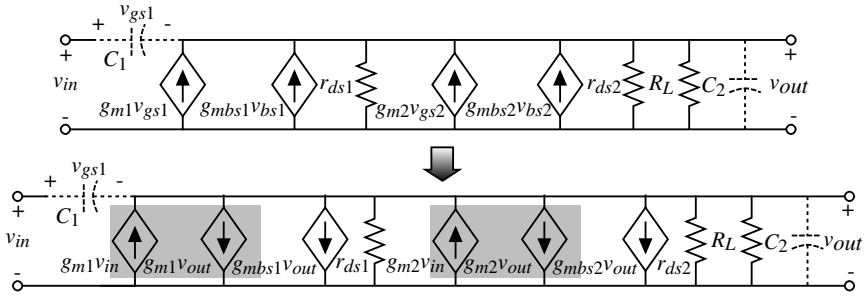


Fig. 5.5-6

$$R_{out} = \frac{1}{g_{ds1}+g_{ds2}+g_{m1}+g_{mbs1}+g_{m2}+g_{mbs2}} \quad \text{(does not include } R_L\text{)}$$

$$\text{Gain} = \frac{v_{out}}{v_{in}} = (g_{m1}+g_{m2})\,R_{out} = \frac{g_{m1}+g_{m2}}{g_{ds1}+g_{ds2}+g_{m1}+g_{mbs1}+g_{m2}+g_{mbs2}}$$

If $V_{DD} = -V_{SS}$ = 2.5V, V_{out} = 0V, $I_{D1} = I_{D2}$ = 500µA, and W/L = 20µm/2µm, A_v = 0.787 (R_L=∞) and R_{out} = 448Ω.

A zero and pole are located at

$$z = \frac{-(g_{m1}+g_{m2})}{C_1} \qquad p = \frac{-(g_{ds1}+g_{ds2}+g_{m1}+g_{mbs1}+g_{m2}+g_{mbs2}+G_L)}{C_1+C_2}.$$

These roots will be high-frequency because the associated resistances are small.

Push-Pull, Common Source Amplifiers

Similar to the class A but can operate as class B providing higher efficiency.

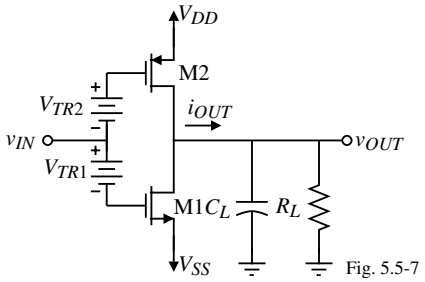


Fig. 5.5-7

Comments:

- The batteries V_{TR1} and V_{TR2} are necessary to control the bias current in M1 and M2.
- The efficiency is the same as the push-pull, source follower.

Practical Implementation of the Push-Pull, Common Source Amplifier

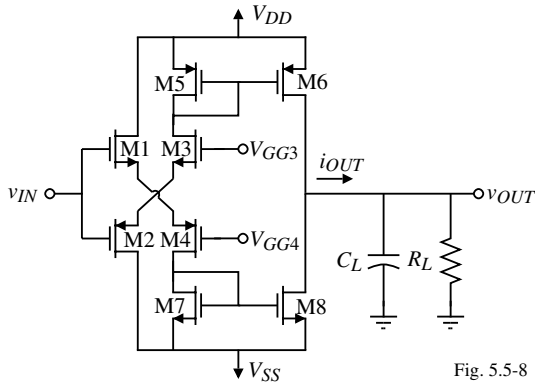


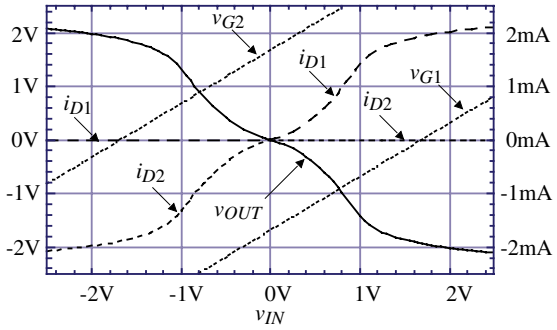
Fig. 5.5-8

V_{GG3} and V_{GG4} can be used to bias this amplifier in class AB or class B operation.

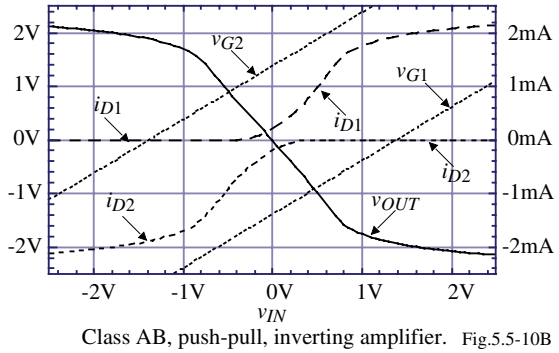
Note, that the bias current in M6 and M8 is not dependent upon V_{DD} or V_{SS} (assuming V_{GG3} and V_{GG4} are not dependent on V_{DD} and V_{SS}).

Illustration of Class B and Class AB Push-Pull, Inverting Amplifier

Output current and voltage characteristics of the push-pull, inverting amplifier (R_L = 1kΩ):



Class B, push-pull, inverting amplifier.

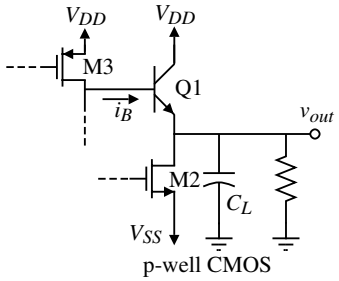


Class AB, push-pull, inverting amplifier. Fig.5.5-10B

Comments:

- Note that there is significant distortion at v_{IN} =0V for the Class B inverter
- Note that v_{OUT} cannot reach the extreme values of V_{DD} and V_{SS}
- I_{OUT}^{+}(max) and I_{OUT}^{-}(max) is always less than V_{DD}/R_L or V_{SS}/R_L
- For v_{OUT} = 0V, there is quiescent current flowing in M1 and M2 for Class AB

What about the use of BJTs?



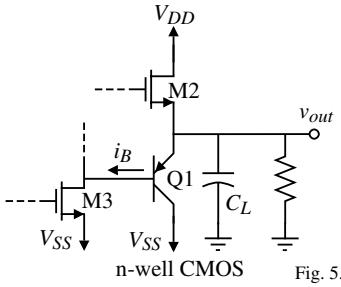


Fig. 5.5-8A

Comments:

- Can use either substrate or lateral BJTs.
- Small-signal output resistance is $1/g_m$ which can easily be less than 100Ω.
- Unfortunately, only PNP or NPN BJTs are available but not both on a standard CMOS technology.
- In order for the BJT to sink (or source) large currents, the base current, i_B, must be large. Providing large currents as the voltage gets to extreme values is difficult for MOSFET circuits to accomplish.
- If one considers the MOSFET driver, the emitter can only pull to within v_{BE}+V_{ON} of the power supply rails. This value can be 1V or more.

We will consider the BJT as an output stage in more detail in Sec. 7.1.

Use of Negative, Shunt Feedback to Reduce the Output Resistance

Concept:

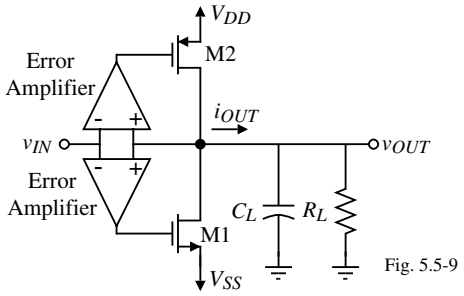


Fig. 5.5-9

$$R_{out} = \frac{r_{ds1} \| r_{ds2}}{1+\text{Loop Gain}}$$

Comments:

- Can achieve output resistances as low as 10Ω.
- If the error amplifiers are not balanced, it is difficult to control the quiescent current in M1 and M2
- Great linearity because of the strong feedback
- Can be efficient if operated in class B or class AB

Simple Implementation of Negative, Shunt Feedback to Reduce the Output Resistance

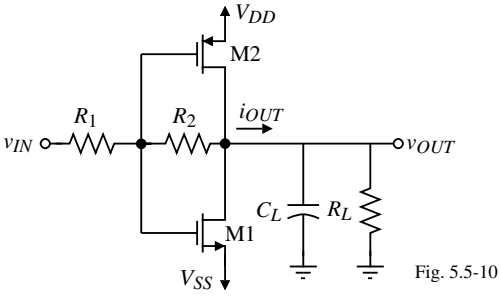


Fig. 5.5-10

$$\text{Loop gain} \approx \left(\frac{R_1}{R_1+R_2}\right)\left(\frac{g_{m1}+g_{m2}}{g_{ds1}+g_{ds2}+G_L}\right)$$

$$\therefore \quad R_{out} = \frac{r_{ds1} \| r_{ds2}}{1+\left(\frac{R_1}{R_1+R_2}\right)\left(\frac{g_{m1}+g_{m2}}{g_{ds1}+g_{ds2}+G_L}\right)}$$

Let $R_1 = R_2$, $R_L = \infty$, I_{Bias} = 500μA, and W_1/L_1 = 100μm/1μm and W_2/L_2 = 200μm/1μm.

Thus, g_{m1} = 3.316mS, g_{m2} = 3.162mS, r_{ds1} = 50kΩ and r_{ds2} = 40kΩ.

$$\therefore \quad R_{out} = \frac{50\text{k}\Omega \| 40\text{k}\Omega}{1+0.5\left(\frac{3316+3162}{25+20}\right)} = \frac{22.22\text{k}\Omega}{1+0.5(143.9)} = 304\Omega \qquad (R_{out} = 5.42\text{k}\Omega \text{ if } R_L = 1\text{k}\Omega)$$

Summary of Output Amplifiers

- The objectives are to provide output power in form of voltage and/or current.
- In addition, the output amplifier should be linear and be efficient.
- Low output resistance is required to provide power efficiently to a small load resistance.
- High source/sink currents are required to provide sufficient output voltage rate due to large load capacitances.
- Types of output amplifiers considered:

  Class A amplifier

  Source follower

  Class B and AB amplifier

  Use of BJTs

  Negative shunt feedback

SECTION 5.6 - HIGH-GAIN AMPLIFIER ARCHITECTURES

High-Gain Amplifiers used in Negative Feedback Circuits

Consider the general, single-loop, negative feedback circuit:

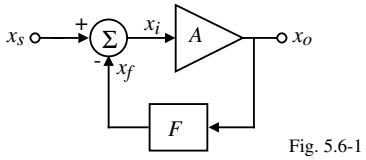


Fig. 5.6-1

x = either voltage or current

$A = \frac{x_o}{x_i}$ = high-gain amplifier

F = feedback network

Closed-loop gain:

$$A_f = \frac{x_o}{x_s} = \frac{A}{1+AF}$$

If $AF >> 1$, then,

$$A_f = \frac{x_o}{x_s} \approx \frac{1}{F}$$

Therefore, to precisely define the closed-loop gain, A_f, we only need to make A large and A_f becomes dependent on F which can be determined by passive elements.

Types of Amplifiers

The gain of an amplifier is given as

$$A = \frac{x_o}{x_i}$$

Therefore, since x can be voltage or current, there are four types of amplifiers as summarized below.

Types of Amplifers	Voltage-controlled, current-source	Voltage-controlled, voltage-source	Current-controlled, current-source	Current-controlled, voltage-source
x_i variable*	Voltage	Voltage	Current	Current
x_o variable	Current	Voltage	Current	Voltage
Desired R_i	Large	Large	Small	Small
Desired R_o	Large	Small	Large	Small

* The x_i , x_s, and x_f must all be the same type of variable, voltage or current.

Voltage-Controlled, Current-Source (VCCS) Amplifier

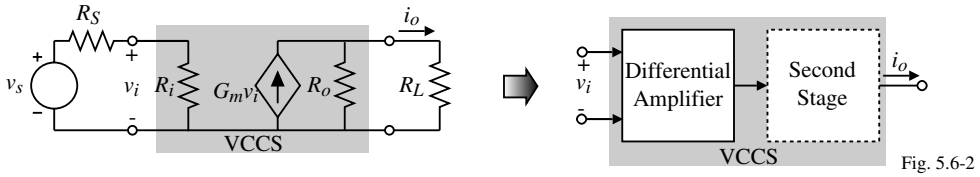


Fig. 5.6-2

$$\frac{i_o}{v_s} = G_M = \frac{G_m R_o R_i}{(R_i + R_S)(R_o + R_L)}$$

This amplifier is sometimes called an *operational transconductance amplifier* (OTA).

Voltage-Controlled, Voltage-Source (VCVS) Amplifier

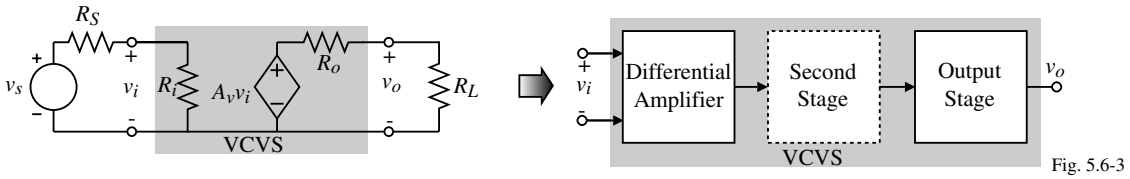


Fig. 5.6-3

$$\frac{v_o}{v_s} = A_V = \frac{A_v R_i R_L}{(R_S + R_i)(R_o + R_L)}$$

This amplifier is normally called an *operational amplifier*.

Current-Controlled, Current-Source (CCCS) Amplifier

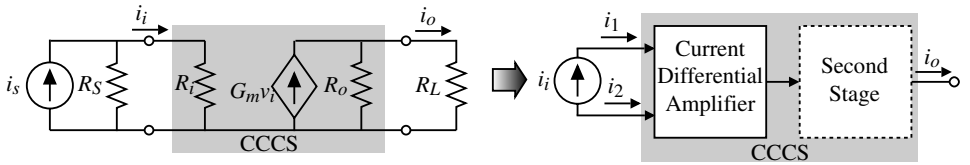


Fig. 5.6-4

$$\frac{i_o}{i_s} = A_I = \frac{A_i R_S R_o}{(R_S + R_i)(R_o + R_L)}$$

Current-Controlled, Voltage-Source (CCVS) Amplifier

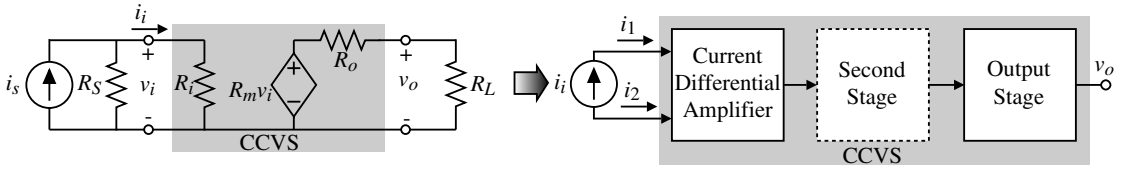


Fig. 5.6-5

$$\frac{v_o}{i_s} = R_M = \frac{R_m R_S R_L}{(R_i + R_S)(R_o + R_L)}$$

SECTION 5.7 - SUMMARY

This chapter presented the following subjects:

5.1 Inverting Amplifiers
- Class A (diode load and current sink/source load)
- Class AB of B (push-pull)

5.2 Differential Amplifiers
- Need good common mode rejection
- An excellent input stage for integrated circuit amplifiers

5.3 Cascode Amplifiers
- Useful for controlling the poles of an amplifier

5.4 Current Amplifiers
- Good for low power supplies

5.5 Output Amplifiers
- Minimize the output resistance
- Maximize the current sinking/sourcing capability

5.6 High-Gain Architectures
- Possible block-level implementations using the blocks of this chapter.

