LECTURE 240 – CASCODE OP AMPS

LECTURE ORGANIZATION

Outline
• Lecture Organization
• Single Stage Cascode Op Amps
• Two Stage Cascode Op Amps
• Summary

CMOS Analog Circuit Design, 2nd Edition Reference
Pages 293-310

Cascode Op Amps
Why cascode op amps?
• Control of the frequency behavior
• Can get more gain by increasing the output resistance of a stage
• In the past section, PSRR of the two-stage op amp was insufficient for many applications
• A two-stage op amp can become unstable for large load capacitors (if nulling resistor is not used)
• The cascode op amp leads to wider ICMR and/or smaller power supply requirements

Where Should the Cascode Technique be Used?
• First stage -
  Good noise performance
  Requires level translation to second stage
  Degrades the Miller compensation
• Second stage -
  Self compensating
  Increases the efficiency of the Miller compensation
  Increases PSRR
SINGLE STAGE CASCODE OP AMPS

Simple Single Stage Cascode Op Amp

R_{out} of the first stage is \( R_I \approx (g_{mC2r_{ds}C2r_{ds2}})(g_{mC4r_{ds}C4r_{ds4}}) \)

Voltage gain = \( \frac{V_{o1}}{V_{in}} = g_{m1}R_I \) [The gain is increased by approximately \( 0.5(g_{MCr_{ds}C}) \)]

As a single stage op amp, the compensation capacitor becomes the load capacitor.

Example 240-1 Single-Stage, Cascode Op Amp Performance

Assume that all \( W/L \) ratios are 10 \( \mu \)m/1 \( \mu \)m, and that \( I_{DS1} = I_{DS2} = 50 \) \( \mu \)A of single stage op amp. Find the voltage gain of this op amp and the value of \( C_I \) if \( GB = 10 \) MHz. Use \( K_N' = 120 \mu A/V^2 \), \( K_P' = 25 \mu A/V^2 \), \( V_{TN} = 0.5 V \), \( V_{TP} = -0.5 V \), \( \lambda_N = 0.06 V^{-1} \) and \( \lambda_P = 0.08 V^{-1} \).

Solution

The device transconductances are

\( g_{m1} = g_{m2} = g_{ml} = 346.4 \) \( \mu \)S
\( g_{mc1} = g_{mc2} = 346.4 \mu S \)
\( g_{mc3} = g_{mc4} = 158.1 \) \( \mu \)S.

The output resistance of the NMOS and PMOS devices is 0.333 \( \Omega \) and 0.25 \( \Omega \), respectively.

\[ R_I = 7.86 \) M\( \Omega \]
\[ A_v(0) = 2.722 V/V. \]

For a unity-gain bandwidth of 10 MHz, the value of \( C_I \) is 5.51 pF.

What happens if a 100pF capacitor is attached to this op amp?

\( GB \) goes from 10MHz to 0.551MHz.
Enhanced Gain, Single Stage, Cascode Op Amp

From inspection, we can write the voltage gain as,

\[ A_v = \frac{v_{OUT}}{v_{IN}} = g_{m1}R_{out} \]

where \( R_{out} = (A_{rds6}g_{m6}r_{ds8}) \parallel (A_{rds4}g_{m4}r_{ds4}) \)

Since \( A = g_m r_d / 2 \), the voltage gain would be equal to 100,000 to 500,000.

Output is not optimized for maximum signal swing.

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TWO-STAGE, CASCODE OP AMPS

Two-Stage Op Amp with a Cascoded First-Stage

- MT1 and MT2 are required for level shifting from the first-stage to the second.
- The PSRR is improved by the presence of MT1.
- Internal loop pole at the gate of M6 may cause the Miller compensation to fail.
- The voltage gain of this op amp could easily be 100,000 V/V.
Two-Stage Op Amp with a Cascode Second-Stage

\[ A_V = g_{m1}g_{m1}R_I R_{II} \]

where \( g_{m1} = g_{m2}, \quad g_{mII} = g_{m6}, \)

\[ R_I = \frac{1}{g_{ds2} + g_{ds4}} = \frac{2}{(\lambda_2 + \lambda_4)I_{D5}} \]

and

\[ R_{II} = (g_{m6}r_{ds6}r_{ds6}) \left| \left| \left( g_{m7}r_{ds7}r_{ds7} \right) \right| \right| \]

Comments:
- The second-stage gain has greatly increased improving the Miller compensation
- The overall gain is approximately \((g_m r_{ds})^3\) or very large
- Output pole, \(p_2\), is approximately the same if \(C_c\) is constant
- The zero RHP is the same if \(C_c\) is constant
- PSRR is poor unless the Miller compensation is removed (then the op amp becomes self compensated)

A Balanced, Two-Stage Op Amp using a Cascode Output Stage

\[ v_{out} = \left( \frac{g_{m1}g_{m8}}{g_{m3}} \right) \frac{v_{in}}{2} + \left( \frac{g_{m2}g_{m6}}{g_{m4}} \right) \frac{v_{in}}{2} R_{II} \]

where

\[ R_{II} = (g_{m7}r_{ds7}r_{ds7}) \left| \left| \left( g_{m12}r_{ds12}r_{ds11} \right) \right| \right| \]

and

\[ k = \frac{g_{m8}}{g_{m3}} = \frac{g_{m6}}{g_{m4}} \]

This op amp is balanced because the drain-to-ground loads for M1 and M2 are identical.

**TABLE 1 - Design Relationships for Balanced, Cascode Output Stage Op Amp.**

<table>
<thead>
<tr>
<th>( I_{out} )</th>
<th>( GB )</th>
<th>( A_v )</th>
<th>( V_{in} ) (max)</th>
<th>( V_{in} ) (min)</th>
</tr>
</thead>
<tbody>
<tr>
<td>( C_L )</td>
<td>( g_{m1}g_{m8} )</td>
<td>( \frac{1}{2} \left( \frac{g_{m1}g_{m8}}{g_{m3}} + \frac{g_{m2}g_{m6}}{g_{m4}} \right) R_{II} )</td>
<td>( V_{DD} - \left</td>
<td>\frac{I_S}{B_3} \right</td>
</tr>
</tbody>
</table>

The op amp becomes self-compensated when the Miller compensation is removed.
Example 240-2  Design of Balanced, Cascoded Output Stage Op Amp

Design a balanced, cascoded output stage op amp using the procedure outlined above. The specifications of the design are as follows:

- $V_{DD} = 2.5 \text{ V (} V_{SS} = 0)$
- Slew rate = 5 V/\mu s with a 50 pF load
- $GB = 10 \text{ MHz with a 25 pF load}$
- $A_v \geq 5000$
- Input CMR = 1V to +2 V
- $0.5 \text{ V < Output swing < 2 V}$

Use $K_N' = 120 \mu A/V^2$, $K_P' = 25 \mu A/V^2$, $V_{TN} = |V_{TP}| = 0.5 \text{ V}$, $\lambda_N = 0.06 \text{ V}^{-1}$, and $\lambda_P = 0.08 \text{ V}^{-1}$ and let all device lengths be 0.5 \mu m.

Solution

While numerous approaches can be taken, we shall follow one based on the above specifications. The steps will be numbered to help illustrate the procedure.

1.) The first step will be to find the maximum source/sink current. This is found from the slew rate.

$$I_{source}/I_{sink} = C_L \times \text{slew rate} = 50 \text{ pF} (5 \text{ V/\mu s}) = 250 \mu A$$

2.) Next some $W/L$ constraints based on the maximum output source/sink current are developed. Under dynamic conditions, all of $I_5$ will flow in M4; thus we can write

$$\text{Max. } I_{out}(source) = (S_6/S_4)I_5 \quad \text{and} \quad \text{Max. } I_{out}(sink) = (S_8/S_3)I_5$$

The maximum output sinking current is equal to the maximum output sourcing current if

$$S_3 = S_4, \quad S_6 = S_8, \quad \text{and} \quad S_10 = S_{11}$$

3.) Choose $I_5$ as 100 \mu A. This current (which can be changed later) gives

$$S_6 = 2.5S_4 \quad \text{and} \quad S_8 = 2.5S_3$$

Note that $S_8$ could equal $S_3$ if $S_{11} = 2.5S_{10}$. This would minimize the power dissipation.

4.) Next design for +0.5V output capability. We shall assume that the output must source or sink the 250 \mu A at the peak values of output. First consider the negative output peak. Since there is 0.5V difference between $V_{SS}(0V)$ and the minimum output, let $V_{DS11\text{(sat)}} = V_{DS12\text{(sat)}} = 0.25 \text{ V}$ (we continue to ignore the bulk effects). Under the maximum negative peak assume that $I_{11} = I_{12} = 250 \mu A$. Therefore

$$0.25 = \sqrt{\frac{2I_{11}}{K'_N S_{11}}} = \sqrt{\frac{2I_{12}}{K'_N S_{12}}} = \sqrt{\frac{500 \mu A}{(120 \mu A/V^2)S_{11}}}$$

which gives $S_{11} = S_{12} = 67$ and $S_9 = S_{10} = 67$. For a maximum output voltage of 2V, we get

$$0.25 = \sqrt{\frac{2I_{6}}{K'_P S_6}} = \sqrt{\frac{2I_{7}}{K'_P S_7}} = \sqrt{\frac{500 \mu A}{(25 \mu A/V^2)S_6}}$$

which gives $S_6 = S_7 = S_8 = 320$ and $S_3 = S_4 = (320/2.5) = 128$. 

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Example 240-2 - Continued

5.) Now we must consider the possibility of conflict among the specifications. First consider the input CMR. $S_3$ has already been designed as 67. Using ICMR relationship, we find that $S_3$ should be at least 8. A larger value of $S_3$ will give a higher value of $V_{in(max)}$ so that we continue to use $S_3 = 67$ which gives $V_{in(max)} = 2.32V$.

Next, check to see if the larger W/L causes a pole below the gainbandwidth. Assuming a $C_{ox}$ of 6fF/μm² gives the first-stage pole of

$$p_3 = \frac{-g_{m3}}{C_{gs3}+C_{gs8}} = \frac{-2K'pS_3I_3}{(0.667)(W_3L_3+W_8L_8)C_{ox}} = 3.125\times10^9 \text{ rads/sec or 497 MHz}$$

which is much greater than $10GB$.

6.) Next we find $g_{m1}$ ($g_{m2}$). There are two ways of calculating $g_{m1}$.

(a.) The first is from the $A_v$ specification. The gain is

$$A_v = (g_{m1/2}g_{m4})(g_{m6} + g_{m8}) R_{II}$$

Note, a current gain of $k$ can be introduced by making $S_6/S_4$ ($S_8/S_3 = S_{11}/S_3$) equal to $k$.

$$g_{m6} = \frac{g_{m11}}{g_{m3}} = \sqrt{\frac{2K'pS_6I_6}{2K'pS_4I_4}} = k$$

Calculating the various transconductances we get $g_{m4} = 566 \ \mu S$, $g_{m6} = g_{m7} = g_{m8} = 1414 \ \mu S$, $g_{m11} = g_{m12} = 1414 \ \mu S$, $r_{ds6} = r_{ds7} = 100 \ \Omega$, and $r_{ds11} = r_{ds12} = 133 \ \kOmega$. Assuming that the gain $A_v$ must be greater than 5000 and $k = 2.5$ gives $g_{m1} > 221 \ \mu S$.

Example 240-2 - Continued

(b.) The second method of finding $g_{m1}$ is from the $GB$ specifications. Multiplying the gain by the dominant pole ($1/C_{II}R_{II}$) gives

$$GB = \frac{g_{m1}(g_{m6} + g_{m8})}{2g_{m4}C_L}$$

Assuming that $C_L = 25 \ \text{pF}$ and using the specified $GB$ gives $g_{m1} = 628 \ \mu S$.

Since this is greater than 221μS, we choose $g_{m1} = g_{m2} = 628\mu S$. Knowing $I_5$ gives $S_1 = S_2 = 32.9 \approx 33$.

8.) The next step is to check that $S_1$ and $S_2$ are large enough to meet the $+1V$ input CMR specification. Use the saturation formula we find that $V_{DSS}$ is 0.341 V. This gives $S_5 = 15$. The gain becomes $A_v = 14,182V/V$ and $GB = 10 \ \text{MHz}$ for a 25 pF load. We shall assume that exceeding the specifications in this area is not detrimental to the performance of the op amp.

9.) Knowing the currents and W/L values, the bias voltages $V_{NB1}$, $V_{NB2}$ and $V_{PB2}$ can be designed.

The W/L values resulting from this design procedure are shown below. The power dissipation for this design is seen to be $350\mu A\cdot2.5V = 0.875 \text{ mW}$.

$$S_1 = S_3 = 33 \quad S_3 = S_4 = 128 \quad S_3 = 15$$
$$S_6 = S_7 = S_8 = 320 \quad S_9 = S_{10} = S_{11} = S_{12} = 67$$
Technological Implications of the Cascode Configuration

Fig. 6.5-5

If a double poly CMOS process is available, inter-node parasitics can be minimized. As an alternative, one should keep the drain/source between the transistors to a minimum area.

Fig. 6.5-5A

Input Common Mode Range for Two Types of Differential Amplifier Loads

Fig. 6.5-6

In order to improve the ICMR, it is desirable to use current source (sink) loads without losing half the gain.

The resulting solution is the folded cascode op amp.
The Folded Cascode Op Amp

Comments:
- $I_4$ and $I_5$, should be designed so that $I_6$ and $I_7$ never become zero (i.e. $I_4=I_5=1.5I_3$)
- This amplifier is nearly balanced (would be exactly if $R_A$ was equal to $R_B$)
- Self compensating
- Poor noise performance, the gain occurs at the output so all intermediate transistors contribute to the noise along with the input transistors. (Some first stage gain can be achieved if $R_A$ and $R_B$ are greater than $g_{m1}$ or $g_{m2}$.

Small-Signal Analysis of the Folded Cascode Op Amp

Model:
Recalling what we learned about the resistance looking into the source of the cascode transistor;

$$ R_A = \frac{r_{ds6} + (1/g_{m1})}{1 + g_{m6}r_{ds6}} \approx \frac{1}{g_{m6}} $$

and

$$ R_B = \frac{r_{ds7} + R_{II}}{1 + g_{m7}r_{ds7}} \approx \frac{R_{II}}{g_{m7}r_{ds7}} $$

where $R_{II} = g_{m9}r_{ds9}r_{ds11}$

The voltage transfer function can be found as follows. The current $i_{10}$ is written as

$$ i_{10} = \frac{-g_{m1}(r_{ds1}||r_{ds4})v_{in}}{2[R_A + (r_{ds1}||r_{ds4})]} \approx \frac{-g_{m1}v_{in}}{2} $$

and the current $i_7$ can be expressed as

$$ i_7 = \frac{g_{m2}(r_{ds2}||r_{ds5})v_{in}}{2[R_{II}] + (r_{ds2}||r_{ds5})} = \frac{g_{m2}v_{in}}{2[1 + (g_{m7}r_{ds7} + R_{II})]} = \frac{g_{m2}v_{in}}{2(1+k)} $$

where

$$ k = \frac{R_{II}(g_{ds2}+g_{ds5})}{g_{m7}r_{ds7}} $$

The output voltage, $v_{out}$, is equal to the sum of $i_7$ and $i_{10}$ flowing through $R_{out}$. Thus,

$$ \frac{v_{out}}{v_{in}} = \left(\frac{g_{m1}}{2} + \frac{g_{m2}}{2(1+k)}\right)R_{out} = \left(\frac{2+k}{2+2k}\right)g_{m1}R_{out} $$

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Intuitive Analysis of the Folded Cascode Op Amp

Assume that a voltage of $\Delta V$ is applied. We know that

$$R_A(M6) \approx 1/g_{m6} \text{ and } R_B(M7) \approx r_{ds}$$

The currents flowing to the output are,

$$\frac{g_{m1}\Delta V}{2} + \frac{g_{m2}\Delta V}{4}$$

The output resistance is approximately,

$$R_{out} \approx (g_{m9}r_{ds9}r_{ds11})[(g_{m7}r_{ds7}(r_{ds2}||r_{ds5})]$$

$$\approx \left(\frac{g_{m9}r_{ds2}}{3}\right)$$

Therefore, the approximate voltage gain is,

$$\frac{v_{out}}{v_{in}} = \left(\frac{g_{m1}}{2} + \frac{g_{m2}}{4}\right)R_{out} \approx \left(\frac{3g_{m}}{4}\right)R_{out} = \left(\frac{g_{m9}r_{ds2}}{4}\right)$$

While the analysis is simpler than small signal analysis, the value of $k$ defined in the previous slide is 1.

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Frequency Response of the Folded Cascode Op Amp

The frequency response of the folded cascode op amp is determined primarily by the output pole which is given as

$$p_{out} = \frac{-1}{R_{out}'C_{out}} \text{ where } R_{out}' = \left(\frac{2+k}{2+2k}\right)R_{out}$$

where $C_{out}$ is all the capacitance connected from the output of the op amp to ground.

All other poles must be greater than $GB = g_{m1}/C_{out}$. The approximate expressions for each pole is

1.) Pole at node A: $p_A = -g_{m6}/(C_{gs}+2C_{db})$
2.) Pole at node B: $p_B = -g_{m7}/(C_{gs}+2C_{db})$
3.) Pole at drain of M6: $p_6 = -g_{m10}/(2C_{gs}+2C_{db})$
4.) Pole at source of M8: $p_8 \approx -(g_{m8}r_{ds8}g_{m10})/(C_{gs}+C_{db})$
5.) Pole at source of M9: $p_9 = -g_{m9}/(C_{gs}+C_{db})$

where the approximate expressions are found by the reciprocal product of the resistance and parasitic capacitance seen to ground from a given node. One might feel that because $R_B$ is approximately $r_{ds}$ that this pole also might be small. However, at frequencies where this pole has influence, $C_{out}$, causes $R_{out}$ to be much smaller making $p_B$ also non-dominant.
**Example 240-3 - Folded Cascode, CMOS Op Amp**

Assume that all $g_{mN} = g_{MP} = 100 \mu S$, $r_{dSN} = 2M\Omega$, $r_{dSP} = 1M\Omega$, and $C_L = 10pF$. Find all of the small-signal performance values for the folded-cascode op amp.

$$R_{II} = 0.4G\Omega, R_A = 10k\Omega, \text{ and } R_B = 4M\Omega$$

$$k = \frac{0.4 \times 10^9 (0.3 \times 10^{-6})}{100} = 1.2$$

$$\frac{v_{out}}{v_{in}} = \left(\frac{2 + 1.2}{2 + 2.4}\right) (100)(57.143) = 4.156V/V$$

$$R_{out} = R_{II} || (g_{m} r_{dS}) || (r_{dS} r_{dS}) = 400M\Omega || (100)(0.667M\Omega) = 57.143M\Omega$$

$$|p_{out}| = \frac{1}{R_{out}C_{out}} = \frac{1}{57.143M\Omega \cdot 10pF} = 1.750 \text{ rads/sec.} \Rightarrow 278Hz \Rightarrow GB = 1.21MHz$$

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**PSRR of the Folded Cascode Op Amp**

Consider the following circuit used to model the PSRR-:

This model assumes that gate, source and drain of M11 and the gate and source of M9 all vary with $V_{SS}$.

We shall examine $V_{out}/V_{ss}$ rather than $PSRR^-$. (Small $V_{out}/V_{ss}$ will lead to large $PSRR^-$.)

The transfer function of $V_{out}/V_{ss}$ can be found as

$$\frac{V_{out}}{V_{ss}} \approx \frac{sC_{gd9} R_{out}}{sC_{out} R_{out} + 1} \text{ for } C_{gd9} < C_{out}$$

The approximate PSRR- is sketched on the next page.
Frequency Response of the PSRR of the Folded Cascode Op Amp

We see that the PSRR of the cascode op amp is much better than the two-stage op amp without any modifications to improve the PSRR.

Design Approach for the Folded-Cascode Op Amp

<table>
<thead>
<tr>
<th>Step</th>
<th>Relationship</th>
<th>Design Equation/Constraint</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Slew Rate</td>
<td>( I_3 = SR \cdot C_L )</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Bias currents in output cascodes</td>
<td>( I_4 = I_5 = 1.2I_3 ) to ( 1.5I_3 )</td>
<td>Avoid zero current in cascodes</td>
</tr>
<tr>
<td>3</td>
<td>Maximum output voltage, ( v_{out(max)} )</td>
<td>( S_5 = K_P \cdot V_{SD5}^2 \cdot S_7 = K_P \cdot V_{SD7}^2 ), ((S_4 = S_5 \text{ and } S_6 = S_7))</td>
<td>( V_{SD5(sat)} = V_{SD7(sat)} = 0.5[V_{DD}-V_{out(max)}] )</td>
</tr>
<tr>
<td>4</td>
<td>Minimum output voltage, ( v_{out(min)} )</td>
<td>( S_{11} = S_{11} = K_{N'} \cdot V_{DS11}^2 \cdot S_9 = K_{N'} \cdot V_{DS9}^2 ), ((S_{10} = S_{11} \text{ and } S_8 = S_9))</td>
<td>( V_{DS9(sat)} = V_{DS11(sat)} = 0.5[V_{out(min)}-V_{SS}] )</td>
</tr>
<tr>
<td>5</td>
<td>( GB = \frac{g_m}{C_L} )</td>
<td>( S_1 = S_2 = \frac{S_{11}^2}{K_{N'} \cdot I_3} = \frac{S_{11}^2}{K_{N'} \cdot I_3} )</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Minimum input CM</td>
<td>( S_3 = \frac{2I_3}{K_{N'} \cdot (V_{in(min)}-V_{SS}) \cdot \sqrt{(S_3/K_{N'} \cdot S_1-1)}-V_{T1}} )</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Maximum input CM</td>
<td>( S_4 = S_5 = K_P \cdot (V_{DD}-V_{in(max)}+V_{T1})^2 )</td>
<td>( S_4 \text{ and } S_5 \text{ must meet or exceed value in step 3} )</td>
</tr>
<tr>
<td>8</td>
<td>Differential Voltage Gain</td>
<td>( \frac{v_{out}}{v_{in}} = \left( \frac{g_m}{2} + \frac{g_m}{2(1+k)} \right) \cdot R_{out} = \left( \frac{2+k}{2+2k} \right) \cdot \frac{g_m R_{out}}{g_m R_{out}} )</td>
<td>( k = \frac{R_{I} (s_{ds2}+s_{ds4})}{s_{m7} r_{ds} s_{7}} )</td>
</tr>
<tr>
<td>9</td>
<td>Power dissipation</td>
<td>( P_{diss} = (V_{DD}-V_{SS}) (I_3+I_{10}+I_{11}) )</td>
<td></td>
</tr>
</tbody>
</table>
**Example 240-4  Design of a Folded-Cascode Op Amp**

Design a folded-cascode op amp if the slew rate is $10\,\text{V/\mu s}$, the load capacitor is $10\,\text{pF}$, the maximum and minimum output voltages are $2\,\text{V}$ and $0.5\,\text{V}$ for a $2.5\,\text{V}$ power supply, the $GB$ is $10\,\text{MHz}$, the minimum input common mode voltage is $+1\,\text{V}$ and the maximum input common mode voltage is $2.5\,\text{V}$. The differential voltage gain should be greater than $3,000\,\text{V/V}$ and the power dissipation should be less than $5\,\text{mW}$. Use $K_N' = 120\,\mu\text{A/V}^2$, $K_P' = 25\,\mu\text{A/V}^2$, $V_{TN} = |V_{TP}| = 0.5\,\text{V}$, $\lambda_N = 0.06\,\text{V}^{-1}$, and $\lambda_P = 0.08\,\text{V}^{-1}$. Let $L = 0.5\,\mu\text{m}$.

**Solution**

Following the approach outlined above we obtain the following results.

$I_3 = SR \cdot C_L = 10 \times 10^6 \cdot 10^{-11} = 100\,\mu\text{A}$

Select $I_4 = I_5 = 125\,\mu\text{A}$.

Next, we see that the value of $0.5(V_{DD}-V_{out\text{(max)}})$ is $0.5\,\text{V}/2$ or $0.25\,\text{V}$. Thus,

$$S_4 = S_5 = \frac{2 \cdot 125\,\mu\text{A}}{25 \cdot 16} = 160$$

and assuming worst case currents in M6 and M7 gives,

$$S_6 = S_7 = \frac{2 \cdot 125\,\mu\text{A}}{25 \cdot 16} = 160$$

The value of $0.5(V_{out\text{(min)}}-|V_{SS}|)$ is $0.25\,\text{V}$ which gives the value of $S_8$, $S_9$, $S_{10}$ and $S_{11}$ as

$$S_8 = S_9 = S_{10} = S_{11} = \frac{2 \cdot I_8}{K_N' \cdot V_{DS8}^2} = \frac{2 \cdot 125}{120 \cdot (0.25)^2} = 20$$

In step 5, the value of $GB$ gives $S_1$ and $S_2$ as

$$S_1 = S_2 = \frac{GB^2 \cdot C_L^2}{K_N^3 I_3} = \frac{(2 \pi \times 10^6)^2(10^{-11})^2}{120 \times 10^{-6} \cdot 100 \times 10^{-6}} = 32.9 \approx 33$$

The minimum input common mode voltage defines $S_3$ as

$$S_3 = \frac{2I_3}{K_N' \left(V_{in\text{(min)}}-V_{SS}\sqrt{\frac{I_3}{K_N^3 S_1} - V_{T1}}\right)^2} = \frac{2 \times 10^6}{120 \times 10^{-6} \left(1.0 + 0.2 \sqrt{100 / 120 \cdot 33 - 0.5}\right)^2} = 14.3 \approx 15$$

We need to check that the values of $S_4$ and $S_5$ are large enough to satisfy the maximum input common mode voltage. The maximum input common mode voltage of 2.5 requires

$$S_4 = S_5 \geq \frac{2I_4}{K_P'[V_{DD}-V_{in\text{(max)}}]+V_{T1}]^2} = \frac{2 \cdot 125\,\mu\text{A}}{25 \times 10^{-6} \cdot \mu\text{A}^2 \cdot 0.5^2} = 40$$

which is less than 160. In fact, with $S_4 = S_5 = 160$, the maximum input common mode voltage is $2.75\,\text{V}$.

The power dissipation is found to be

$$P_{diss} = 2.5\,\text{V}(125\,\mu\text{A}+125\,\mu\text{A}) = 0.625\,\text{mW}$$
Example 240-4 - Continued

The small-signal voltage gain requires the following values to evaluate:

- \( S_4, S_5: \quad g_m = \sqrt{2 \cdot 125 \cdot 25 \cdot 160} = 1000 \mu S \quad \text{and} \quad g_{ds} = 125 \times 10^{-6} \cdot 0.08 = 10 \mu S \)
- \( S_6, S_7: \quad g_m = \sqrt{2 \cdot 75 \cdot 25 \cdot 1600} = 774.6 \mu S \quad \text{and} \quad g_{ds} = 75 \times 10^{-6} \cdot 0.08 = 6 \mu S \)
- \( S_8, S_9, S_{10}, S_{11}: \quad g_m = \sqrt{2 \cdot 75 \cdot 120 \cdot 20} = 600 \mu S \quad \text{and} \quad g_{ds} = 75 \times 10^{-6} \cdot 0.06 = 4.5 \mu S \)
- \( S_1, S_2: \quad g_{mI} = \sqrt{2 \cdot 50 \cdot 120 \cdot 33} = 629 \mu S \quad \text{and} \quad g_{ds} = 50 \times 10^{-6} (0.06) = 3 \mu S \)

Thus,

\[
R_{II} = g_m 9 r_{ds} 9 r_{ds} 11 = (600 \mu S) \left( \frac{1}{4.5 \mu S} \right) \left( \frac{1}{4.5 \mu S} \right) = 29.63 \text{M\Omega}
\]

\[
R_{out} \approx 29.63 \text{M\Omega} \left( \frac{1}{6 \mu S} \right) \left( \frac{1}{10 \mu S + 3 \mu S} \right) = 7.44 \text{M\Omega}
\]

\[
k = \frac{R_{II}(g_{ds} 2 + g_{ds} 4)}{g_m 7 r_{ds} 7} = \frac{7.44 \text{M\Omega} (3 \mu S + 10 \mu S) (6 \mu S)}{774.6 \mu S} = 0.75
\]

The small-signal, differential-input, voltage gain is

\[
A_{vd} = \left( \frac{2 + k}{2 + 2k} \right) g_{mI} R_{out} = \left( \frac{2 + 0.75}{2 + 1.5} \right) 0.629 \times 10^{-3} \cdot 7.44 \times 10^6 = (0.786)(4680) = 3.678 \text{ V/V}
\]

The gain is slightly larger than the specified 3,000 V/V.

Comments on Folded Cascode Op Amps

- Good PSRR
- Good ICMR
- Self compensated
- Can cascade an output stage to get extremely high gain with lower output resistance (use Miller compensation in this case)
- Need first stage gain for good noise performance
- Widely used in telecommunication circuits where large dynamic range is required
**Enhanced-Gain, Folded Cascode Op Amps**

If more gain is needed, the folded cascode op amp can be enhanced to boost the output impedance even higher as follows.

Voltage gain = \( g_m R_{out} \),

where

\[
R_{out} \approx [A_{rd}s78m7(r_{ds1}||r_{ds5})]|| (A_{rd}s98m9r_{ds11})
\]

Since \( A \approx g_m r_{ds} \) the voltage gain would be in the range of 100,000 to 500,000.

Note that to achieve maximum output swing, it will be necessary to make sure that M5 and M11 are biased with \( V_{DS} = V_{DS}(sat) \).

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**What are the Enhancement Amplifiers?**

Requirements:

1.) Need a gain of \( g_m r_{ds} \).

2.) Must be able to set the dc voltage at its input to get wide-output voltage swing.

Possible Enhancement Amplifiers:
**Enhanced-Gain, Folded Cascode Op Amp**

Detailed realization:

![Enhanced-Gain, Folded Cascode Op Amp Diagram]

**Frequency Response of the Enhanced Gain Cascode Op Amps**

Normally, the frequency response of the cascode op amps would have one dominant pole at the output. The frequency response would be,

\[
A_v(s) = g_{m1} \left( \frac{R_{out}(1/sC_{out})}{R_{out} + 1/sC_{out}} \right) = g_{m1}R_{out} \frac{R_{out}}{sR_{out}C_{out} + 1} = \frac{g_{m1}R_{out}}{1 - \frac{s}{p_1}}
\]

If the amplifier used to boost the output resistance had no frequency dependence then the frequency response would be as follows.
**Frequency Response of the Enhanced Gain Cascode Op Amp – Continued**

- Does the pole in the feedback amplifier $A$ have an influence?
  
  Although the output resistance can be modeled as,
  
  \[
  R_{out}' = R_{out}A_o \left( 1 - \frac{s}{p^2} \right) \left( 1 - \frac{s}{p^2A_o} \right)
  \]

  it has no influence on the frequency response because $C_{out}$ has shorted out any influence a change in $R_{out}$ might have.

- Higher order poles come from a diversion of the current flow in the op amp to ground rather than the intended destination of the current to the output. These poles that divert the current are:
  
  - Pole at the source of M6 ($A_{gm6}/C_6$)
  - Pole at the source of M7 ($A_{gm7}/C_7$)
  - Pole at the drain of M8 ($g_{m10}/C_8$)
  - Pole at the source of M9 ($A_{gm9}/C_6$)
  - Pole at the drain of M10 ($g_{m8}r_{ds8}g_{m10}/C_{10}$)

  Note that the enhancement amplifiers cause most of the higher-order poles to be moved out by $|A|$. However, each of the enhancement amplifiers introduce a pole at their output which is approximately $-1/[r_{ds}(C_{gs}+2C_{db}+2C_{gd})]$. These poles become the dominant poles that limit $GB$.

**SUMMARY**

- Cascode op amps give additional flexibility to the two-stage op amp
  - Increase the gain
  - Control the dominant and nondominant poles
- Enhanced gain, cascode amplifiers provide additional gain and are used when high gains are needed
- Folded cascode amplifier is an attractive alternate to the two-stage op amp
  - Wider ICMR
  - Self compensating
  - Good PSRR