LECTURE 070 – RESISTORS AND INDUCTORS

LECTURE ORGANIZATION

Outline
- Resistors
- Inductors
- Summary

CMOS Analog Circuit Design, 2nd Edition Reference
Pages 47-48, 60-63 and new material

RESISTORS

Types of Resistors Compatible with CMOS Technology
1.) Diffused and/or implanted resistors.
2.) Well resistors.
3.) Polysilicon resistors.
4.) Metal resistors.
**Characterization of Resistors**

1.) Value

\[ R = \frac{\rho L}{A} \]

AC and DC resistance

2.) Linearity

Does \( V = IR \)?

Velocity saturation of carriers

3.) Power

\[ P = VI = I^2R \]

4.) Current

Electromigration

5.) Parasitics

\[ R \quad \text{and} \quad Cp \]

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**MOS Resistors - Source/Drain Resistor**

Diffusion:

- 10-100 ohms/square
- Absolute accuracy = ±35%
- Relative accuracy=2% (5μm), 0.2% (50μm)
- Temperature coefficient = +1500 ppm/°C
- Voltage coefficient = 200 ppm/V

Ion Implanted:

- 500-2000 ohms/square
- Absolute accuracy = ±15%
- Relative accuracy=2% (5μm), 0.15% (50μm)
- Temperature coefficient = +400 ppm/°C
- Voltage coefficient = 800 ppm/V

Comments:

- Parasitic capacitance to substrate is voltage dependent.
- Piezoresistance effects occur due to chip strain from mounting.
**Polysilicon Resistor**

30-100 ohms/square (unshielded)
100-500 ohms/square (shielded)
Absolute accuracy = ±3.0%
Relative accuracy = 2% (5 μm)
Temperature coefficient = 500-1000 ppm/°C
Voltage coefficient ≈ 100 ppm/V

Comments:
• Used for fuzzes and laser trimming
• Good general resistor with low parasitics

**N-well Resistor**

1000-5000 ohms/square
Absolute accuracy = ±40%
Relative accuracy = 5%
Temperature coefficient = 4000 ppm/°C
Voltage coefficient is large ≈ 8000 ppm/V

Comments:
• Good when large values of resistance are needed.
• Parasitics are large and resistance is voltage dependent
• Could put a $p^+$ diffusion into the well to form a pinched resistor
**Metal as a Resistor**

Illustration:

Resistance from A to B = Resistance of segments $L_1$, $L_2$, $L_3$, $L_4$, and $L_5$ with some correction subtracted because of corners.

Sheet resistance:

- 50-70 mΩ/□ ± 30% for lower or middle levels of metal
- 30-40 mΩ/□ ± 15% for top level metal

Watch out for the current limit for metal resistors. Contact resistance varies from 5Ω to 10Ω.

Tempco ≈ +4000 ppm/°C

Need to derate the current at higher temperatures:

$$I_{DC}(T_j) = D_T I_{DC}(T_r)$$

<table>
<thead>
<tr>
<th>$T_j$(°C)</th>
<th>$T_r$(°C)</th>
<th>$D_T$</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;85</td>
<td>85</td>
<td>1</td>
</tr>
<tr>
<td>100</td>
<td>85</td>
<td>0.63</td>
</tr>
<tr>
<td>110</td>
<td>85</td>
<td>0.48</td>
</tr>
<tr>
<td>125</td>
<td>85</td>
<td>0.32</td>
</tr>
<tr>
<td>150</td>
<td>85</td>
<td>0.18</td>
</tr>
</tbody>
</table>

**Thin Film Resistors**

A high-quality resistor fabricated from a thin nickel-chromium alloy or a silicon-chromium mixture.

Uppermost metal layer:

Performance:

- Sheet resistivity is approximately 5-10 ohms/square
- Temperature coefficients of less than 100 ppm/°C
- Absolute tolerance of better than ±0.1% using laser trimming
- Selectivity of the metal etch must be sufficient to ensure the integrity of the thin-film resistor beneath the areas where metal is etched away.
**Resistor Layout Techniques**

End structure calculations:

$$
\Delta R_1 = \frac{R_{\text{cont}}}{N_{\text{cont}}} + R_{\text{sh(sil)}} \left( \frac{X_{c-r} + 0.75 \cdot L_{\text{con}}}{W - 2 \cdot D W_{\text{sil}}} \right) \\
\Delta R_{\text{total}} = \left( \frac{1}{\Delta R_1} + \frac{1}{\Delta R_2} + \cdots \right)^{-1}
$$

$$
(L_{\text{con}} = \text{width of the contact})
$$

$$
\Delta R_2 = \frac{R_{\text{cont}}}{N_{\text{cont}}} + R_{\text{sh(sil)}} \left( \frac{X_{c-r} + X_{\text{con}} + 1.75 \cdot L_{\text{con}}}{W - 2 \cdot \Delta W_{\text{sil}}} \right)
$$

**Extending the Length of Resistors**

Snaked Resistors:

Corner corrections:

Fig. 2.6-16B
**Extending the Length of Resistors**

Series Resistors:

![Diagram of series resistors](060220-02)

Resistor Ending Influence:

![Diagram of resistor endings and influence](050416-02)

**Process Bias Influence on Resistors**

Process bias is where the dimensions of the fabricated geometries are not the same as the layout data base dimensions.

Process biases introduce systematic errors.

Consider the effect of over-etching:

Assume that etching introduces a process bias of 0.1\( \mu \)m. Two resistors designed to have a ratio of 2:1 have equal lengths but the widths are different by a factor of two.

![Diagram of process bias impact](041020-01)

The actual matching ratio due to the etching bias is,

\[
\frac{R_2}{R_1} = \frac{W_1}{W_2} = \frac{4-0.2}{2-0.2} = \frac{3.8}{1.8} = 2.11 \quad \rightarrow \quad 5.6\% \text{ error in matching}
\]

Use the replication principle to eliminate this error.
**Etch Rate Variations – Polysilicon Resistors**

The size of the area to be etched determines the etch rate. Smaller areas allow less access to the etchant while larger areas allow more access to the etchant. This is illustrated below:

The objective is to make $A = B = C$. In the left-hand case, B is larger due to the slower etch rates on both sides of B. In the right-hand case, the dummy strips have caused the etch rates on both sides of A, B and C to be identical leading to better matching. It may be advisable to connect the dummy strips to ground or some other low impedance node to avoid static electrical charge buildup.

**Diffusion Interaction – Diffused Resistors**

Problem:

Consider three adjacent $p^+$ diffusions into a $n$ epitaxial region,

If A, B, and C are resistors that are to be matched, we see that the effective concentration of B is larger than A or C because of diffusion interaction. This would cause the B resistor to be smaller even though the geometry is identical.

Solution: Place identical dummy resistors to the left of A and right of C. Connect the dummy resistors to a low impedance to prevent the formation of floating diffusions that might increase the sensitivity to latchup.
Thermoelectric Effects
The thermoelectric effect, also called the Seebeck effect, is a potential difference that is developed between two dissimilar materials that are at different temperatures. The potential developed is given as,

\[ V = S \cdot \Delta T \]

where,

- \( S = \) Seebeck coefficient (≈ 0.4mV/°C)
- \( \Delta T = \) temperature difference between the two metals

Thus, a temperature difference between the contacts to a resistor and the resistor of 1°C can generate a voltage of 0.4mV causing problems in certain circuits (bandgap).

Two possible resistor layouts with regard to the thermoelectric effect:

- High Sheet Resistivity Resistor Layout
  - High sheet resistivity resistors must use p+ or n+ in order to make contacts to metal. Thus, there is plenty of opportunity for the thermoelectric effect to cause problems if care is not taken. Below are three high sheet resistor layouts with differing thermoelectric performance.

  - Sensitive to thermoelectric effects.
  - Sensitive to misalignment.
  - Resistor layout that minimizes thermoelectric effect and misalignment.
Future Technology Impact on Resistors
What will be the impact of scaling down in CMOS technology?
• If the size of the resistor remains the same, there will be little impact.
• If the size scales with the technology, the contacts and connections to the resistors will have more influence on the resistor.

MOS Passive RC Component Performance Summary

<table>
<thead>
<tr>
<th>Component Type</th>
<th>Range of Values</th>
<th>Absolute Accuracy</th>
<th>Relative Accuracy</th>
<th>Temperature Coefficient</th>
<th>Voltage Coefficient</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOSFET gate Cap.</td>
<td>6-7 fF/µm²</td>
<td>10%</td>
<td>0.1%</td>
<td>20ppm/°C</td>
<td>±20ppm/V</td>
</tr>
<tr>
<td>Poly-Poly Capacitor</td>
<td>0.3-0.4 fF/µm²</td>
<td>20%</td>
<td>0.1%</td>
<td>25ppm/°C</td>
<td>±50ppm/V</td>
</tr>
<tr>
<td>Metal-Metal Capacitor</td>
<td>0.1-1fF/µm²</td>
<td>10%</td>
<td>0.6%</td>
<td>??</td>
<td>??</td>
</tr>
<tr>
<td>Diffused Resistor</td>
<td>10-100 Ω/sq.</td>
<td>35%</td>
<td>2%</td>
<td>1500ppm/°C</td>
<td>200ppm/V</td>
</tr>
<tr>
<td>Ion Implanted Resistor</td>
<td>0.5-2 kΩ/sq.</td>
<td>15%</td>
<td>2%</td>
<td>400ppm/°C</td>
<td>800ppm/V</td>
</tr>
<tr>
<td>Poly Resistor</td>
<td>30-200 Ω/sq.</td>
<td>30%</td>
<td>2%</td>
<td>1500ppm/°C</td>
<td>100ppm/V</td>
</tr>
<tr>
<td>n-well Resistor</td>
<td>1-10 kΩ/sq.</td>
<td>40%</td>
<td>5%</td>
<td>8000ppm/°C</td>
<td>10kppm/V</td>
</tr>
<tr>
<td>Top Metal Resistor</td>
<td>30 mΩ/sq.</td>
<td>15%</td>
<td>2%</td>
<td>4000ppm/°C</td>
<td>??</td>
</tr>
<tr>
<td>Lower Metal Resistor</td>
<td>70 mΩ/sq.</td>
<td>28%</td>
<td>3%</td>
<td>4000ppm/°C</td>
<td>??</td>
</tr>
</tbody>
</table>
**INDUCTORS**

**Characterization of Inductors**

1.) Value of the inductor

Spiral inductor$^1$:

$$L \approx \mu_0 n^2 r = 4\pi \times 10^{-7} n^2 r \approx 1.2 \times 10^{-6} n^2 r$$

2.) Quality factor, $Q = \frac{\omega L}{R}$

3.) Self-resonant frequency: $f_{self} = \frac{1}{\sqrt{LC}}$

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**IC Inductors**

What is the range of values for on-chip inductors?

Consider an inductor used to resonate with 5pF at 1000MHz.

$$L = \frac{1}{4\pi^2 f_o^2 C} = \frac{1}{(2\pi \times 10^9)^2 \times 5 \times 10^{-12}} = 5 \text{nH}$$

Note: Off-chip connections will result in inductance as well.
Candidates for inductors in CMOS technology are:
1.) Bond wires
2.) Spiral inductors
3.) Multi-level spiral
4.) Solenoid

Bond wire Inductors:

- Function of the pad distance \( d \) and the bond angle \( \beta \)
- Typical value is 1nH/mm which gives 2nH to 5nH in typical packages
- Series loss is 0.2 \( \Omega/mm \) for 1 mil diameter aluminum wire
- \( Q \approx 60 \) at 2 GHz

Planar Spiral Inductors in CMOS Technology

Typically: \( 3 < N_{\text{turns}} < 5 \) and \( S = S_{\text{min}} \) for the given current

Select the OD, \( N_{\text{turns}} \), and \( W \) so that ID allows sufficient magnetic flux to flow through the center.

Loss Mechanisms:
- Skin effect
- Capacitive substrate losses
- Eddy currents in the silicon
### Planar Spiral Inductors on a Lossy Substrate

- Spiral inductor is implemented using metal layers in CMOS technology
- Topmost metal is preferred because of its lower resistivity
- More than one metal layer can be connected together to reduce resistance or area
- Accurate analysis of a spiral inductor requires complex electromagnetic simulation
- Optimize the values of $W$, $S$, and $N$ to get the desired $L$, a high $Q$, and a high self-resonant frequency
- Typical values are $L = 1$-8nH and $Q = 3$-6 at 2GHz

### Inductor Modeling

Model:

$$
L \approx \frac{37.5 \mu_0 N^2 a^2}{11D - 14a}
$$

$$
R_s \approx \frac{L}{W \sigma \delta (1-e^{-\tau/\delta})}
$$

$$
C_p = NW^2L \frac{\varepsilon_{ox}}{t_{ox}}
$$

where

- $\mu_0 = 4\pi \times 10^{-7}$ H/m (vacuum permeability)
- $\sigma$ = conductivity of the metal
- $a$ = distance from the center of the inductor to the middle of the windings
- $L$ = total length of the spiral
- $t$ = thickness of the metal
- $\delta$ = skin depth given by $\delta = \sqrt{\frac{2}{W \mu_0 \sigma}}$
- $G_{sub}(C_{sub})$ is a process-dependent parameter
**Inductor Modeling – Continued**

Definition of the previous components:

- $R_s$ is the low frequency resistive loss of a metal and the skin effect
- $C_p$ arises from the overlap of the cross-under with the rest of the spiral. The lateral capacitance from turn-to-turn is also included.
- $C_{ox}$ is the capacitance between the spiral and the substrate
- $R_1$ is the substrate loss due to eddy currents
- $C_1$ is capacitance of the substrate

Design specifications:

- $L$ = desired inductance value
- $Q$ = quality factor
- $f_{SR}$ = self-resonant frequency. The resonant frequency of the $LC$ tank represents the upper useful frequency limit of the inductor. Inductor operation frequency should be lower than $f_{SR}$, $f < f_{SR}$.

ASITIC: A software tool for analysis and simulation of CMOS spiral inductors and transformers.

http://formosa.eecs.berkeley.edu/~niknejad/asitic.html

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**Guidelines for Designing CMOS Spiral Inductors**

- **$D$** – Outer diameter:
  - As $D$ increases, $Q$ increases but the self-resonant frequency decreases
  - A good design generally has $D < 200\mu m$

- **$W$** – Metal width:
  - Metal width should be as wide as possible
  - As $W$ increases, $Q$ increases and $R_s$ decreases
  - However, as $W$ becomes large, the skin effects are more significant, increasing $R_s$
  - A good value of $W$ is $10\mu m < W < 20\mu m$

- **$S$** – Spacing between turns:
  - The spacing should be as small as possible
  - As $S$ and $L$ increase, the mutual inductance, $M$, decreases
  - Use minimum metal spacing allowed in the technology but make sure the inter-winding capacitance between turns is not significant

- **$N$** – Number of turns:
  - Use a value that gives a layout convenient to work with other parts of the circuit

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**Design Example**

A 2GHz LC tank is to be designed as a part of LC oscillator. The C value is given as 3pF. (a) Find value of L. (b) Design a spiral inductor with L value (± 5% range) from (a) using ASITIC. Optimize design parameters, W, S, D and N to get a high Q \( Q_{\text{min}} = 5 \). Show L, Q, \( f_{SR} \) value obtained from simulation. (c) Show the layout. (d) Give a lumped circuit model.

**Solution**

(a) LC tank oscillation frequency is given as 2GHz.

\[
\omega_{osc} = \frac{1}{\sqrt{LC}}, \quad L = \frac{1}{\omega_{osc}^2 \cdot C} = \frac{1}{(2\pi \cdot 2 \times 10^9)^2 \cdot (3 \times 10^{-12})} = 2.11 \times 10^{-9}
\]

\[\therefore \quad L = 2.11\text{nH} \text{ is desired.}\]

(b) \( L = 2.11\text{nH}(\pm 5\%) \) is used as input parameter. Several design parameters are tried to get high Q and \( f_{SR} \) values. Final design has

- Parameters: \( W = 19\text{um}, S = 1\text{um}, D = 200\text{um}, N = 3.5 \)
- Resulting inductor: \( L = 2.06\text{nH}, Q = 7.11, f_{SR} = 9.99\text{GHz} @ 2\text{GHz} \)

This design is acceptable as \( Q > Q_{\text{min}} \) and \( f < f_{SR} \).

(c.) ASITIC generates a layout automatically. It can be saved and imported to use in other tools such as Cadence, ADS and Sonnet.

(d) Analysis in ASITIC gives the following \( \pi \) model.

![Diagram of π model](image)

The π model is usually not symmetrical and this can be used for differential configuration where none of the two ports are ac-grounded.
Reduction of Capacitance to Ground

Comments concerning implementation:

1.) Put a metal ground shield between the inductor and the silicon to reduce the capacitance.
   - Should be patterned so flux goes through but electric field is grounded
   - Metal strips should be orthogonal to the spiral to avoid induced loop current
   - The resistance of the shield should be low to terminate the electric field

2.) Avoid contact resistance wherever possible to keep the series resistance low.

3.) Use the metal with the lowest resistance and farthest away from the substrate.

4.) Parallel metal strips if other metal levels are available to reduce the resistance.

Example →

Fig. 2.5-12

Multi-Level Spiral Inductors

Use of more than one level of metal to make the inductor.

• Can get more inductance per area
• Can increase the interwire capacitance so the different levels are often offset to get minimum overlap.
• Multi-level spiral inductors suffer from contact resistance (must have many parallel contacts to reduce the contact resistance).
• Metal especially designed for inductors is top level approximately 4μm thick.

\[ Q = 5-6, f_{SR} = 30-40 \text{GHz} \]
\[ Q = 10-11, f_{SR} = 15-30 \text{GHz} \]

1 The skin effect and substrate loss appear to be the limiting factor at higher frequencies of self-resonance.

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Inductors - Continued
Self-resonance as a function of inductance. Outer dimension of inductors.

Transformers
Transformer structures are easily obtained using stacked inductors as shown below for a 1:2 transformer.

Method of reducing the inter-winding capacitances.

Measured 1:2 transformer voltage gains:
Transformers – Continued

A 1:4 transformer:

Structure-

Measured voltage gain-

(CL = 0, 50fF, 100fF, 500fF and 1pF. CL is the capacitive loading on the secondary.)

Summary of Inductors

Scaling? To reduce the size of the inductor would require increasing the flux density which is determined by the material the flux flows through. Since this material will not change much with scaling, the inductor size will remain constant.

Increase in the number of metal layers will offer more flexibility for inductor and transformer implementation.

Performance:

• Inductors
  Limited to nanohenrys
  Very low Q (3-5)
  Not variable

• Transformers
  Reasonably easy to build and work well using stacked inductors

• Matching
  Not much data exists publicly – probably not good
SUMMARY

• Types of resistors include diffused, well, polysilicon and metal

• Resistors are characterized by:
  - Value
  - Linearity
  - Power
  - Parasitics

• Technology effects on resistors includes:
  - Process bias
  - Diffusion interaction
  - Thermoelectric effects
  - Piezoresistive effects

• Inductors are made by horizontal metal spirals, typically in top metal

• Inductors are characterized by:
  - Value
  - Losses
  - Self-resonant frequency
  - Parasitics

• RF transformers are reasonably easy to build and work well using stacked inductors