CMOS TECHNOLOGY

Classification of Silicon Technology

Silicon IC Technologies
  └── Bipolar
      ├── Junction Isolated
      └── Dielectric Isolated
  └── Bipolar/CMOS
      ├── Oxide isolated
      └── CMOS
          ├── PMOS (Aluminum Gate)
          └── NMOS
              ├── Aluminum
              └── Silicon
                  └── Silicon-Germanium

060112-02
Categorization of CMOS Technology

- Minimum feature size as a function of time:

![Graph showing the minimum feature size over time for different categories of CMOS technology: Submicron, Deep Submicron, and Ultra Deep Submicron.]

- Categories of CMOS technology:
  1. Submicron technology – \( L_{min} \geq 0.35 \text{ microns} \)
  2. Deep Submicron technology (DSM) – \( 0.1 \text{ microns} \leq L_{min} \leq 0.35 \text{ microns} \)
  3. Ultra-Deep Submicron technology (UDSM) – \( L_{min} \leq 0.1 \text{ microns} \)

Why CMOS Technology?

Comparison of BJT and MOSFET technology from an analog viewpoint:

<table>
<thead>
<tr>
<th>Comparison Feature</th>
<th>BJT</th>
<th>MOSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cutoff Frequency ((f_T))</td>
<td>100 GHz</td>
<td>50 GHz ((0.25\mu m))</td>
</tr>
<tr>
<td>Noise (thermal about the same)</td>
<td>Less 1/f</td>
<td>More 1/f</td>
</tr>
<tr>
<td>DC Range of Operation</td>
<td>9 decades of exponential current versus (v_{BE})</td>
<td>2-3 decades of square law behavior</td>
</tr>
<tr>
<td>Transconductance (Same current)</td>
<td>Larger by 10X</td>
<td>Smaller by 10X</td>
</tr>
<tr>
<td>Small Signal Output Resistance</td>
<td>Slightly larger</td>
<td>Smaller for short channel</td>
</tr>
<tr>
<td>Switch Implementation</td>
<td>Poor</td>
<td>Good</td>
</tr>
<tr>
<td>Capacitor</td>
<td>Voltage dependent</td>
<td>More options</td>
</tr>
<tr>
<td>Performance/Power Ratio</td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td>Technology Improvement</td>
<td>Slower</td>
<td>Faster</td>
</tr>
</tbody>
</table>

Therefore,

- Almost every comparison favors the BJT, however a similar comparison made from a digital viewpoint would come up on the side of CMOS.
- Therefore, since large-volume mixed-mode technology will be driven by digital demands, CMOS is an obvious result as the technology of availability.
**How Does IC Technology Influence Analog IC Design?**

Characteristics of analog IC design:
- Continuous in signal amplitude
- Discrete or continuous in time
- Signal processing primarily depends on ratios of values and time constants
  - Ratios are generally resistance, conductance, or capacitance
  - Time constants are generally products of resistance and capacitance
- Dynamic range is determined by the largest and smallest signals

Influence of IC Technology:
- Accuracy of signal processing depends on the accuracy of the ratios of values
- The dynamic range depends upon the linearity of the circuit elements and the noise
- The value of components is limited by area considerations
- IC technology introduces resistive, capacitive and inductive parasitics that cause deviation from desired behavior
- The analog circuit is subject to the influence of other circuits fabricated in the same substrate

---

**FUNDAMENTAL IC PROCESS STEPS**

**Basic Steps**
- Oxide growth
- Thermal diffusion
- Ion implantation
- Deposition
- Etching
- Shallow trench isolation
- Epitaxy

**Photolithography**
Photolithography is the means by which the above steps are applied to selected areas of the silicon wafer.

**Silicon Wafer**

[Diagram of a silicon wafer with dimensions and electrical specifications]
**Oxidation**

Description:
Oxidation is the process by which a layer of silicon dioxide is grown on the surface of a silicon wafer.

Uses:
- Protect the underlying material from contamination
- Provide isolation between two layers.

Very thin oxides (100Å to 1000Å) are grown using dry oxidation techniques. Thicker oxides (>1000Å) are grown using wet oxidation techniques.

**Diffusion**

Diffusion is the movement of impurity atoms at the surface of the silicon into the bulk of the silicon.
Always in the direction from higher concentration to lower concentration.

Diffusion is typically done at high temperatures: 800 to 1400°C
**Ion Implantation**

Ion implantation is the process by which impurity ions are accelerated to a high velocity and physically lodged into the target material.

- Annealing is required to activate the impurity atoms and repair the physical damage to the crystal lattice. This step is done at 500 to 800°C.
- Ion implantation is a lower temperature process compared to diffusion.
- Can implant through surface layers, thus it is useful for field-threshold adjustment.
- Can achieve unique doping profile such as buried concentration peak.

![Path of impurity atom](image1)

**Deposition**

Deposition is the means by which various materials are deposited on the silicon wafer.

Examples:
- Silicon nitride (Si$_3$N$_4$)
- Silicon dioxide (SiO$_2$)
- Aluminum
- Polysilicon

There are various ways to deposit a material on a substrate:
- Chemical-vapor deposition (CVD)
- Low-pressure chemical-vapor deposition (LPCVD)
- Plasma-assisted chemical-vapor deposition (PECVD)
- Sputter deposition

Material that is being deposited using these techniques covers the entire wafer and requires no mask.
**Etching**

Etching is the process of selectively removing a layer of material. When etching is performed, the etchant may remove portions or all of:

- The desired material
- The underlying layer
- The masking layer

Important considerations:

- **Anisotropy** of the etch is defined as,
  \[ A = 1 - \frac{\text{lateral etch rate}}{\text{vertical etch rate}} \]
- **Selectivity** of the etch (film to mask and film to substrate) is defined as,
  \[ S_{\text{film-mask}} = \frac{\text{mask etch rate}}{\text{film etch rate}} \]

A = 1 and \( S_{\text{film-mask}} = \infty \) are desired.

There are basically two types of etches:

- Wet etch which uses chemicals
- Dry etch which uses chemically active ionized gases.

**Epitaxy**

Epitaxial growth consists of the formation of a layer of single-crystal silicon on the surface of the silicon material so that the crystal structure of the silicon is continuous across the interfaces.

- It is done externally to the material as opposed to diffusion which is internal
- The epitaxial layer (epi) can be doped differently, even opposite to the material on which it is grown
- It is accomplished at high temperatures using a chemical reaction at the surface
- The epi layer can be any thickness, typically 1-20 microns
Photolithography

Components
- Photoresist material
- Mask
- Material to be patterned (e.g., oxide)

Positive photoresist
Areas exposed to UV light are soluble in the developer

Negative photoresist
Areas not exposed to UV light are soluble in the developer

Steps
1. Apply photoresist
2. Soft bake (drives off solvents in the photoresist)
3. Expose the photoresist to UV light through a mask
4. Develop (remove unwanted photoresist using solvents)
5. Hard bake (~100°C)
6. Remove photoresist (solvents)

Illustration of Photolithography - Exposure

The process of exposing selective areas to light through a photo-mask is called printing.

Types of printing include:
- Contact printing
- Proximity printing
- Projection printing
**Illustration of Photolithography - Positive Photoresist**

![Photolithography Process](image)

- **Develop**
- **Etch**
- **Remove photoresist**
- **Fig. 150-11**

---

**TYPICAL SUBMICRON CMOS FABRICATION PROCESS**

**N-Well CMOS Fabrication Major Steps**

1. Implant and diffuse the n-well
2. Deposition of silicon nitride
3. n-type field (channel stop) implant
4. p-type field (channel stop) implant
5. Grow a thick field oxide (FOX)
6. Grow a thin oxide and deposit polysilicon
7. Remove poly and form LDD spacers
8. Implantation of NMOS S/D and n-material contacts
9. Remove spacers and implant NMOS LDDs
10. Repeat steps 8.) and 9.) for PMOS
11. Anneal to activate the implanted ions
12. Deposit a thick oxide layer (BPSG - borophosphosilicate glass)
13. Open contacts, deposit first level metal and etch unwanted metal
14. Deposit another interlayer dielectric (CVD SiO₂), open vias, deposit 2nd level metal
15. Etch unwanted metal, deposit a passivation layer and open over bonding pads
**Major CMOS Process Steps**

Step 1 - Implantation and diffusion of the n-wells

Step 2 - Growth of thin oxide and deposition of silicon nitride

Step 3 - Implantation of the n-type field channel stop

Step 4 - Implantation of the p-type field channel stop
Major CMOS Process Steps – Continued

Step 5.) Growth of the thick field oxide (LOCOS - localized oxidation of silicon)

Step 6.) Growth of the gate thin oxide and deposition of polysilicon. The thresholds can be shifted by an implantation before the deposition of polysilicon.

Major CMOS Process Steps – Continued

Step 7.) Removal of polysilicon and formation of the sidewall spacers

Step 8.) Implantation of NMOS source and drain and contact to n-well (not shown)
**Major CMOS Process Steps - Continued**

Step 9.) Remove sidewall spacers and implant the NMOS lightly doped source/drains

![Diagram showing NMOS implant process]

Step 10.) Implant the PMOS source/drains and contacts to the p⁻ substrate (not shown), remove the sidewall spacers and implant the PMOS lightly doped source/drains

![Diagram showing PMOS implant process]

Step 11.) Anneal to activate the implanted ions

![Diagram showing annealing process]

Step 12.) Deposit a thick oxide layer (BPSG - borophosphosilicate glass)

![Diagram showing BPSG deposit process]
**Major CMOS Process Steps - Continued**

Step 13.) Open contacts, deposit first level metal and etch unwanted metal

![Illustration of Major CMOS Process Step 13]

Step 14.) Deposit another interlayer dielectric (CVD SiO2), open contacts, deposit second level metal

![Illustration of Major CMOS Process Step 14]

Step 15.) Etch unwanted metal and deposit a passivation layer and open over bonding pads

![Illustration of Major CMOS Process Step 15]

p-well process is similar but starts with a p-well implant rather than an n-well implant.
**Approximate Side View of CMOS Fabrication**

Planarization attempts to minimize the variation in surface height of the wafer.

Planarization techniques
- Repeated applications of SOG
- Resist etch-back – highest areas of oxide are exposed longest to the etchant and therefore erode away the most.

Influence of planarization on analog design:
+ Number of levels of metal and the metal integrity depends on planarization
+ Thin film components at the surface require good planarization
+ Without planarization, resistance of conductors increases
+ Planarization at the top level leads to less package induced stress (trimming?)
+ Planarized passivation helps printing when the depth of field is small.
- With planarization, the capacitance of the interdielectric isolation can vary (a good reason to extract capacitance!)
- Significant difference in contact aspect ratio (deep versus shallow contacts)
Chemical Mechanical Polishing

CMP produces the required degree of planarization for modern submicron technology.

- Both chemical effect (slurry) and mechanical (pad pressure) take place.
- Although CMP is superior to SOG and resist etchback, large areas devoid of underlying metal or poly produce low regions in the final surface.
- Challenge: Achieve a highly planarized surface over a wide range of pattern density.

Impact on analog design:

- Makes the surface flatter
  - Vias and plugs can become longer adding resistance
- More uniform surface giving better metal coverage and foundation for thin film components
  - Thickness varies with pattern density

Examples of pattern fill:

Pattern density design rules are both local and global.
Silicide/Salicide Technology
Used to reduce interconnect resistivity by placing a low-resistance silicide such as TiSi$_2$, WSi$_2$, TaSi$_2$, etc. on top of polysilicon.
Salicide technology (self-aligned silicide) provides low resistance source/drain connections as well as low-resistance polysilicon.

SUMMARY
• Fabrication is the means by which the circuit components, both active and passive, are built as an integrated circuit.
• Basic process steps include:
  1.) oxide growth  2.) Thermal diffusion  3.) Ion implantation
  4.) Deposition  5.) Etching  6.) Epitaxy
• The complexity of a process can be measured in the terms of the number of masking steps or masks required to implement the process.
• Major CMOS Processing Steps:
  1.) Well definition
  2.) Definition of active areas and substrate/well contacts (SiNi3)
  3.) Thick field oxide (FOX)
  4.) Thin field oxide and polysilicon
  5.) Diffusion of the source and drains (includes the LDD)
  6.) Dielectric layer/Contacts (planarization)
  7.) Metallization
  8.) Dielectric layer/Vias